



European Organization for Nuclear Research(CERN)

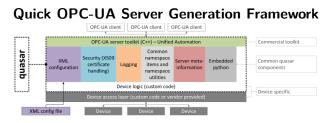
## OPC-UA LAr LpGBT status LAPP

March 20, 2025

#### Etienne FORTIN, Olivier ARNAEZ

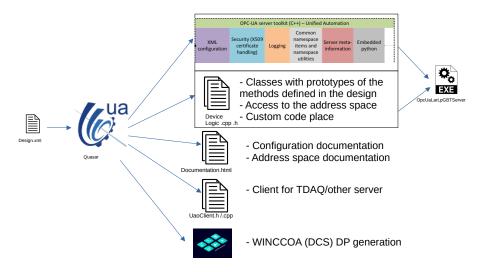
### Overview



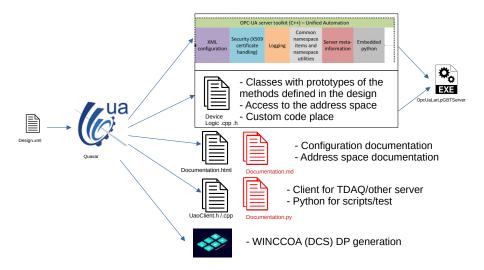


- Ecosystem for the devellopment of OPC-UA
  - in OPC-UA a varaible is always value + timestamp + validity
- Initially developed by ATLAS DCS for generation of OPC-UA server
- The devellopers focus on the "Device logic" and "Device Access layer"
  - No devellopment work needed on OPC-UA protocol and server
- Maintened by a collaboration of CERN-JCOP(Joint COntrols Project)
   , ATLAS central DCS, me...
- Used in ATLAS,LHCb,CMS,BEAM,DUNE ...
- Collaboration agrement with CAEN, ISEG, Wiener.





# Quasar generation, modification for LAr ph-II

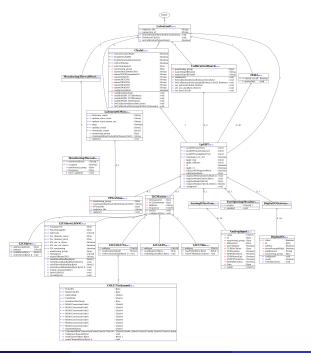


Documentation integrated in quasar v1.7 ...

Etienne FORTIN, Olivier ARNAEZ (CERN)

OPC-UA LAr LpGBT status

- PH-II operation manual : Link to CDS
- A unique server will implement Atomic functions with elementary low level functionalities that can be used to perform higher level actions such as monitoring, configurations, and scans.
- Atomic functions we mean function that perform that need continuous uninterrupted discussion with the hardware e.g. a sequence of I2C commands to write a specific register.
- Clashes between DCS and TDAQ actions will be handled in the server.
- Low level retries will be also handled in the server
- TDAQ will use these functions to implement the needed configurations and scans. The configurations and scans that are the responsibility of DCS will be implemented mainly in the server



Etienne FORTIN, Olivier ARNAEZ (CERN)

OPC-UA LAr LpGBT status

- LpGBT,I2CMaster,AnalogInput,EyeOpenningMonitor, etc...
- Give abstraction over the functionality of the LpGBT chips.
- Client developer don't need to know the details of the LpGBT
- Same LpGBT for calibration and FEB2 -> No specific function

- As almost all our I2C chips use indirect addressing:
  - Several I2C frame are needed to address 1 register
  - To keep the **atomic functions** of the specification: specific class in the server
- Provide method to read/write registers

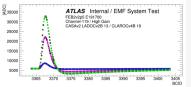
- FEB2: host DCS functionnalities
- CALIB: host DCS functionalities + some LATOURNETT functionalitis for the calibration

- DCS monitoring : handled by a threadpool on the server
  - Reading on the board and writting to cache variable
- TDAQ monitoring:
  - By method, direct reading of the values
  - Can also use the threadpool

## Integration

OPC-UA Server Connection status	Pre Ampli PA1_1P21 EMF D		2.464
ELMB ph-I Probe 0.000	PA2_1P2V_PHON PA3_1P2V_MON 1.267 PA4_1P2V_MON 1.276 PA5_1P2V_MON 1.243	TEMP_LPGBT3 46.103 VTRX1_TEMP_10 TEMP_LPGBT4 53.367 VTRX 2 VTRX 2 VTRX2 1P2 MON	
LATOURNETT	PA5_1P2V_MON 1.243 PA6_1P2V_MON 1.292		2.511
ipbus_ping TRUE	PA7_1P2V_MON 1.263		
Power	PA8_1P2V_MON 1.291 PA9_1P2V_MON 1.302	OPC-UA Monitor	LAPP DCS (Web)
V2P5 MON A 2.525	PA10_1P2V_MON 1.311		LITI DOD (WCD)
V2P5_MON_8 2.487	PA11_1P2V_MON 1.311	. Refresh every (seconds): 60 0 Set	
Temperatures	PA12_1P2V_MON 1.261 PA13_1P2V_MON 1.267	Reload config	
TEMP_T1 42.742	PA13_1P2V_MON 1.278	CHALET	CABANE
TEMP_B1 42,132	PA15 1P2V MON 1.272	CHALET	CABANE
TEMP_T2 49.463 TEMP 82 49.463	PA16_1P2V_MON 1.239	LpGBT	LeGBT A
TEMP_T3 48.240	PA17_1P2V_MON 1.274 PA18 1P2V_MON 1.274	Configuration	
TEMP_83 40.911	PA18_1P2V_MON 1.274 PA19_1P2V_MON 1.287	Calib mode: 1	LpGBT
TEMP_T4 28.732	PA20 1P2V MON 1.267		Link A ready: 1
TEMP_04 41.521 TEMP_TS 20.124	PA21_1P2V_MON 1.245	DC os pulsing: true	Configuration
TEMP 85 35.425	PA22_1P2V_MON 1.272 PA23_1P2V_MON 1.265	<ul> <li>Selected channel: 0</li> </ul>	Calib mode: 1
TEMP_T6 40.911	PA24 1P2V MON 1.250	. LpGBT	
TEMP_86 37.862	PA25 1P2V MON 1.258	Link 0 ready: 1	Temperatures
	PA26_1P2V_MON 1.256	Temperatures	Temp. 1: 25.722569688246
	PA27_1P2V_MON 1.289 PA28_1P2V_MON 1.295	<ul> <li>Temp. CLAROC: 22.6921834880</li> </ul>	PIER73 Temp. 2: 25.178587173836
	PA29 1P2V MON 1287	Temp. LADOC: 23.13471210749	
	PA30 1P2V MON 1.291	GPIOs	Temp. 4: 55.245078059274
	PA31_1P2V_MON 1.311	MUX Atn: true	
	PA32_1P2V_MON 1.259		Temp. 5: 24.822751235239
		MUX Sel 0: true	Temp. 6: 25.178587173836
DCDC		<ul> <li>MUX Sel 1: false</li> </ul>	Terro, 7: 25.722569688246
p3p5V_PA_LEFT TRUE p	1p4V slice9to12 TRUE p1p4V sl	OMUX output sel.: true	LADOCs
3p5V PA RIGHT TRUE p1	p4V slice13to16 TRUE	LADOC	
	p4V_slice17to20 TRUE	DAC value: N/A	M0
	p4V_slice21to24 TRUE	Fine tuning DAC: N/A	LADOC_1
RSTB		Tuning IV ref.: N/A	DAC value: 0
	VTRXS-RSTB TRUE PA7-9_RST		Fine tuning DAC: 12
	VTRX6-RSTB TRUE ADC7-9_RST		Tuning IV ref.: 0
	VTRX7-RST8 TRUE PA10-12_RST VTRX8-RST8 TRUE ADC10-12_RST		
	PA1-3 RSTB TRUE PA13-15 RST		LADOC_2
VTRX2-RSTB TRUE A	DC1-3_RSTB TRUE ADC13-15_RST		DAC value: 0
	PA4-6 RSTB TRUE PA16 RST IDC4.6 BSTB TRUE ADC16 BST		Fine tuning DAC: 12
VTRX4-RSTB TRUE A	DC4-6_RST8 TRUE ADC16_RST	0	<ul> <li>Tuning 1V ref.: 0</li> </ul>
			MI
EME		F DAO	LADOC_1





6097 6036 6036 442 914 6036 6097 ODAC value: 0 Fine tuning DAC: 128 Tuning 1V ref.: 0 M2 LADOC\_1 DAC value: N/A Fine tuning DAC: N/A Tuning IV ref.: N/A LpGBT\_B Configuration Calib mode: 1 LøGBT Link B ready: 1 Temperatures Temp. 1: 24.294452691241702 Temp. 2: 25.17972900157298 Temp. 3: 24.821626512007356

OPC-UA LAr LpGBT status

12/13

### Status

- On the server:
  - All the mains functionalities are made all boards are configured by the server at EMF everyday.
  - Prototype presented at LAr week in mars 2024, and accepted by steering to go to production.
  - Mising one class for the I2C chip for HEC
  - Several optimisations are possible
  - Support of Real calibration/latournett boards
  - Uniformisation of error code
- On the clients:
  - FEB2:
    - Client using the real functionalities of the server to configure the board
    - Partition and cpp client
  - Calibration:
    - Partition and cpp client
    - DCS Winccoa client
- At we need more HW to test in real condidition EMF:
  - several FEB2
  - calibration board
  - latournett board