Application of FPGA devices in experimental high-energy physics

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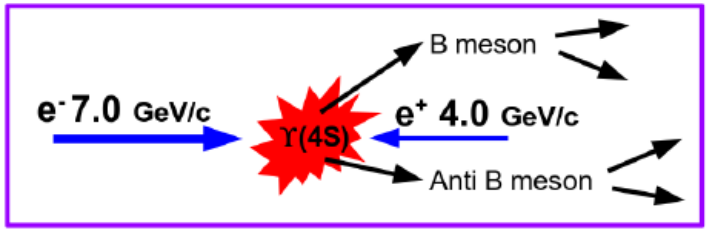
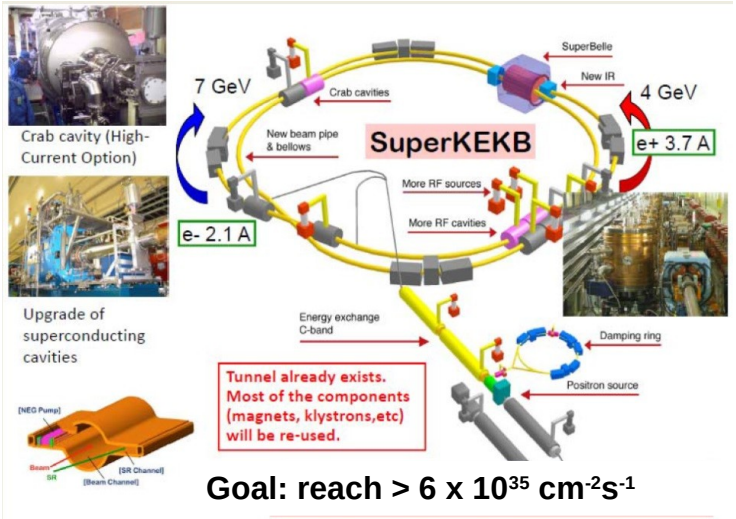
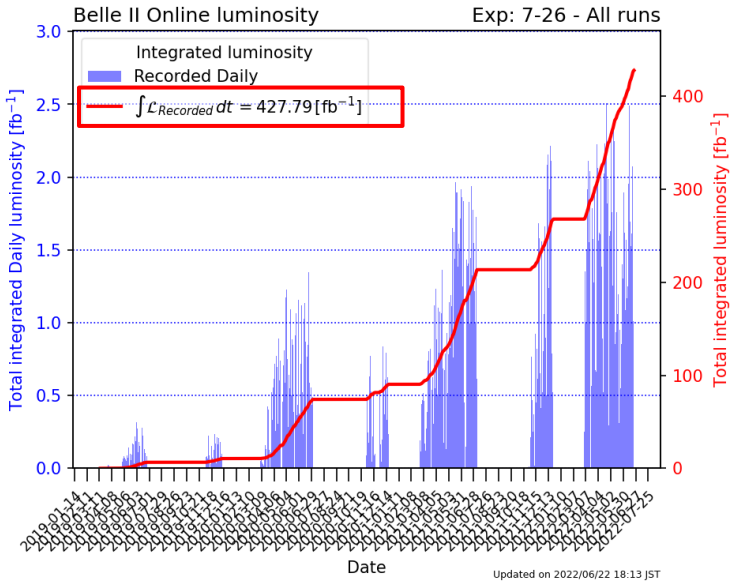
SuperKEKB

- SuperKEKB: Upgraded from KEKB.
  - More than 30 times larger luminosity of KEKB with nano beam scheme.
- Asymmetric energy collider:
  - 7.0 GeV e^- and 4.0 GeV e^+ for Y(4S) $\rightarrow B\overline{B}$.



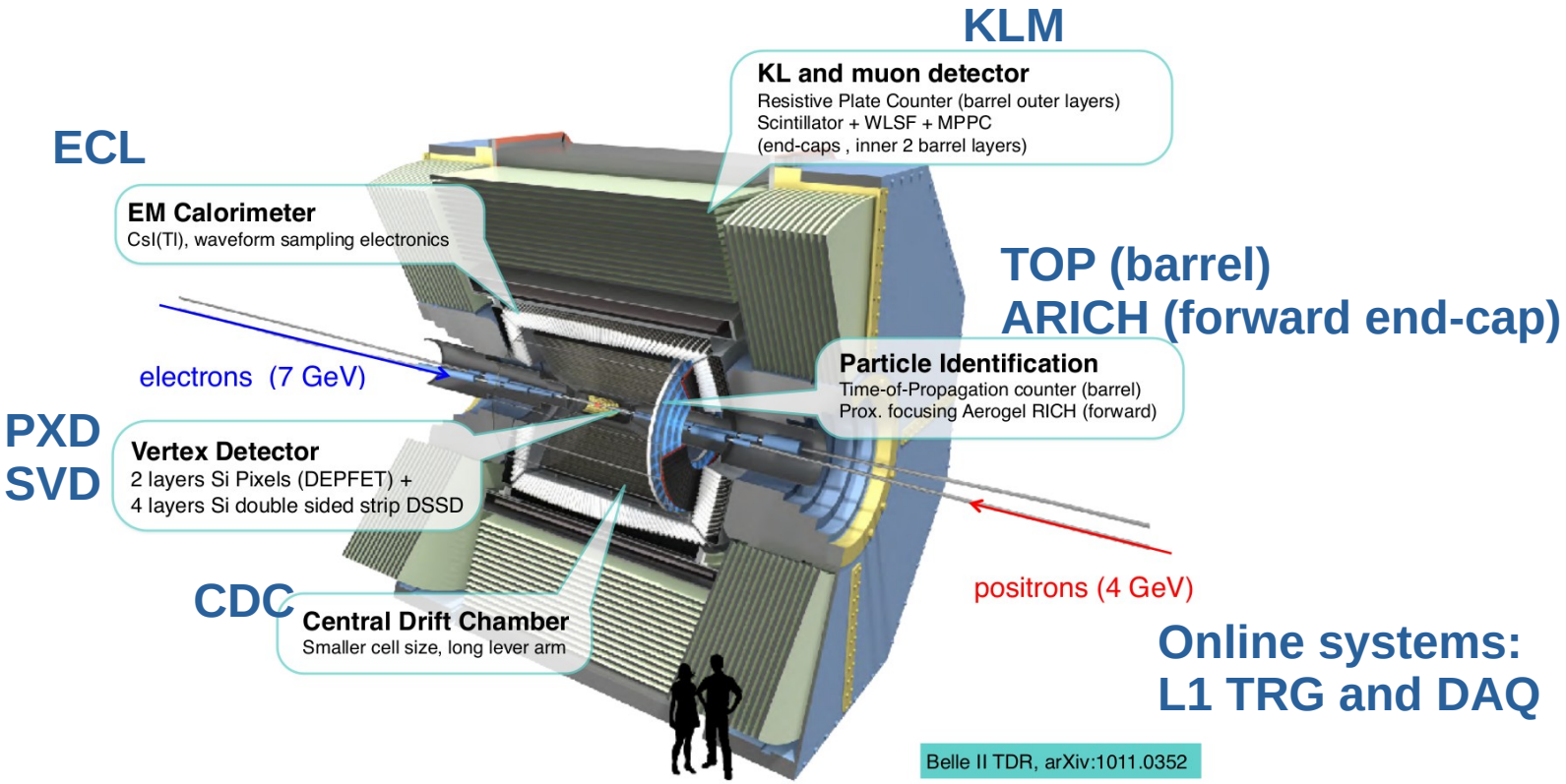
- Luminosity achievement:
  - L_{peak} = 4.65 x 10^{34} $cm^{-2}s^{-1}$.
    World record. ~Two times of KEKB record with much smaller beam current.
  - L_{int} = ~427 fb^{-1} up to Jun. 2022.
- Resumed beam collision in 2024 with PXD full installation.





Belle II

- Belle II: Newly-designed sub-detectors set to improve detection performance.

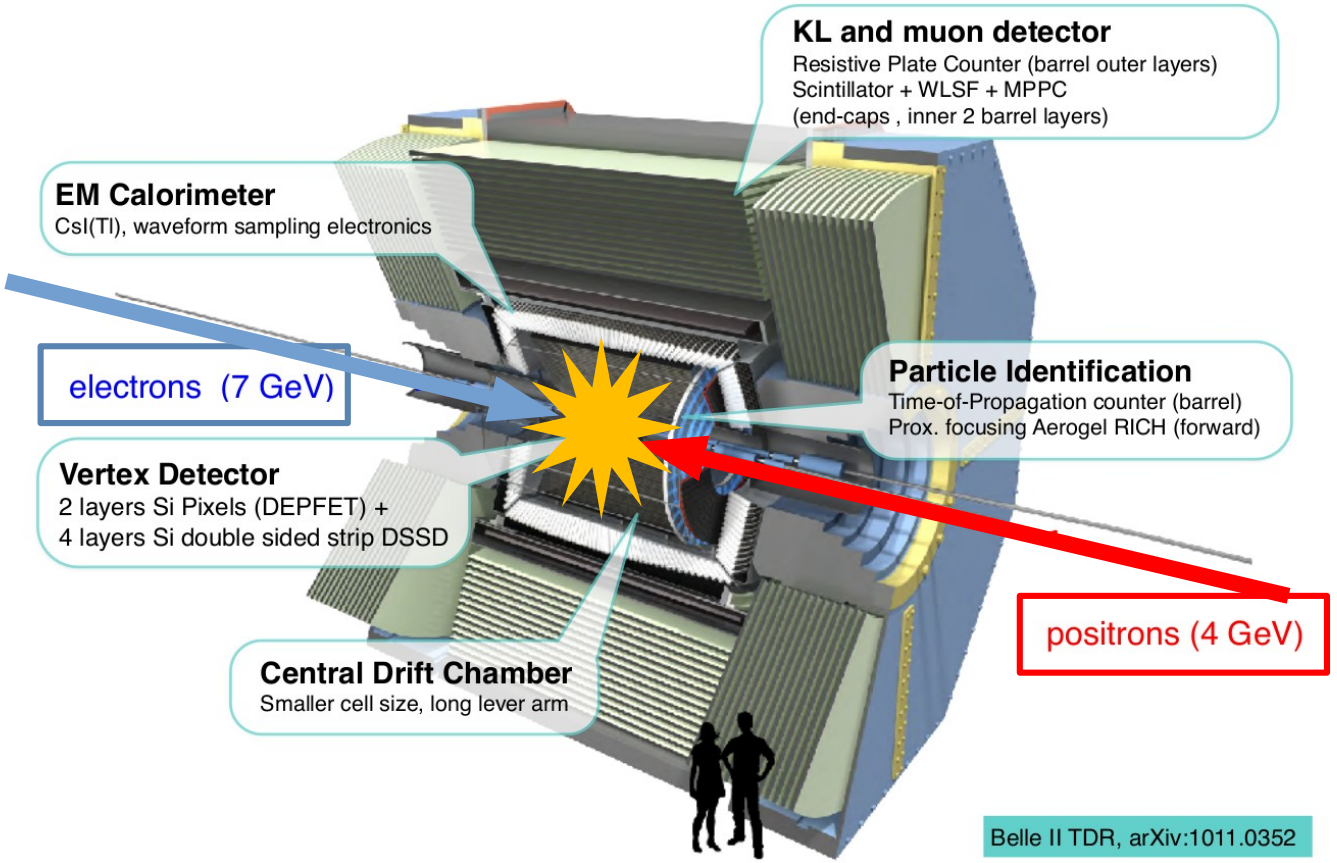


- Physics target of Belle II:
  - Rare B, τ, charm physics, Dark Matter search, CP Violation.

- Requirement for data taking:
  - High L1 trigger rate (~30 kHz), high background, and large event size.

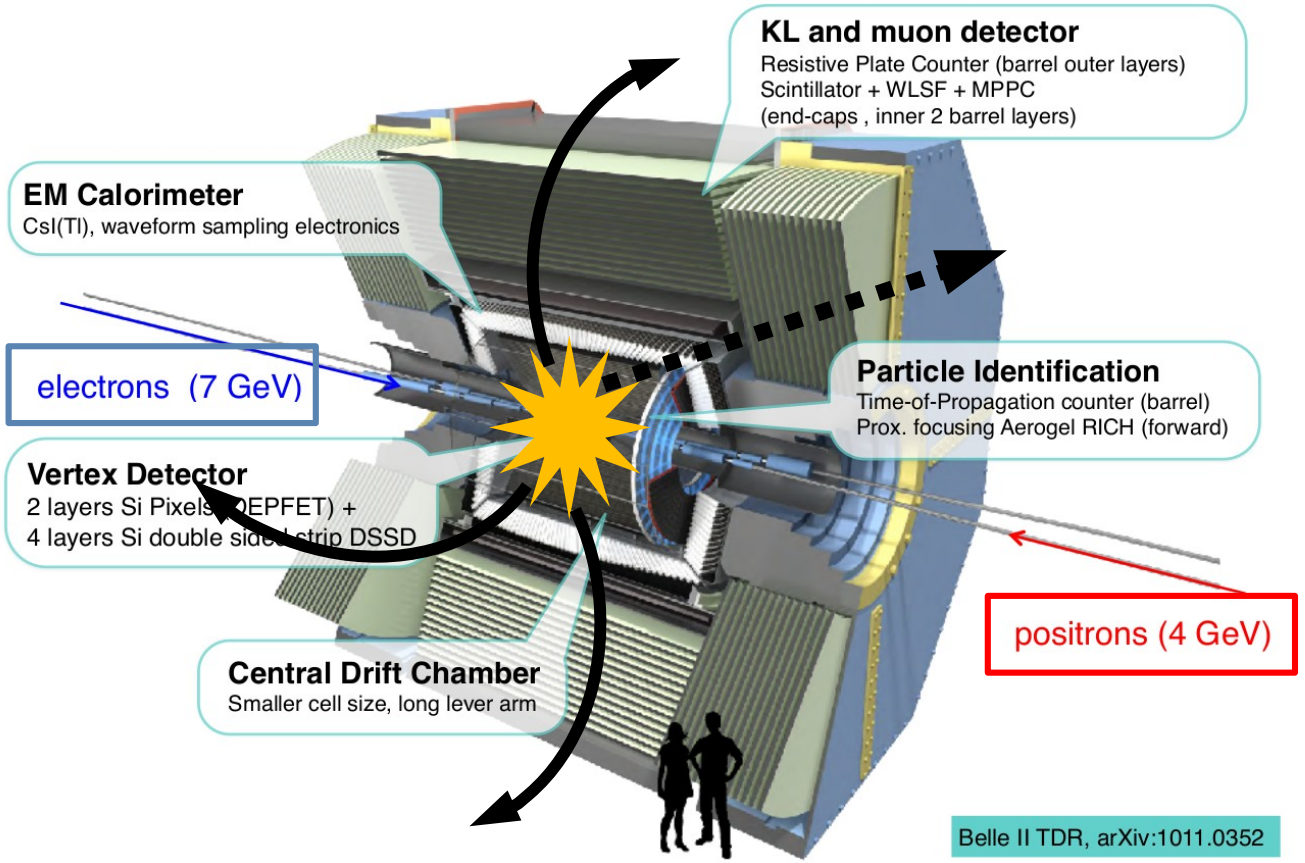
Data taking in HEP

- First, let's paint a picture about what is going on during the experiment.
- Electronics (7 GeV) and Positron (4 GeV) are collided with high rate: luminosity
  - **O(10 kHz)**



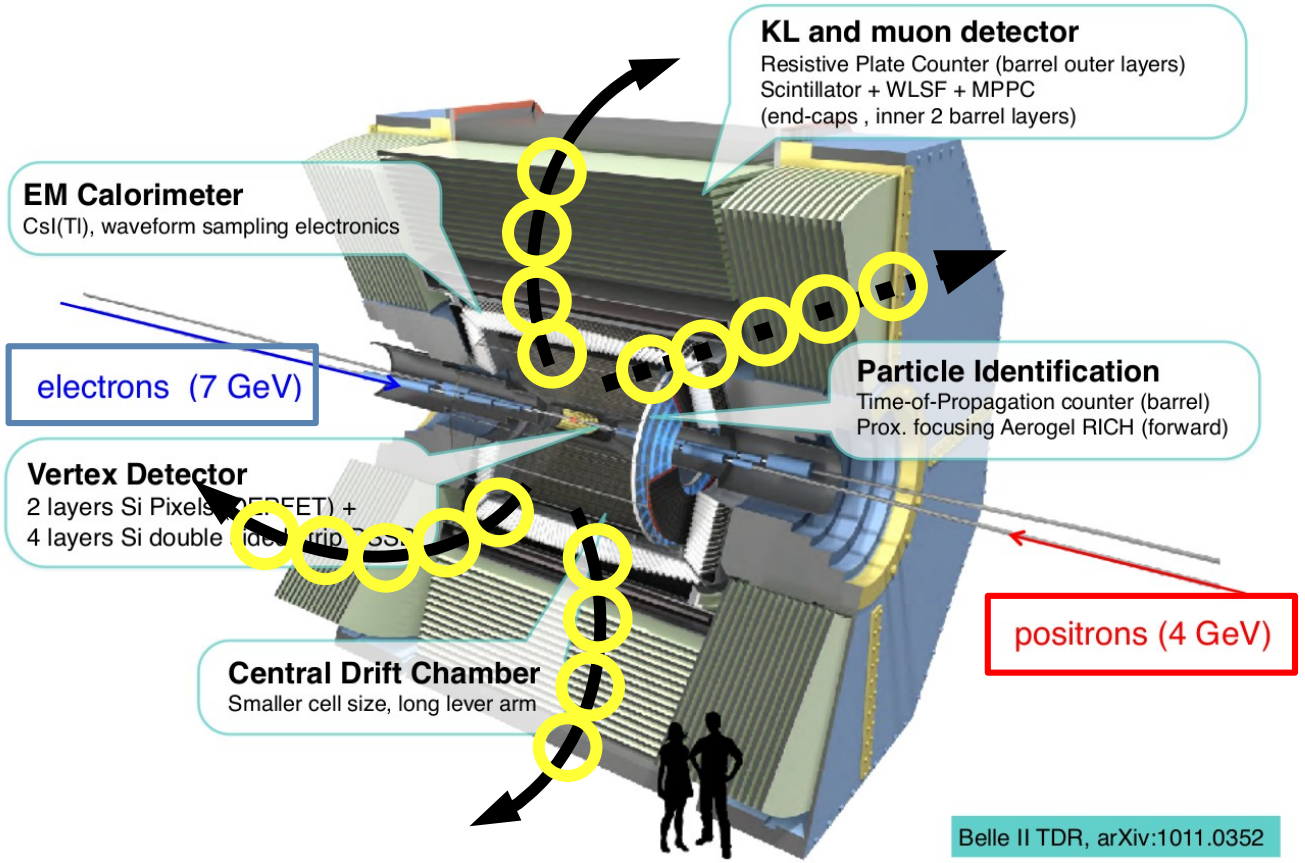
Data taking in HEP (cont'd)

- Collision will produce some kinds of rare particles, then they will decay immediately (**O(ps)**).
  - B meson, D meson, τ lepton, or even Dark Matter particles.
- Then decayed particles will fly out of the detectors with close to the speed of light.



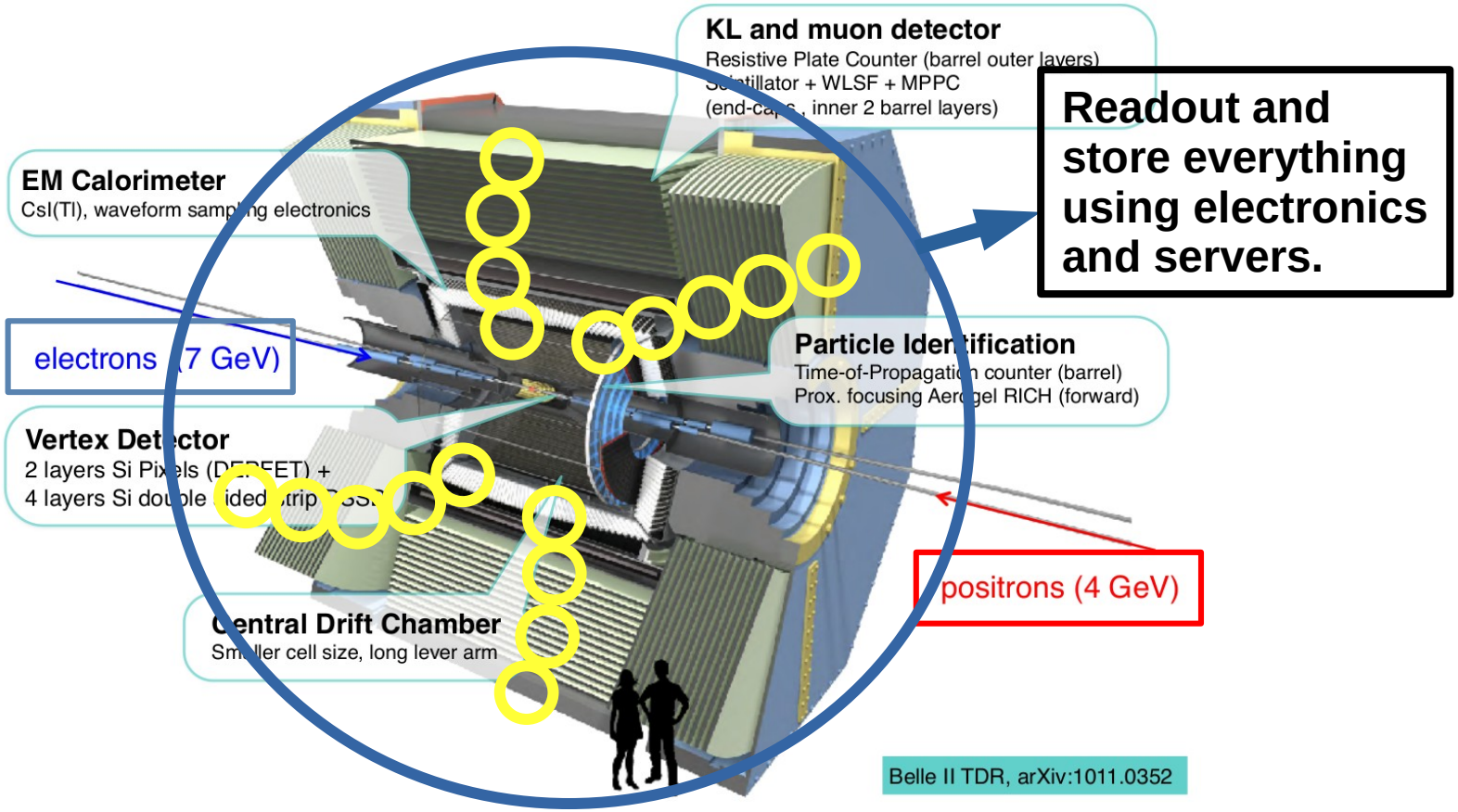
Data taking in HEP (cont'd)

- There are many different types of detectors to capture different types of particles
  - Crystal, PMT, plastic scintillator, sense wire, silicon, ...
  - Signal is generated in **O(10~100 ns)** after the particles flies through.

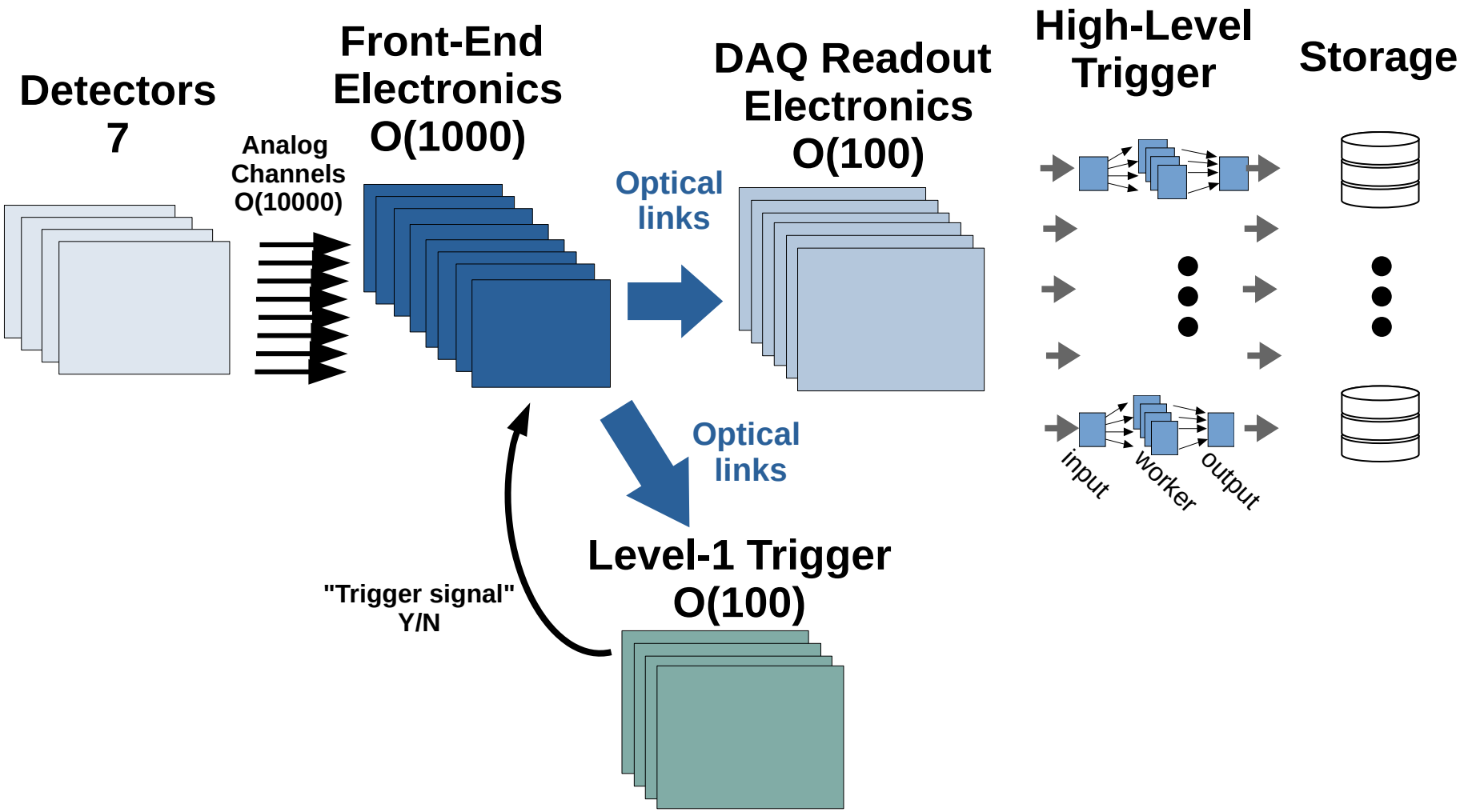


Data taking in HEP (cont'd)

- For all the signals from the detectors, the number of channels is O(10000).
- We will readout and store them by using electronics system and computing servers.
  - "Data acquisition" (DAQ).
  - Fast data collection and processing in real-time and limited latency.



Data flow in Belle II DAQ



Data flow in Belle II DAQ (cont'd)

Mostly FPGA!

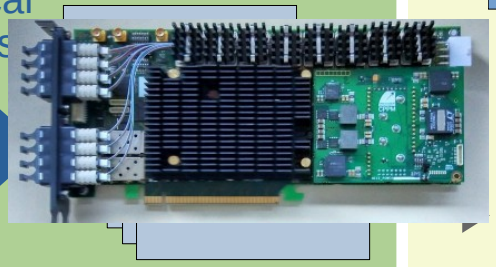
Detectors
7

Analog
Channels
O(10000)

Front-End
Electronics
O(1000)

Optical
links

DAQ Readout
Electronics
O(100)



Optical
links

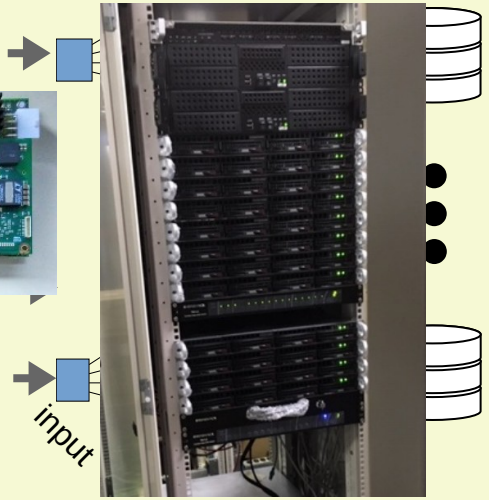
"Trigger signal"
Y/N

Level-1 Trigger
O(100)

Computing servers

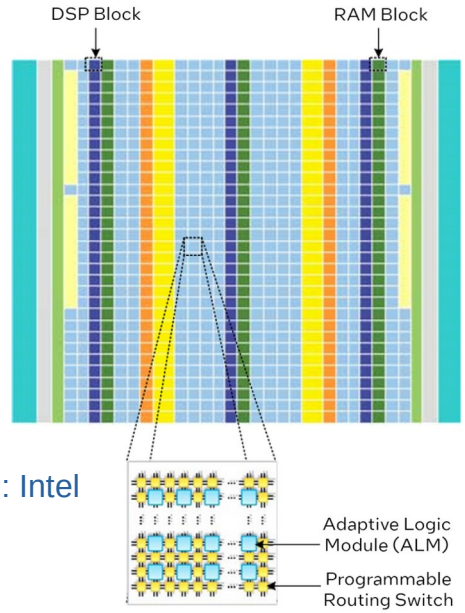
High-Level
Trigger

Storage



FPGA

- FPGA: Field-Programmable-Gate-Array
  - Configurable integrated circuit
  - Array of programmable logic cells interconnected to each other. Based on the user's design using Hardware Description Language (HDL), the logic cells' array will be configured to realize different digitized logics.
  - Programmable: better flexibility.
  - High speed, small latency.
  - Application in industry: Aerospace, military, telecommunication, video/image processing, data center, etc.



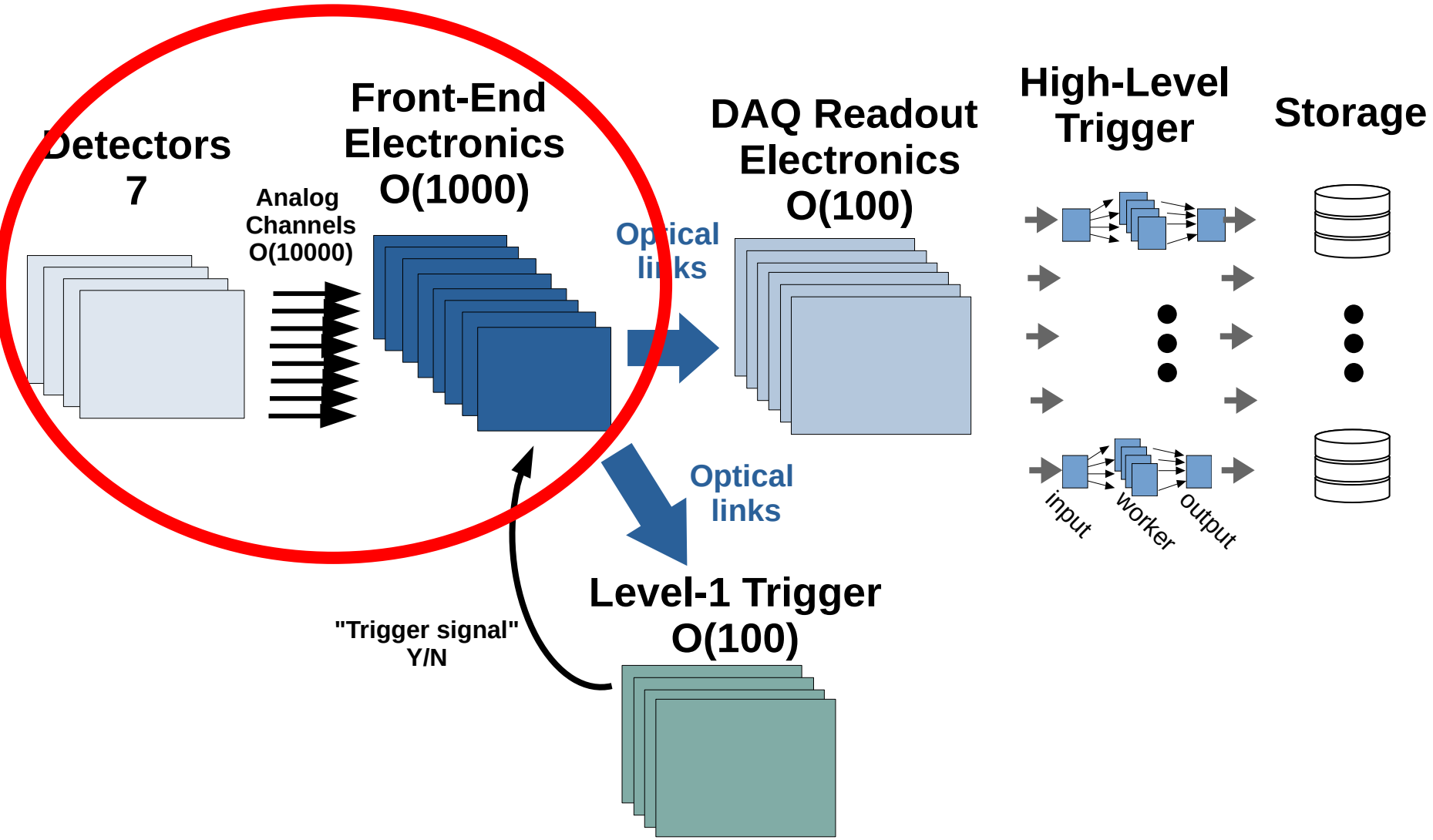
source: Intel

- Why FPGA in HEP?
  - Fast processing on large amount of data in real-time and limited latency.
  - Flexibility on the processing design.

source: AMD Xilinx

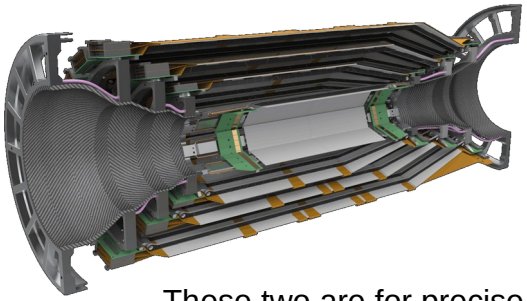
Versal series:
One of the latest product from AMD Xilinx for high-end application

Data flow in Belle II DAQ

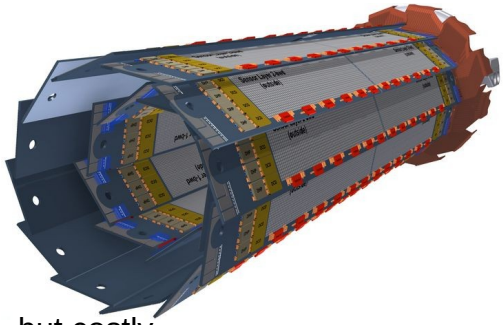


Detectors in Belle II

- Silicon Vertex Detector (SVD):
  - double-sided silicon-strip
  - Precise charged tracking.

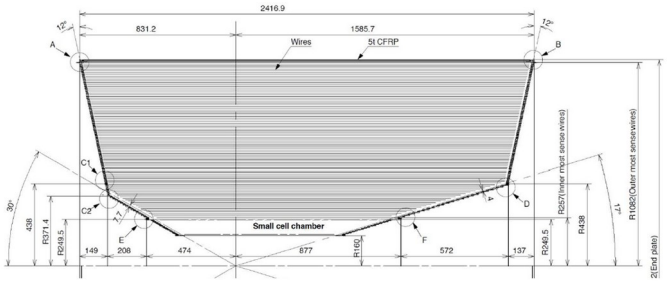


- Pixel Detector (PXD):
  - Pixelated DEPFET sensors
  - Precise charged tracking.

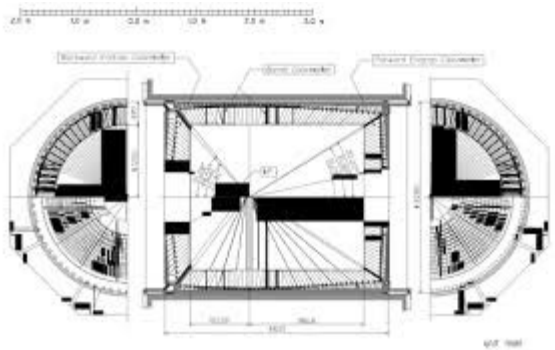


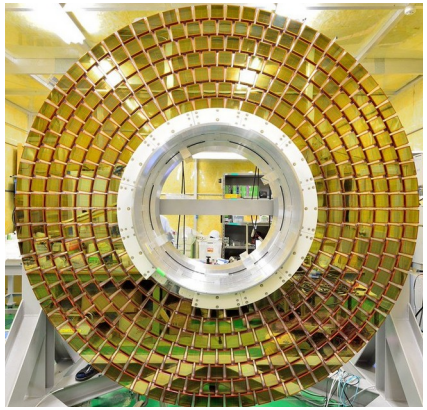
These two are for precise tracking, but costly, so usually at the inner-most region.

- Central Drift Chamber (CDC):
  - Wire chamber with ionization gas
  - Precise charged tracking.

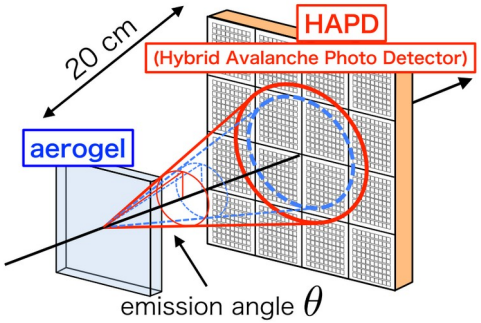


- Electromagnetic Calorimeter (ECL):
  - Array of CsI(Tl) crystal with PMT
  - For electronics and photon.





- Aerogel Ring Image Cherenkov Counter (ARICH):
  - For hadron identification.

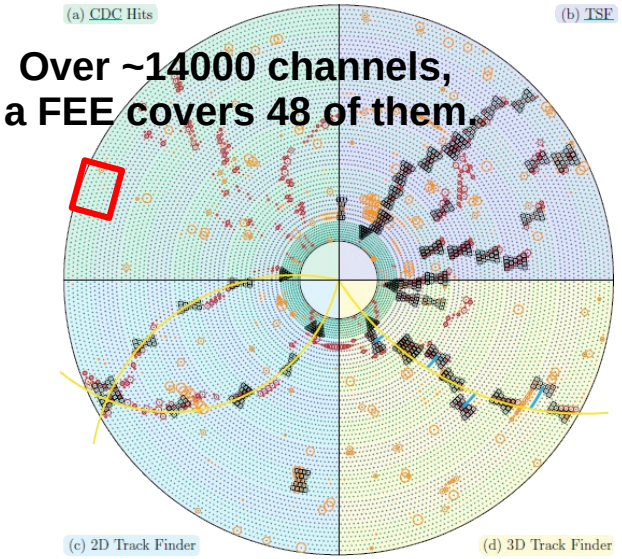


Front-End Electornics

- Front-End Electronics (FEE):
  - Readout the analog signals from detectors, and record the digitized signal.
  - A FEE receives a part of channels of an entire detector.
  - Near collision: Rad-hardness is critical.

- For different types of the detector sensors:
  - Sense wire, crystal+PMT, semiconductor, etc
  - Their analog responses are also different.
  - The design of FEE is hence dedicated.

- CDC:
  - ADC: custom designed ASIC.
    - Amp, ADC, shaping, TDC, ..
  - Xilinx Virtex-5 FPGA for digital signal processing.
    - Zero suppression.
  - Output to downstream: SFP and QSFP modules with FPGA MGT.

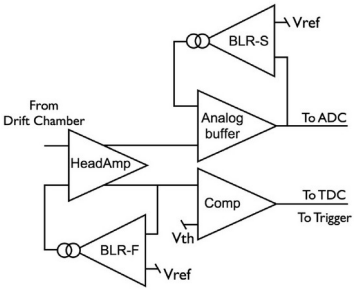


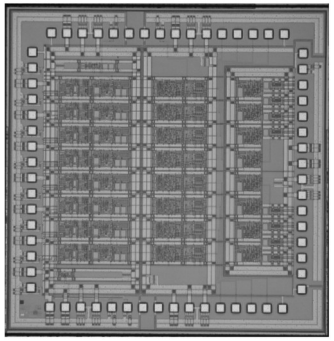
Over ~14000 channels, a FEE covers 48 of them.

Xilinx Virtex-5

Single channel

2.5x2.5 mm^2

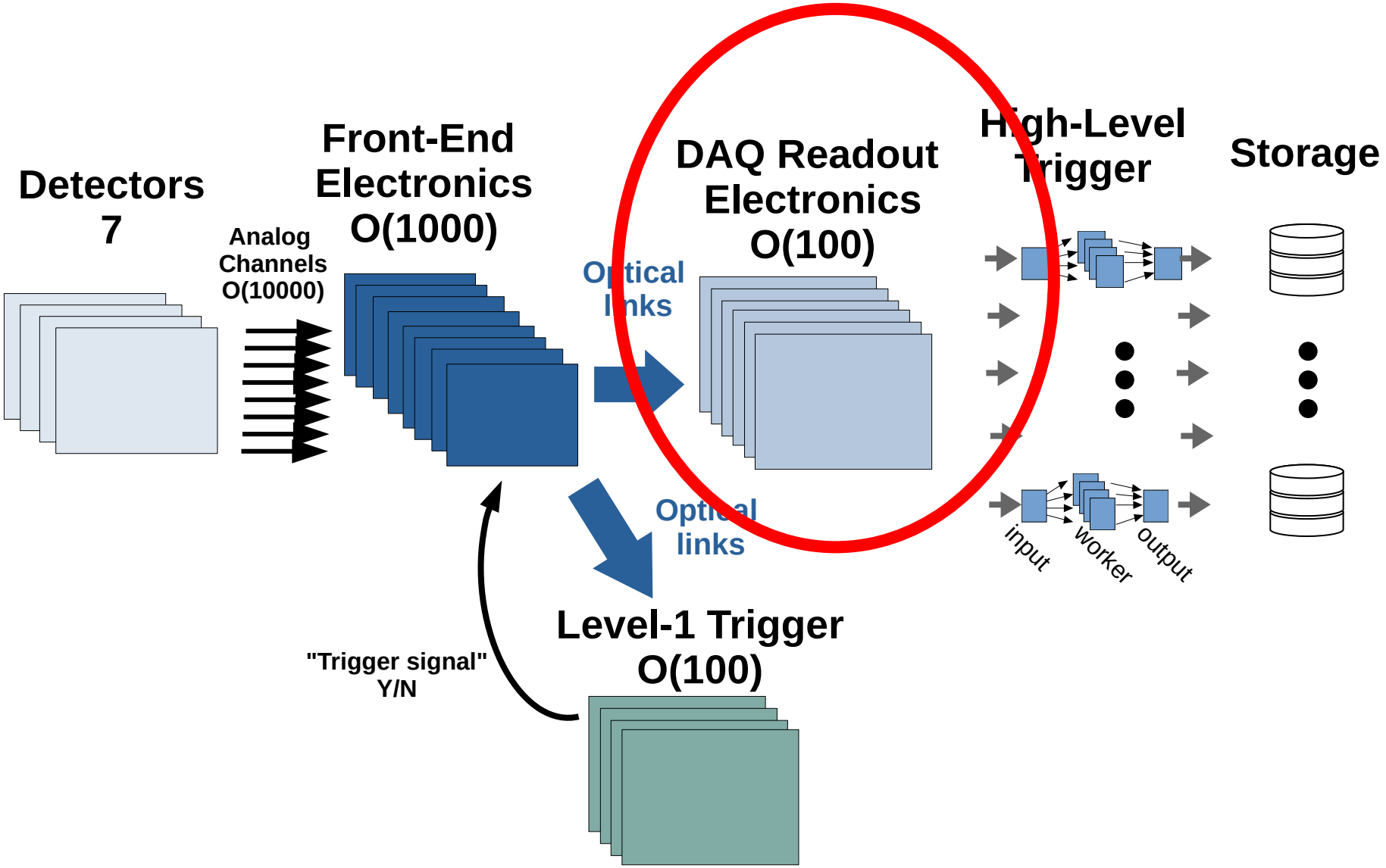




NIM A 735 (2014) 193-197

ASIC: CMOS 65nm

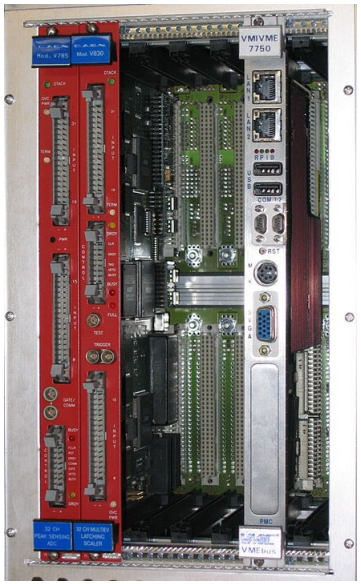
Data flow in Belle II DAQ



DAQ readout board

- Readout: receives data from O(10)~O(100) of FEE via optical links, performs event building, and transfer data from readout board (FPGA) to server (PC).

- Possible options for FPGA → PC:



VME

source: Wiki

ATCA

source: Wiki

GbE

source: Intel

PCI-Express

source: Wiki

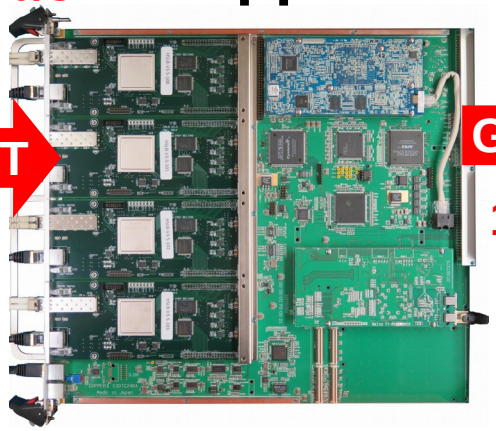
DAQ readout board in Belle II

- PCI-Express is the popular nowadays.
- The PCIe40 board was newly installed in Belle II in 2023.
  - ALICE and LHCb at the LHC have been using it.
- The upgrade project was carried out with collaborating KEK (Japan) and IJCLab-Orsay (France).

Copper

3.75 Gb/s /link

4xOPT



GbE

1 Gb/s

- 4 Xilinx Virtex-5 receiver boards.
- PrPMC: data procession, pre event building.
- In total **203 coppers** were used in Belle II.
  - **203 x 6 daughter boards**.

Upgrade

PCIe40

17.5 Gb/s /link

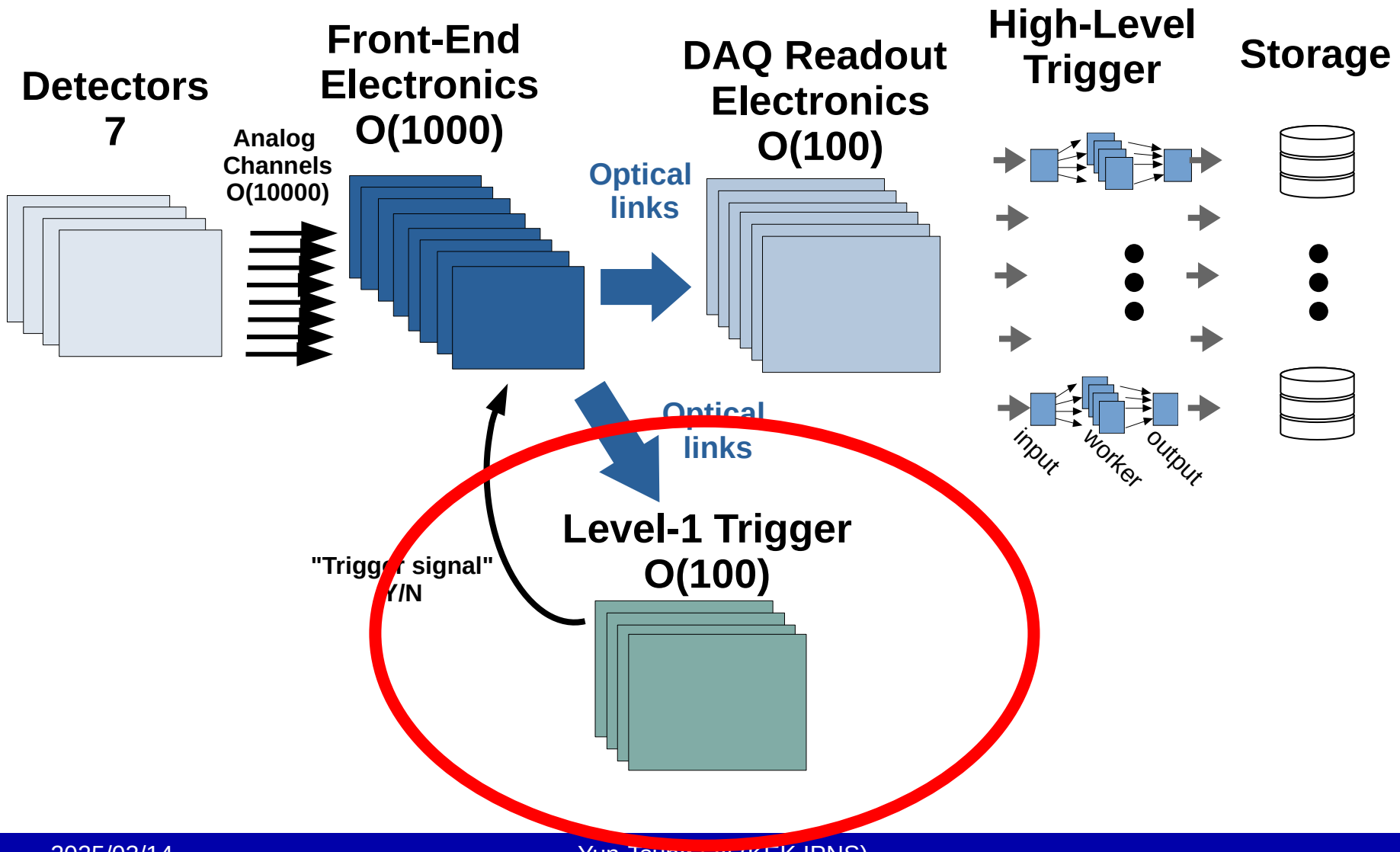
48xOPT

2x8 PCIe Gen3

16 GB/s

- Intel Arria 10.
- Developed in LHCb and ALICE.
- 48 optical links.
- 2x8 PCIe Gen3.
- In total **21 PCIe40 boards** are used in Belle II.

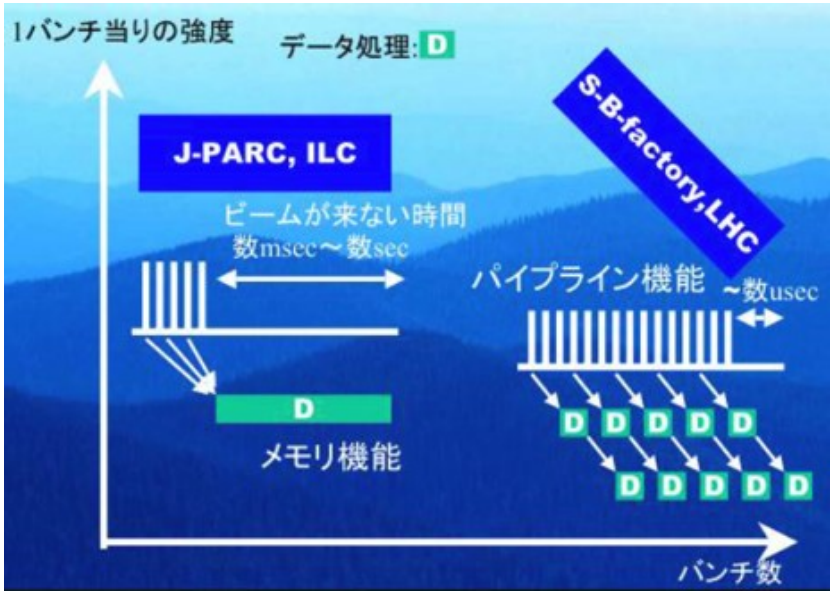
Data flow in Belle II DAQ



L1 trigger

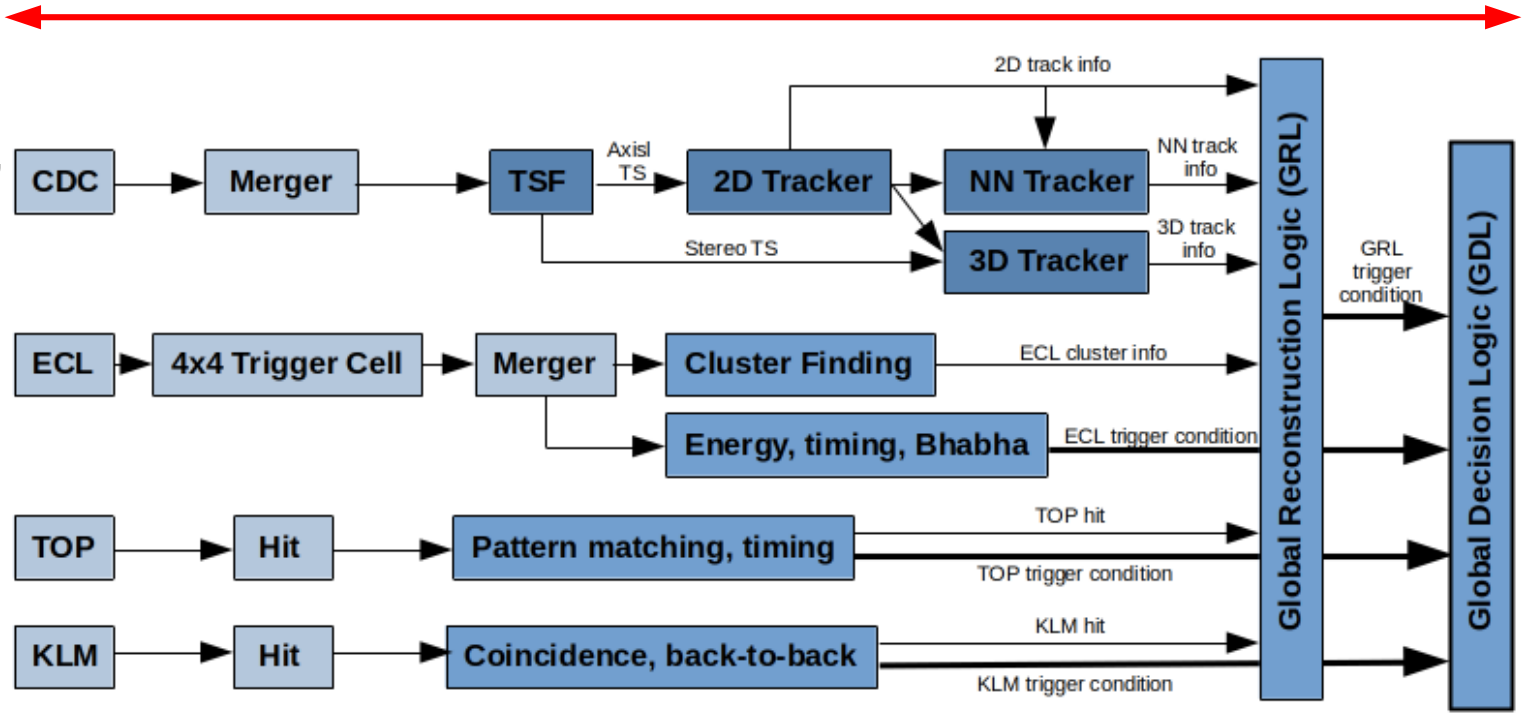
- Provide L1 trigger signal to DAQ using FPGA chips for real-time processing on detector raw data within limited latency (~5 μs).

- Why L1?
  - Buffer storage are not enough for all data due to high event rate and short bunch spacing in collider experiment.
  - But hardware-based trigger system design is complicated and costly.
  - Some of the experiments are based on trigger-less streaming DAQ: LHCb, ILC, nuclear experiments, etc.



Belle II L1 trigger

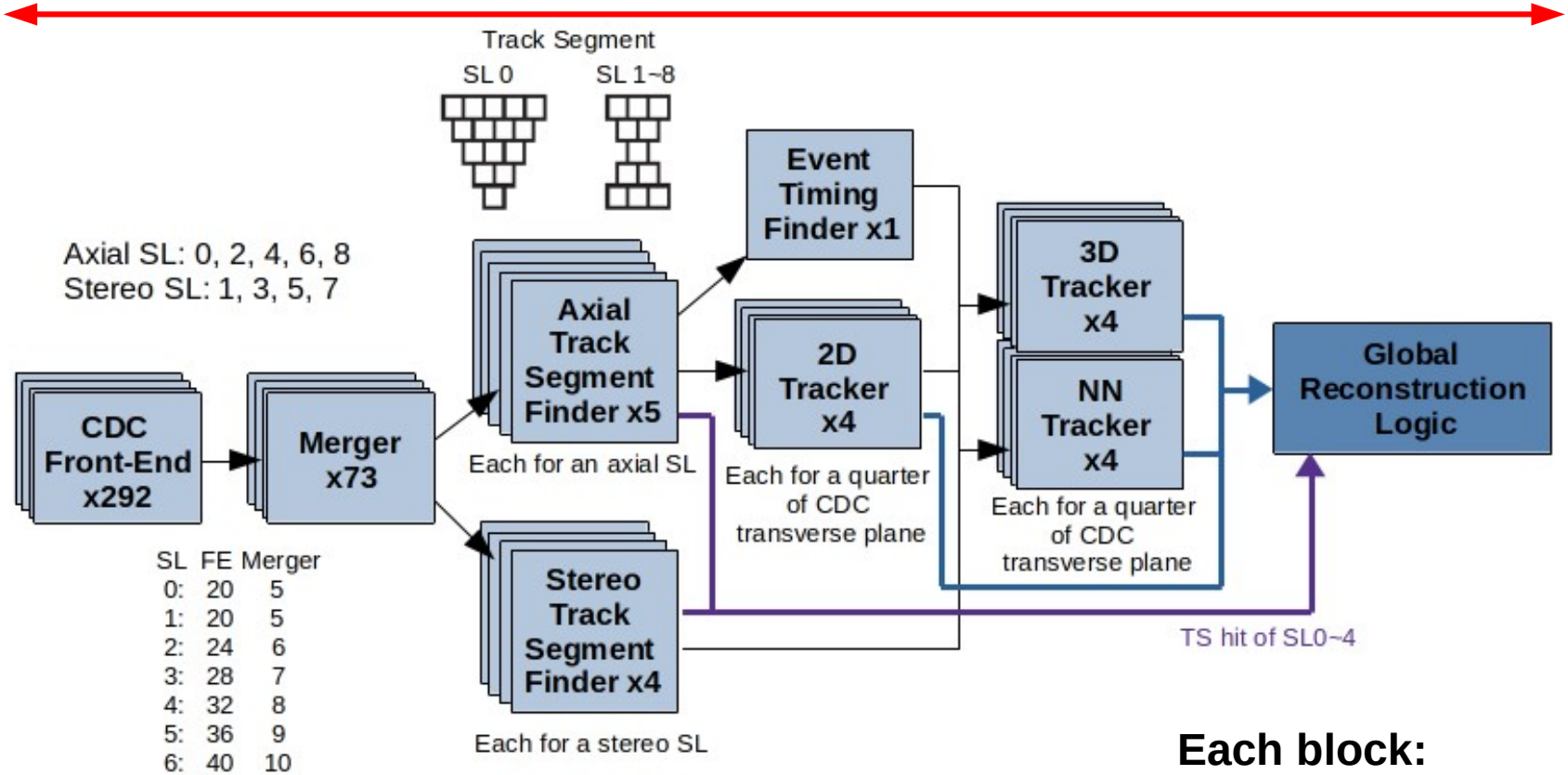
- 4 sub-trigger systems + 2 global trigger systems.
- Every block is FPGA boards with specific algorithm.
- Comprehensive trigger menu to select various kinds of physics events.
- Everything in this chain has to be finished **in ~5 μs**.



KEK, NTU, NCU

Belle II CDC trigger

- A sub-trigger system in Belle II with one of the detector.
- Everything in this chain has to be finished **in ~5 μs**.



Each line with arrow:
Optical link
(max. 25 Gb/s/link)

Each block:
A FPGA board with complicated algorithm logic design.

FPGA in L1 trigger

- For TRG purpose, complicated algorithm is implemented to process detector raw data in real-time. Utilization of machine-learning in the logic design became a trend recently.
- Strong FPGA with large resource: improve the logic itself, resolution of triggering, reduce the background rate, and perform everything within a latency limit.

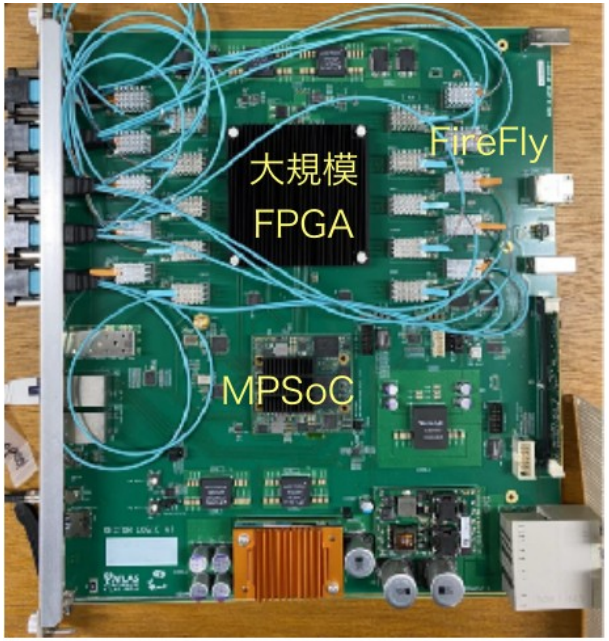
Belle II UT3

Xilinx Virtex-6
xc6vhx380t, xc6vhx565t
11.2 Gbps with 64B/66B

Belle II UT4

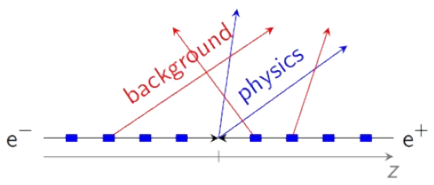
Xilinx UltraScale
XCVU080, XCVU160
25 Gbps with 64B/66B

ATLAS Muon Trigger processor

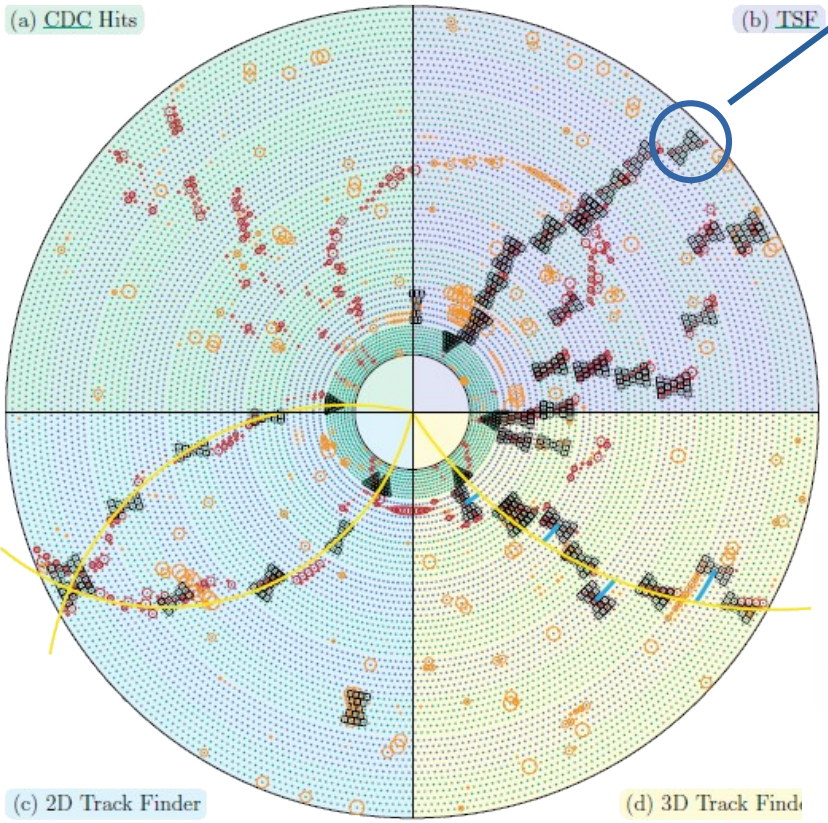


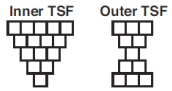
Xilinx UltraScale+
XCVU13P XCZU5EV
GTH,GTY: 16.8 Gbps
with 64B/66B

L1 track trigger algorithms

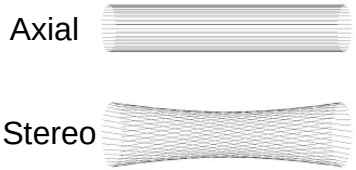


Tracking in L1 trigger

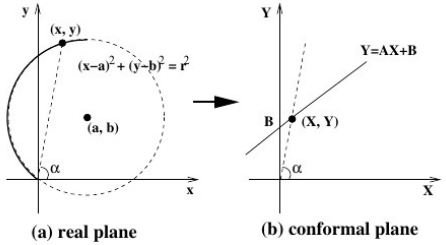




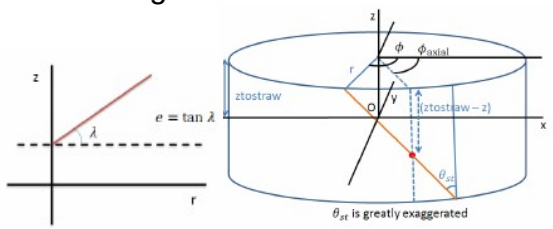
Track Segment:
Simplification on the algorithm

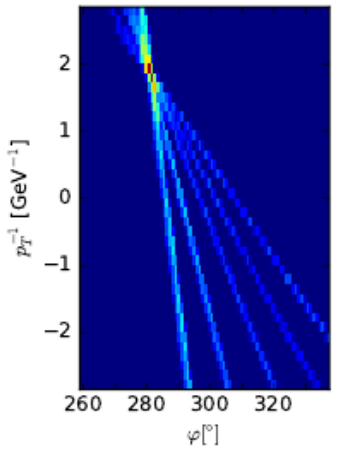


2D Track Finding:
Hough transformation.
Limited track condition.

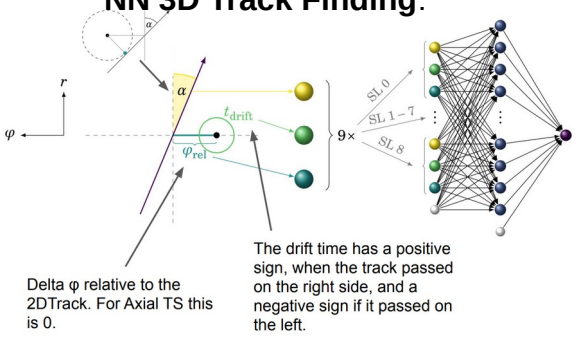


3D Track Finding:
Fitting with Stereo wire info





NN 3D Track Finding:

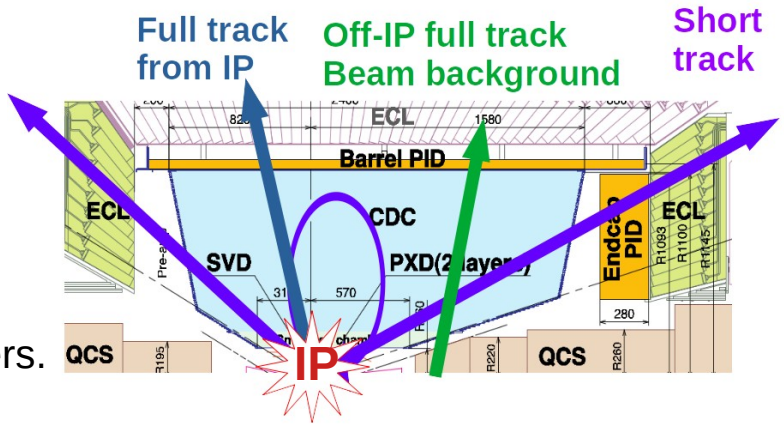


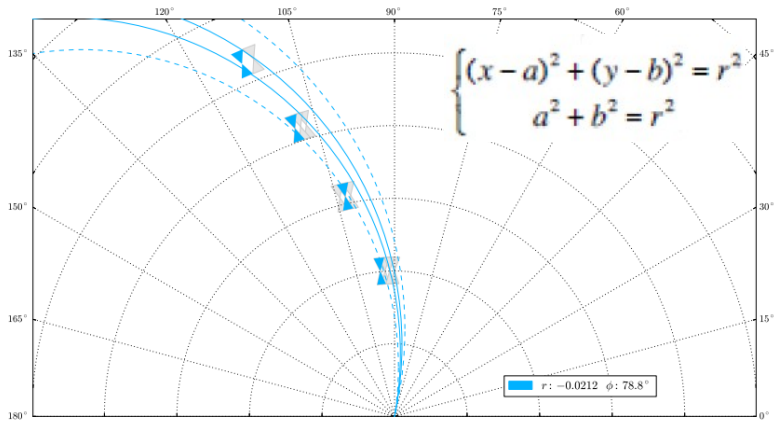
2D tracker: Hough transformation

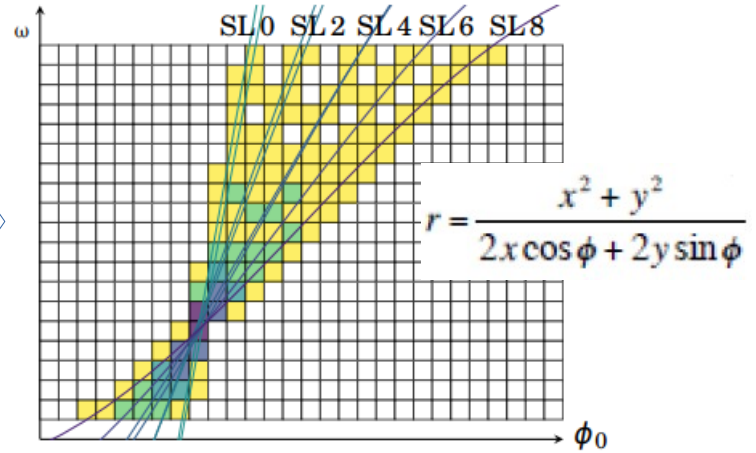
- Full track: The charged tracks which go through all of the layers of CDC.

- 2D algorithm: Hough transformation.
  - Assuming a circle.
  - TS from 5 Axial SL are transferred into 5 lines in the conformal plane.
  - Find the peak, which corresponds to track parameters.

T.-A. Sheng. Master thesis
https://doi.org/10.6342/NTU201802022
Ping Ni. Master thesis



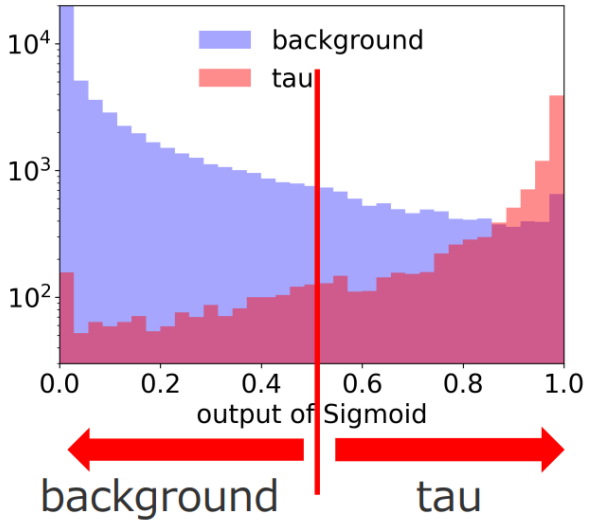




tau event trigger: NN

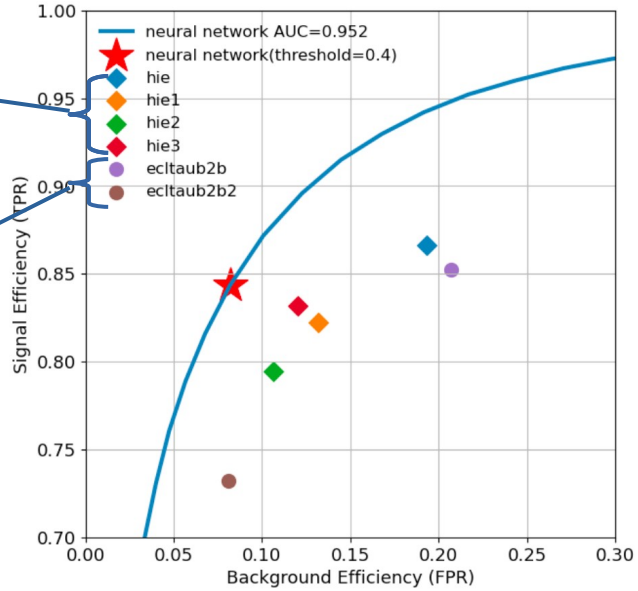
- In L1 trigger, not only the particle information from detector (charged track), but also the "physics event type" can be determined by ML in FPGA.
  - A very advanced logic in L1 trigger.

- ML tau trigger:
  - Input the position and energy information of clusters to a Neural Network, and determine if it is a tau event or not.
  - A kind of topological application.
  - Based on hls4ml.
  - Validated and will be implemented in 2024 runs.



hie: ECL energy sum

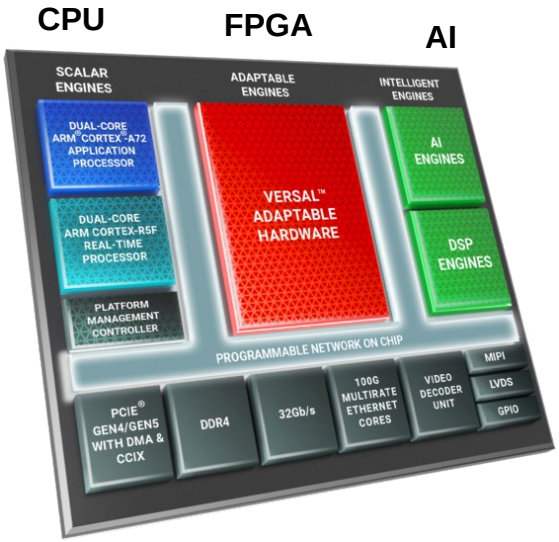
ecltaub2b: ECL cluster based logic

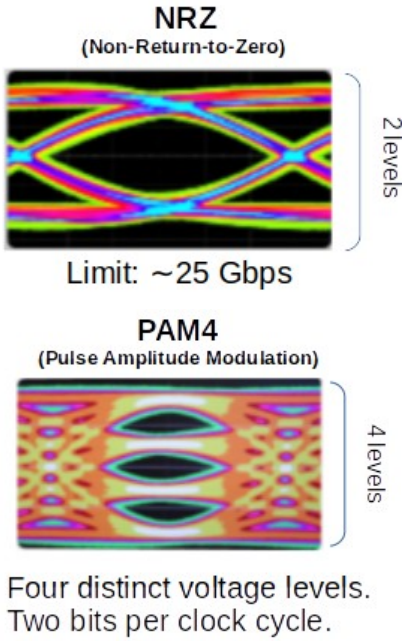


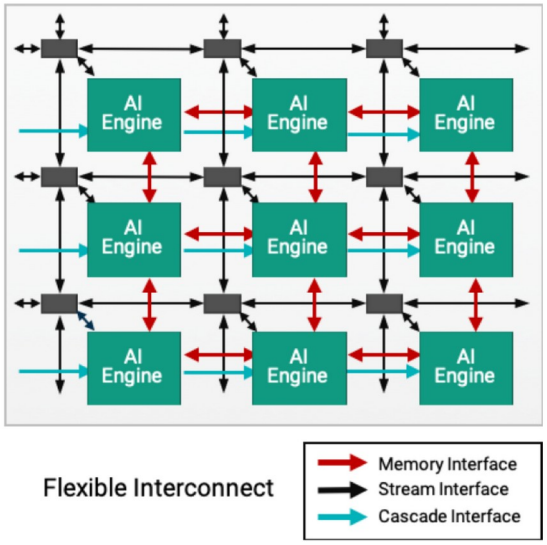
Toward the future: Versal ACAP

- Our group is targeting on using the Xilinx Versal ACAP for future electronics device's R&D. Now we plan to use Versal for L1 Trigger, DAQ or HLT purpose.

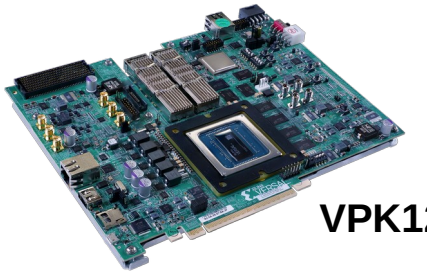
- The features of different Versal series ACAP:
  - AI engine, DPU: stronger computing engine for ML.
  - High Bandwidth Memory (HBM).
  - Larger number of cells + High transmission bandwidth.
    - PAM4, PCIe Gen5.

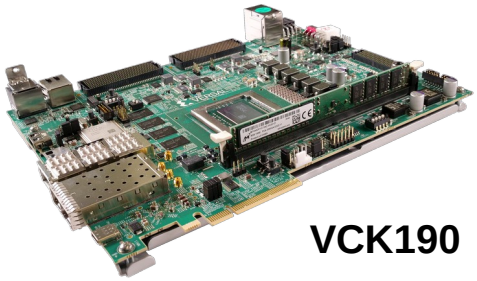






source: AMD Xilinx



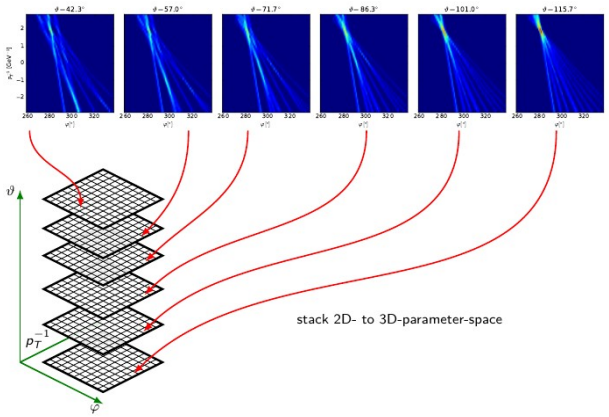


New ideas for L1 trigger

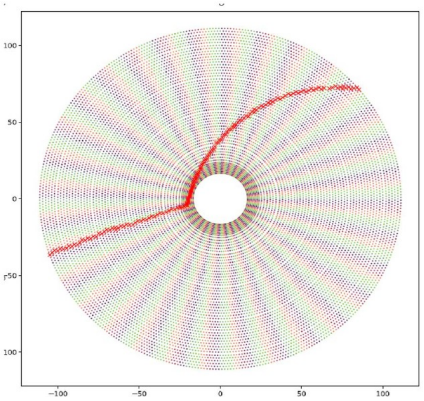
Karlsruher Institut für Technologie

S. Skambraks. Thesis

2D→3D Hough tracking:

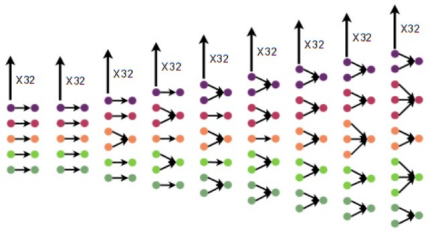


Displaced tracking with CNN:



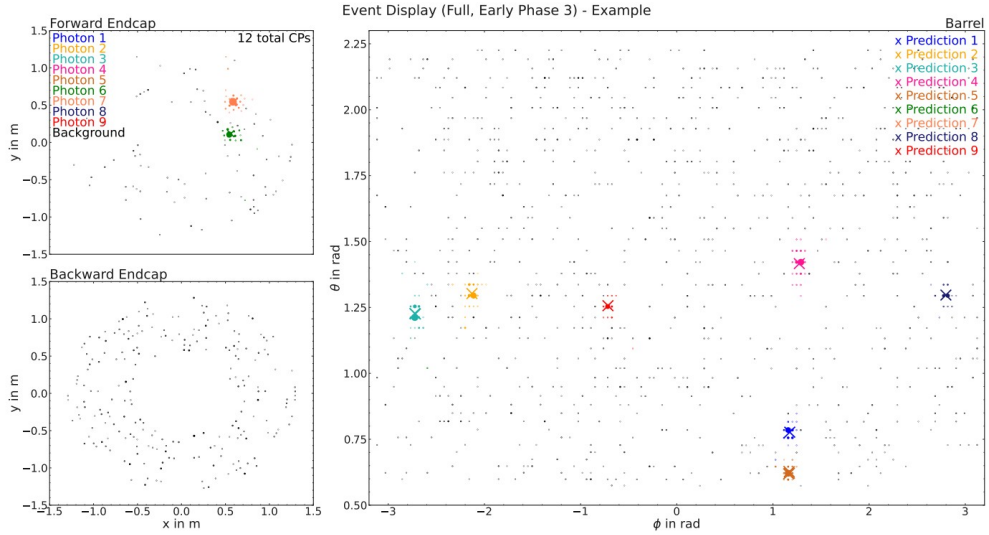
Aglining methode ploted on the CDC cross-section

SL	0	1	2	3	4	5	6	7	8
Sense wires	160	160	192	224	256	288	320	352	384
/ 32	5	5	6	7	8	9	10	11	12

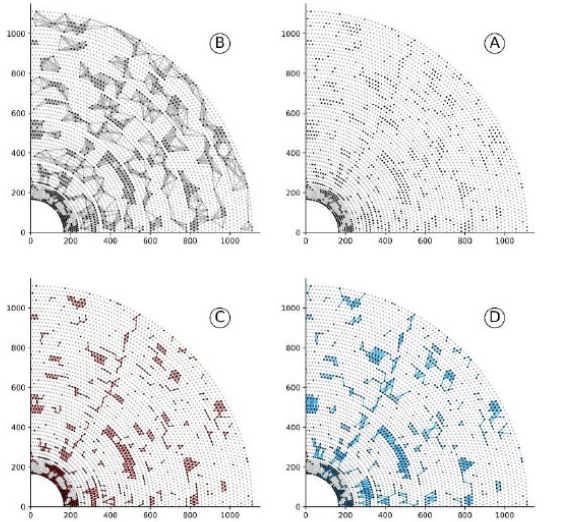


Proposed aglining methode with a agning width of 5 within each segment

ECL clustering with GNN:



Tracking with GNN:



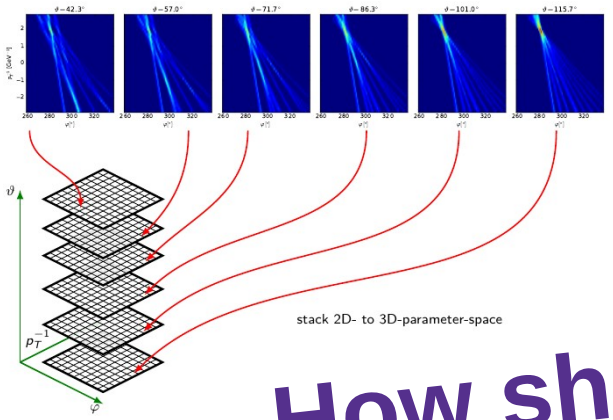
Dataset: displaced_processed_simulated_2_tracks_0_nominal-phase3

New ideas for L1 trigger

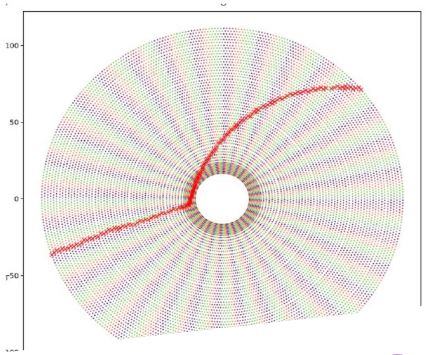
Karlsruher Institut für Technologie

S. Skambraks. Thesis

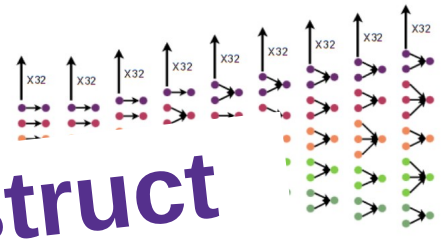
2D → 3D Hough tracking:



Displaced tracking with CNN:



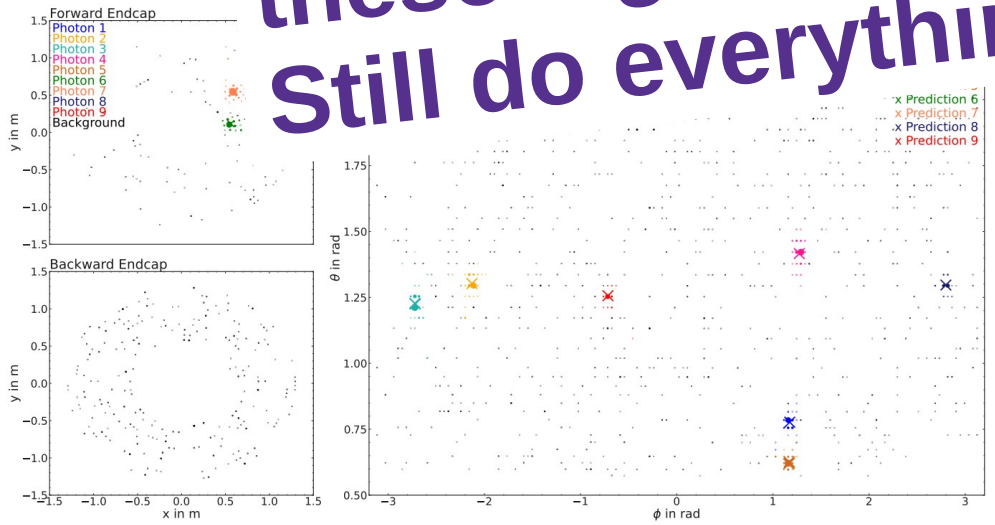
SL	0	1	2	3	4	5	6	7	8
Sense wires	160	160	192	224	256	288	320	352	384
/ 32	5	5	6	7	8	9	10	11	12

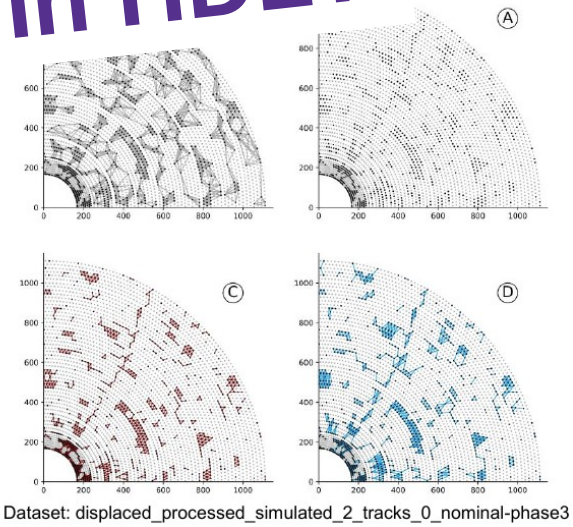


width of 5 within

How should we construct these algorithms in FPGA? Still do everything in HDL?

IN:

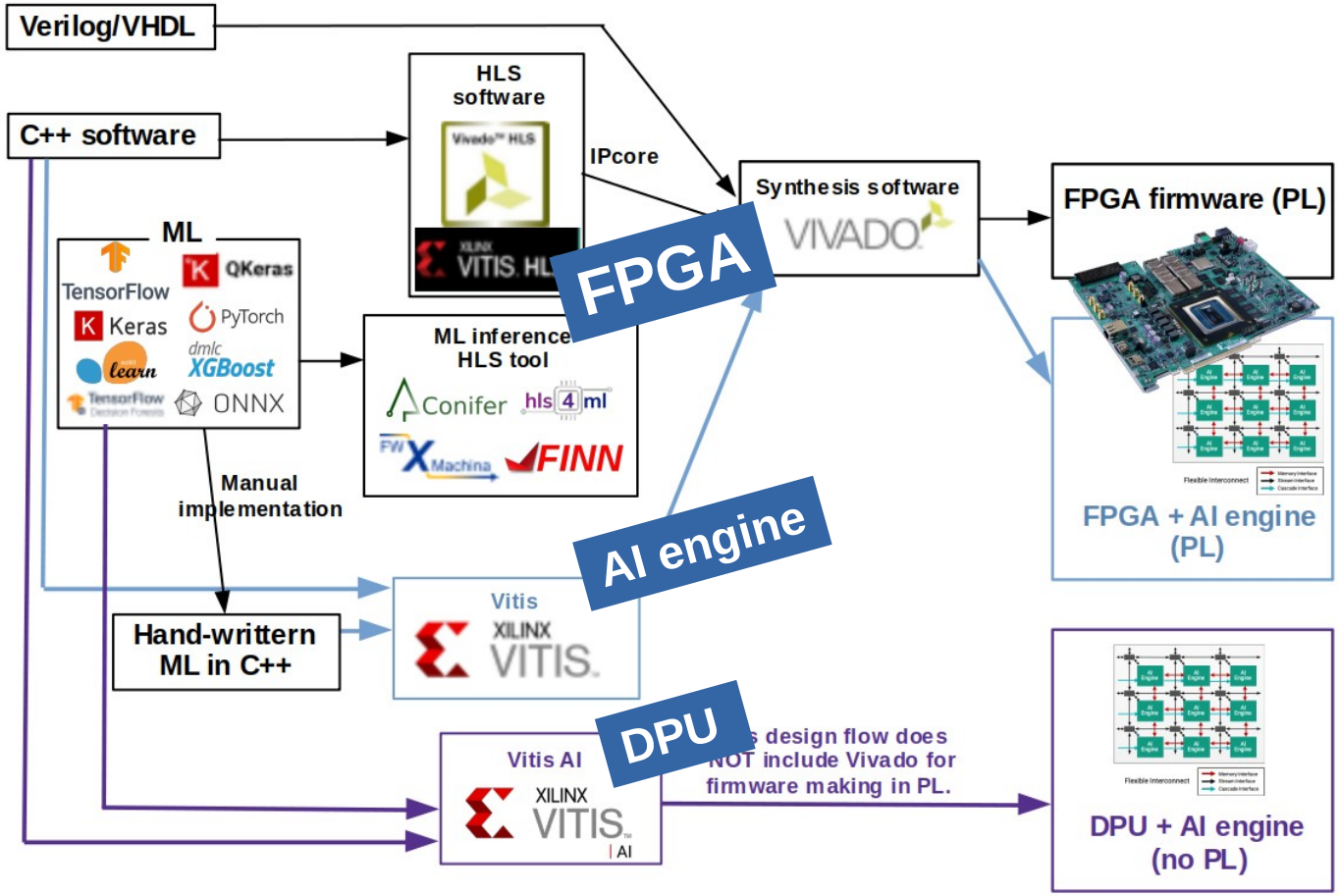




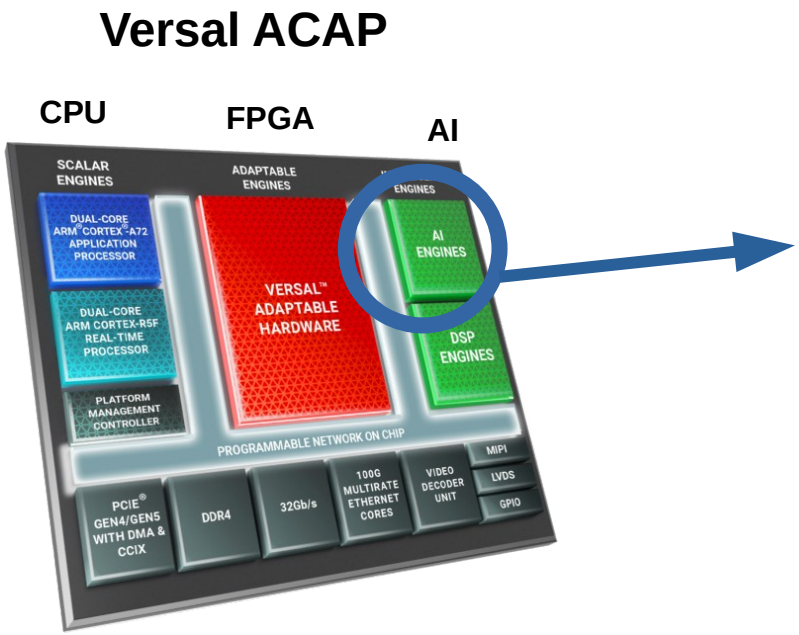
Dataset: displaced_processed_simulated_2_tracks_0_nominal-phase3

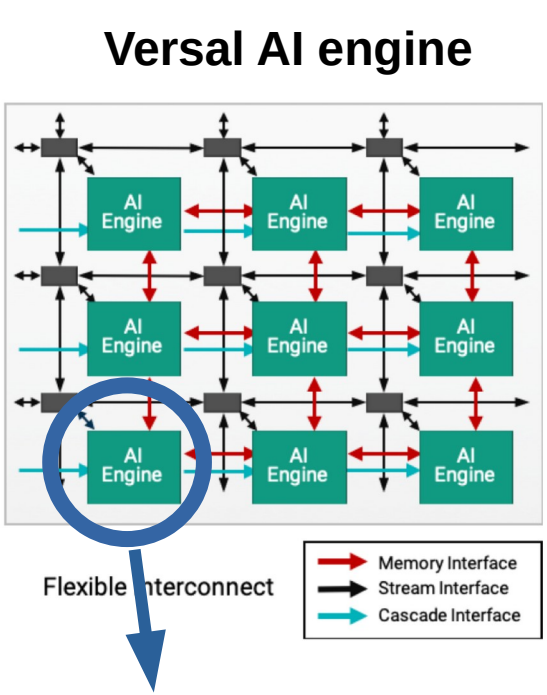
Algorithm development: HDL, HLS, ML, AI engine

- Other than writing HDL, we have more options to construct our algorithms: HLS, ML/AI, etc.
- We have been trying to go through each path in this map, and to build up a database of technical knowledge.
  - To support our experimental colleagues by proper documentations and hand-on lectures.
- We are mostly ready.

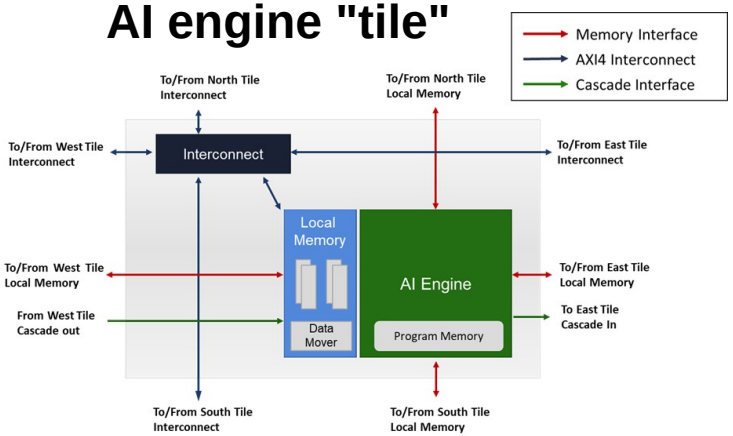


Versal AI engine



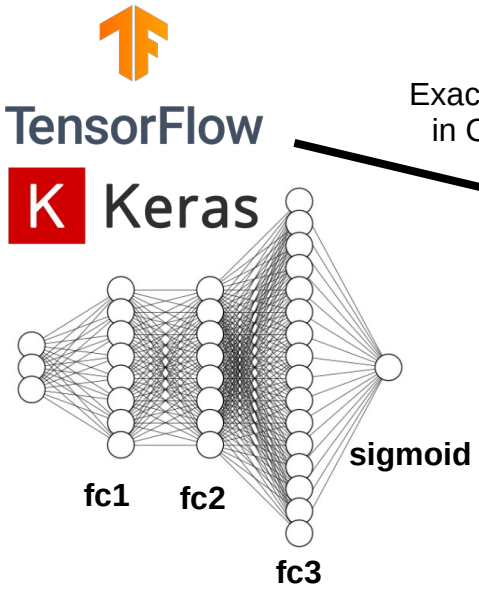


- Computation acceleration engine of Versal ACAP.
- Embedded processor of FPGA.
  - High bandwith between FPGA and AI engine.
- **C programmable**.
  - High precision.
  - No quantization loss on ML.
- **Low latency**.

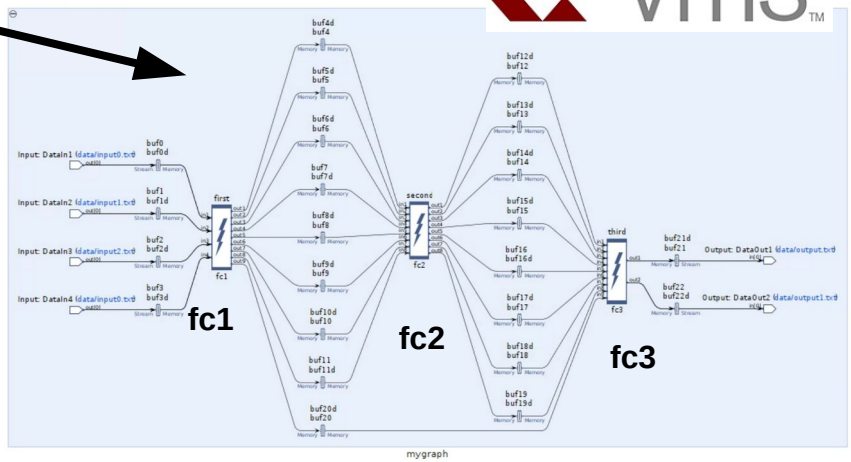


Versal AI engine: ML inplementation

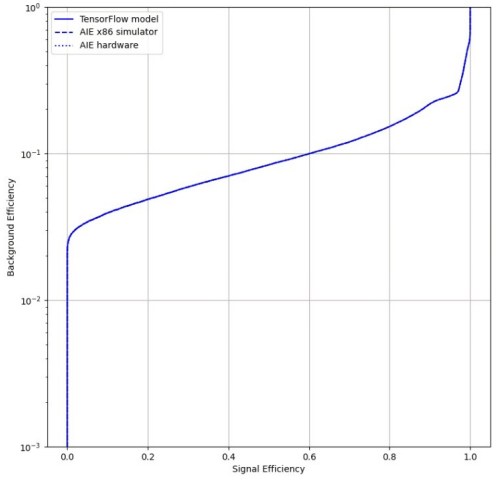
- We have been studying on the utilization of AI engine for the future application purpose.
- A NN model is built by Keras. 3 inputs → 3 hidden layers (8,8,16) → 1 output with sigmoid.
- Coding in C++ in Xilinx Vitis software.
  - **Everything for AI engine is in C++ and single-precision floating point.**
  - **No quantization loss.**
- **Latency: ~3 μs.**



Exact math form
in C++ in float



XILINX VITIS



Summary

- In the field of experimental particle physics, we utilize FPGA device to process high-rate data from detector in real-time in many different aspects. Our research group is working the R&D of various kinds of FPGA devices.
- Front-End Electronics: Interface to analog signals with using manual ASIC.
- DAQ: Data collection and transfer to PC via GbE, PCIe, etc.
- Trigger: Real-time physics algorithms in FPGA within limited latency based on different methods: HLS, ML, etc.
- Regarding the prospect for upgarde, we also have a project based on fundamental investigation on the Xilinx Versal device.

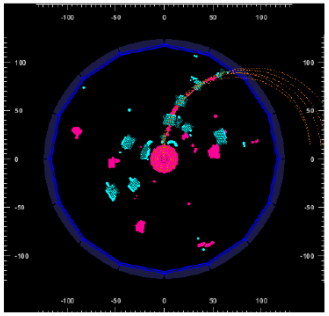
Backup

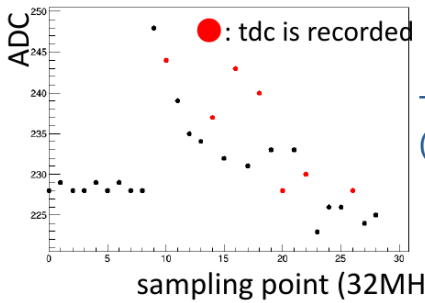
Considerations for FEE design/upgrade

- Newer FPGA chip: More resource for data processing and larger data output bandwidth.

- Usually, the FEE boards are close to collision: radiation damage as "Single-Event-Upset".
  - Radiation hardness is important for all the chips: FPGA, ASIC, optical modules, etc.
    - Hence, FPGA in FEE is usually not very strong one.
  - We can also choose to pull down all the channels, but number of cables will be huge.

- ASIC: Improve the performance, precision and reduce the "cross-talk noise".
  - Largely affects tracking performance



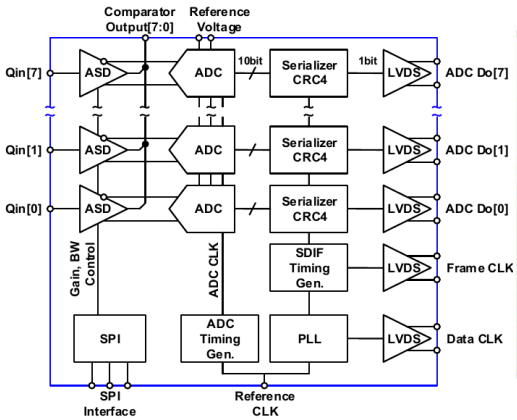


T. Koga *et al.* (KEK IPNS)

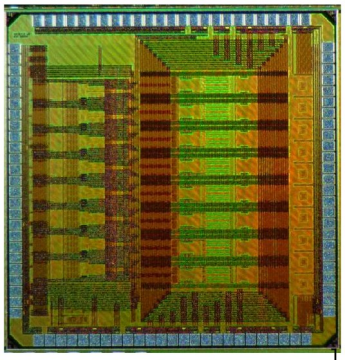
Xilinx Virtex-5

Upgrade

Xilinx Kintex-7



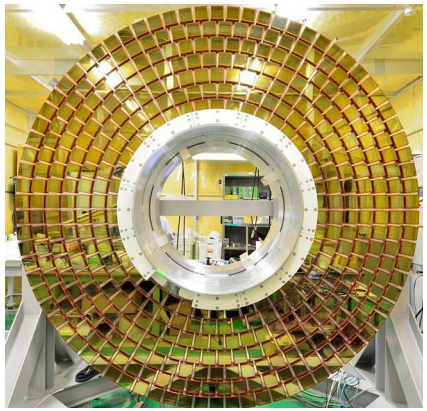
2x2 mm^2

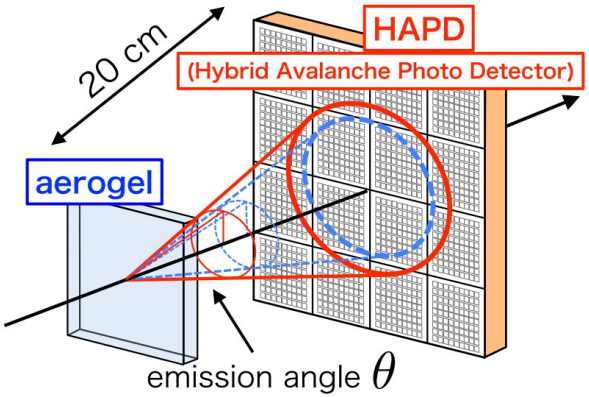


Designed by M. Miyahara (KEK IPNS)

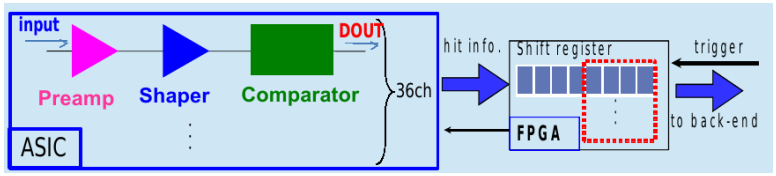
Different design of system: FEE + Merger

- Belle II ARICH detector:
  - Cherenkov ring image produced by the aerogel.



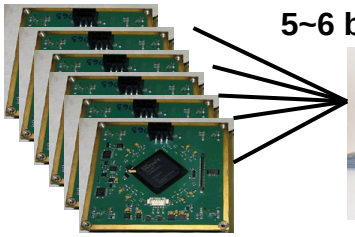


- FEE + Merger design
  - 1 ASIC: 36 ch
  - 1 FEE: 4 ASIC
  - 1 Merger: 5~6 FEE
  - Overall: 72 Mergers, 420 FEEs

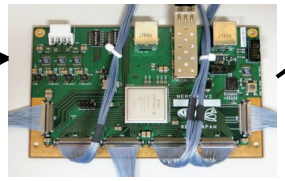


ASIC (36ch) design in FEE

4 ASIC/FEE



5~6 boards



Downstream

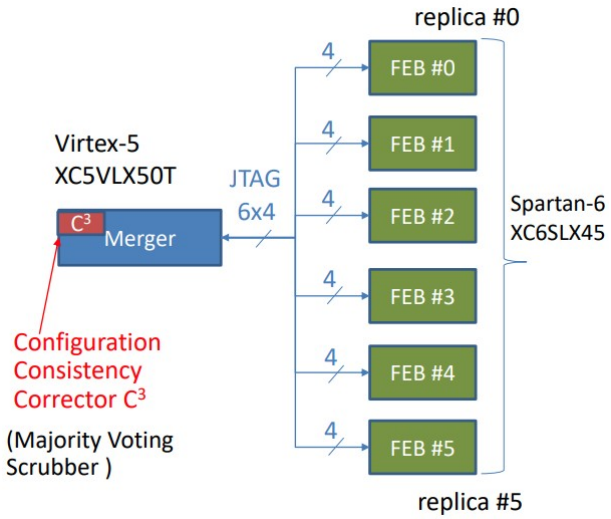
FEB
Xilinx Spartan-6

Merger
Xilinx Virtex-5

- Merger is served as a master to:
  - Configure/control/monitor the FEE.
  - Merge FEE data with zero suppression: effectively reduce the data size and number of links.

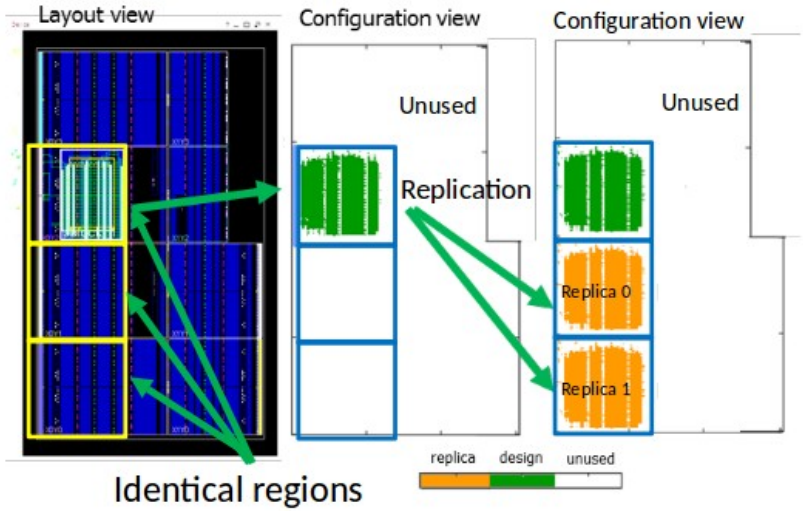
Different design of system: FEE + Merger (cont'd)

- Radiation damage on FPGA:
  - Single-Event-Upset (SEU): Transistor signal is inverted while high-energy particle hits.
  - One of the essential issue for electronics R&D of HEP.
- For Belle II ARICH, we expect to see 0.2/hr uncorrectable SEU error in peak luminosity.



R. Giordano *et al.*, Instruments 2019, 3(4), 56

- A special SEU correction design in ARICH:
  - Merger can readout the configuration frame of each FEE, and do majority voting on all.
  - Voting can find the redundant frame bit on which FEE.
  - Repair it in real-time by partial reconfiguration.
  - Does not require any manual operation.
  - Better performance than the Xilinx IPcore.



Conditions and requirements for TRG

- Requirements:
  - Overall latency < 4.4 μs.
  - ~100% eff. for hadronic events.
  - Max 30 kHz @ $8*10^{35}$ $cm^{-2}s^{-1}$
  - Timing precision: < 10 ns
  - Event separation: 500 ns
- Physics processes in interest:

- Examples of technical challenges so far:
  - Low-multiplicity trigger mainly based on ECL, but contamination from noise, beam bkg or Bhabha.
  - Energy trigger with high eff. but high rate too.
  - Injection bkg.
  - Drawback of track trigger at endcap.
  - High track trigger rate due to crosstalk noise.
  - Latency budget due to transmission or complicated logics.
  - .....

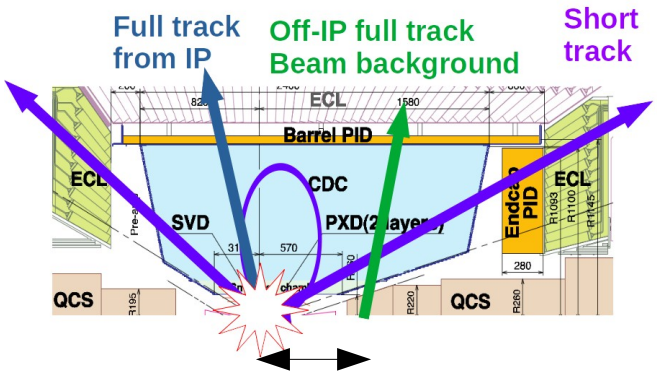
Phase2 Lum. Record

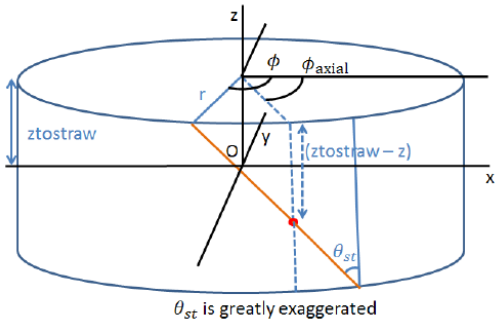
L1 trigger condition for Belle II: Depend on you physics target!

Process	C.S. (nb)	R@L=5.5x10^{33} (Hz)	R@L=8x10^{35} (Hz)	TRG logic
Upsilon(4S)	1.2	6.6	960	CDC 3trk(fff) ECL high energy(hie) ECL 4 clusters(c4)
Continuum	2.8	15.4	2200	
μμ	0.8	4.4	640	CDC 2trk(ffo) etc
ττ	0.8	4.4	640	
Bhabha	44	242	350 *	ECL Bhabha(bhabha, 3D bhabha)
γ-γ	2.4	13.2	19 *	
Two photon	13	71.5	10000	CDC 2trk(ffo) etc
Total	67	357.5	~15000	

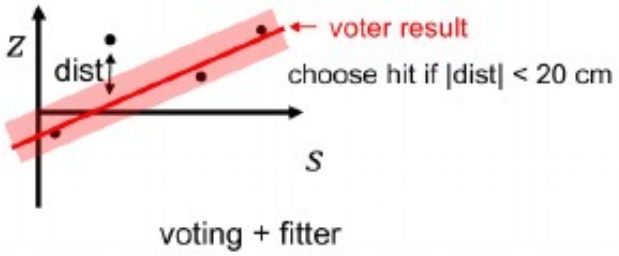
3D tracker

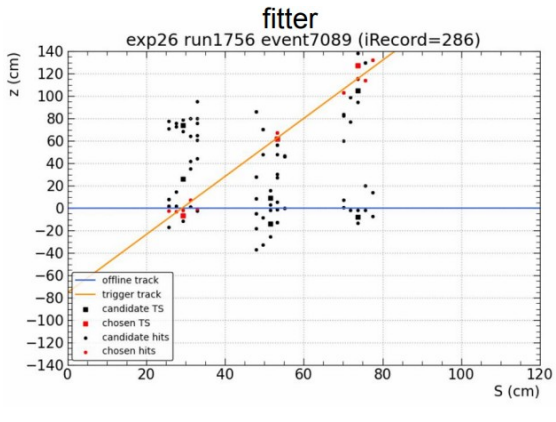
- Purpose: find the longitudinal displacement of a track (z_0) to separate the off-IP track, e.g. beam background.
- Based on the 2D track, and perform fitting on the 4 stereo SL TS.

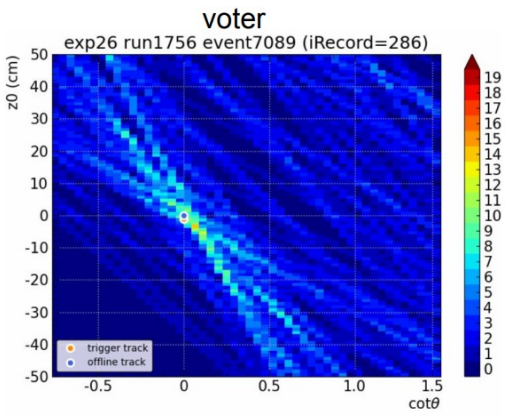




Cylinder: CDC
Gold: Sense wire
Dash line: The wire if stereo wire was an a wire.





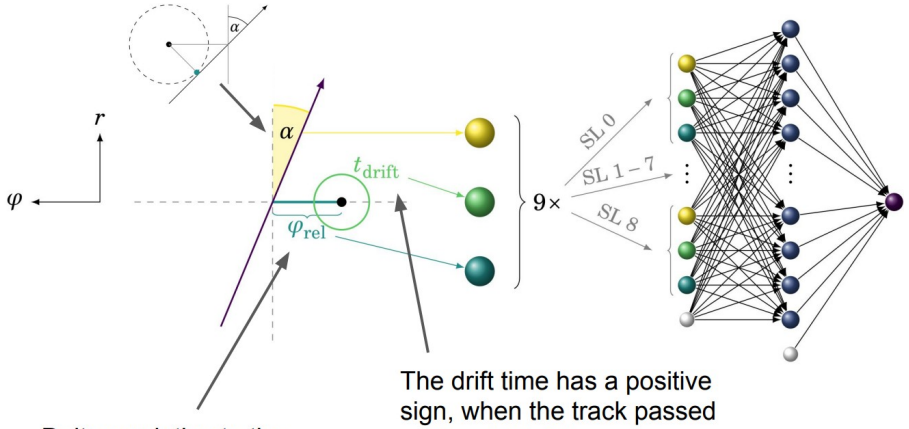


3D tracker with NN

Karlsruher Institut für Technologie

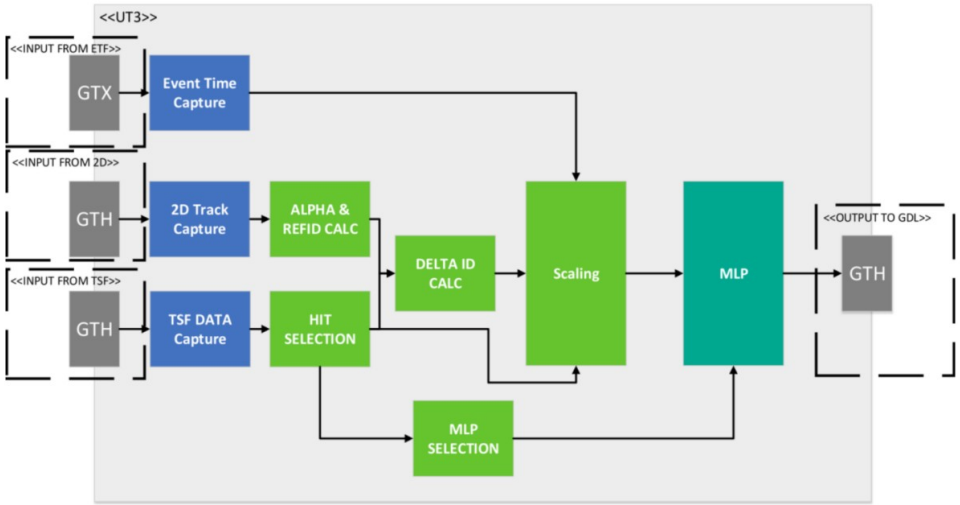
S. Neuhaus et al 2015 J. Phys.: Conf. Ser. 608 012052
Kai Lukas Unger et al 2023 J. Phys.: Conf. Ser. 2438 012056
F. Meggendorfer, DPG Conference 2021
Thesis: S. Skambraks, S. Pohl

- In addition to the conventional 3D tracker based on fitting method, Belle II has a Neural Network 3D tracker (NN) running in parallel in the system.
- Input the 2D tracker and stereo TS info
  - Crossing angle, drift time, φ relative to 2D Track .
  - Obtain z_0 and θ.
- NN is implemented in FPGA mainly with LUT.



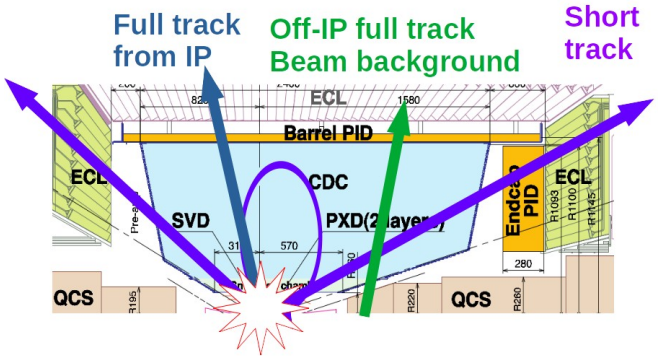
Delta φ relative to the 2DTrack. For Axial TS this is 0.

The drift time has a positive sign, when the track passed on the right side, and a negative sign if it passed on the left.

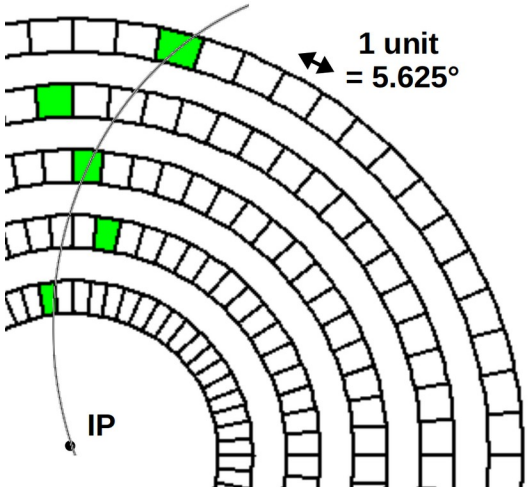


Short tracker

- The logic is implemented in part of the global trigger (GRL).
  - Use the TS of inner 5 SL (3 axial, 2 stereo).
  - Pattern recolonization over a 64 x 5 array. Simple design.
    - Consider the resource of FPGA device.
  - The logic is implemented as a LUT.

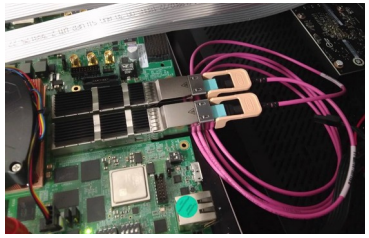


- Improve the angular acceptance of CDCTRG toward endcap.
- Also the curling-back tracks within the chamber: low-pt.

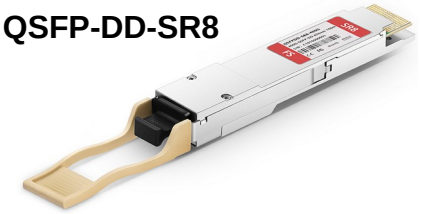


PAM4 study of Versal

- We have successfully tested the real transmission with PAM4 and QSFPDD:
  - QSFPDD-SR8 with MPO16, from FS company.
  - 53.125 Gb/s x 16 lanes.
    - Only this line rate is supported.

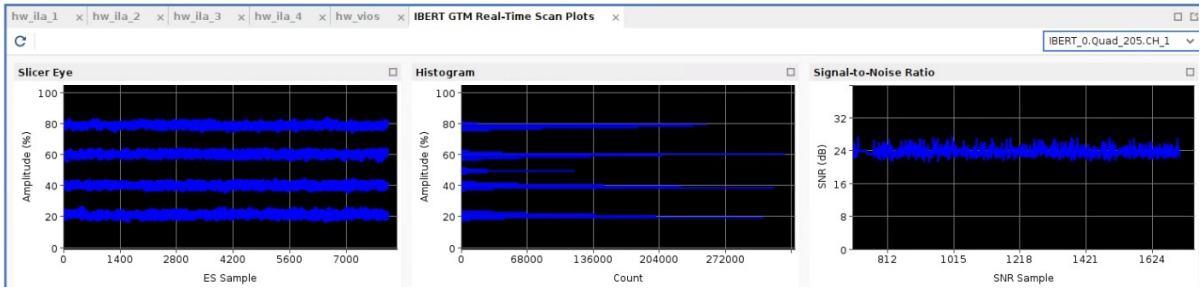


QSFP-DD-SR8

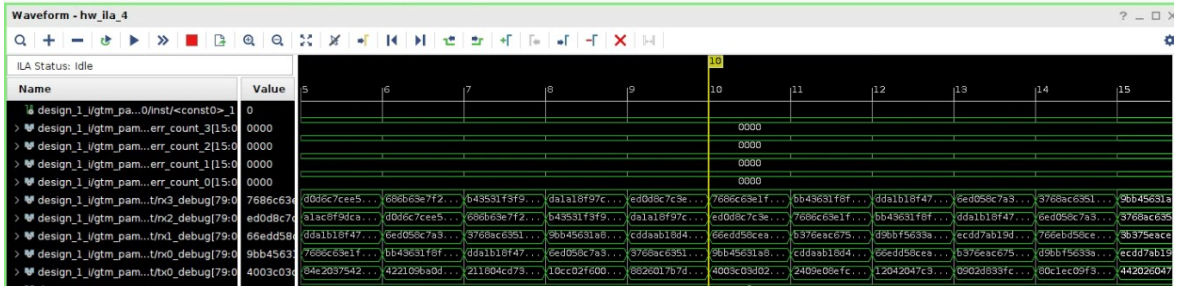


- 3-day BERT, Our self-designed protocol, PRBS16:
  - BER of the worst lane: **9.0×10^{-14}**
  - 16-lane combined BER: **6.7×10^{-15}**
  - Latency: **210~240 ns**

- Based on our experience, NRZ is usually O(10^{-16})
- This BER for PAM4 looksl acceptable.

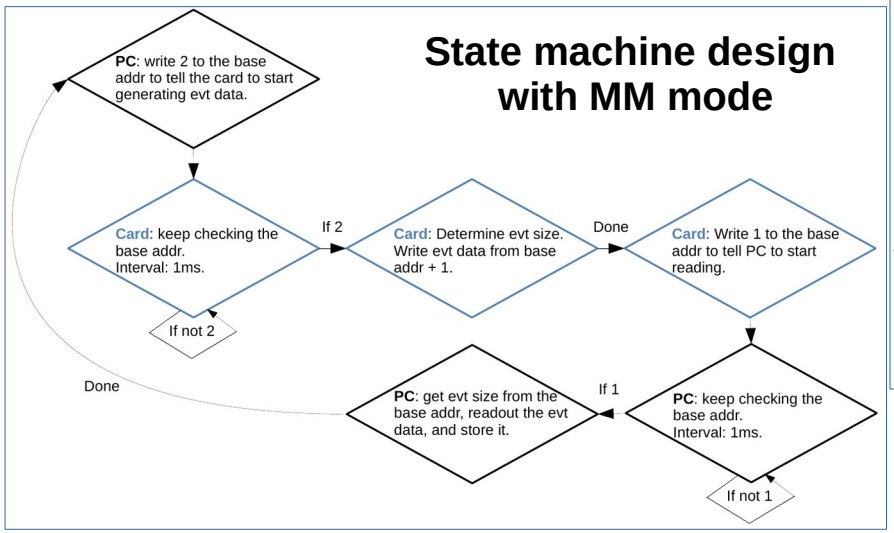


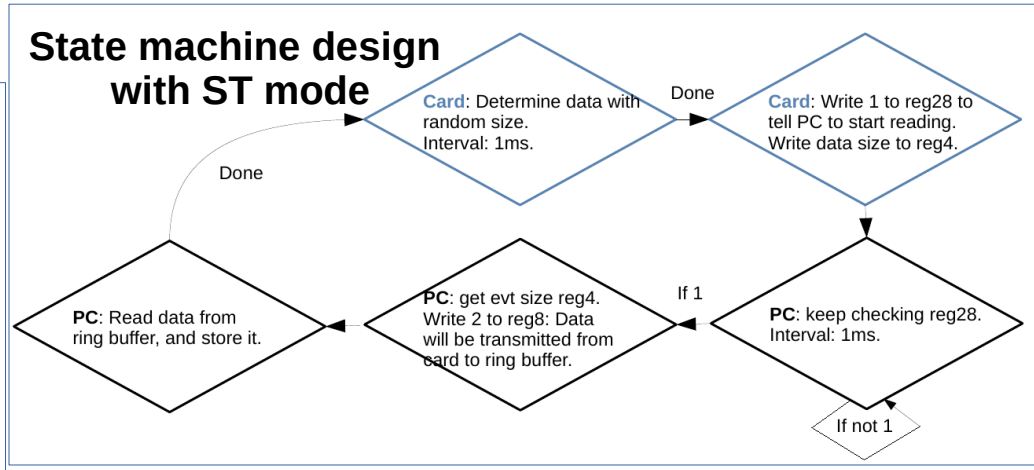
PRBS16 patterns



PCIe study of Versal

- State machine of the readout protocol between PC and FPGA.
  - Basically, handshake between PC and FPGA to know when is ready, what is data size, and when to take data.
- Random data size in the data generator.
- Not fully optimized yet: Long waiting time.
  - 1 ms waiting time in idle state to repeat.






```
root@cef01:/home/ytlai/versal/dma_ip_drivers-master_202311/QDMA/linux-kernel/apps/user-readout# ./user-readout -d /dev/qdma02000-MM
-2 -c 10
host buffer 0x1008, 0x5558ab141000.
evt filled
1 192 0 64
evt size:384 bytes
evt taking done
waiting...
waiting...
waiting...
evt filled
3 128 0 64
evt size:832 bytes
```

Manual readout software

Store event data with random size

```
512  3月   5 11:01 0.log
192  3月   5 11:01 10.log
512  3月   5 11:01 11.log
448  3月   5 11:01 12.log
384  3月   5 11:01 13.log
128  3月   5 11:01 14.log
  0  3月   5 11:01 15.log
  0  3月   5 11:01 16.log
  0  3月   5 11:01 17.log
576  3月   5 11:01 18.log
512  3月   5 11:01 19.log
448  3月   5 11:01 1.log
448  3月   5 11:01 20.log
```