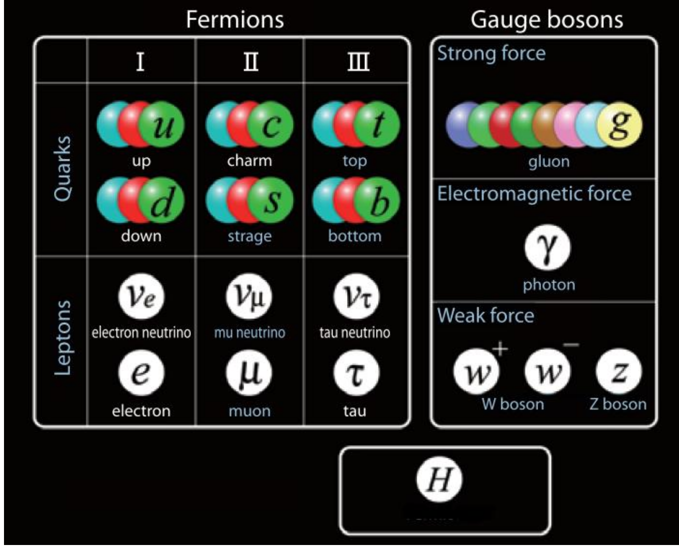
Belle II experiment and its data acquisition system

SATORU YAMADA(KEK)

Flavor physics (quark sector)



- There are three generations of quarks and leptons
  - Only difference of the generations
    -> Yukawa coupling with Higgs field
  - How a quark decays to another quark with different flavor
    - Cabibbo-Kobayashi-Maskawa matrix

$$\begin{bmatrix} d' \\ s' \\ b' \end{bmatrix} = \begin{bmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{bmatrix} \begin{bmatrix} d \\ s \\ b \end{bmatrix}$$

Questions in flavor physics

- Why three generations ?
- Why CKM matrix elements take the values ?
- CKM matrix is the only source of CP violation ?

Good probe for new physics

- Heavy flavor particle -> decay to lighter flavor particles
- Many suppressed decays in the Standard Model

Why B factory ?

B meson (b-quark)

- In the heaviest generation (top, bottom)
- Heaviest quark to form hadron

-> Many decay modes through different flavors

  - Large CP violation was expected
  - Rare decays suppressed in the Standard Model

- Energy frontier
  - Direct search of new particle
  - LHC (ATLAS, CMS experiments)

  -> Aim at production of “real” new particles

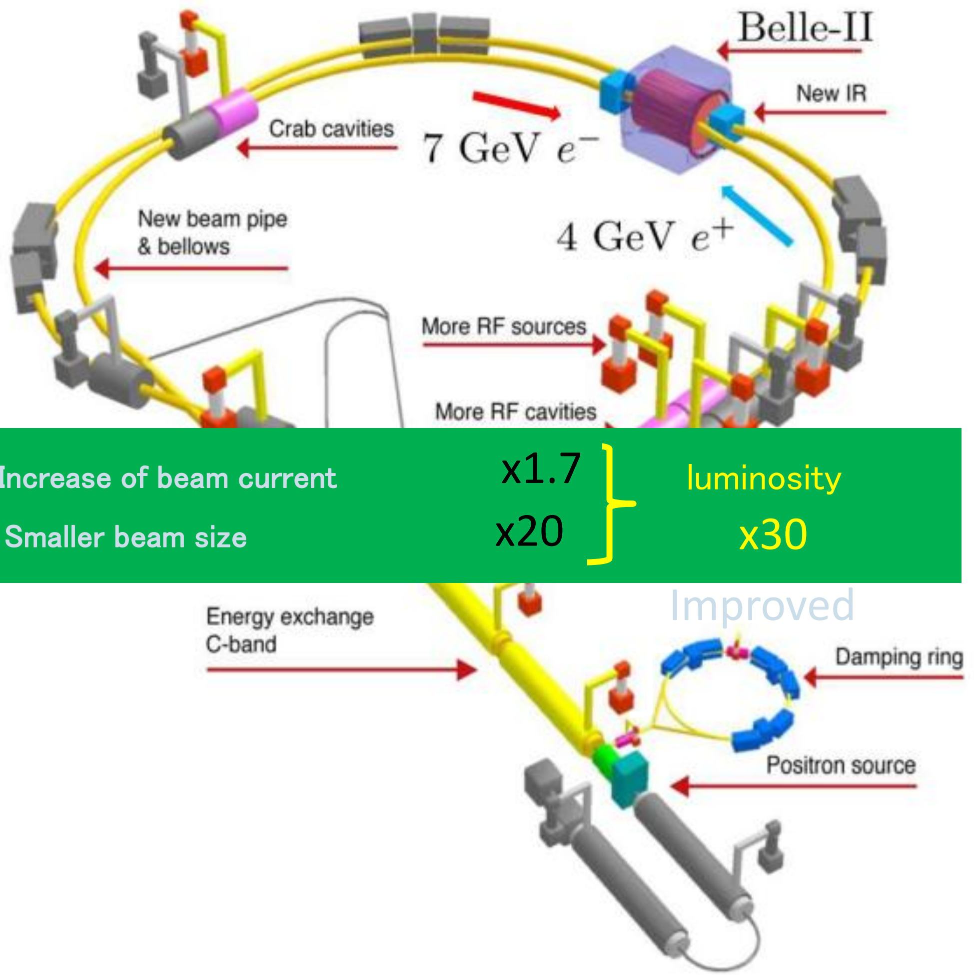
- Luminosity frontier (High precision measurement)
  - Indirect search of new particle
  - Hadron collider : LHCb
    - ➢ Cross section is higher than Belle II
  - B factory experiment : SuperKEKB (Belle II experiment)
    - ➢ Clean environment. Reconstruction efficiency is higher than LHCb

Belle II Experiment

➢ Search for new physics beyond the Standard Model(SM) via high precision measurement with high statistics samples of B/D/tau decays.

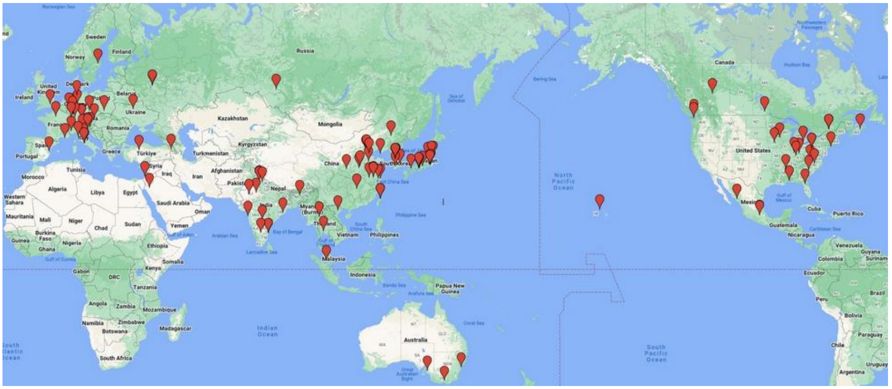
- **SuperKEKB accelerator**
  - Designed luminosity: 30times as large as KEKB
  - 50 ab^{-1} in ～10 years
    (cf. 1ab^{-1} @ Belle experiment)

Belle II collaboration :
>1000 collaborators from 27 countries and region
with many CPPM colleagues participating !



Increase of beam current	x1.7	luminosity
Smaller beam size	x20	x30

Belle II Collaboration Map



Belle II

Precise measurement of Unitarity triangle

Belle II : Unitarity triangle as a probe for new Physics

- If there is inconsistency in measurement of the triangle, it is expected that new physics beyond SM contributes it.

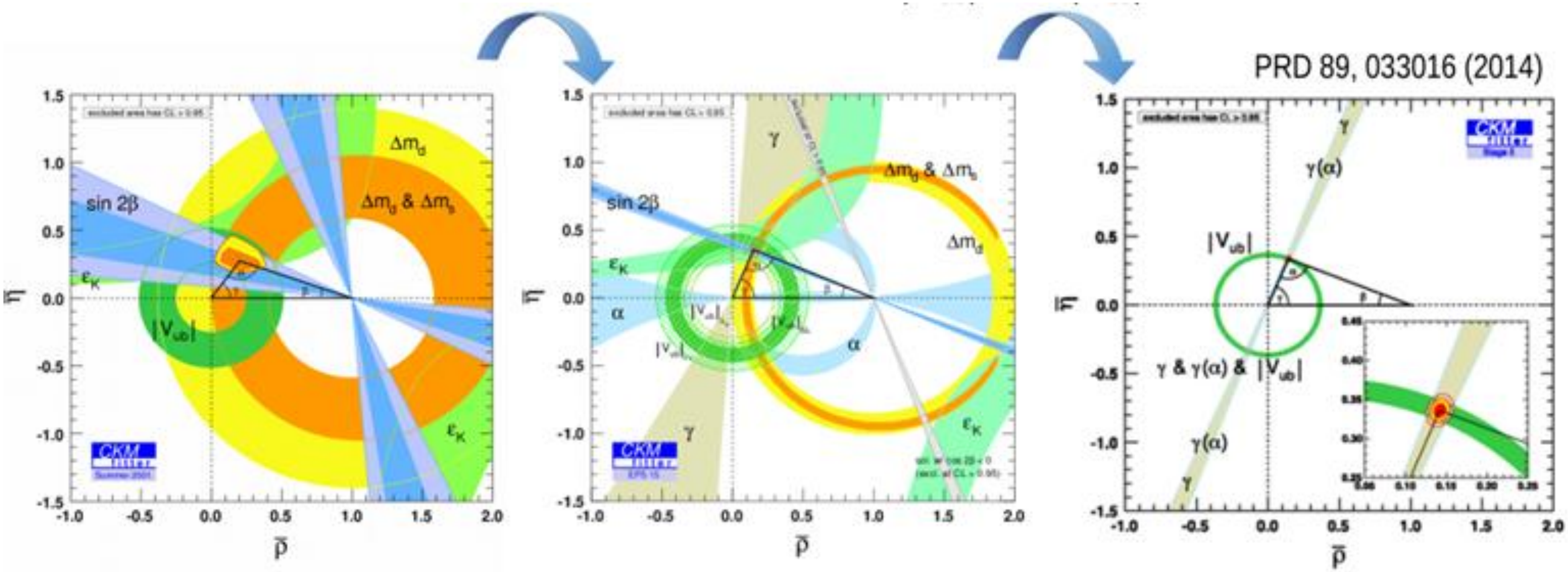
- Angle measurement :
  - Belle II 50ab-1 : $\phi_1(\beta) < 0.3^\circ$, $\phi_2(\alpha) < 1^\circ$, $\phi_3(\gamma) < 1.5^\circ$
  - If the triangle does not close -> New physics
- Sides of the triangle
  - To resolve tension between inclusive and exclusive measurements of $|V_{ub}|$

Before B-factories

Current status

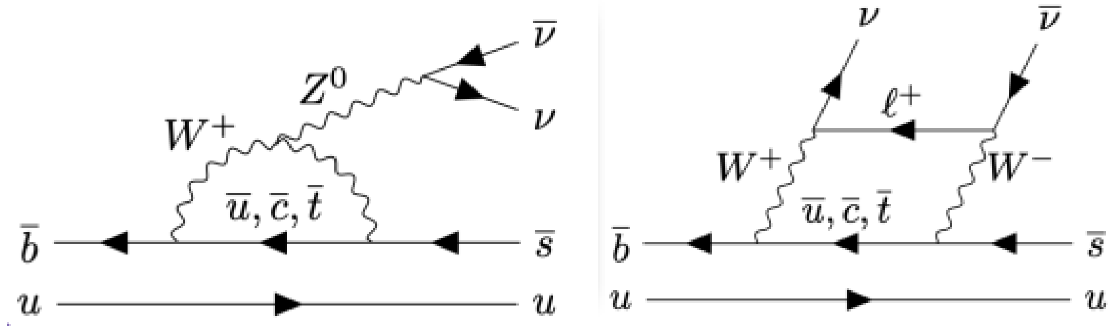
Belle II

50ab-1 Belle II, 50fb-1 LHCb



One of Belle II highlights : B->Kvv decay

Decay in Standard Model : very rare decay

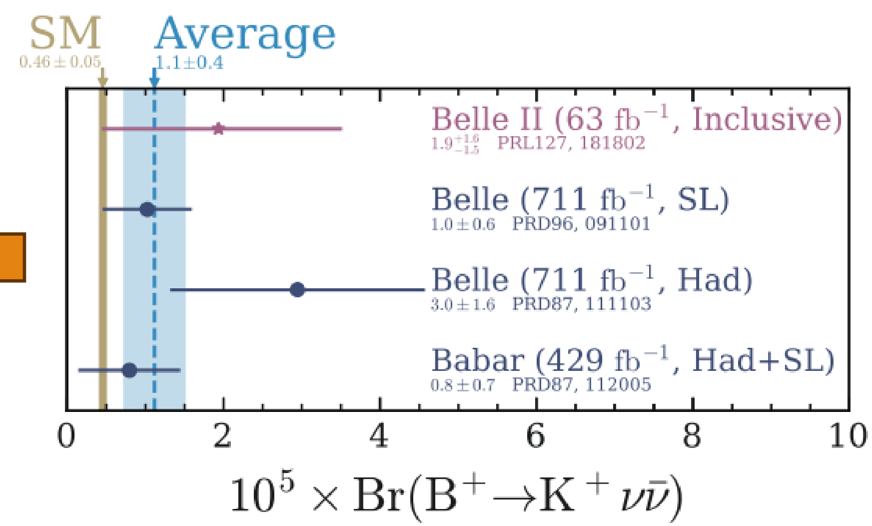


Preceise prediction for SM decay modes is possible.
Br(B->Knunu) = 0.56+/-0.04 e-5
->
Sensitive probe for new physics !

It had not been discovered.

- Two neutrinos carries energy away.
- B.g. is relatively large compared with the branching ratio.

Experimental result for the BR of B->Knunu before 2023



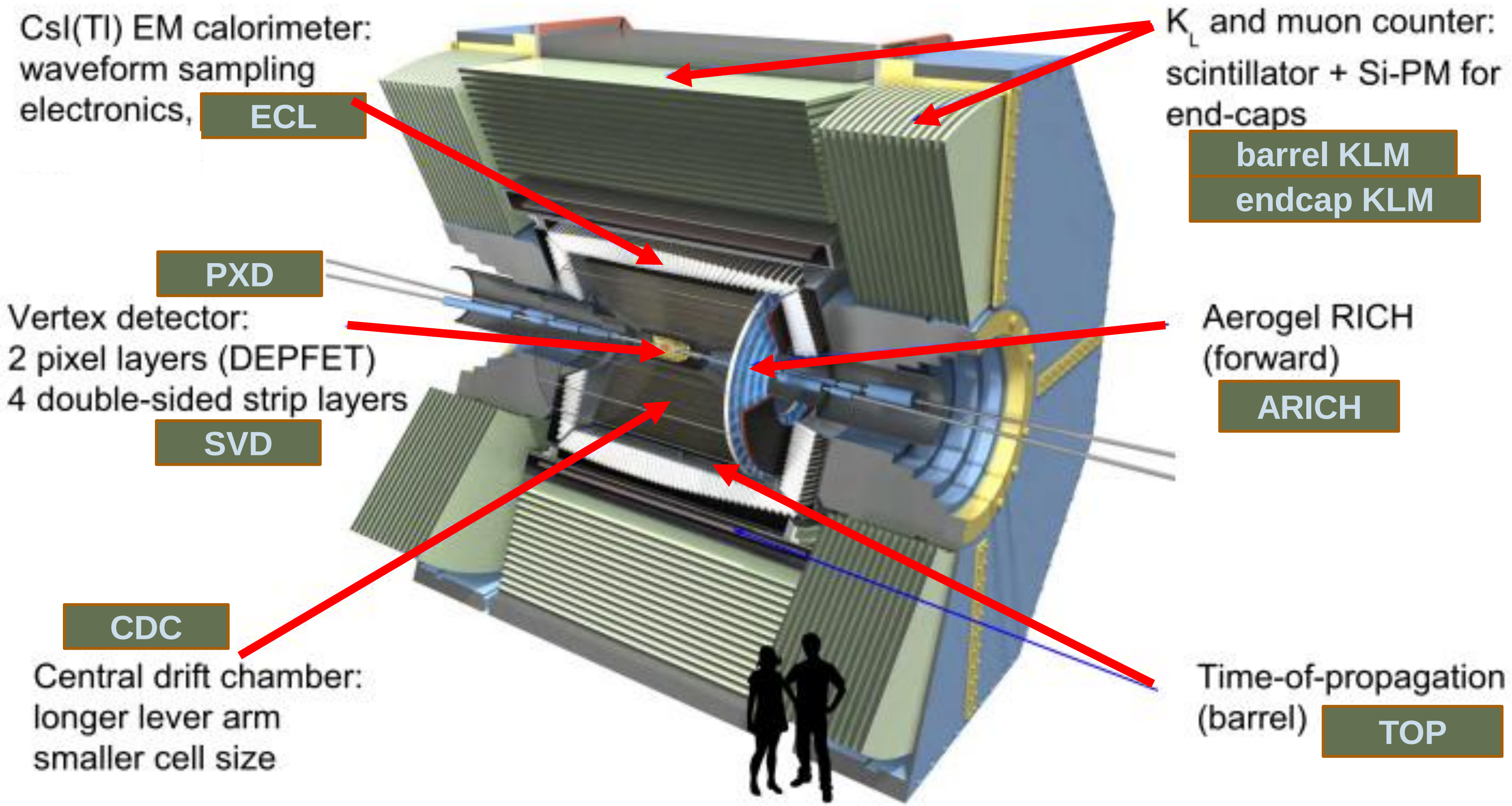
$$BR(B^+ \to K^+\nu\overline{\nu}) = [2.4 \pm 0.5(\text{stat})^{+0.5}_{-0.4}(\text{sys})] \times 10^{-5}$$

- 3.6sigma from the null hypothesis
- The measured branching ratio has the tension of 2.7sigma from the SM prediction

Belle II Data Acquisition system

Belle II Detector

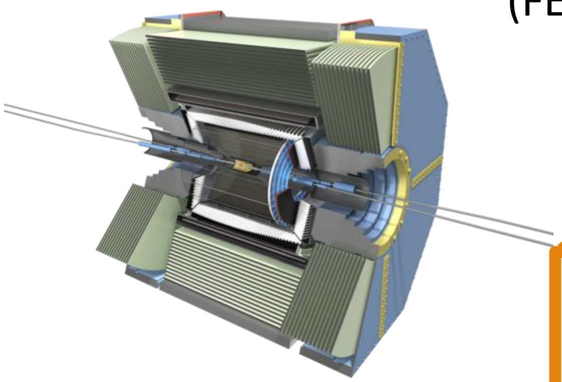
- Vertex determination: → **PXD, SVD**
- Tracking : → **CDC**
- Particle ID : → **TOP, ARICH**
- Calorimeter : → **ECL**
- Muon, neutral Kaon → **KLM**



Flow of data in experiment

Online (realtime) | offline

Sensor (detector) → Front-end Electronics (FEE) → Online data Acquisition system → Storage | Offline data analysis

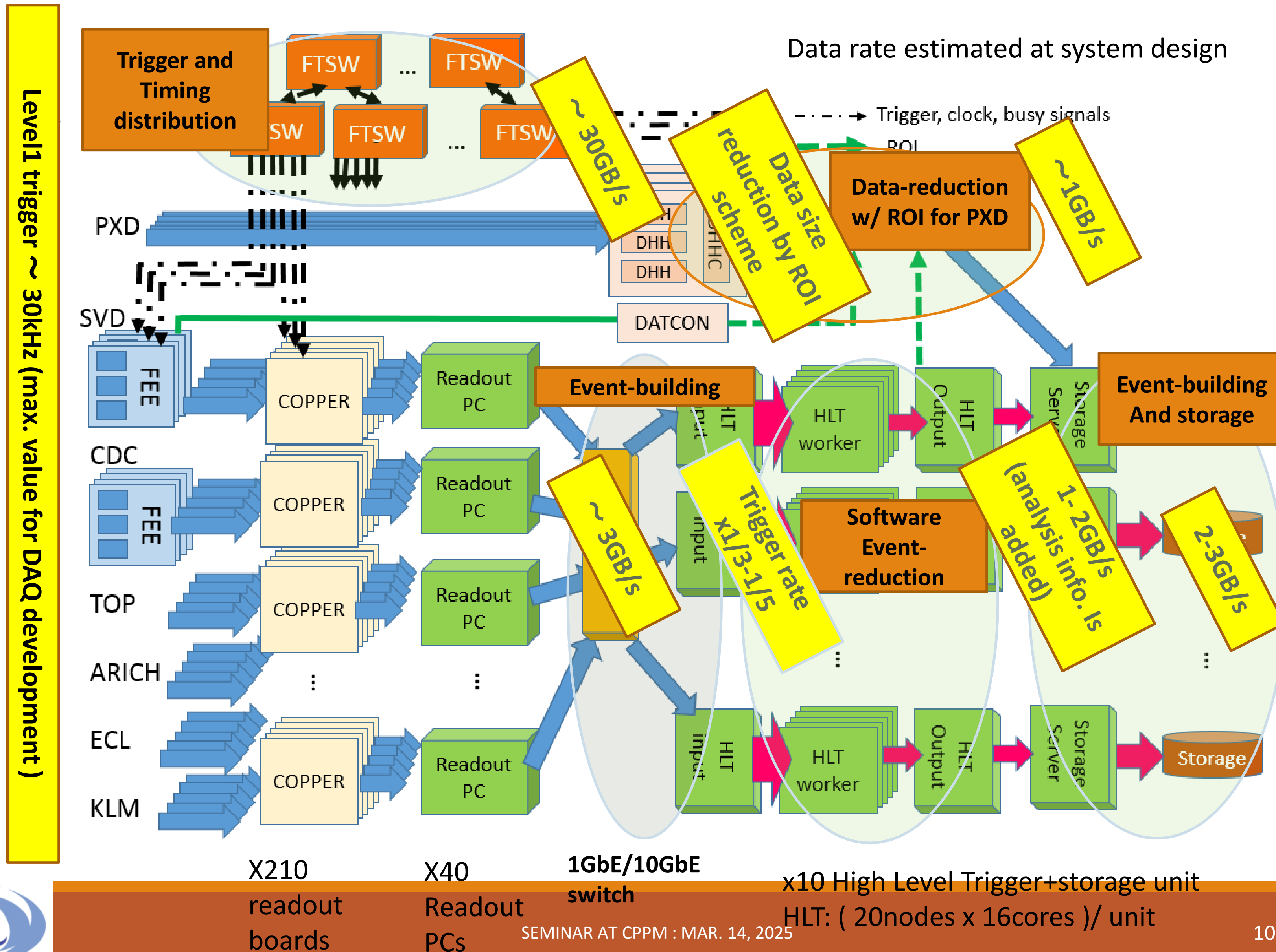


Functionalities of the online DAQ system

- Readout data from FEE
- Event building
- Online data reduction
- Recording

- Data formatting
- Sanity check of data
- System control (slow-control, run control)

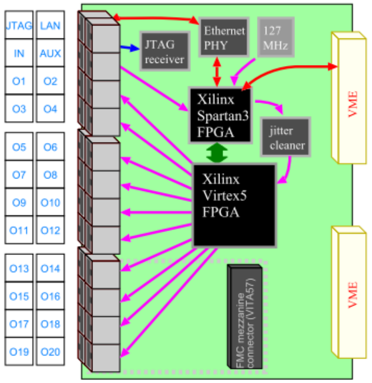
DAQ(DATA ACQUISITION SYSTEM)



Trigger and Timing distribution

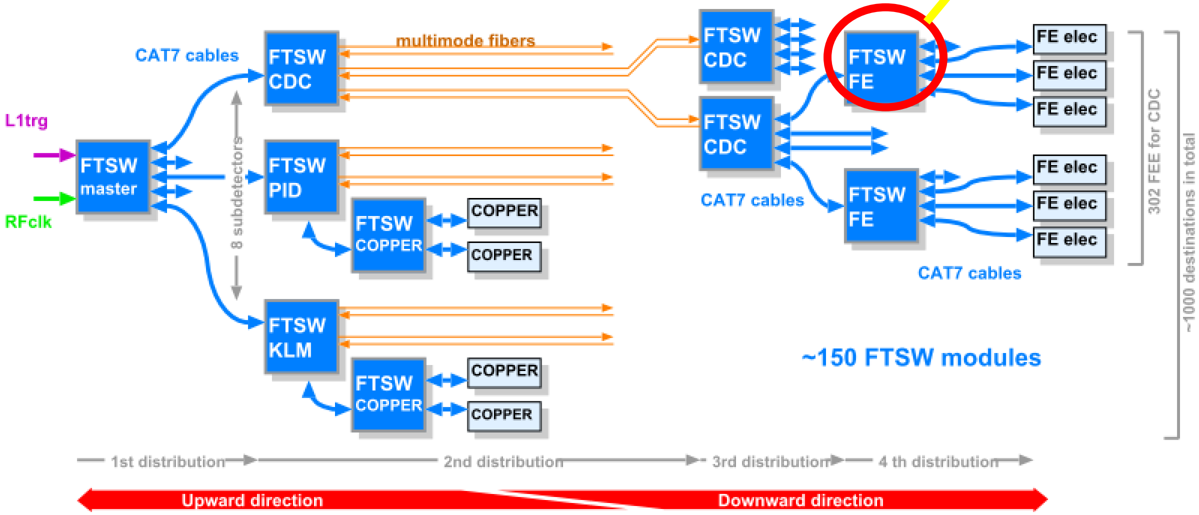
- Distribution of clock and trigger
  - Need to distribute system-clock over nodes (O(1000))
    - Clock : 127.216MHz (from SuperKEKB RF)
    - Jitter < 20ps
  - Trigger issued by Global Trigger Logic is also distributed
- Collection of the status of FEE and readout boards
  - Fast control : status info. of each node, busy handshake

Fast timing switch(FTSW)
FPGA : Xilinx Virtex-5
I/O ports :
* Optical fiber
* LAN cable (CAT7)



FTSW-S

Block diagram of Belle2 clock distribution

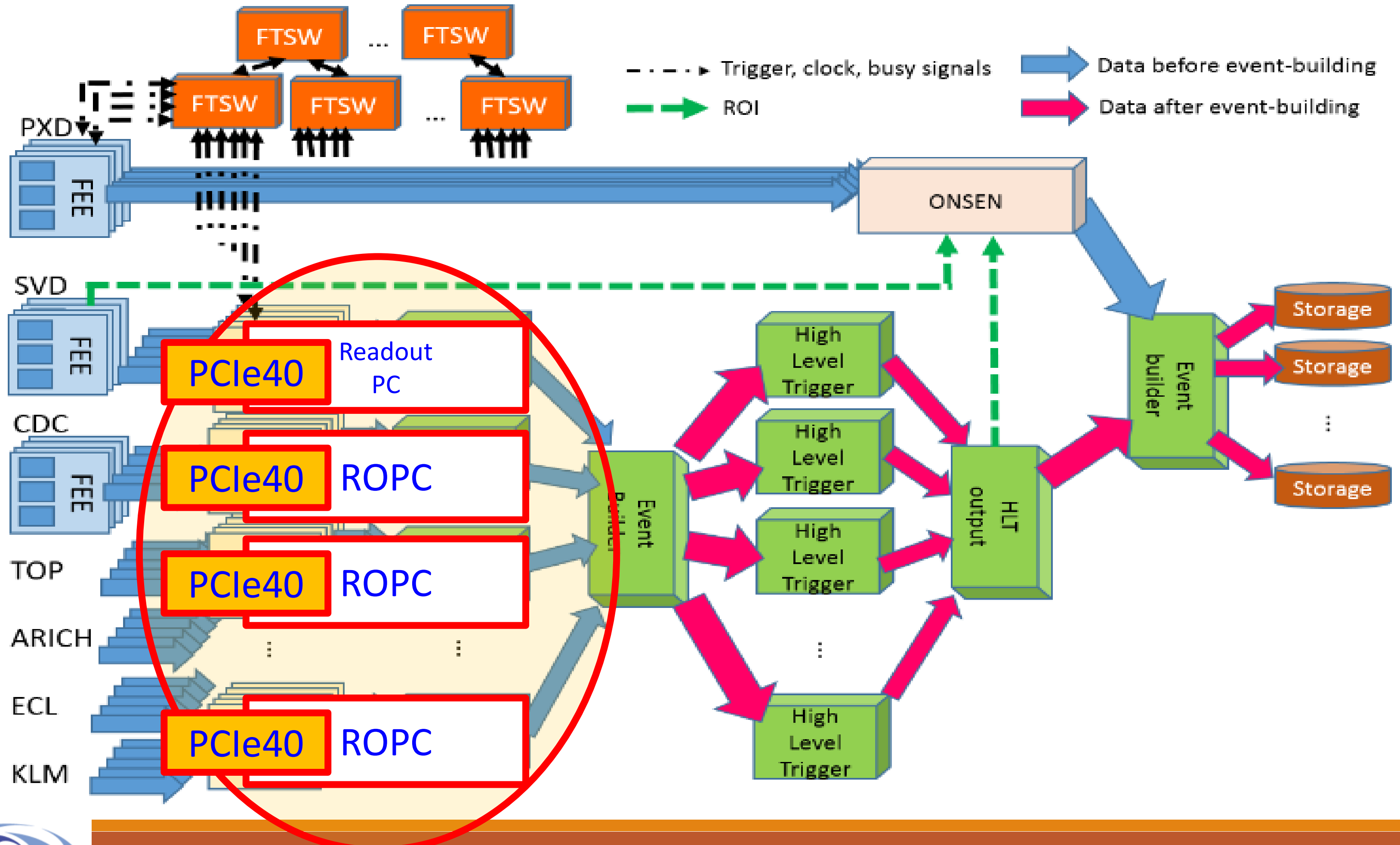


(M.Nakao)

Upgrade of the Belle II readout system for Run2(2024-)

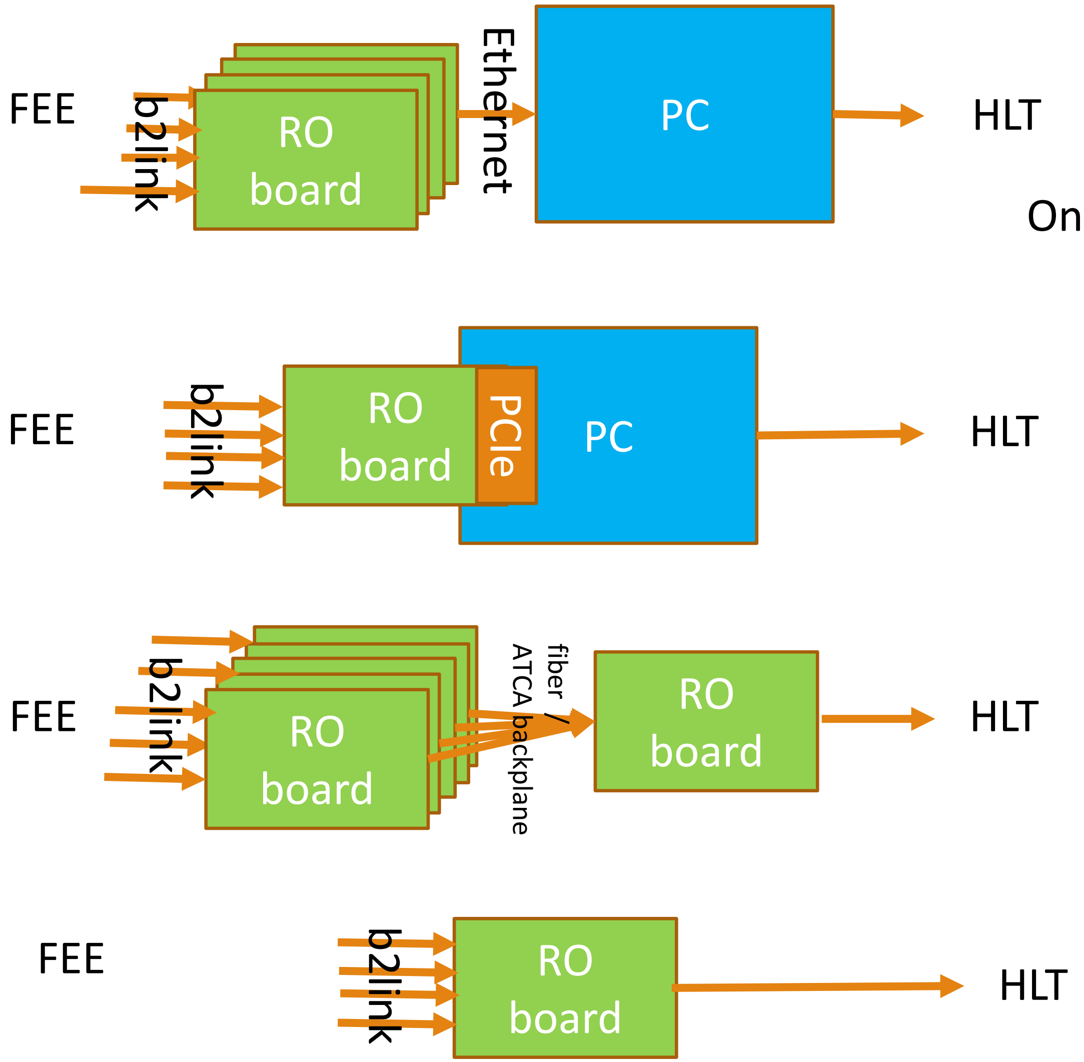
Motivation

- Difficulty in maintenance during the entire Belle-II experiment period
- Upgrade the current bottlenecks in COPPER (CPU, PCIbus, GigabitEthernet etc.)



Possible frameworks

FPGA
CPU



(a) COPPER-like

On-board CPU talks TCP/IP protocol

(b) PCIe

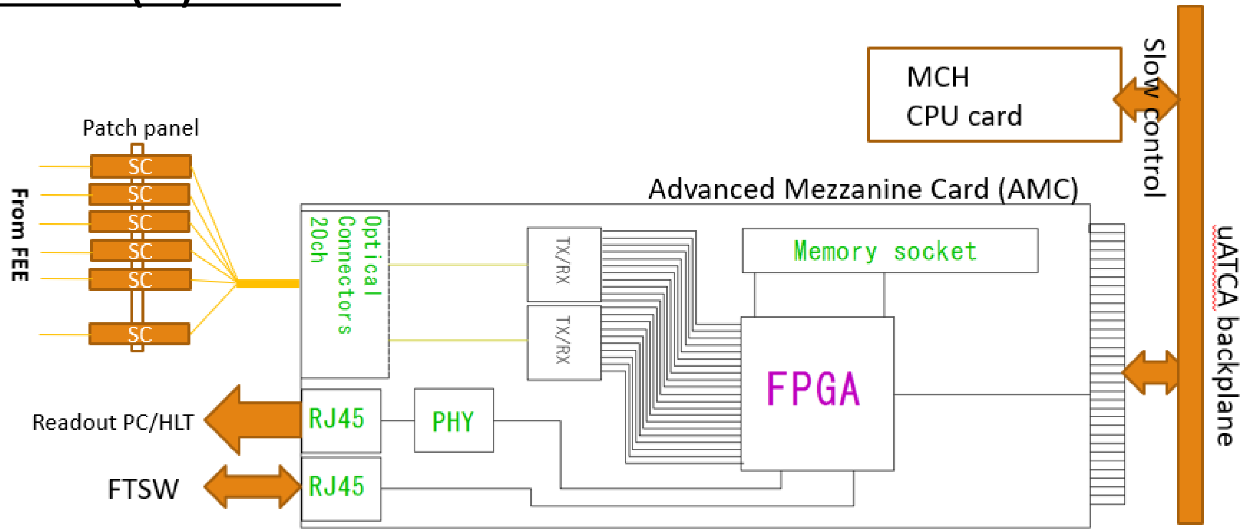
PC server talks TCP/IP protocol

(c) 2 step

FPGA core for TCP/IP stack

(d) 1 step

Proposal (0) : KEK



Proposal (1) : BNL

- ***Front End LInk eXchange (FELIX)***
  - Developed for ATLAS Phase-I Trigger/DAQ Upgrade (for 2021)
    - BNL designed hardware & co-developed firmware
  - **Generic PCIe card** with Kintex Ultrascale FPGA
    - 48-channels Tx & Rx links in 8 miniPODs
    - PCIe Gen3 x16 lanes interface to host
    - **Supports versatile line rates & timing systems**
      - ***TTC; TTC-PON; White Rabbit***
    - **Supports Belle II TTD recently**
  - Capacity:
    - 460 Gb/s input/output via optical fiber
    - Up to 128 Gb/s to host

Collaboration between BNL and ANL, CERN, Irvine, Nikhef, UCL, Weizmann [with FNAL (artDAQ)]

Proposal (2) : IJCLab, CPPM

Developed for LHCb(+ALICE) upgrade

仕様:

- I/O : 48 bidirectional link
- FPGA : Intel Arria10 (10AX115S3F45E2SG)
- PCIExpress : Gen3x8 x2
- 8 LVDS links

Proposal (3) : IHEP

CPPF Module for Belle II DAQ Upgrade

Originally designed for CMS by IHEP/Beijing

It is running in CMS Trigger System(Minor revision for FTSW interface)

uTCA compliant : Double width AMC card

IO(>10 Gbps, suitable also for Belle II future upgrade)

Inputs : **Four** 12ch MiniPoD connectors(48)

Outputs: **Two** 12ch MiniPoD connectors(24)

Processing and Control

FPGA

-- XC7VX415T-2FFG1157C(48 GTH)

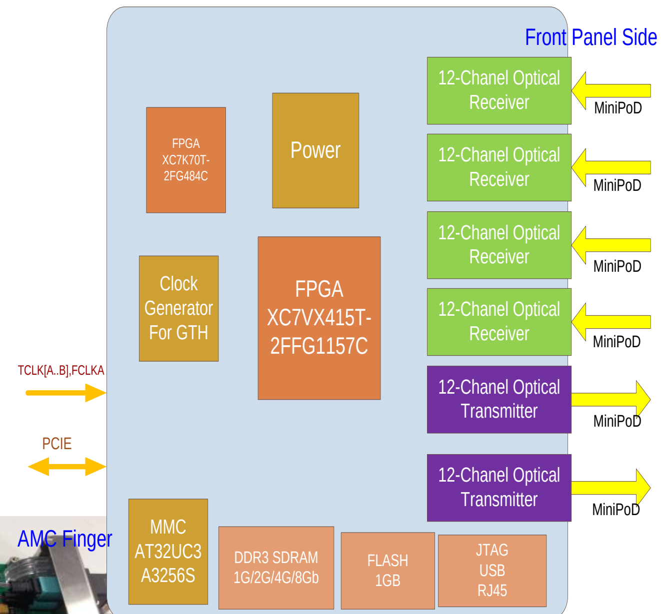
-- XC7K70T-2FG484C

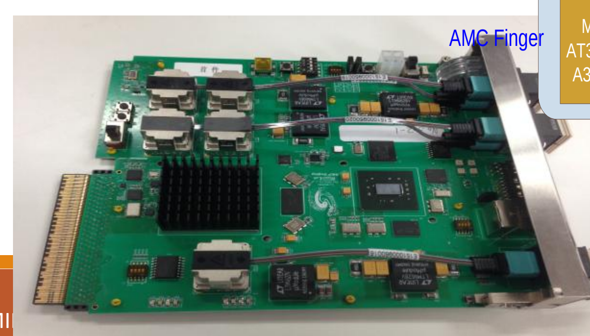
Flash

-- PC28F00AG18FE

DDR4: 1/2/4/8 Gb

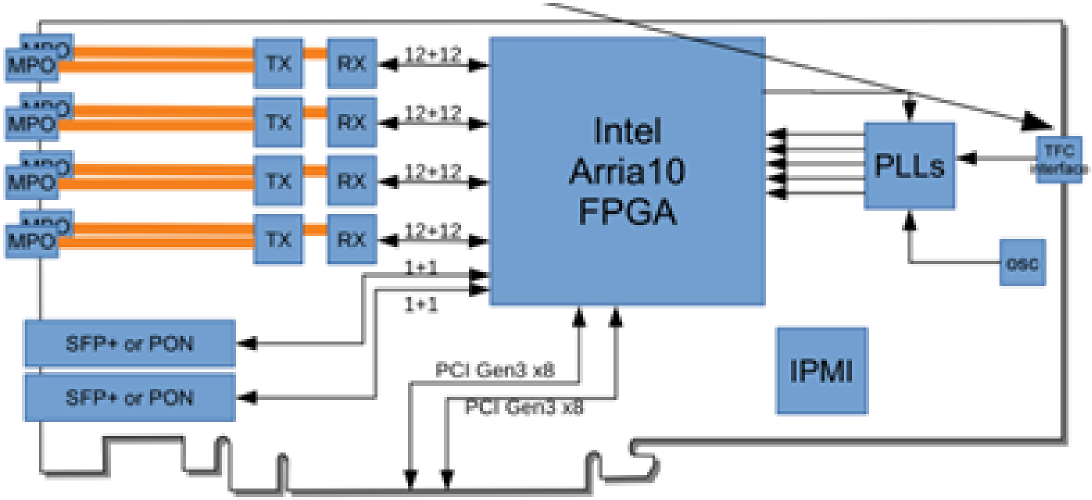
Protocol : PCIE ,Slink





PCIe40 board

- PCI Express board with a large FPGA and 48 optical transceivers
- Originally developed for LHCb and ALICE
- Its functionality is also suitable for the readout hardware of the Belle II DAQ.



COPPER
(VME-9U board)

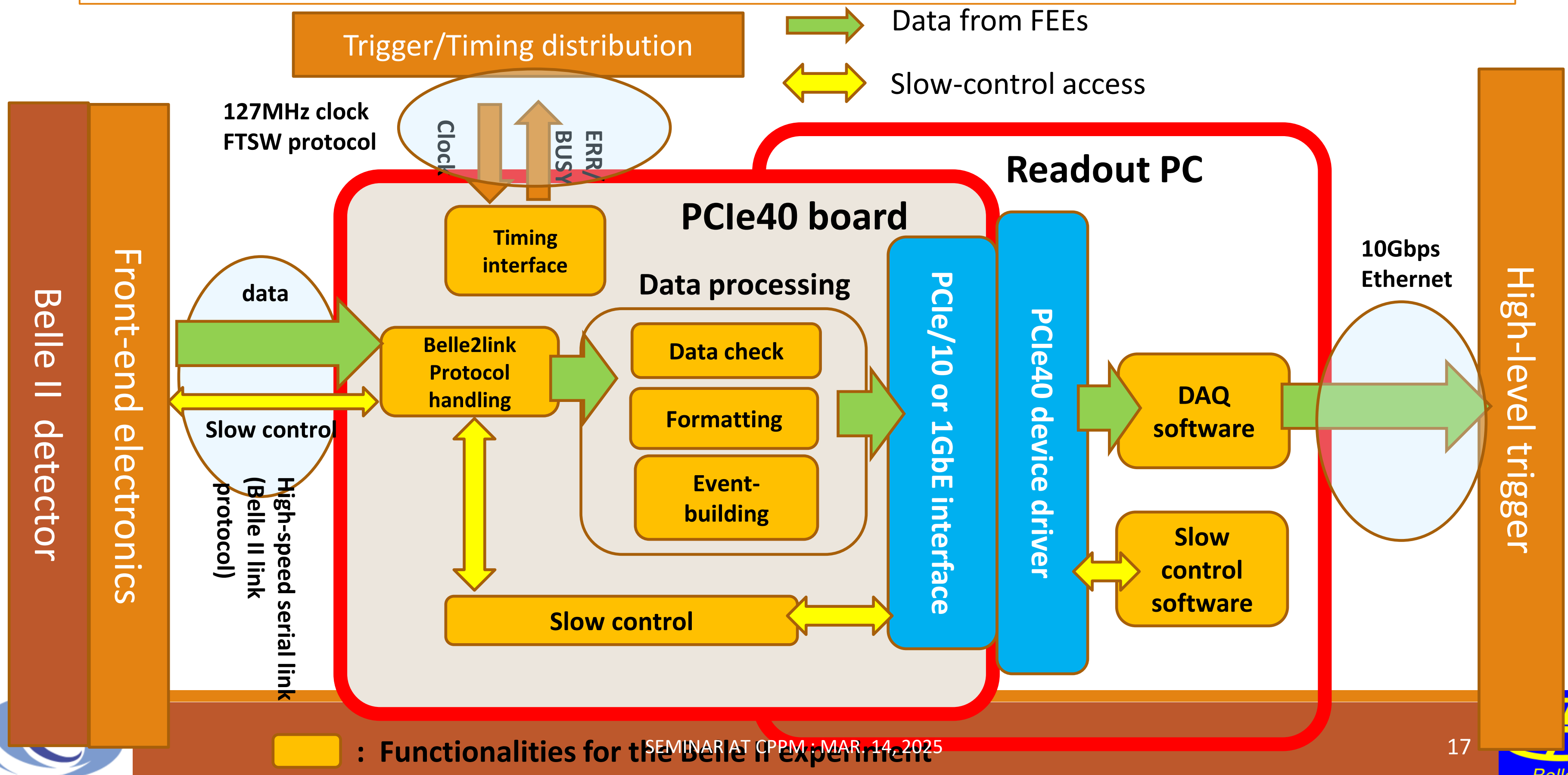
PCIe40
(PCIExpress card)

# of input channels :
COPPER : max 4
PCIE40 : max 48

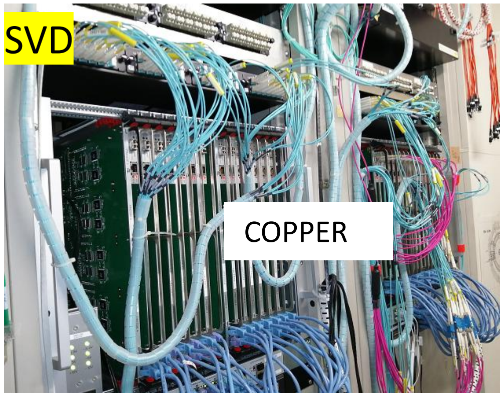
# of readout boards used for Belle II :
～200 COPPER boards -> 21 PCIe40 boards

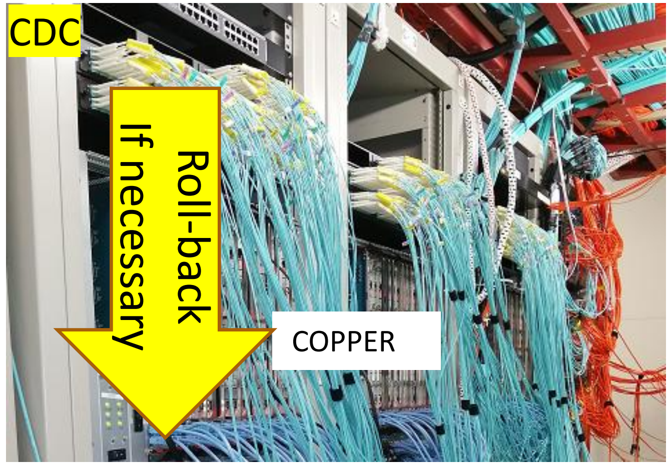
Firmware and software development for the new system

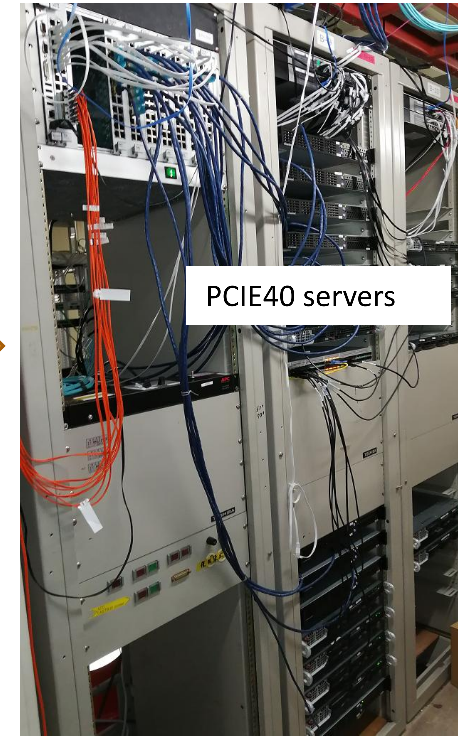
- Keep the three interfaces with the other system.
  - FEE : belle2link protocol (data readout, slow-control)
  - TTD : FTSW protocol
  - HLT : Ethernet
- Data-processing done by COPPER CPU moves to FPGA in PCIe40
  - Data-formatting, data-check, and partial even-building
- Software on readout PC
  - DAQ software, slow-control software

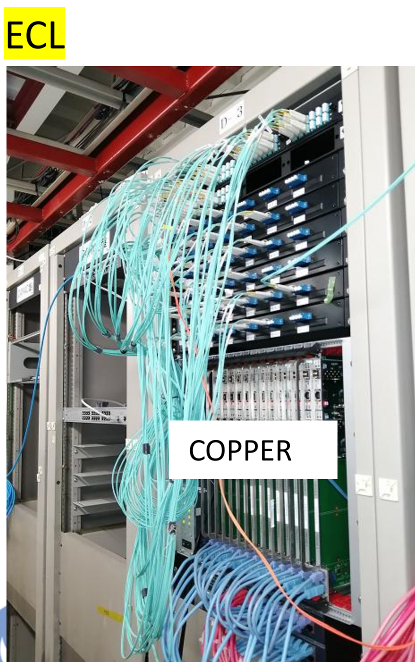


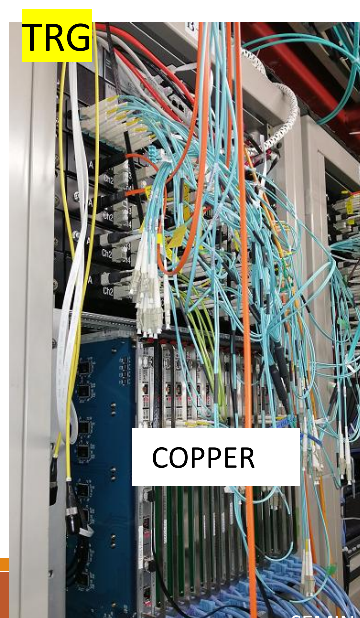
Replacement schedule of readout system (COPPER -> PCIe40)







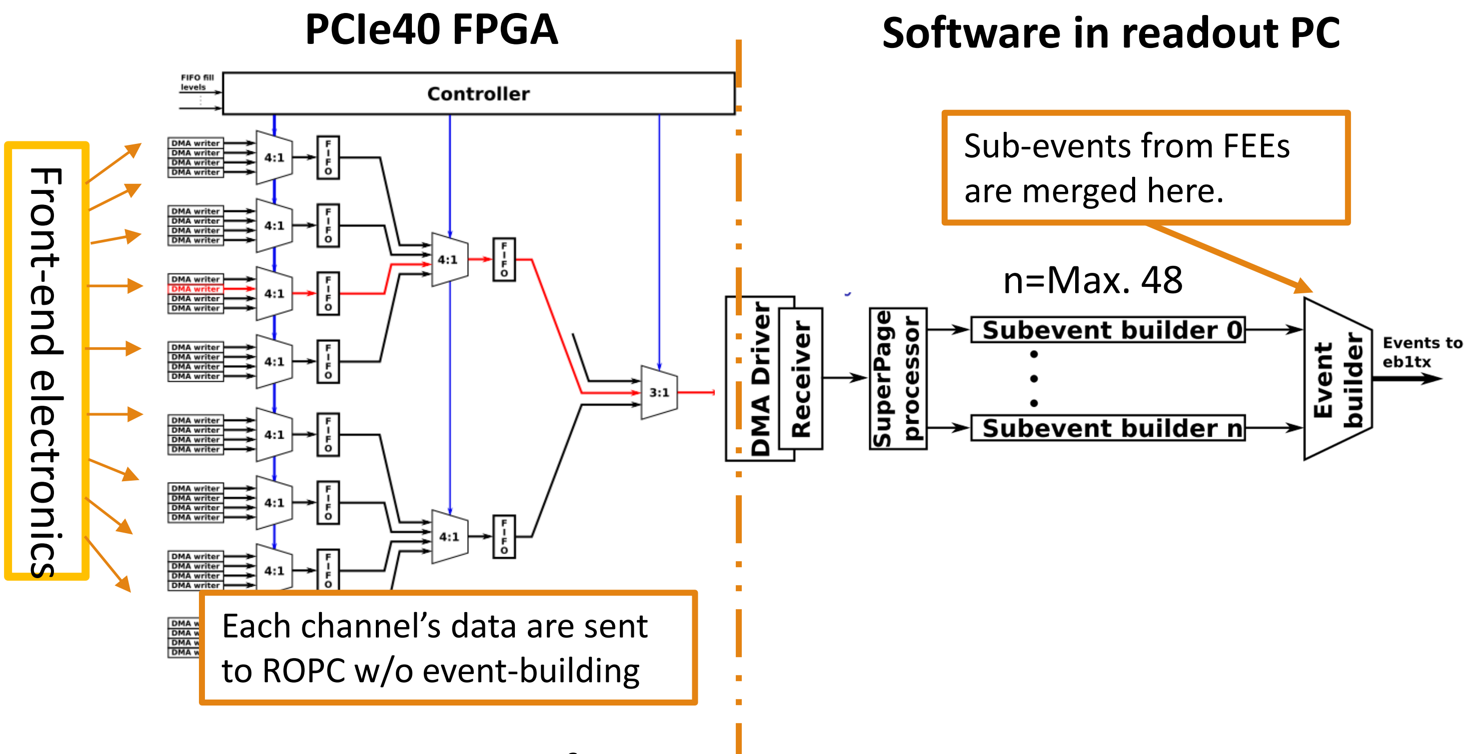




- COPPER system for all sub systems(but PXD) will be kept for a while as backup so that we can roll back quickly in case of a serious trouble.
- Actually, at the beginning of physics run, it was reverted to the old system for a month due to slow-control issue.

Recent progress : event building by software

- Before LS1, event-building was performed in PCIe40 FPGA on-chip memory.
- The new scheme has been developed in LS1 by using PC server memory for event-building.
  - Larger memory increases the room to wait for events from FEEs before buffer-full.



Performance improvements

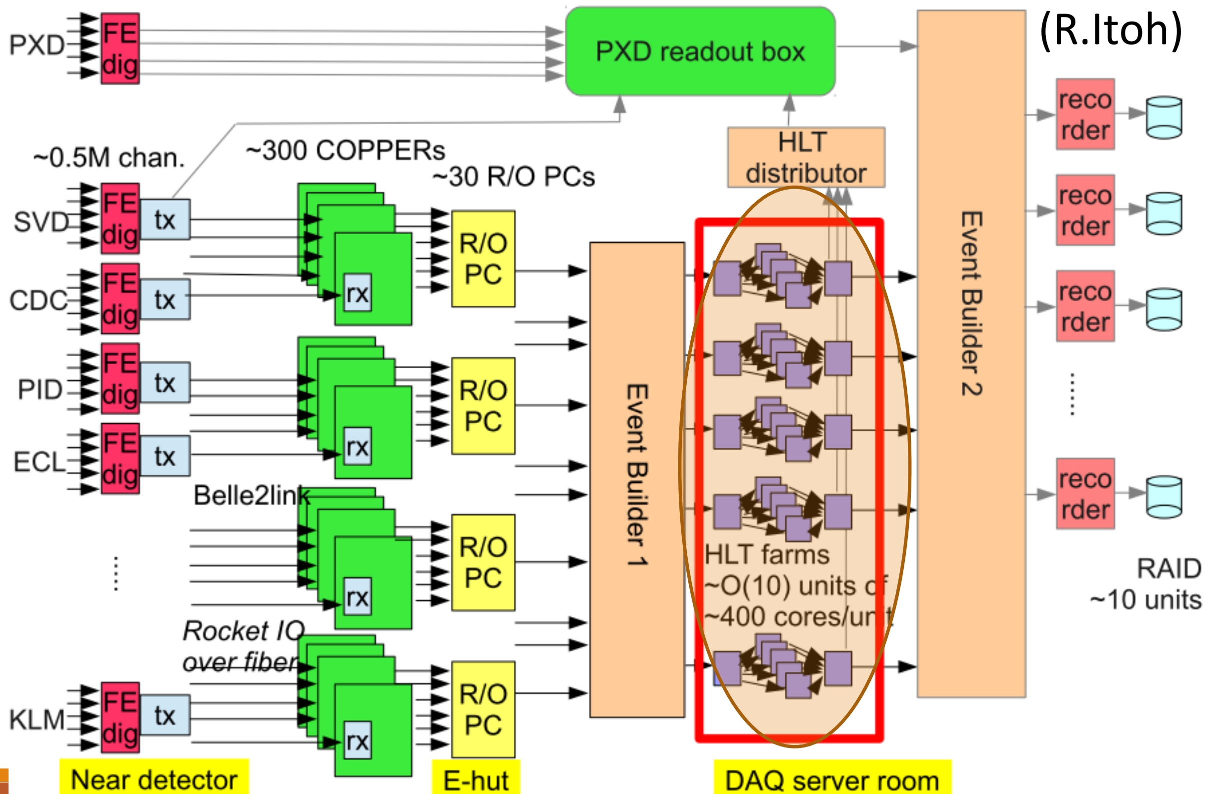
- Throughput up to ROPC : FEE->PCIe40->ROPC software : 4.9GB/s
  - Note : Data were not sent to HLT in this measurement
- In a high-rate test including data-transfer to HLT, 800MB/s/ROPC at 32kHz was achieved.
  - Trigger holdoff to avoid buffer-full in FEE is the current bottleneck.

High level trigger

Functions

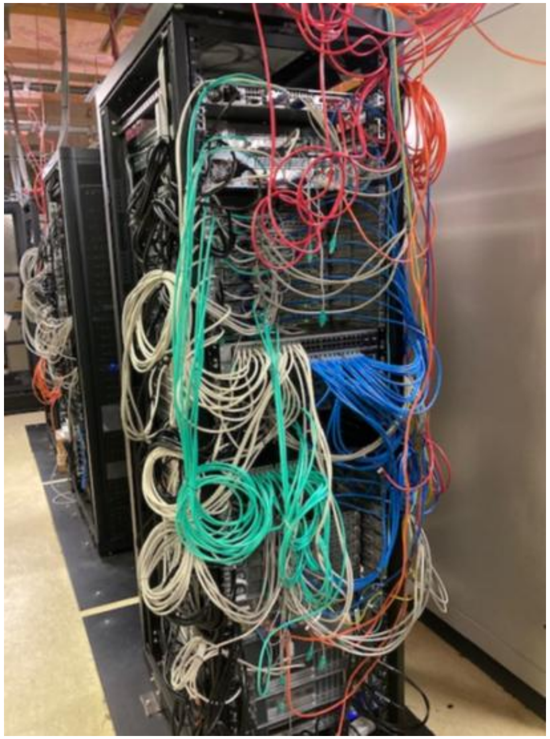
1. Event reconstruction from data of all detectors except for PXD
2. Reconstruction software developed for offline analysis is also used in HLT
3. For trigger selection, physics event selection is applied. (rate reduction : 1/3)
4. ROI information from reconstructed SVD tracks is fed to PXD for data size reduction

Complex operation needs large CPU power
→ parallel processing



Tsukuba B3 HLT server room

- 1 rack has one HLT + STORAGE unit
- 10 units in operation (4800 cores) + 3 more units under preparation (-> 6400 cores)
- All assembled by Belle II researchers



Trigger rate and HLT throughput

R. Tiwary(TYL)

- We assume a linear increase in the processing time and L1 trigger rate with the average instantaneous luminosity, and extrapolate the scenario for higher luminosity with a straight line fit.
- Next, we look at the HLT throughput ⇒ Put L1 trigger rate in the same plot and add contingency bands.

HLT throughput = # of cores / processing time

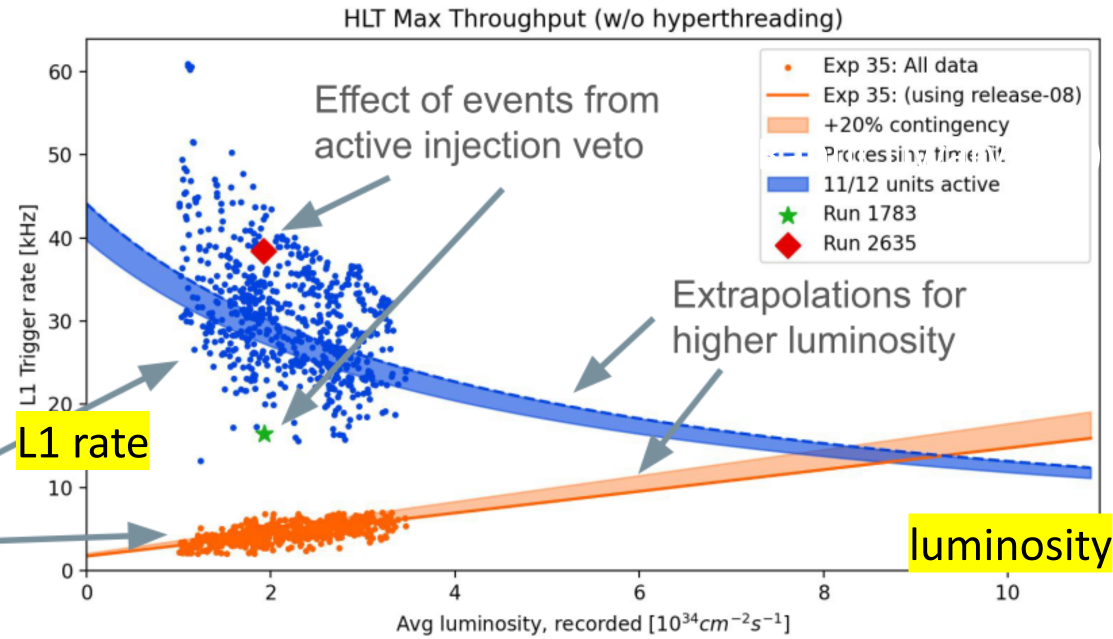
Processing time scales linearly with luminosity

↓

HLT throughput scales inversely with luminosity

Scatter plot of HLT throughput

Scatter plot of L1 trigger rate

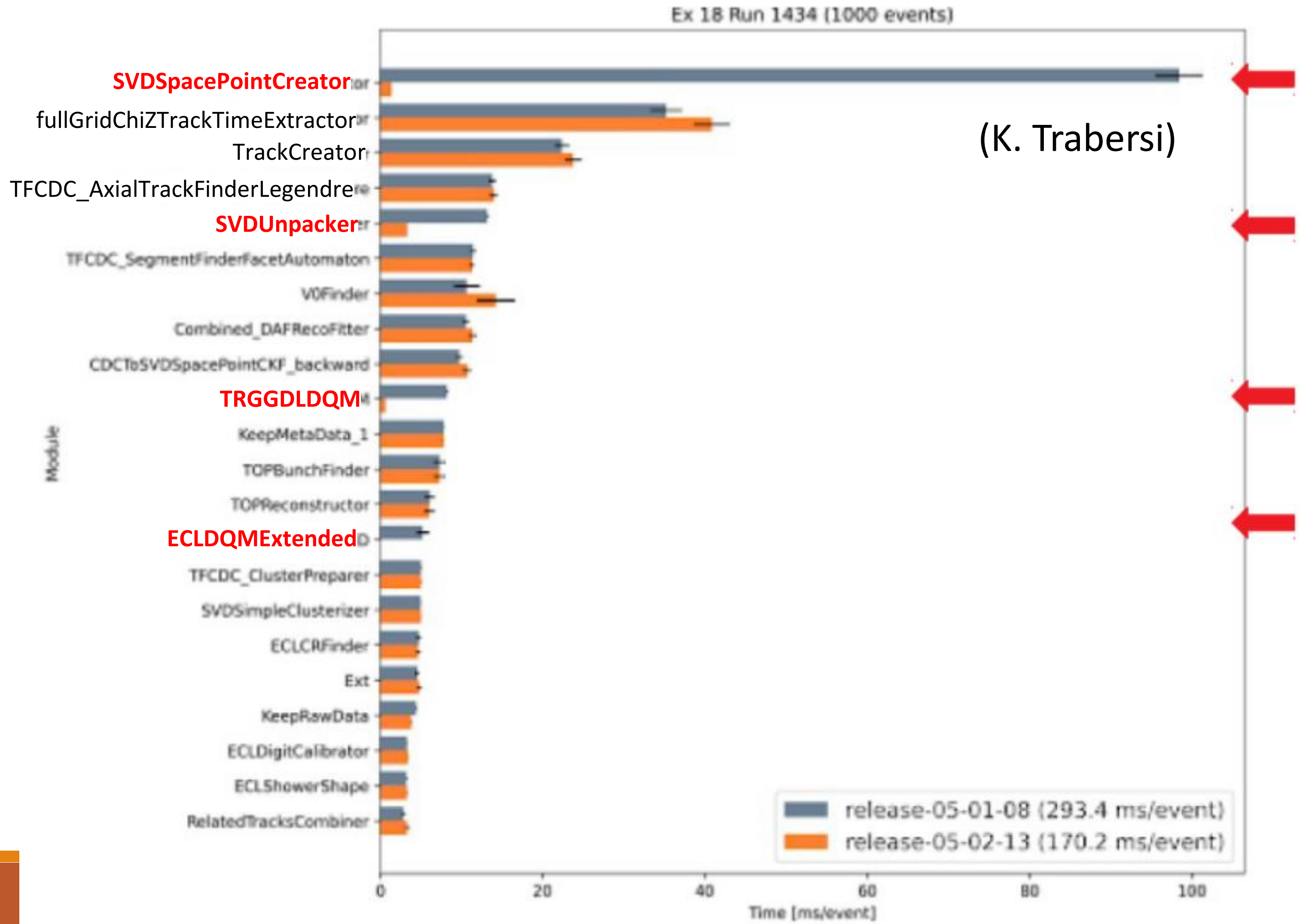


HLT reinforcement

- In 2019, the operation started with 10 HLT units.
- Since it is parallelized system, we can add up new servers for the performance improvements.
- So far 4 HLT units have been added. 15th unit will be installed this summer.

Processing time for online event reconstruction

- Efforts for reconstruction software tuning of each sub-system is important.
- Since this software is developed for offline analysis, developers sometimes does not pay so much attention about resource usage…

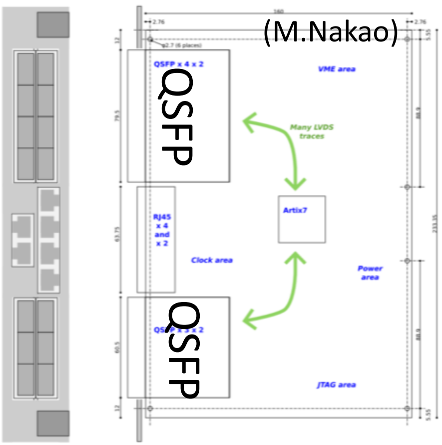


OTHER LONG-TERM DEVELOPMENTS

NEW FTSW MODULE : FTSW4

- FTSW4 (FTSW with fully optical ports) development status
  - Main target of application : CDC new FEE(RECBE2)
  - Testing a prototype module.
  - The 2nd version of protype has been ordered and will be available in this JFY. Mass production in the next JFY.

FTSW4



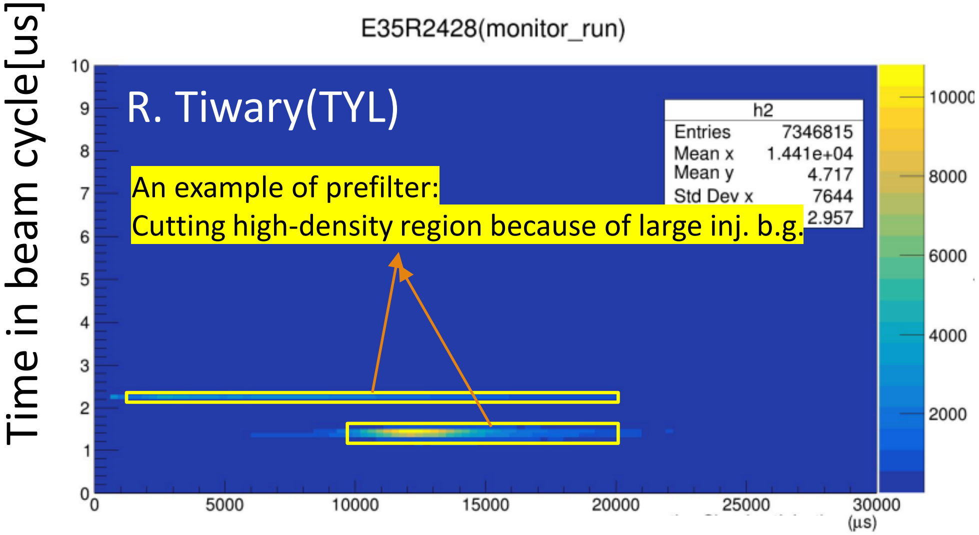
VARIOUS IDEAS FOR HLT PERFORMANCE IMPROVEMENTS

Near-term project with software :

- Pre-filtering study (TYL)

Long-term project :

- GPU acceleration(KEK)
- FPGA acceleration(Shandong, KEK)



Readout upgrade with PCIe400 ?

- Currently, PCIe40 performance is good enough.
- Probably, readout for a new sub-detector in future or a new data-path for triggerless readout for anomaly detection ?

Summary

- The Belle II experiment
  - The Belle II experiment aims to discover new physics beyond the Standard Model using the SuperKEKB electron-positron collider at KEK.
  - Both the accelerator and detector have been upgraded from the former Belle/KEKB experiment.
    The target integrated luminosity is 30 times larger than that of the Belle experiment.

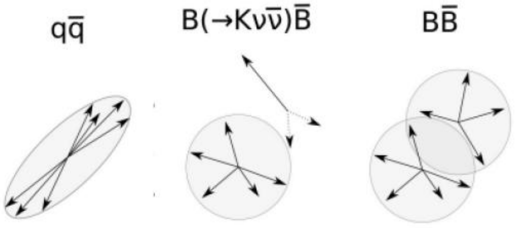
- Belle II data acquisition system
  - The replacement of the Belle II readout system with PCIe40 boards developed by CPPM was completed last year.
  - A throughput of around 5 GB/s was measured in a performance test.
  - The PCIe40 currently provides sufficient performance for the Belle II DAQ system, but we are also interested in a new PCIe400 technology for a future front-end electronics (FEE) upgrade or a dedicated path to detect exotic events at high throughput, for example.

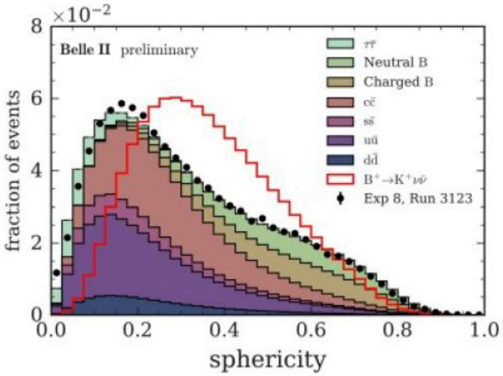
END

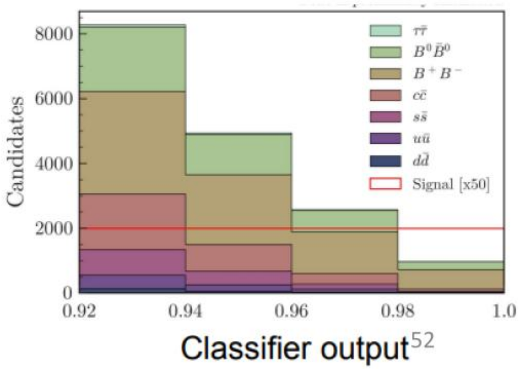
Belle II paper in preparation

$B^+ \to K^+\nu\bar{\nu}$: Analysis strategy

- Two methods: an inclusive tag (8% efficiency) and conventional hadronic tag (0.4% efficiency)
  - many common features except tag
- Use event variables to suppress background
  - Inclusive:
    1. preselect events where missing momentum and signal kaon well reconstructed
    2. First boosted decision tree (BDT1): 12 variables
    3. Second BDT2: 35 variables – 3 times sensitivity
    4. BDT2 fit extraction variable in bins of $\nu\bar{\nu}$ mass-squared – q^2
  - Hadronic tag: single BDT for fit
    - key variable any additional calorimeter energy other than K+tag





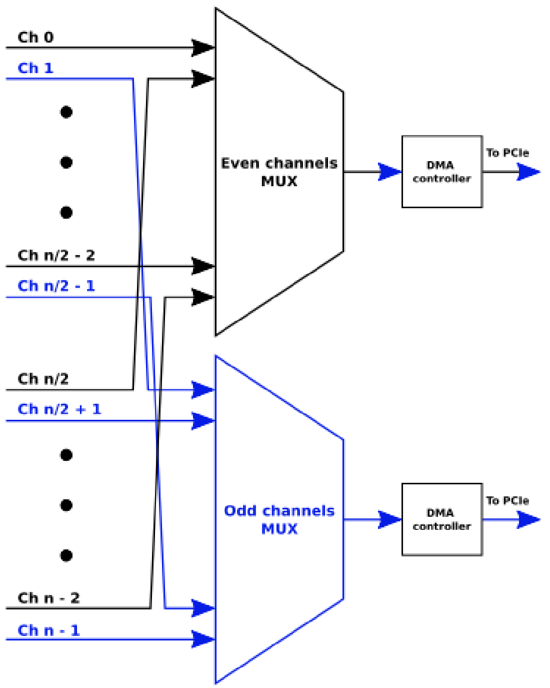


Readout : Improvement in throughputs

(D. Levit)

- PCIe3.0 x 8lanes -> 2x PCIe3.0x8lanes

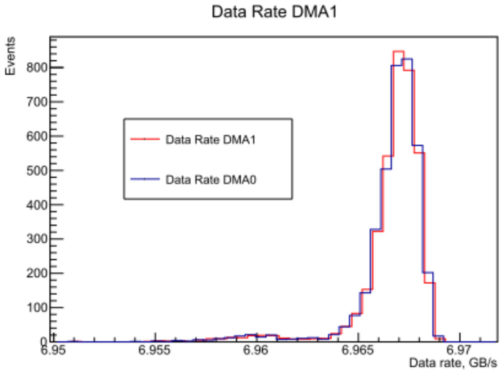
  - Integrated 2xPCIe interface into sweb firmware
  - Connect even and odd channels to different DMA controllers for load balancing
  - Busy as an OR of the programmable full of both DMA descriptors FIFOs



- Data transfer speed via PCIExpress has been doubled in the B4 test bench.
- Deployment of this feature in Belle II DAQ is to be done.

(Please note that the current bottleneck is not this PCIExpress transfer but CPU usage of readout PC software.)

- Throughput test with data generator in firmware and discarding data in software



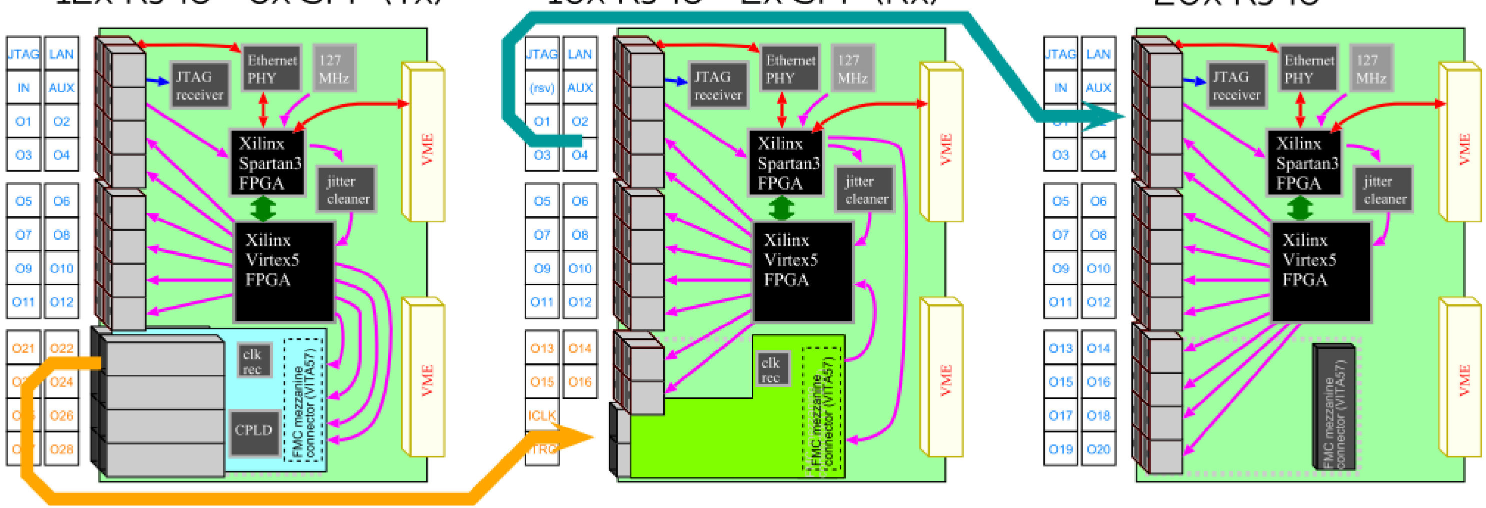
14GB/s !!

Component : FTSW module

- VME6U module
- Xilinx Virtex5 (reasonable but not so much resource)
- 24x RJ45 ports on 2 slots-width
  - Some modules are equiped with SFP(small form-factor pluggable) transceivers for optical communication by using 2 types of FMC(FPGA Mezzanine Card)
- Distribute signals to 8-20 destinations
  - In total around 1000 devices are connected to the TTD system.
- Clock : 127 MHz (RF freq./4)
- Custom protocol (b2tt) : 254 Mbps

Different I/O types of FTSW

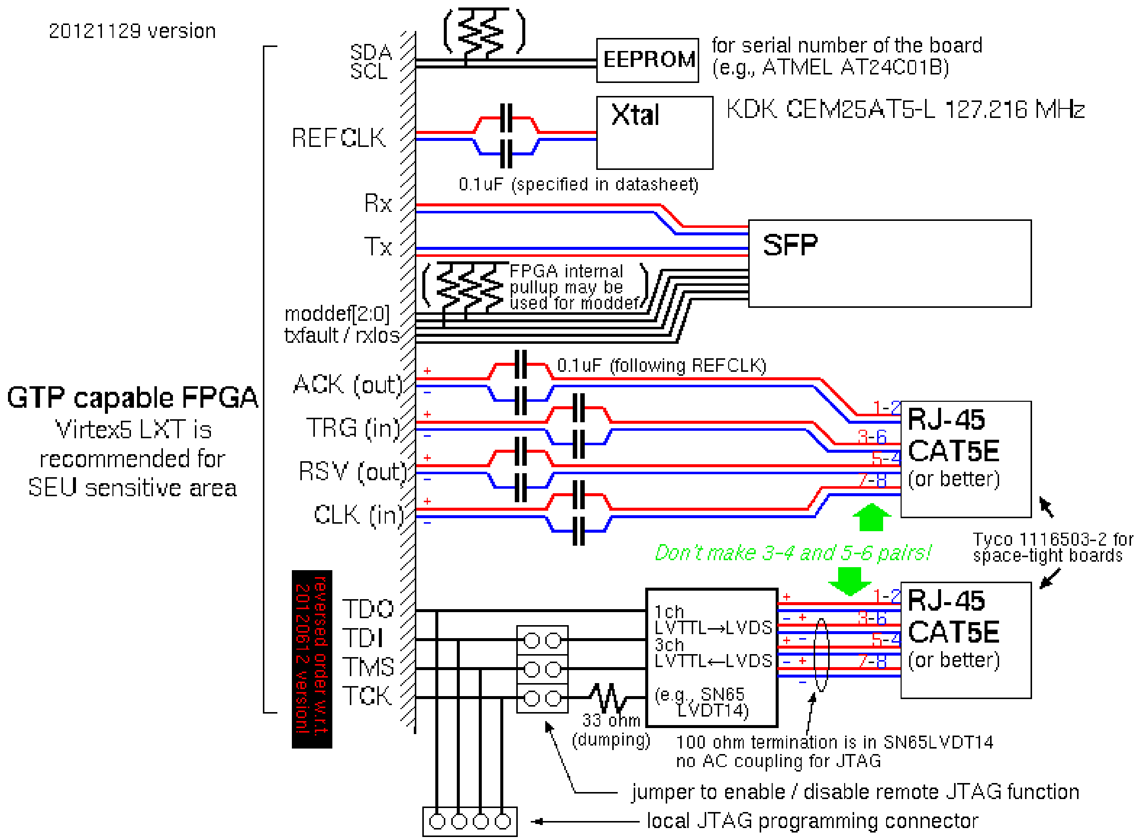
12x RJ45 + 8x SFP (Tx) | 16x RJ45 + 2x SFP (Rx) | 20x RJ45



Belle II

I/O of FTSW module

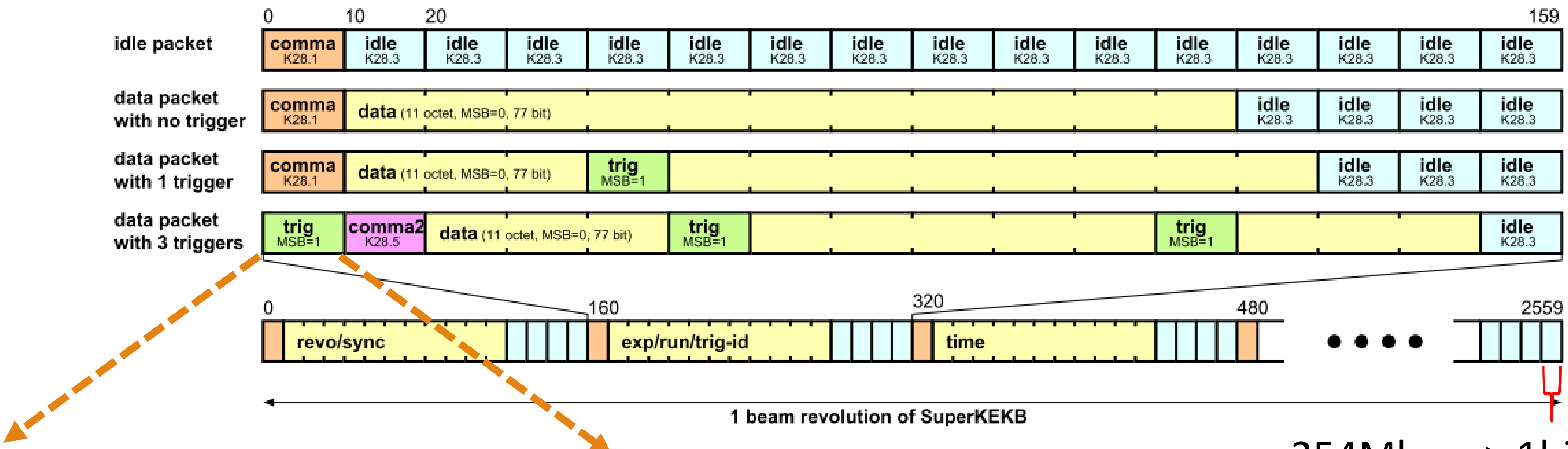
- 4 pairs in a LAN cable are used for signal transmission
  - 2 pairs for incoming and other 2 pairs for out-going
- JTAG signal can be distributed on a dedicated cable.
  - Programming firmware on FrontEnd Electronics(FEE) can be done quickly



From FTSW to FEE (clock and trigger signals)

- Bunch crossing : around 4ns
- Minimum 190 ns interval between two triggers
  - SVD readout requirement (APV chip 6samples)
  - Also too small interval makes it difficult to separate CDC tracks

Data format:



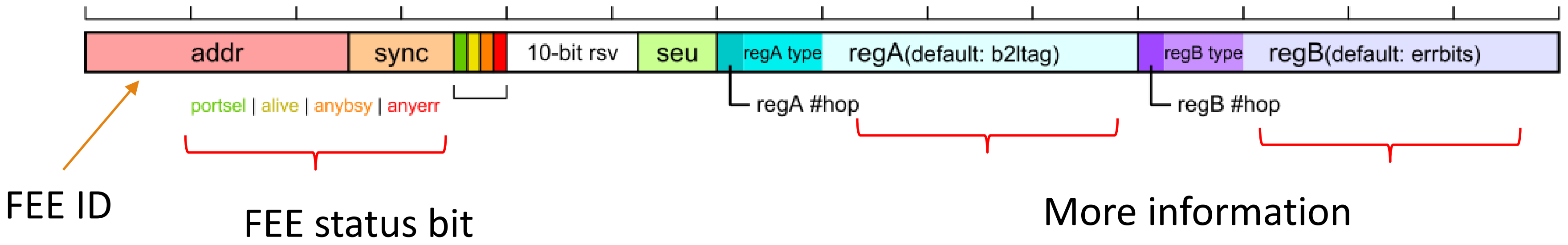
254Mbps -> 1bit = 4ns

- Trigger types are as follows (defined in b2tt_symbols.vhd)

PID0	0x0	fine-timing trigger, $t_{fine}=0$
PID1	0x4	fine-timing trigger, $t_{fine}=1$
PID2	0x8	fine-timing trigger, $t_{fine}=2$
PID3	0xc	fine-timing trigger, $t_{fine}=3$
RSV0	0x2	reserve 0
RSV1	0x6	reserve 1
RSV2	0xa	reserve 2
RSV3	0xe	reserve 3
ECL	0x1	ECL trigger, coarse-timing
CDC	0x3	CDC trigger, coarse-timing
DPHY	0x5	delayed physics trigger
RAND	0x7	random trigger
TEST	0x9	test trigger
RSV4	0xb	reserve 4
RSV5	0xd	reserve 5
NONE	0xf	not a trigger

From FEE/ROB to FTSW(BUSY, ERROR etc.)

From FEE/ROB to FTSW



- If error is reported -> DAQ stops
- If busy is reported -> pause the trigger distribution (BUSY handshake)

Busy handshake

- For any DAQ systems, we need to consider

“What will happen when input data from FEE > max. throughput of DAQ ?”

-> In Belle II DAQ, the TTD system takes care of it.

If trigger rate becomes too high for DAQ system

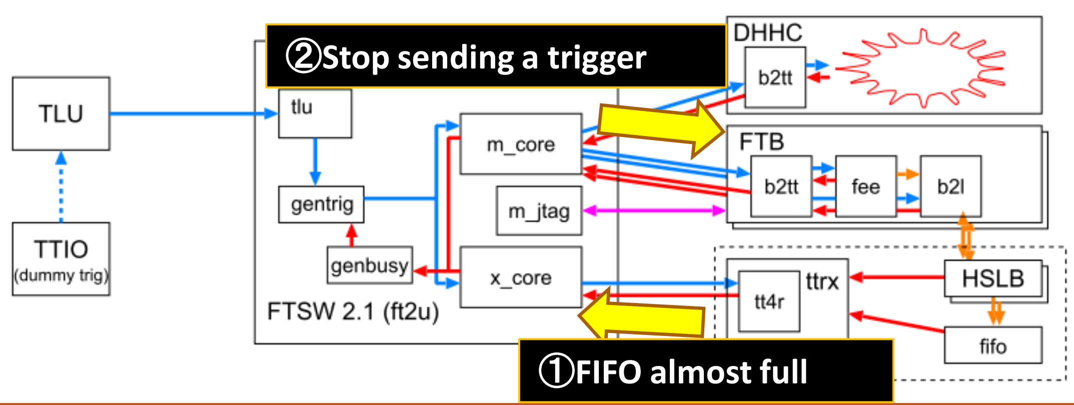
- Unprocessed data are accumulated in buffer of DAQ nodes
- If buffer becomes completely full -> part of events are lost
- Usually, in this case, data processing cannot continue, because data format is broken.

To avoid this issue, we monitor the usage of FIFO on readout board.

- If buffer become almost full, the readout board send busy signal to the trigger distribution module to stop issuing trigger.
- By using this fast control, but we can control the throughput of data.

TTD (for telescope test)

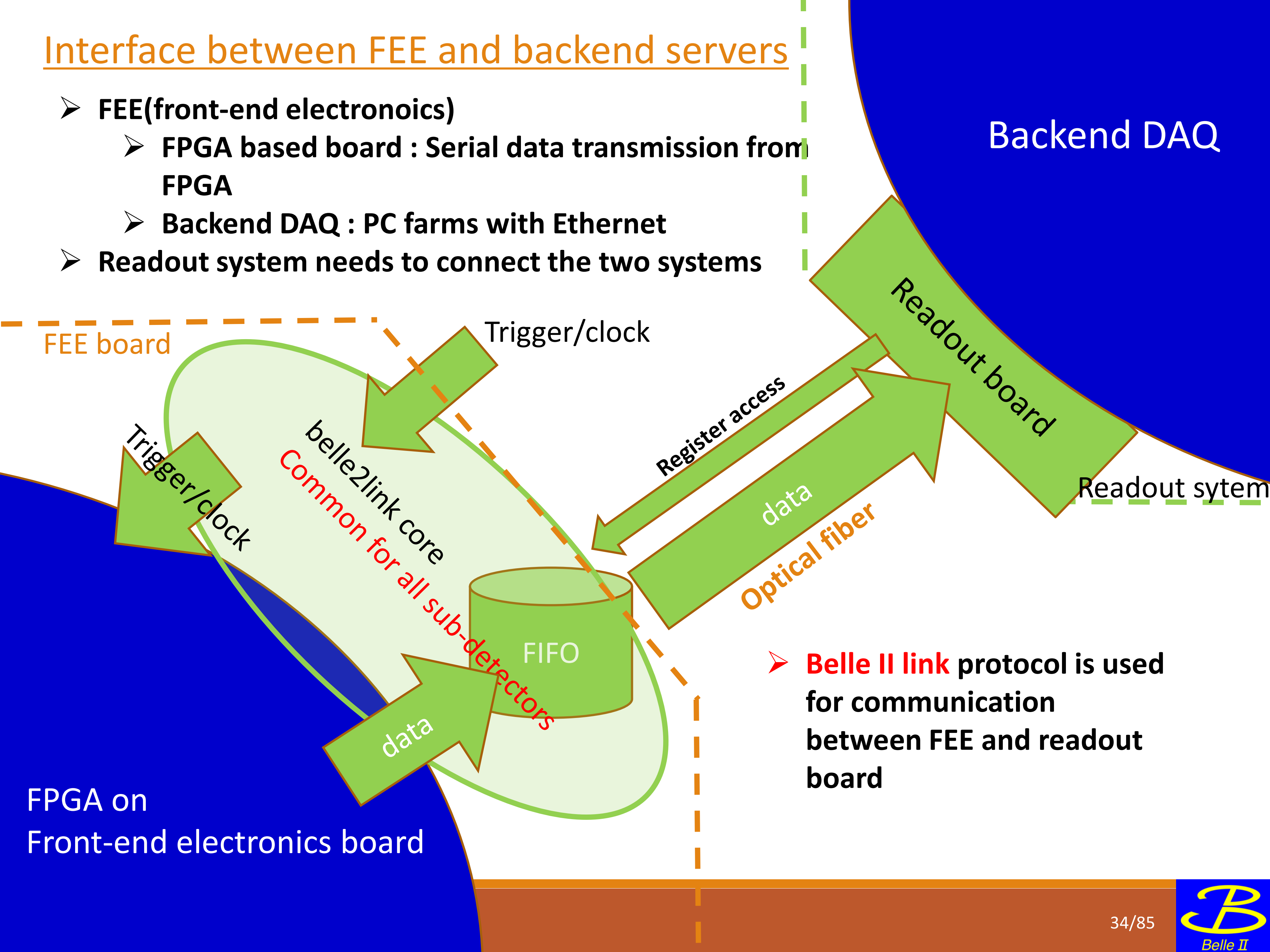
(M.Nakao)



Belle II

Interface between FEE and backend servers

- **FEE(front-end electronoics)**
  - **FPGA based board : Serial data transmission from FPGA**
  - **Backend DAQ : PC farms with Ethernet**
- **Readout system needs to connect the two systems**



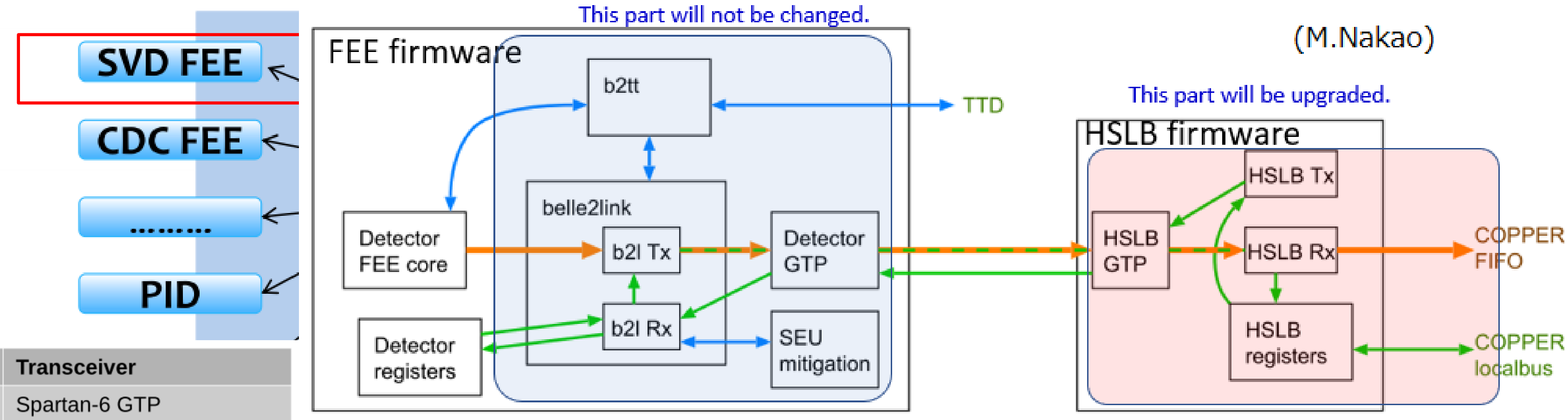
- **Belle II link protocol is used for communication between FEE and readout board**

Overview for Belle2Link

Belle2Link is a name for global fast data readout and transmission between Detector Front-End Electronics(FEE) and Back-End DAQ system of Belle II experiment. It features, with system simplicity and reliability, as:

1. unification in hardware design(for each detector sub-system)
2. unification in firmware design(for each detector sub-system)
3. provides electrical isolation
4. provides high speed transmission rate
5. work at different input data rate(with different detector sub-system)
6. home brew transmission protocol
7. Slow control on the same link

Line rate 2.54Gps



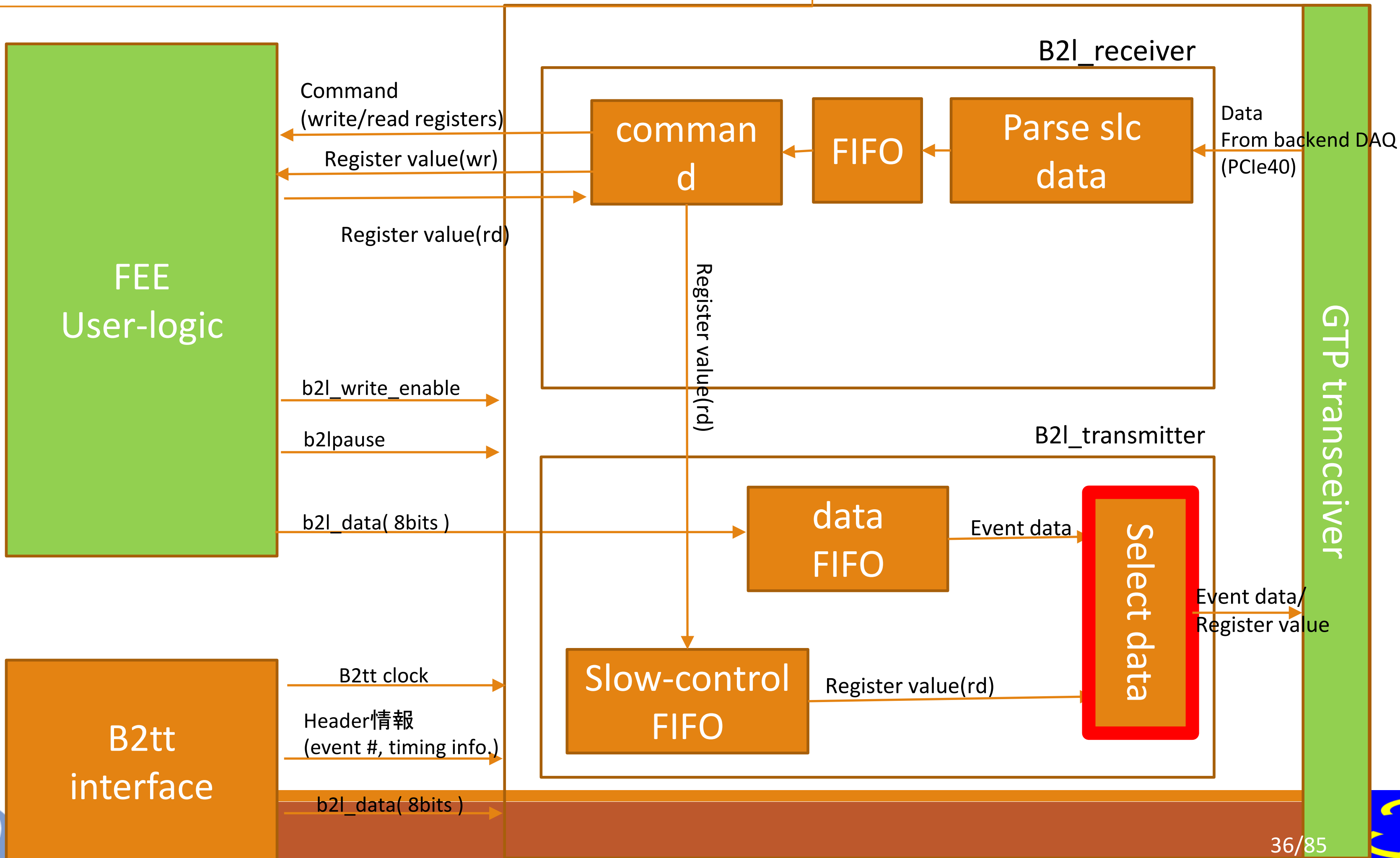
Detector FEE	Transceiver
SVD	Spartan-6 GTP
CDC	Virtex-5 GTP
TOP	Kintex-7 GTX
ARICH	Virtex-5 GTP
ECL	Spartan-6 GTP
KLM	Virtex-6 GTX
TRG	UT3: Virtex-6 GTX, GTH UT4: UltraScale GTH, GTY

Belle2link paper
https://doi.org/10.1016/j.phpro.2012.01.036

Belle2link core in FEE FPGA

- From Readout board : R/W of FEE registers
- To Readout board
  - Event data
  - Register value (read access from readout system)

Common FPGA IP core is prepared and each sub-detector FEE experts implement the core in their firmware

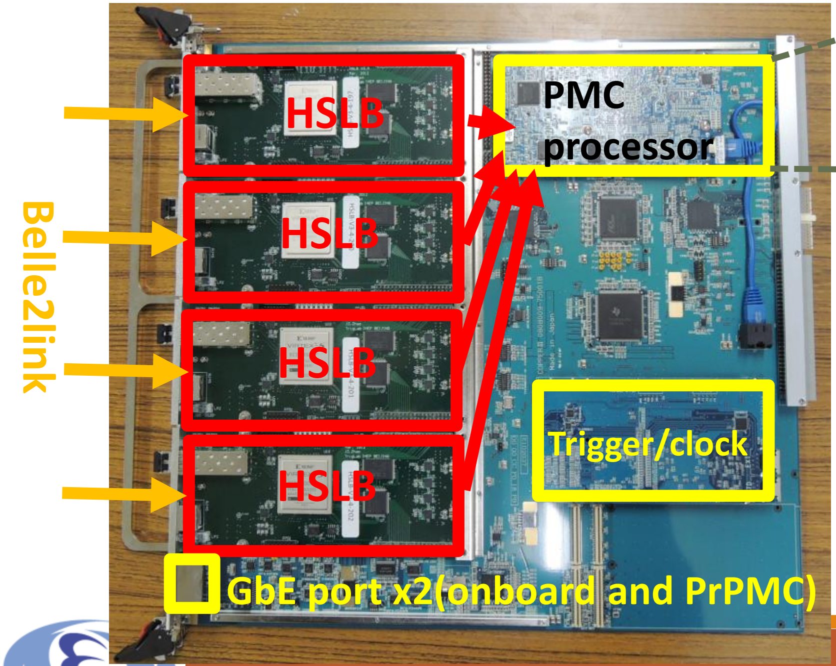


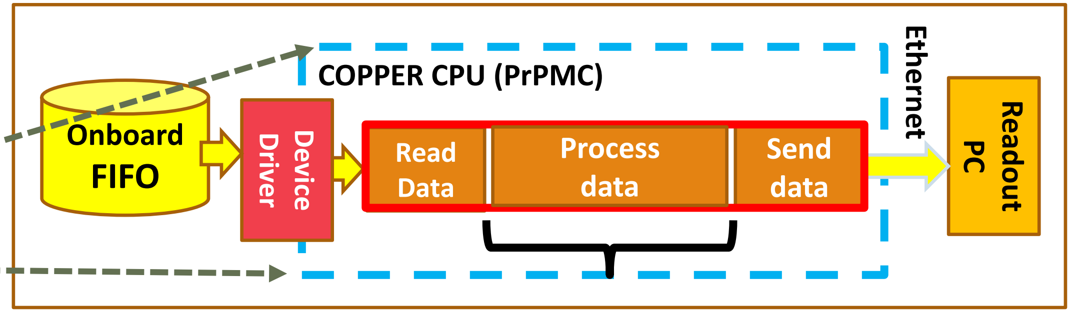
Data processing on readout board

- Readout board (-LS1) : COPPER (COmmon Pipelined. Platform for Electronics Readout)
  - Versatile DAQ board developed at KEK
    -> basically same functionality in the previous Belle experiment
  - can be equipped with various I/O cards and CPU card
    -> new daughter-boards for Belle II are used

- CPU: Intel Atom 1.6GHz Z530P
- DDR2 SDRAM 512MB
- PXE boot from ROPC
- Gigabit Ethernet x1

COPPER board





- **Data processing on COPPER CPU**
  - Data formatting (Add header and trailer to raw data)
  - Plain data check
    - Event incrementation, check magic word etc.
  - Add XOR checksum
  - Report data-flow status to slow control

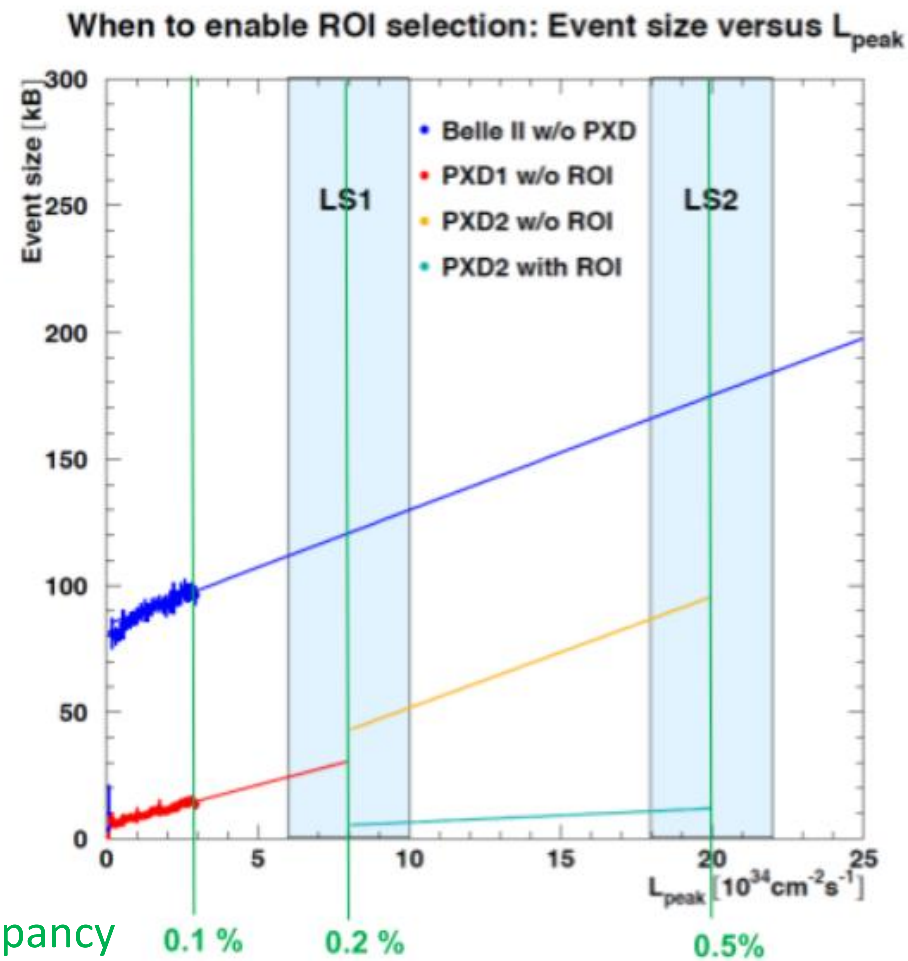
Current data size of PXD and other sub-systems

- PXD data size depends on hit occupancy
  - Since PXD data size is not so large, the ROI reduction has not been turned on yet.

- Detector occupancy in 2021 runs
 0.1 % => 15 kB/ev => 150MB/s
(L1 trigger rate = 10kHz)
- Expectations before LS2
- 0.5 % => 100 kB/ev => 3 GB/s @
(L1 trigger rate = 30kHz)

- Expected that fraction of PXD data wo ROI will grow from
10% to 60% to compare to all other detectors before LS2

(I.Koronov @FSP Workshop: Slow pion tracking)



Trigger system

Sub-Triggers

- CDC : for charged tracks (barrel only)
  - Momentum measurements : 2D and 3D
  - Impact parameter : dz (no dr)
  - Track counting : up to 12 tracks / charge
  - Event timing : jitter ~ 30ns
  - Event topology : back-to-back, opening angles, etc
- ECL : for neutral and charged tracks
  - Energy sum
  - Position and energy measurements : cluster by cluster
  - Cluster counting
  - Event timing : jitter ~ 30ns
  - Bhabha event ID
- TOP : for timing for charged tracks (barrel only)
  - Event timing : jitter < 10ns
- KLM
  - Muon tracking

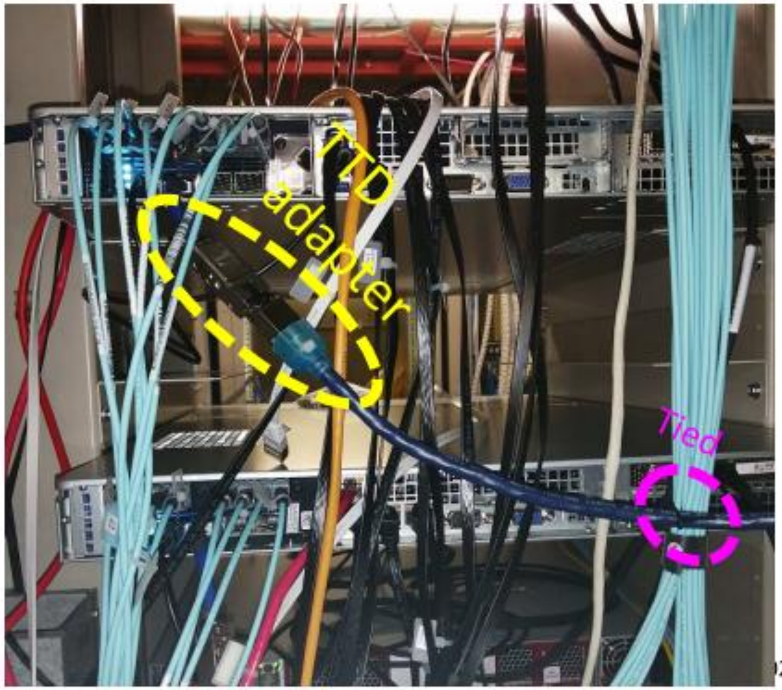
		Belle	Belle II
Process	C.S. (nb)	R @ L=10^{34} (Hz)	R @ L=8×10^{35} (Hz)
Upsilon(4S)	1.2	12	960
Continuum	2.8	28	2200
μμ	0.8	8	640
ττ	0.8	8	640
Bhabha *	44	4.4	350
γ-γ *	2.4	0.24	19
Two photon **	13	130	10000
Total	67	~190	~15000

* Rate of Bhabha and γ-γ are pre-scaled by factor 100

** Rates are estimated by the luminosity component in Belle L1 trigger rate

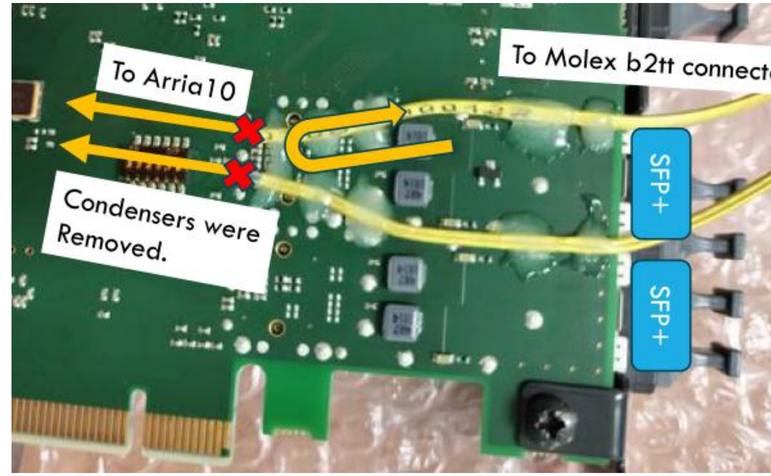
TROUBLES IN CONNECTION

- B2ldown in a channel (July. 20)
    - Reconnect connectors inside a patch-box -> recovered.
- frequent ttdown issues (July. 20)
    - After the TTD cable for rtop1 was tied to other cables, the TTD error signals disappeared. Tension in the TTD adapter was reduced ?



LAN cable interface -> optical interface :

- Motivation : Use SFP+ connector for the TTD system instead of a copper LAN cable.
  - For a test, soldering to connect SFP+ to general I/O port of Arria 10 was done by a company for one PCIe40 board.

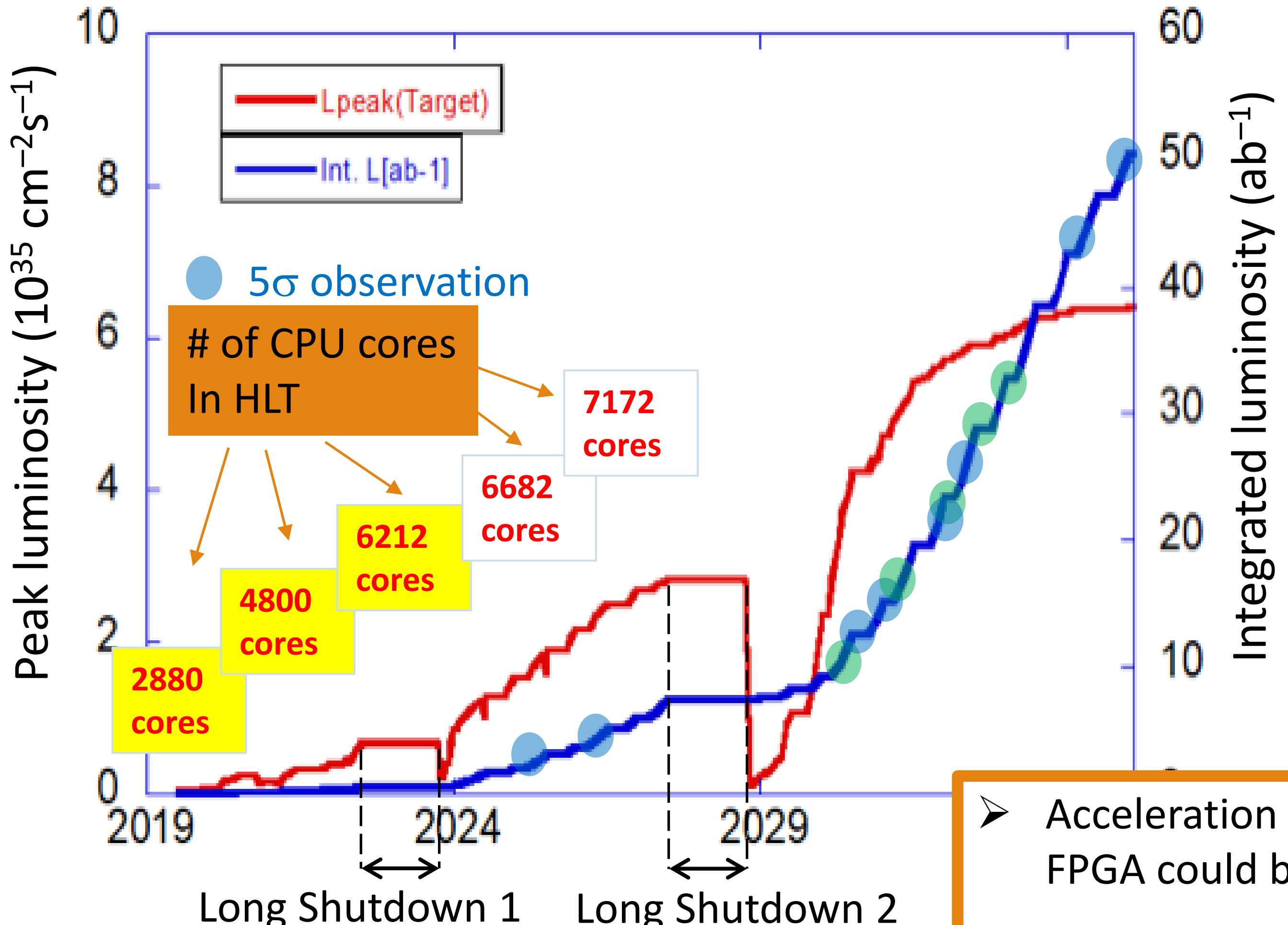


- The board works fine at B4 test bench(b3ropc06) but after it was moved to a KLM readout PC no TTD link was established. It was not working when putting back to the test bench. So, some mechanical damage might have happened on the fragile part.

- Since this soldering is an irreversible modification to the PCIe40 hardware, currently soldering on other PCIe40 boards is on hold.
- Hopefully, implementation of "auto-reset" scheme explained in this talk could help the reduction of ttlost from PCIe40.

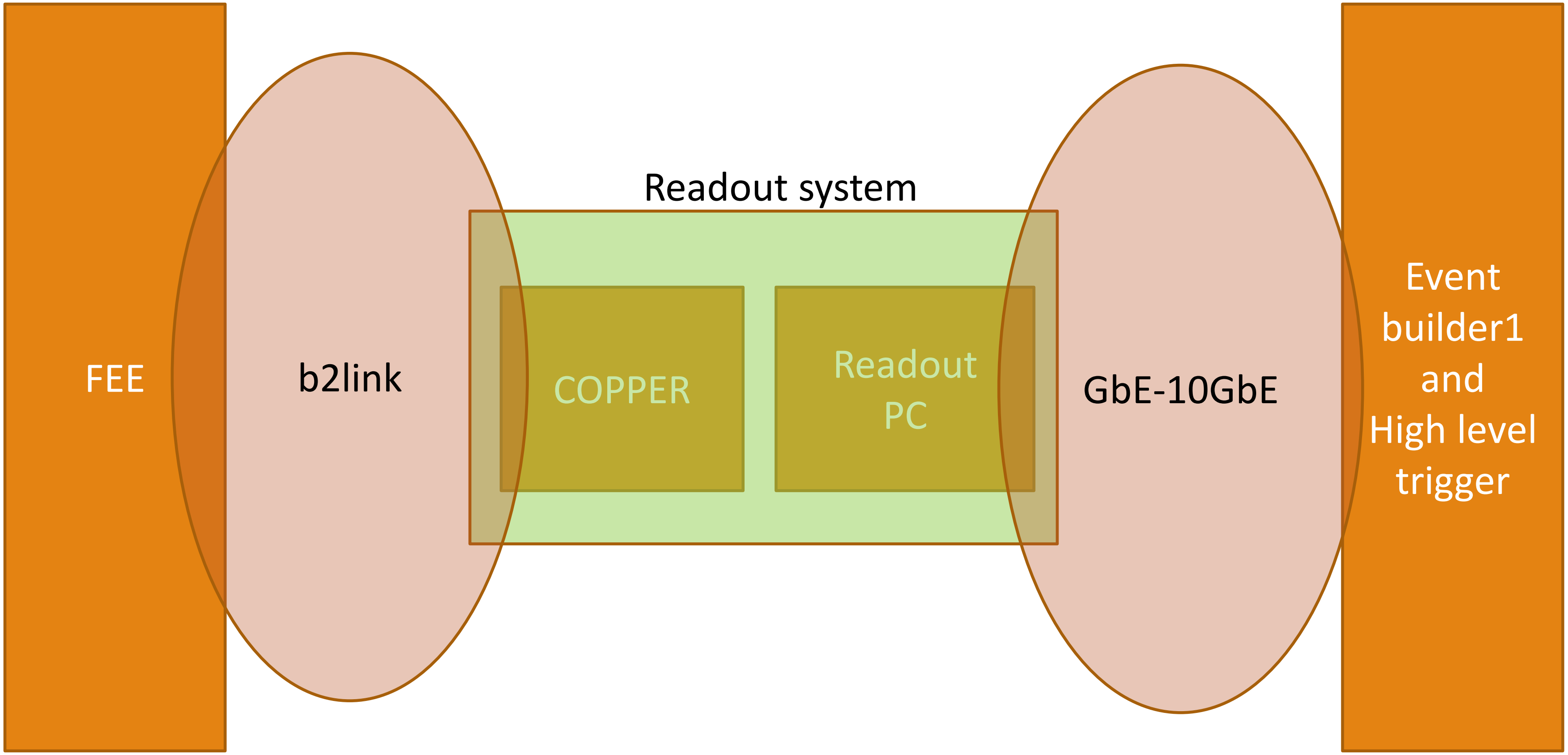
Increasing computational powers of HLT (# of CPU cores)

- Together with the tuning of reconstruction software, # of HLT units will be increased.
- It is a scalable system because event-building is done before HLT.
  - Increase # of HLT units and different events can be processed in parallel.



- Acceleration with GPU or FPGA could be another option.

Considering upgrade of readout system : boundary condition

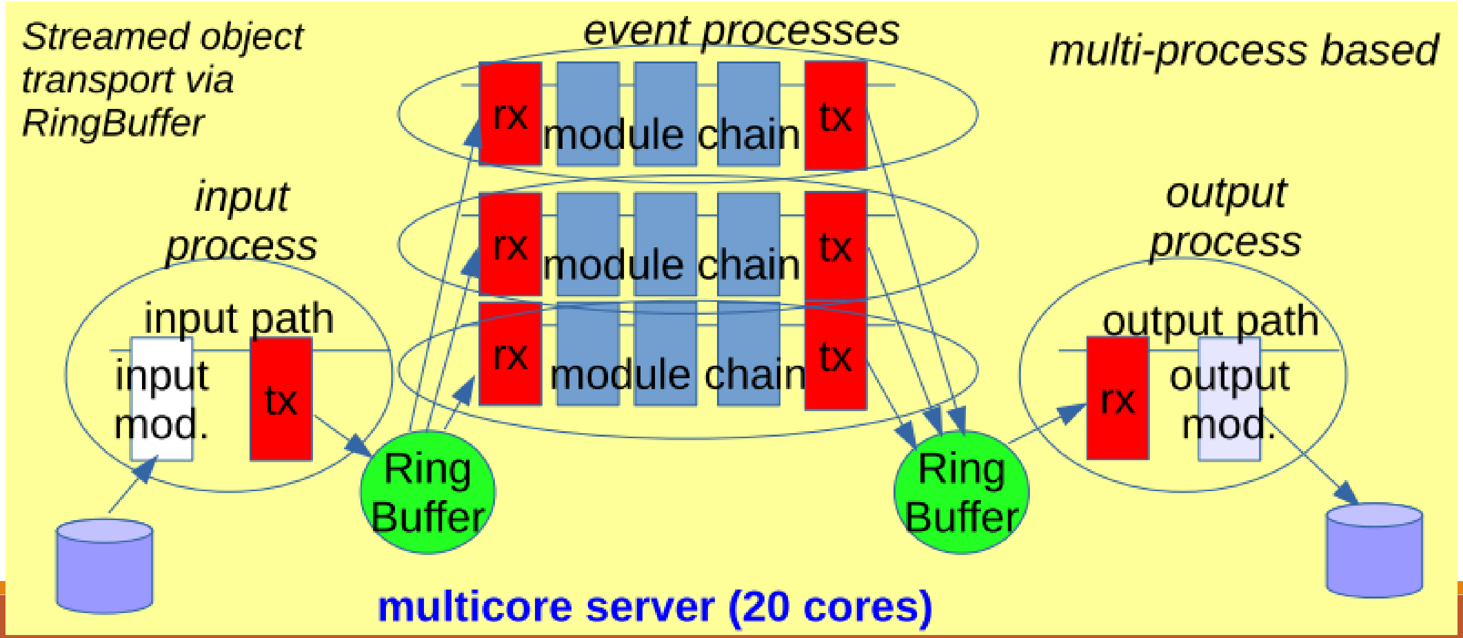


Basic framework of belle2link (Rocket-IO based serial link) should be the same. Otherwise FEE's FW/HW update might be needed.

Upgrade like GbE -> 10GbE will be possible, if we upgrade switches.

Software framework of high-level trigger

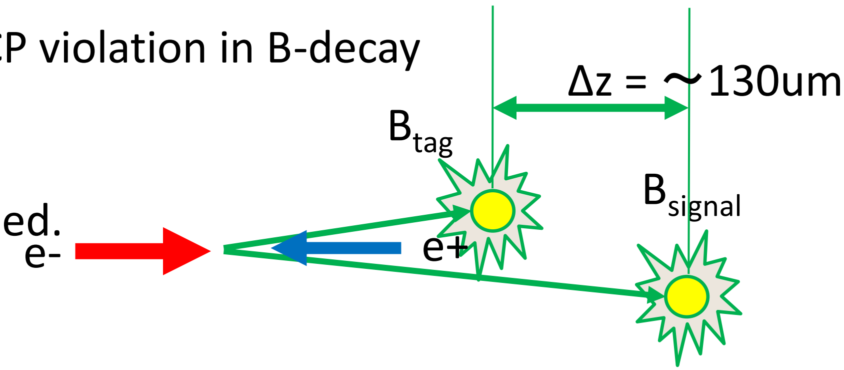
- Based on the event-by-event parallel processing implemented in Belle2 Analysis Framework (basf2).
- One HLT unit consists of :
  - Input server
  - Worker nodes
  - Output server
- We use multiple HLT units to achieve high performance.
- Unit structure. One unit houses 320 cores. Current : 5 units = 1600 cores (of 6400)



Golden mode for CP violation measurement : B→J/ΨK s

- This mode was used for the discovery of CP violation in B-decay
- Sensitive to ϕ1 angle

- Time dependent measurement is performed.



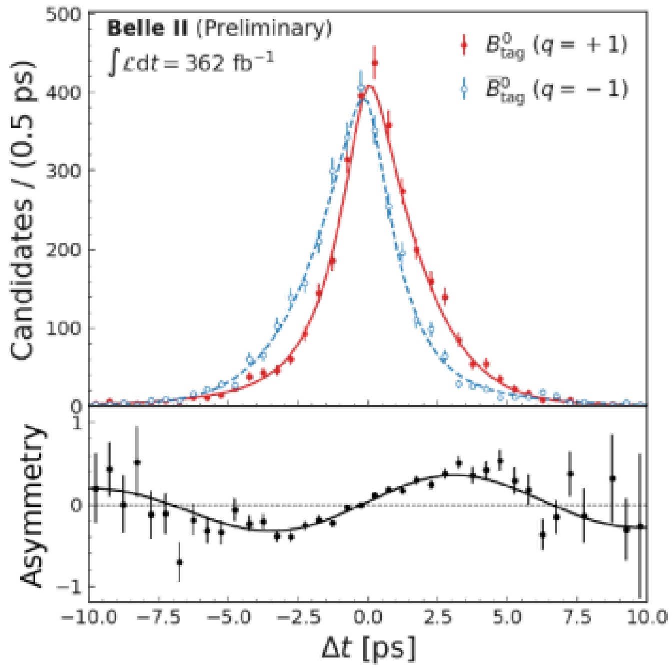
$$\mathcal{A}_{CP}(t) = \frac{N(\bar{B}^0 \to f_{CP}) - N(B^0 \to f_{CP})}{N(\bar{B}^0 \to f_{CP}) + N(B^0 \to f_{CP})}(t)$$

$$= S_{CP}\sin(\Delta m_d t) - C_{CP}\cos(\Delta m_d t)$$

The result with 362fb-1 of Belle II data

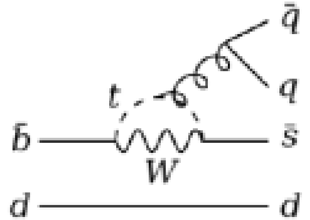
$$C_{CP} = -0.035 \pm 0.026 \pm 0.012$$
$$S_{CP} = \quad 0.724 \pm 0.035 \pm 0.014$$

HFLAV: $C_{CP} = 0.000 \pm 0.020$ $S_{CP} = 0.695 \pm 0.019$

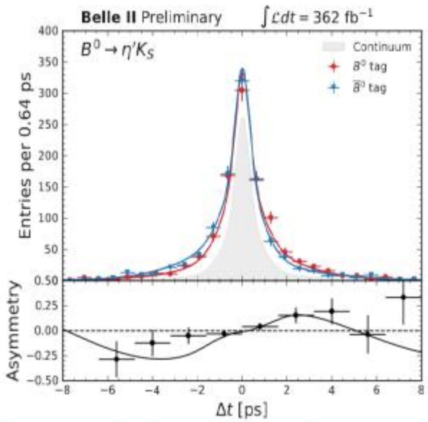


CP violation in penguin decays : B→η’K s , B→K s π 0 γ

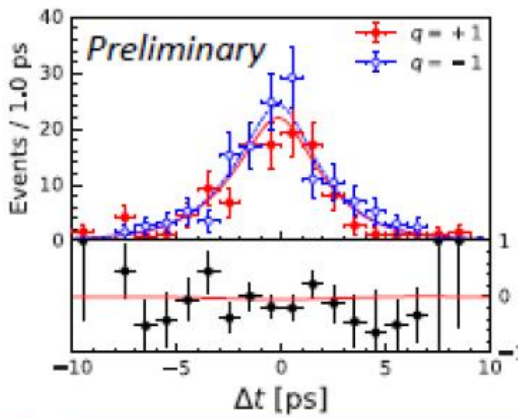
- Penguin mode : Contribution from new Physics to a loop can be expected.
- Time-dependent CPV was measured for some decay modes.
- Belle II has good sensitivity to decays including gamma.



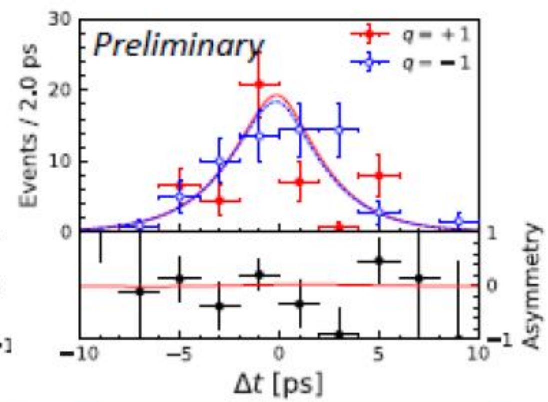
$B^0 \to \eta' K_S$



$K^{*0}\gamma$



$K_S\pi^0\gamma$



C_{CP} =-0.19 ± 0.08 ± 0.03
$S_{CP} = 0.67 \pm 0.10 \pm 0.04$

$C_{CP} = 0.10 \pm 0.13 \pm 0.03$
$S_{CP} = 0.00^{+0.27+0.03}_{-0.26-0.04}$

$C_{CP} = -0.06 \pm 0.25 \pm 0.07$
$S_{CP} = 0.04^{+0.45}_{-0.44} \pm 0.10$

HFLAV: $C_{CP} = -0.05 \pm 0.04$ $S_{CP} = 0.63 \pm 0.06$

HFLAV:
$K^{*0}\gamma$: $C_{CP} = -0.04 \pm 0.14$ $S_{CP} = -0.16 \pm 0.22$
$K_S\pi^0\gamma$: $C_{CP} = -0.07 \pm 0.12$ $S_{CP} = -0.15 \pm 0.20$

World record

- Currently, the result from 362fb-1 data is consistent with SM .

Unitarity triangle の精密測定

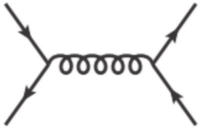
SM の非自明なチェック

BSM は量子効果により CP violation や B, K meson oscillation に影響

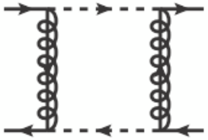
例：余剰次元模型 (Randall-Sundrum): たくさんのプロセス @ tree

超対称性模型: $\sin 2\varphi_1$ via $b \to s\bar{s}s$, ε_K, $\Delta M_{d,s}$ @ loop

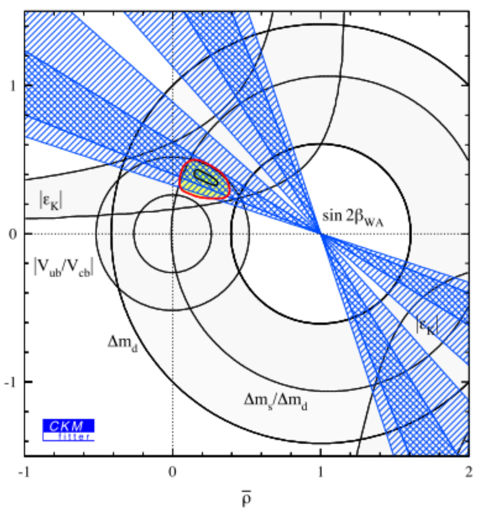
Randall-Sundrum



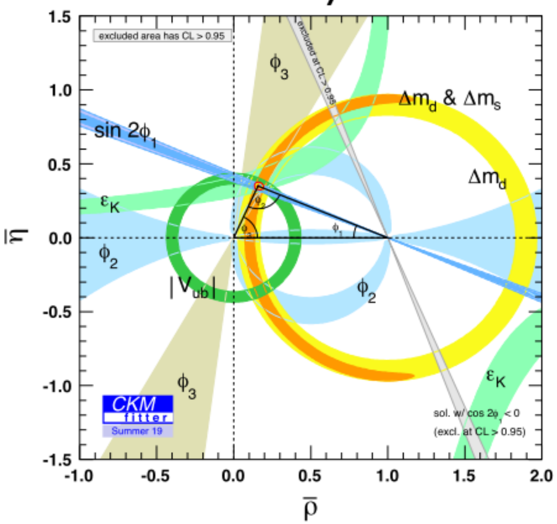
SUSY



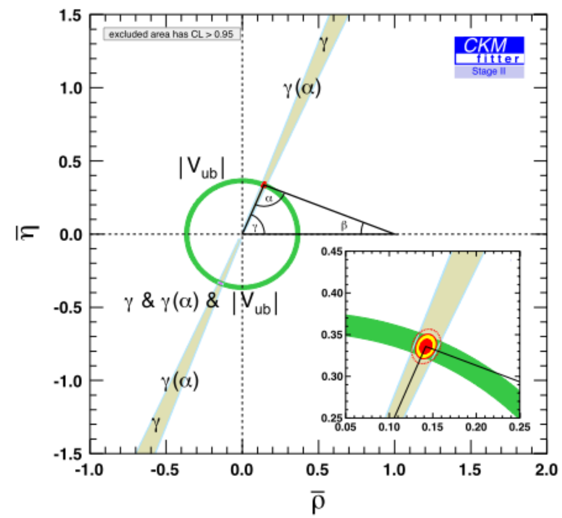
Past 2001



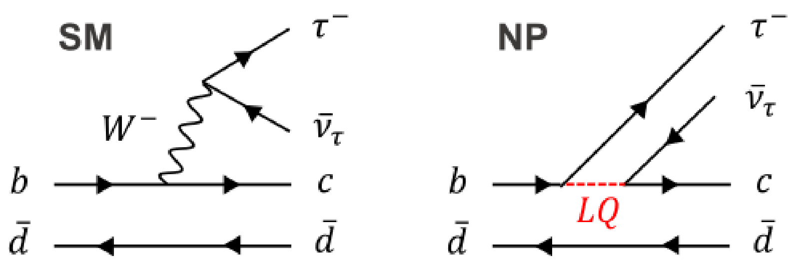
Today



Future [1309.2293]



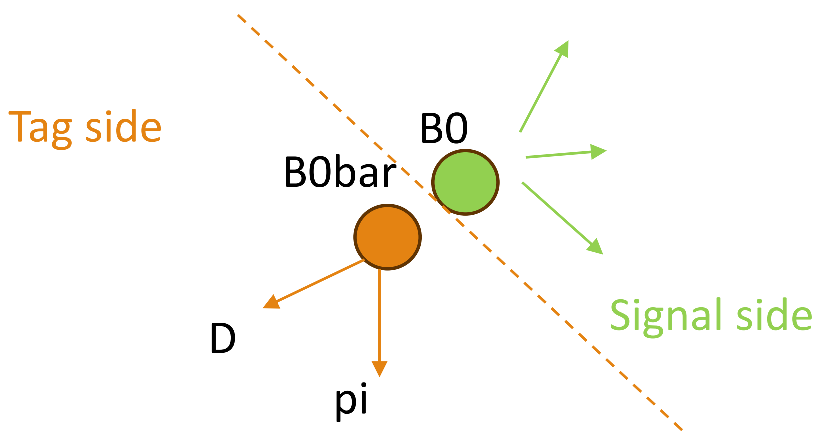
Anomaly(?) : B -> D(*)tau nu measurement : overview



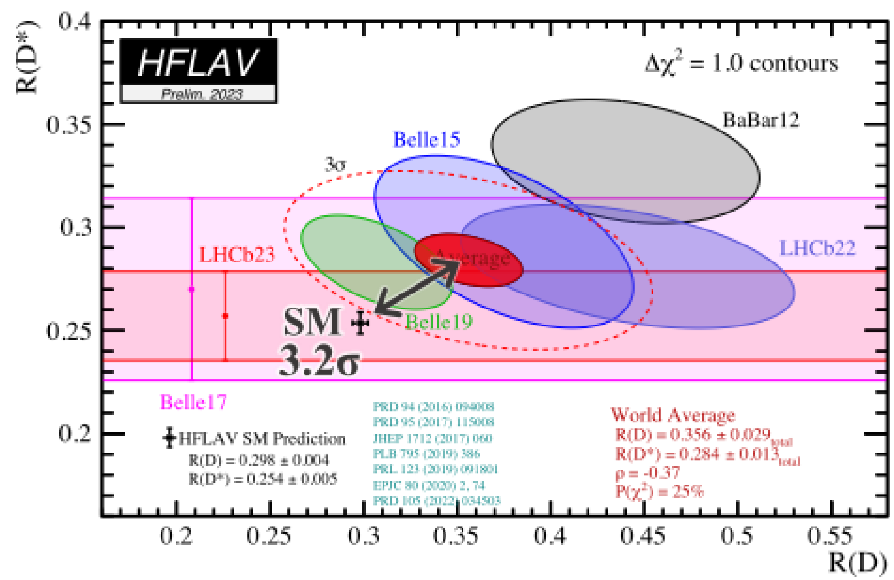
- Possible NP effect at tree level
- R(D*),R(D) : Clean theoretical prediction
- Tension(?) from SM prediction from combined results (Belle, Babar and LHCb)

R(D) = Br(B->Dτν)/ Br(B->Dlν)
R(D*) = Br(B->D*τν)/ Br(B->D*lν)

- Belle II recently report a new result of R(D*) with a hadronic tag method.



Current status of R(D*) and R(D)

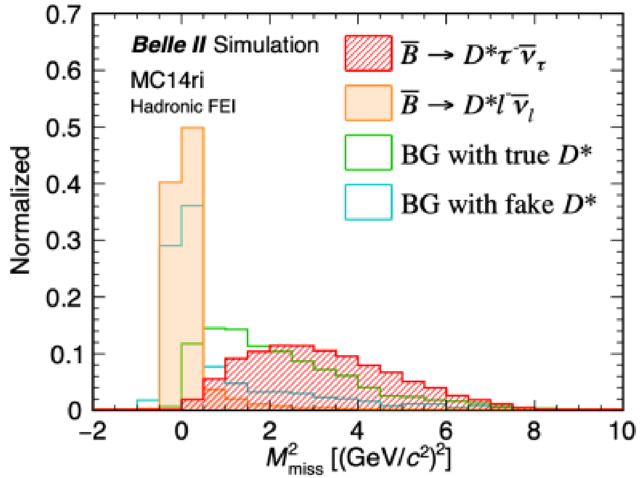


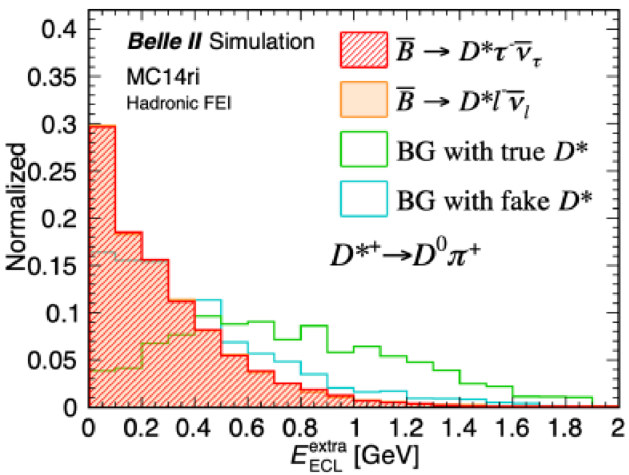
B -> D(*)tau nu measurement : Belle II new result

- Belle II 1st result with 189fb-1 data

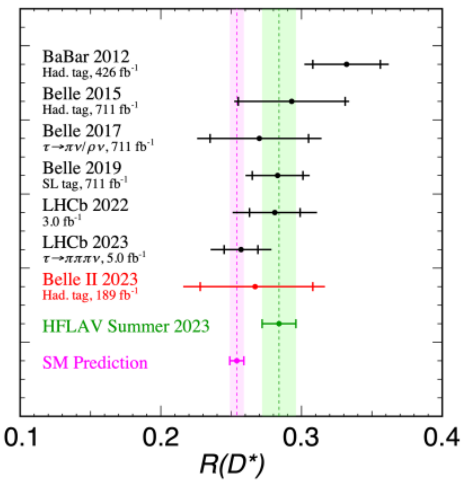
K. Kojima@2023JPS autumn

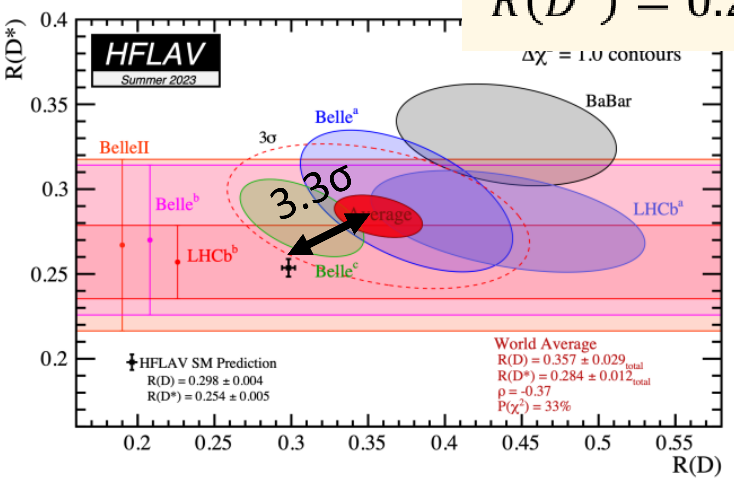
Fitting missing mass and extra energy on ECL calorimeter





$$R(D^*) = 0.267\ ^{+0.041}_{-0.039}(\text{stat.})\ ^{+0.028}_{-0.033}(\text{syst.})$$

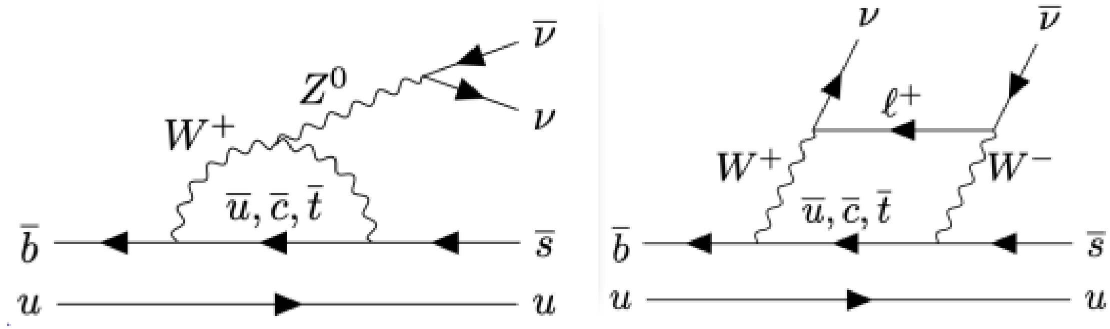




- Consistent with SM
- Analysis with semi-leptonic tagging would be available at winter conferences.

1^{st} evidence : B->Kνν decay

Decay in Standard Model : very rare decay

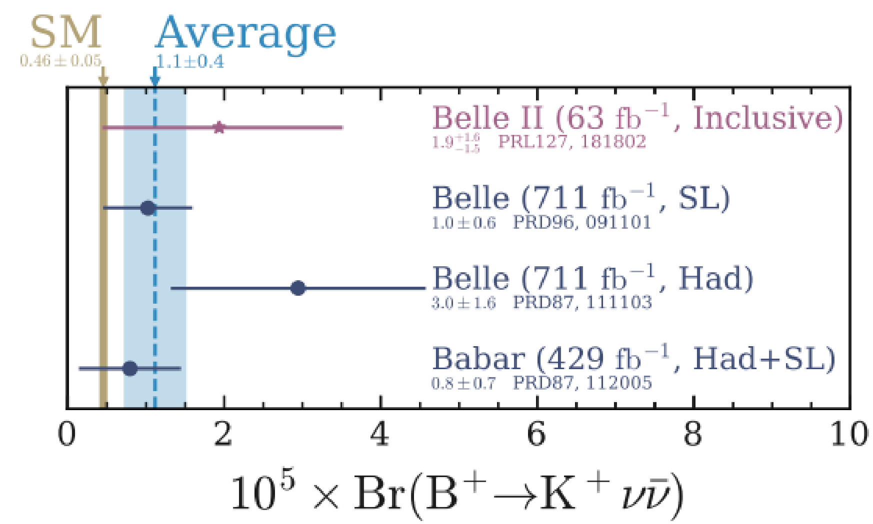


Preceise prediction for SM decay modes is possible.
Br(B->Knunu) = 0.56+/-0.04 e-5
->
Sensitive probe for new physics !

It has not bee discovered so far.

- Two neutrinos carries energy away.
- B.g. is relatively large compared with the branching ratio.

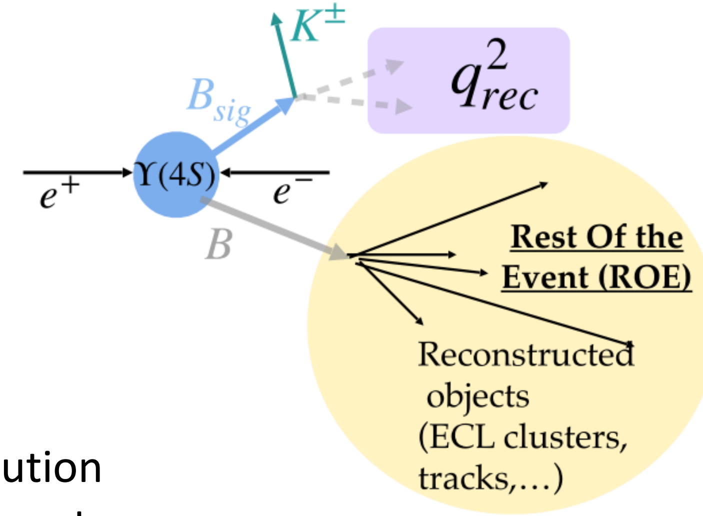
Experimental result for the BR of B->Knunu



B->Kvv decay : Inclusive tag analysis(ITA)

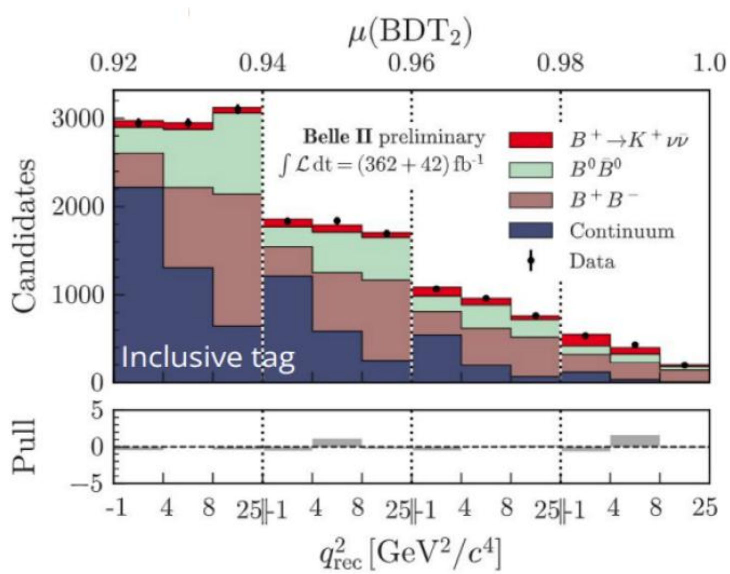
K^+ selection
Reconstruct a track with at least one pixel hit in and use PID to identify it askaon

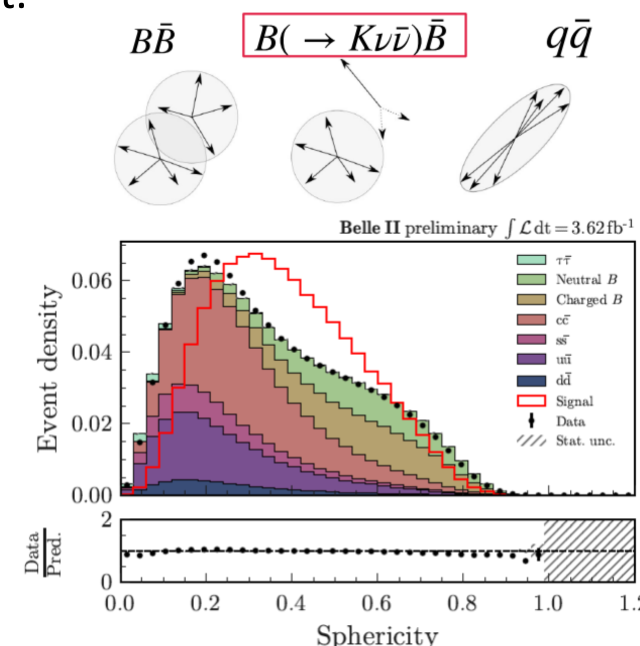
- ϵ(KaonID) $\sim$ 68 %
- mis-tag rate ($\pi \rightarrow K$) $\sim$ 1.2 %



Rest of the Event (ROE)
- Charged particles
- Neutrals
- Ks

Backgrounda suppressution with sphericyt of the event.

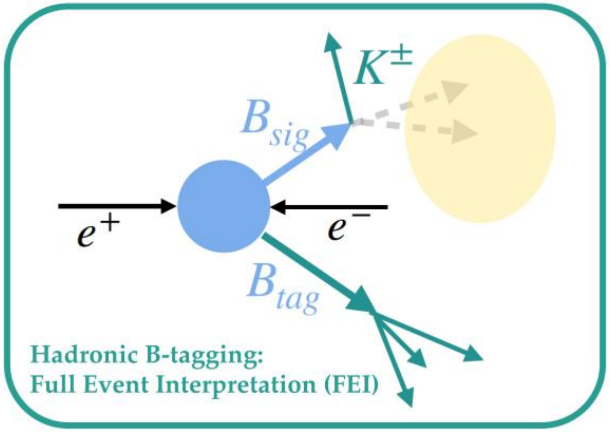




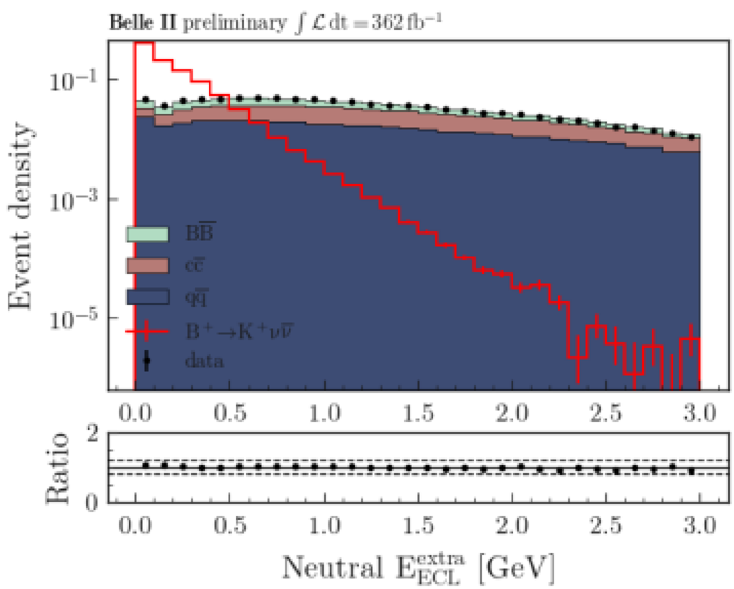
Inclusive tag:
B(B→Kvv)=(2.8±0.5(stat.)±0.5(sys.))×10^{-5}

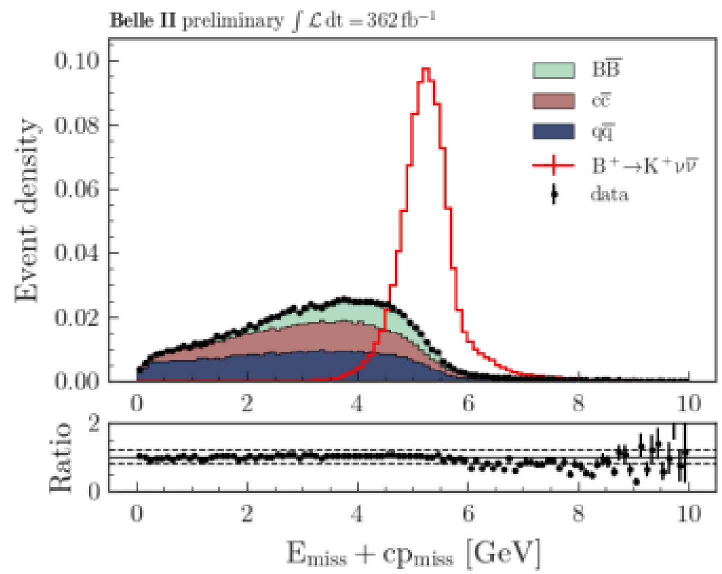
B->Kνν decay : Hadronic tag analysis(HTA)

- Reconstruct Btag events with 35 different hadronic decay modes
- Events from the HTA signal region represent only 2% of the signal region ITA



B.g. suppression with :
- Extra energy on ECL
- Missing energy and momentum



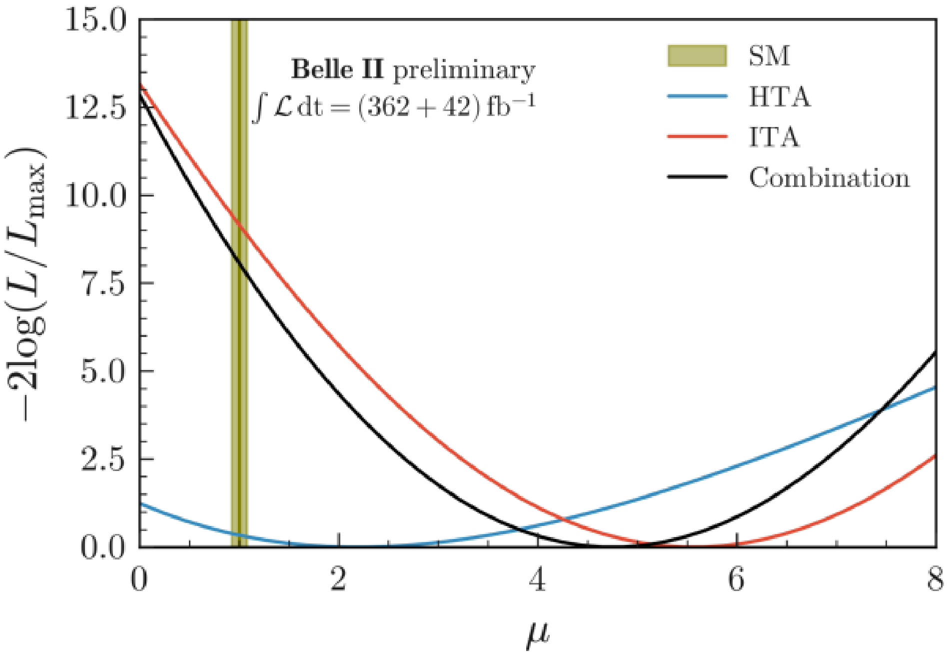


hadronic tag: B(B→Kνν)=(1.1+0.9/-0.8 (stat.)+0.8/-0.5 (sys.)) × 10^{-5}

B->Kνν decay : Combination of the results from two analysis

- 1st Belle II result with 63fb^{-1} data did not show the signal
- 362fb^{-1} result was reported in August this year.

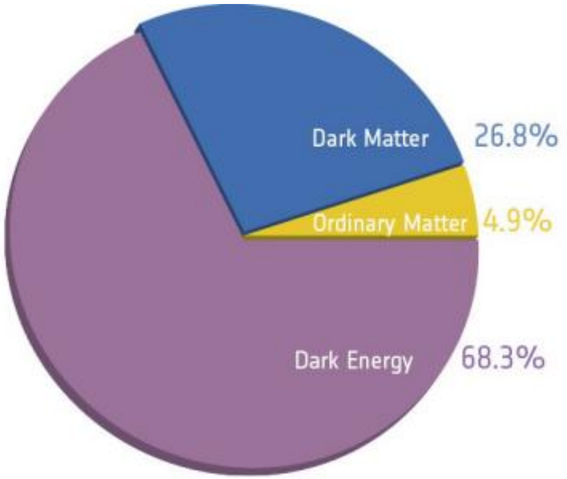
$$BR(B^+ \to K^+\nu\bar{\nu}) = [2.4 \pm 0.5(\mathrm{stat})^{+0.5}_{-0.4}(\mathrm{sys})] \times 10^{-5}$$



- 3.6sigma from the null hypothesis
- The measured branching ratio has the tension of 2.8sigma from the SM prediction

Direct search for new particle at Belle II : Dark sector

- Dark matter is still one of the biggest mystery in physics.
- WIMP around O(100)GeV has been the most prominent candidate but so far it has not been discovered yet at direct DM searches and the LHC experiments.
- Attempts to search DM in a wider field is ongoing.

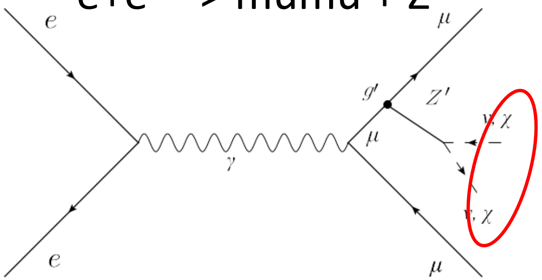


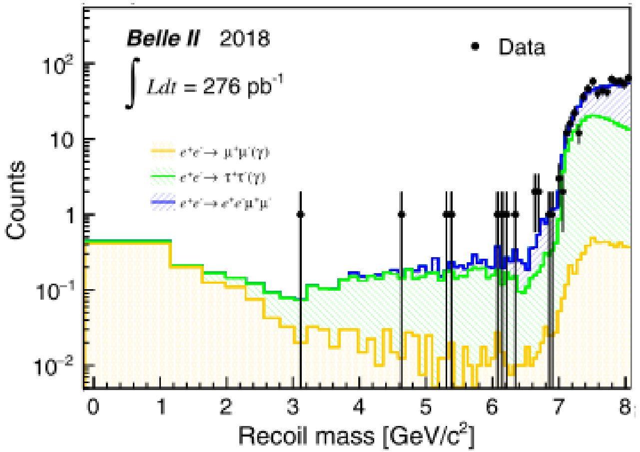
- When a hypothesis particle in a dark sector has slight coupling with SM particles, the decay to dark sector particles could be measured in accelerator experiments.
  - Belle II has sensitivity to the low mass (<10GeV)region.

Z' search : the 1st Belle II physics result

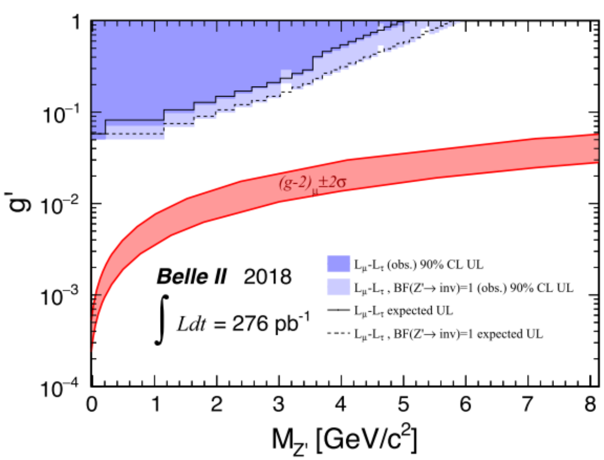
- Z' is produced by e+e- collision and decays into invisible particles(nu, dark matter)
- Z' mass can be measured from u+u- momentum
  - Peak should be found in recoil mass spectrum
- The biggest b.g. is:
  - e+e- -> τ+τ- and tau decays to mu and neutrino
- Set the limit to Mz' and coupling constant g' in Lmu-Ltau model

e+e- -> mumu + Z'

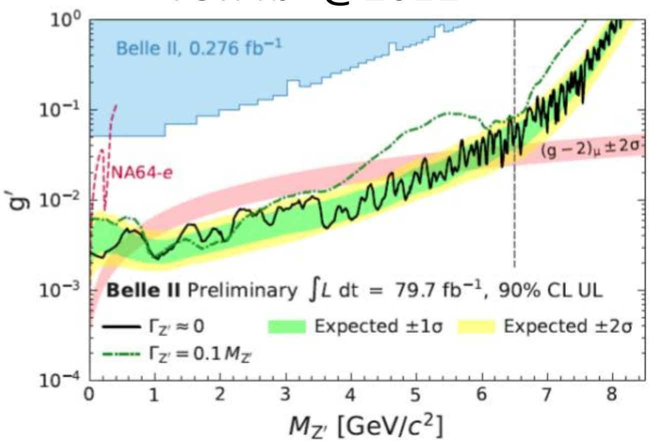




276pb^{-1} (1st result)

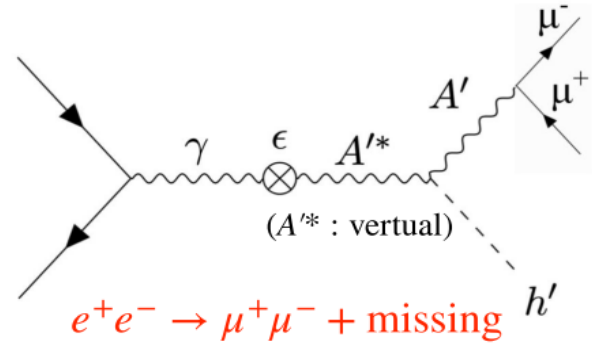


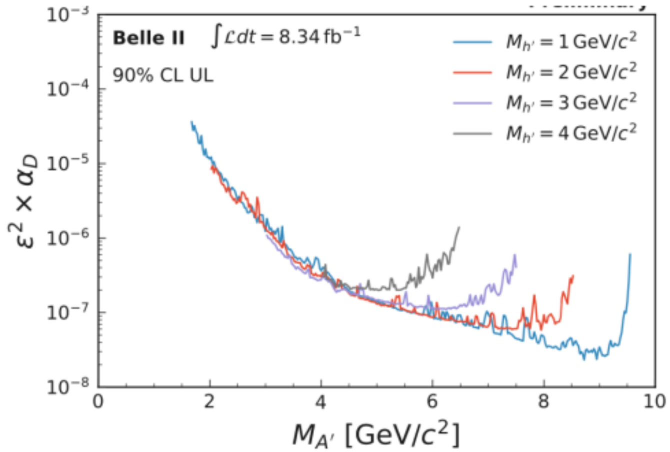
79.7fb^{-1}@2022

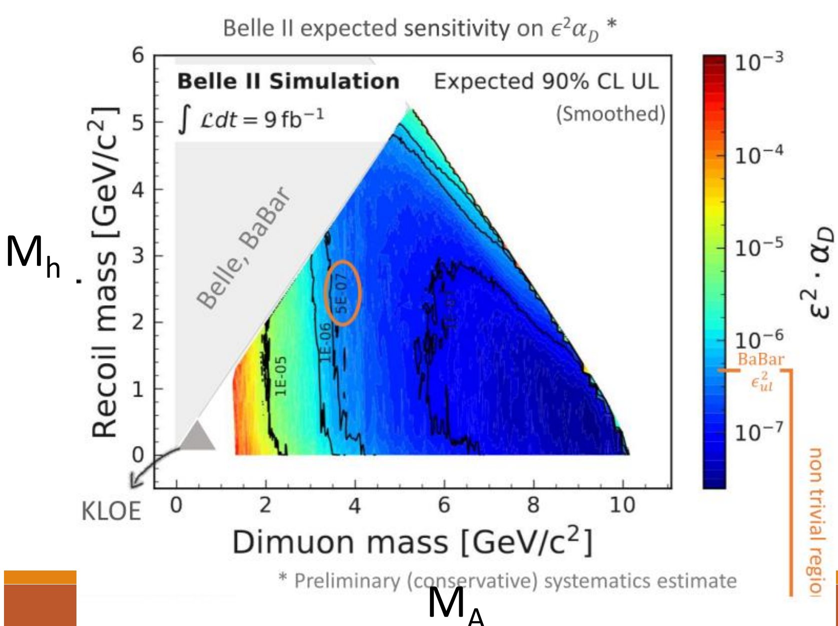


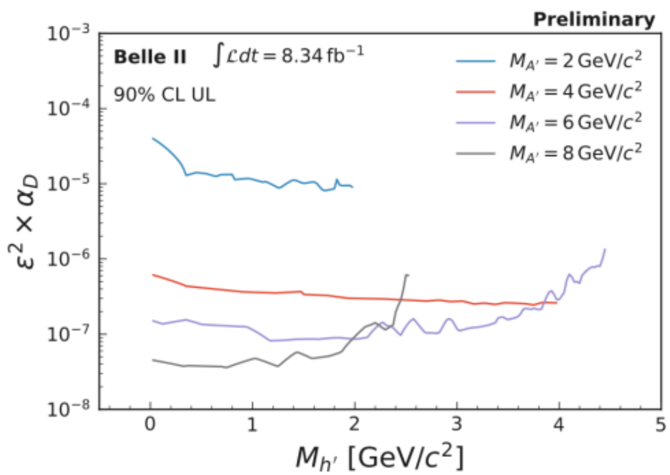
Dark photon and dark Higgs search

- E+e- -> A'(dark photon) + h'(dark Higgs)
- A' decays into u+u-
  - If A' is heavier than h' : h' is invisible
  - Missing energy : Strong field of Belle II
- World first limitation in Mass of A'[1.65-10.51 GeV] even with a small amount of data (=8.34fb-1)









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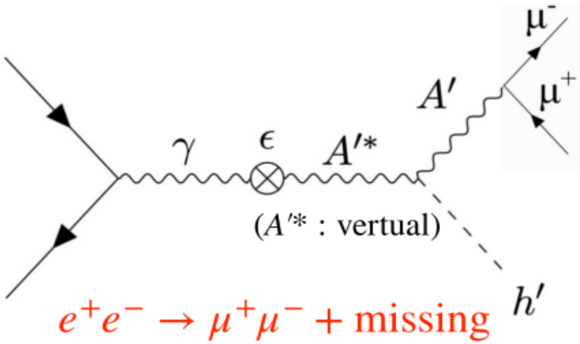
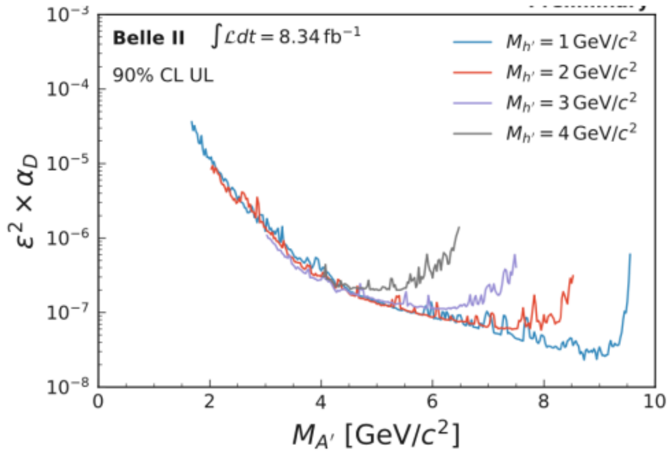
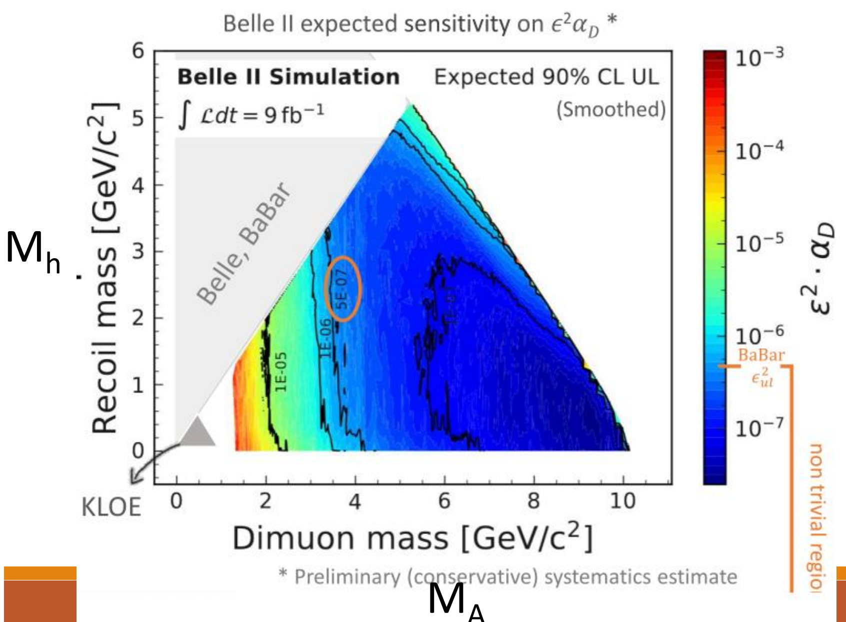
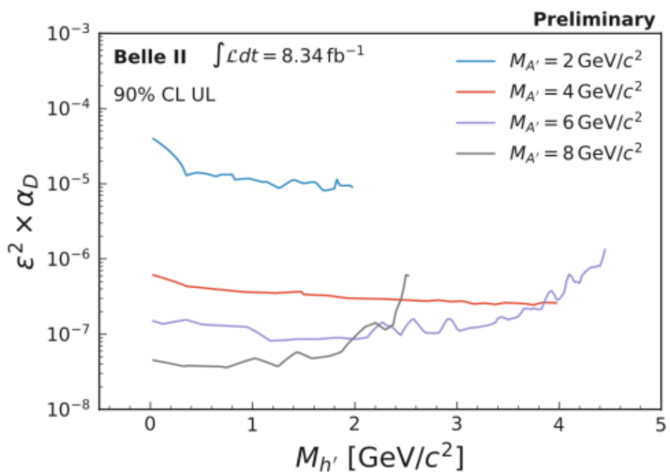


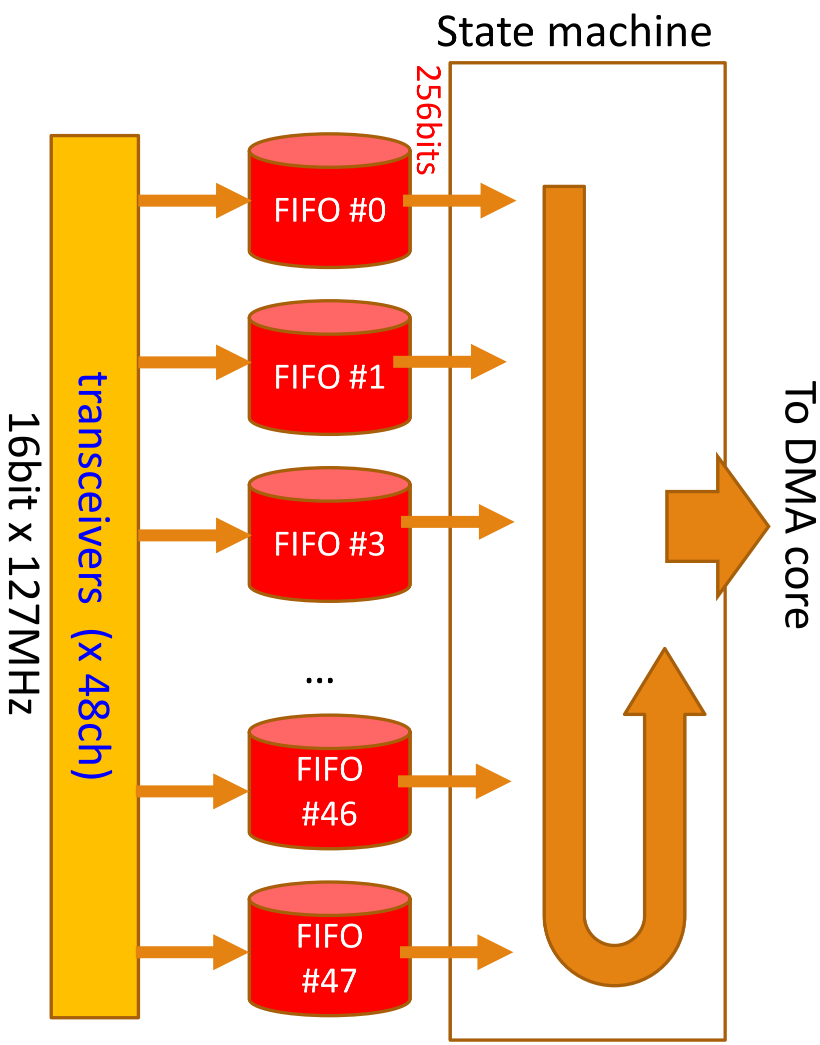






PCIe40 firmware user-logic part

- Implement the COPPER functions(fw+sw) to PCIe40 firmware



Functionalities of user-logic
- Event-building
- Formatting
- Data-check