Rubidium clock drift correction for HK timing system



Claire Dalmazzone, 2nd April 2025





Contents

- DAQ software installation on lpnlp3
- Cs clock



DAQ software installation on Ipnlp3

ClockDAQ on lpnlp3

- this should be avoided!!
- ~/Documents/dag
- the Rb.



The code under ~/Documents/daq had significantly diverged from master:

The new correction frontends were pushed to master and are also now in

 However, the srs frontend and instrument was refactored 2 months ago and I am not sure how to make it work anymore (would like the correction frontend to modify the ODB of SRS and that consequently a command to change the SF parameter of the clock is sent). I need it for the tests of SF correction with

First results with Cs

Cs clock

- are:
 - OUT3 TTL (front of the clock)
 - OUT4 TTL (back of the clock, left column)
- 10MHz as external reference.



• Was not using the correct output for the previous results... The PPS outputs

This time, used correct PPS output vs UTC(OP) measured by counter with Cs

First tests with the Cs



Drifted by ~20 ns in 5 days: would still need a correction. Would use at least ~50000s of GPS data for correction (~50 measurements).

Hyper-Kamiokande





Conclusion

- Two possible plans:
 - 1. Test correction method with the Cs clock
 - 2. Continue testing of SF correction with the Rb clock
- Difficult to do in parallel as it would require 2 receivers and 2 PPS UTC(OP)
- The setup is ready for number 2, would just require ~2-4 weeks, if I manage to send commands to the Rb to change SF through the srs frontend.
- Should not be difficult to change the setup for number 1 but it would require a longer data-taking (~1-2 months). Maybe need to fix the offset of PPS wrt UTC(OP).

