

OSCILLOQUARTZ SA

Factory Acceptance Tests

Model: OSA-3235B

S/N: N-4047360002-25078

Oscilloquartz S.A	Customer
Title: Lead Production Technician Date: 16.01.2025 Signature:  	Signature/Date:
Title: Senior Production Technician Date: 21.01.2025 Signature: 	

1 Scope

This document is the Factory Acceptance Test for the OSA-3235B Cesium Clock. The tests are performed according to the defined tests procedure, which are reported hereafter. The tests are verified against the technical specifications

2 List of equipment

Equipment Nr.	Function	Model	S/N or SW version
E1	DC Power Supply	TXL 750-48S	-
E2	Control Personal Computer (CPC) equipped with: Command and Management Software	CMSW	Last version
E3	Multichannel Frequency Comparator	VCH-315	Last version
E4	Measurement Personal Computer (MPC) equipped with: - frequency acquisition software - frequency analysis software	TSC 5110A Communication Stable32	Last version
E5	Reference frequency standard (FREF) compared to UTC	Active Hydrogen Maser	-
E6	Phase Noise Measurement System (PN)	EuropTest PN8000	E-692.00-C
E7	Ultra-low noise quartz oscillator (PREF)	Oscilloquartz 8788-AS	REF 004 et REF 002 (10MHz) Ref_3 et Ref_2 5MHz
E8	Oscilloscope 200 MHz (OSC)	Keysight DS0X2024A	TS 5836
E9	Oscilloscope	TDS 3032	TS 5375
E10	Digital Multimeter (DMM)	Fluke 73-III	TS 5033
E11	Digital Multimeter (DMM)	Fluke 75	TS 5025
E12	Power supply 0-60V 10A	SM 7020	05076
E13	Power supply 0-65V 10A	EA-PS 3065-10B	-

3 Test setup

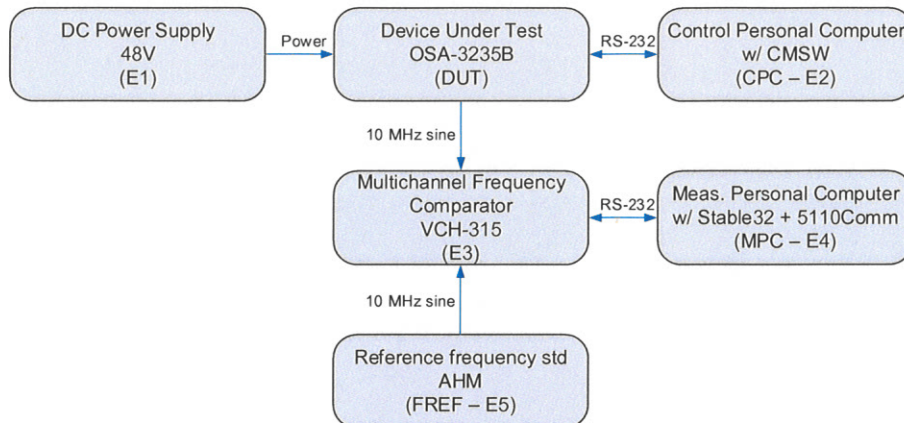


Figure 1: Test setup for clock frequency stability measurement: the Device Under Test (DUT) and the Reference frequency standard (FREF) are connected to the Multichannel Frequency Comp. (E3); the relative frequency difference is acquired and computed by the Personal Computer (MPC-E4).

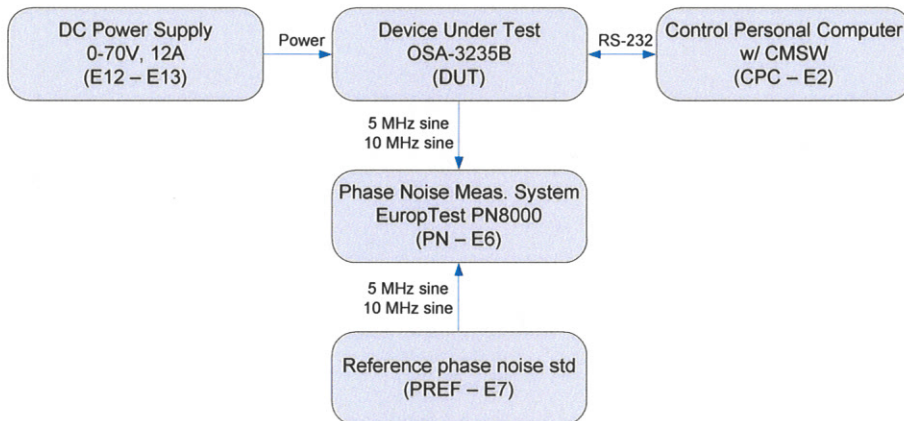


Figure 2: Test setup for clock phase noise measurement: the Device Under Tests (DUT) and the Reference phase noise standard (PREF-E7) are connected to the Phase Noise measurement system (PN-E6), which acquires the phase noise spectrum.

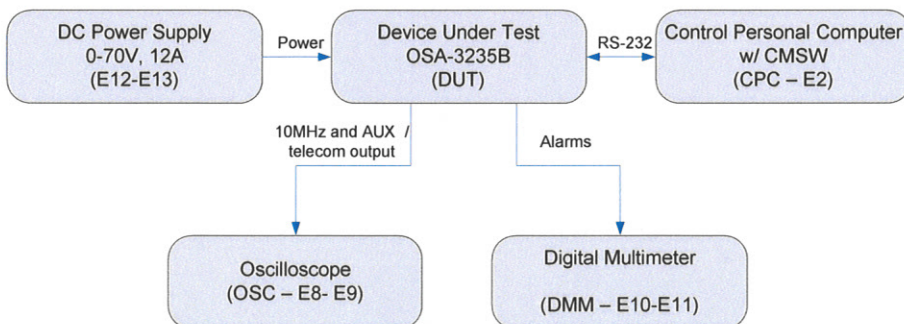


Figure 3: Test setup for clock interface verifications: the Device Under Tests (DUT) is connected either to the Oscilloscope (OSC-E8-E9) for the main sine wave and the auxiliary square wave output signal verification, and to the Digital Multimeter (DMM-E10-E11) for alarms verification.

4 Technical specifications compliance matrix

Test ID	Test Parameter	Test procedure	Specification	Test results	Compl. [C/PC/NC/NA]	Remark
Performance						
1	Accuracy	Record the relative frequency difference of the DUT as per Figure 1 in steady state environmental conditions. Compute its averaged value.	$\pm 1 \times 10^{-12}$	-0.11 x10 ⁻¹³ compared to UTC	C	
2	Short-term stability (Allan standard deviation, 10 MHz output): $\tau = 1$ s $\tau = 10$ s $\tau = 100$ s $\tau = 1'000$ s $\tau = 10'000$ s $\tau = 100'000$ s Floor	Record the relative frequency difference of the DUT as per Figure 1 in steady state environmental conditions for five uninterrupted days. Compute the Allan standard deviation for the specified integration time τ .	$\leq 1.2 \times 10^{-11}$ $\leq 8.5 \times 10^{-12}$ $\leq 2.7 \times 10^{-12}$ $\leq 8.5 \times 10^{-13}$ $\leq 2.7 \times 10^{-13}$ $\leq 8.5 \times 10^{-14}$ $\leq 5 \times 10^{-14}$	Not measured 5.61 x10 ⁻¹² 1.98 x10 ⁻¹² 6.21 x10 ⁻¹³ 2.18 x10 ⁻¹³ 6.43 x10 ⁻¹⁴ Not measured	C C C C C C NA	Refer to Figure 4 Not enough data points
3	Phase noise L(f) (10 MHz output): f = 1 Hz f = 10 Hz f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	Record the phase noise of the DUT as per Figure 2.	≤ -100 dBc/Hz ≤ -130 dBc/Hz ≤ -145 dBc/Hz ≤ -150 dBc/Hz ≤ -154 dBc/Hz ≤ -154 dBc/Hz	- 105 dBc/Hz - 138 dBc/Hz - 153 dBc/Hz - 159 dBc/Hz - 162 dBc/Hz - 163 dBc/Hz	C C C C C C	Refer to Figure 5

Test ID	Test Parameter	Test procedure	Specification	Test results	Compl. [C/PC/NC/NA]	Remark
4	Phase noise L(f) (5 MHz output): f = 1 Hz f = 10 Hz f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	Record the phase noise of the DUT as per Figure 2.	≤ -106 dBc/Hz ≤ -136 dBc/Hz ≤ -145 dBc/Hz ≤ -150 dBc/Hz ≤ -154 dBc/Hz ≤ -154 dBc/Hz	- 108 dBc/Hz - 141 dBc/Hz - 153 dBc/Hz - 160 dBc/Hz - 166 dBc/Hz - 167 dBc/Hz	C C C C C C	Refer to Figure 6
5	Reproducibility	Record the relative frequency difference of the DUT as per Figure 1 in steady state environmental conditions. Shut down the Cs clock and wait at least two hours to be cold. Restart the Cs clock and repeat the relative frequency measurement in the same environmental conditions. Record the variation of the relative frequency difference before and after the power shut-down.	$\pm 1 \times 10^{-12}$	3.48×10^{-15}	C	
6	Fractional frequency deviation over temperature cycle	Record the relative frequency difference of the DUT as per Figure 1 for a complete operational thermal cycle (-5°C to +55°C). Compute the maximum average frequency difference over the thermal cycle.	$\pm 2 \times 10^{-12}$	3.51×10^{-13} (peak-to-peak)	C	Refer to Figure 7

Test ID	Test Parameter	Test procedure	Specification	Test results	Compl. [C/PC/NC/NA]	Remark
	Interface					
7	OUT 1 10MHz sinewave Low noise	Measure the main 10 MHz output frequency. Please check if squelch function is available.	10 MHz sine, 1 Vrms $\pm$ 20% / 50 Ω Squelch on/off	10 MHz sine, 0.96 Vrms/ 50 Ω Squelch on/off	C	
8	OUT 2 5MHz sinewave Low noise	Measure the main 5 MHz output frequency. Please check if squelch function is available.	5 MHz sine, 1V _{RMS} (-10%+30%)/50 Ω Squelch ON/OFF	5 MHz sine, 1.18 Vrms/ 50 Ω Squelch on/off	C	
9	OUT 3 to OUT 5, Individually configurable TTL	Measure the auxiliary square wave outputs. Check if squelch function is available.	OUT 3: 1PPS, 0-3V/50 Ω OUT 4: 1MHz, 0-3V/50 Ω OUT 5: 10 MHz, 0-3V/50 Ω	1PPS, 3.26V/50 Ω 1MHz, 3.24V/50 Ω 10MHz, 3.22V/50 Ω	C C C	
10	OUT 6 Sinewave configurable	Measure the auxiliary sine wave output frequency. Check if squelch function is available.	Frequency range Min: 100kHz (>280mVrms/50 Ω) (>350mVrms/50 Ω) Max: 50MHz typ. 500mVrms/50 Ω)	100kHz 315mV/50 Ω 10MHz 494mV/50 Ω 50MHz 430mV/50 Ω	C C C	
11	Sync IN1 and IN2	Plug PPS signal reference in SYNC IN.1 Plug PPS signal reference from RF synthesizer lock on OSA Cs and add 1e-6Hz before synchronize. Use CMSW to set external Sync.	Check all outputs synchronization Positive edge synchronization Time delay: < 50 ns	Sync IN1: 12 ns Sync IN2: 10 ns	C C	

Test ID	Test Parameter	Test procedure	Specification	Test results	Compl. [C/PC/NC/NA]	Remark
12	PPS Delay at start	Set outputs to PPS mode, restart the clock, measure delay between all PPS including extension immediately when available. With no prior synchronization.	Time delay : <50 ns	1 ns	C	
	Option: Additional outputs					
13	OUT 1 to OUT 4 Individually programmable Telecom outputs: - E1 (2.048Mbits/s) - T1 (1.544Mbits/s) 2.048MHz 1PPS TTL 10MHz TTL	Measure the Telecom outputs. Check if squelch function is available. Asym: 75Ω, Sym: 120Ω 100Ω, Asym: 75Ω, Sym: 120Ω, 50Ω, 50Ω	OUT 1: 1PPS, ≥2.5Vpp/50Ω OUT 2: 10 MHz, ≥2.5Vpp/50Ω OUT3: E1 (G703-9) OUT4: 2.048 MHz (G703-13)	1PPS, 2.79 Vpp/50Ω 10MHz, 2.71 Vpp/50Ω E1/75Ω 2.048 MHz/75Ω	C C C C	
14	OUT 5 Sinewave configurable	Measure the auxiliary sine output frequency. Check if squelch function is available.	Frequency range Min: 100kHz (>280mVrms/50Ω) (>350mVrms/50Ω) Max: 50MHz typ: 500mVrms/50Ω	100kHz 390mV/50Ω 10MHz 530mV/50Ω 50MHz 500mV/50Ω	C C C	

Test ID	Test Parameter	Test procedure	Specification	Test results	Compl. [C/PC/NC/NA]	Remark
15	Alarm port: Critical Major Minor	When the 3235B is locked (LED fixed green), verify that the relays are properly contacted	Contact 1 & 3 Contact 4 & 6 Contact 7 & 9	Alarm port: Critical Major Minor	C C C	
16	Power	Measure the consumption (Steady state)	Power 1: <140VA Power 2: <70W	AC : 98 VA DC : 48 W	C C	

5 Test results

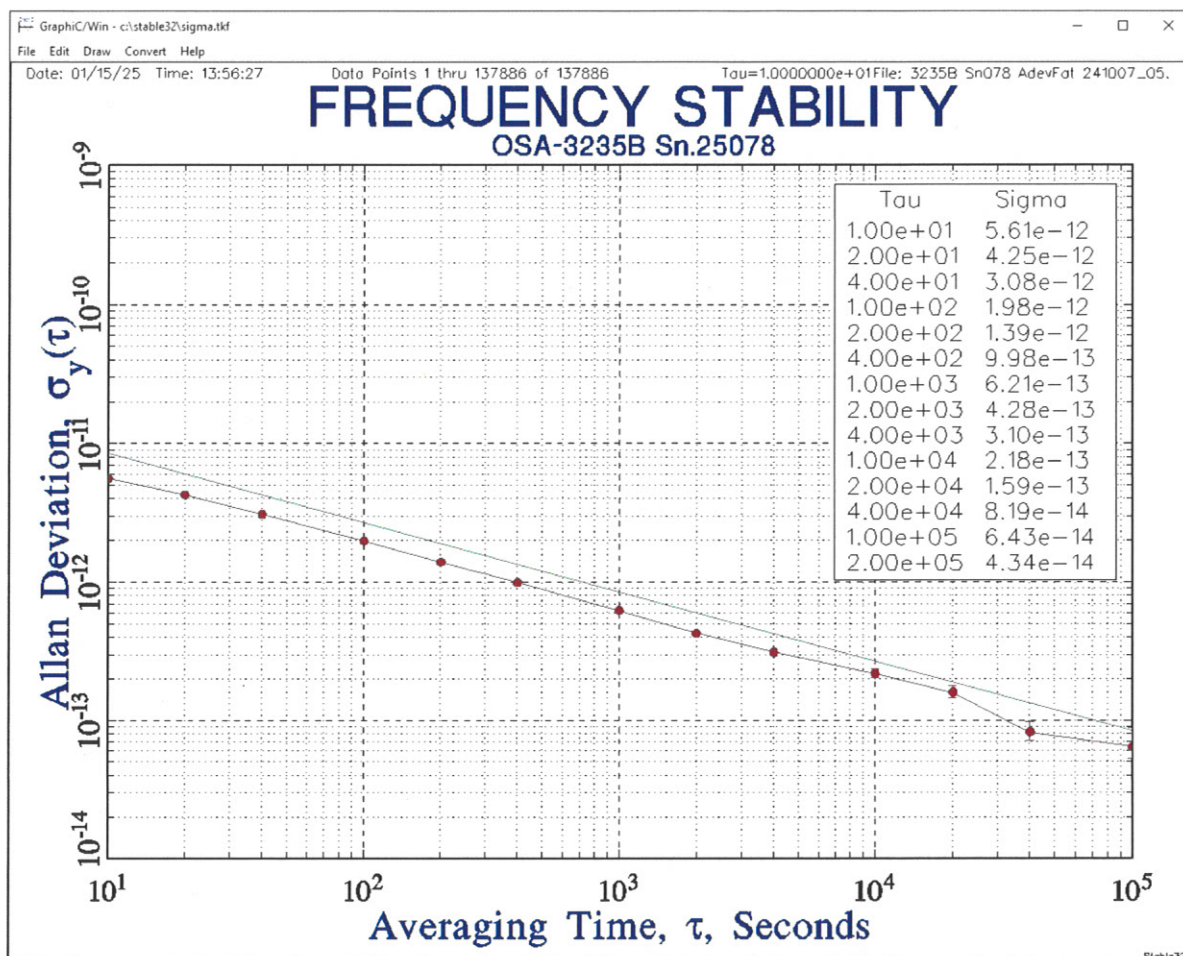
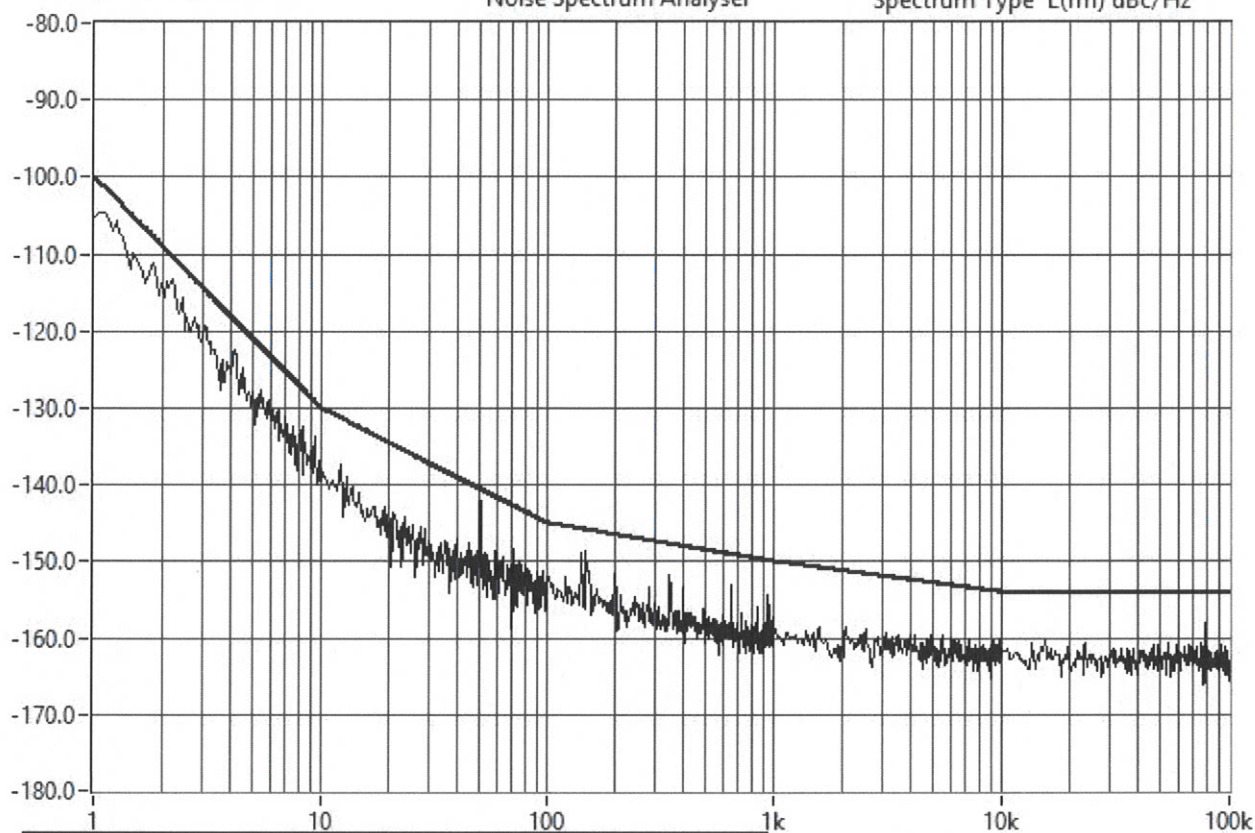


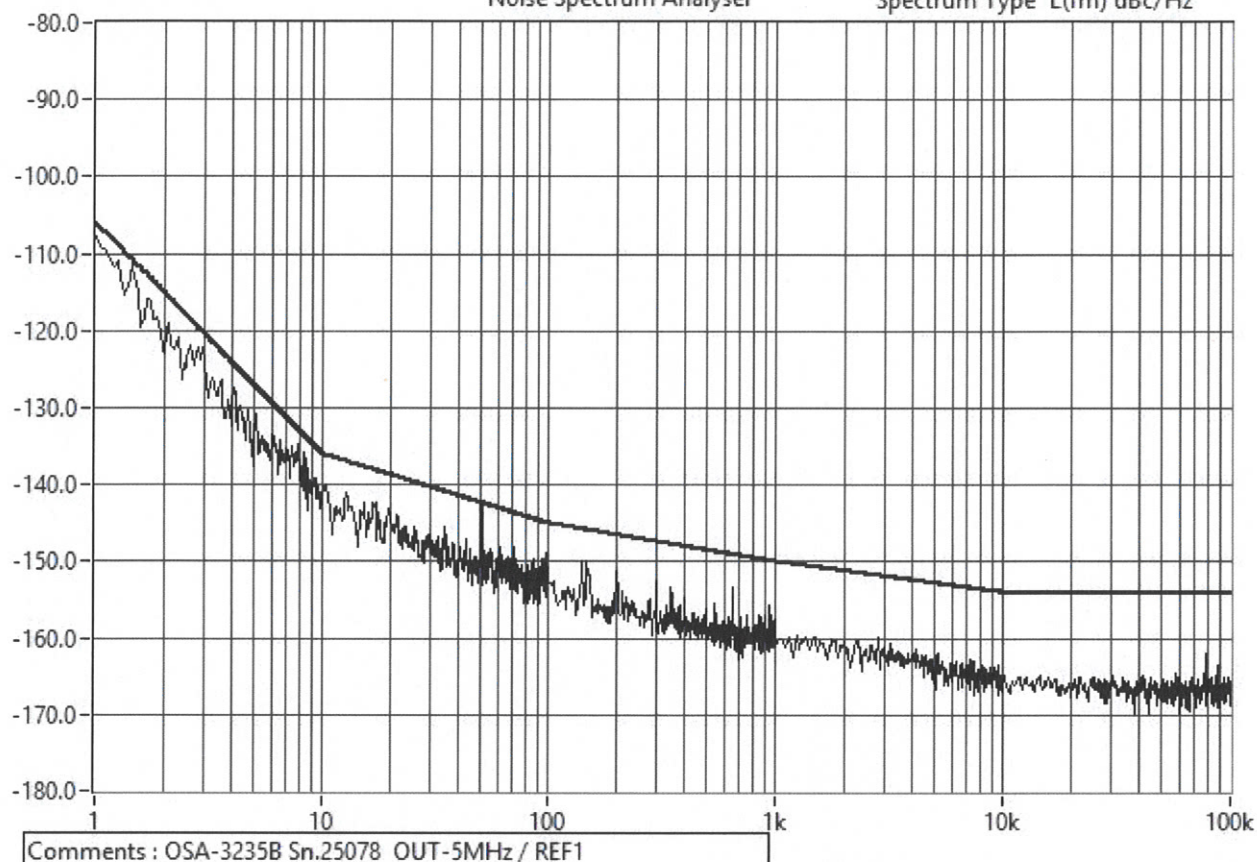
Figure 4: Short-term frequency stability (refer to Test ID Nr. 2).



Comments : OSA-3235B Sn.25078 OUT-10MHz / REF.003

3235B Sn25078
16 January 2025 16:22
SN : 07C00A0664 calibrated :08/05/2018
Phase
Kphi : 0.370
Loop BW : 1.0Hz
Tune Slope : 1.8Hz/V
Offset Ref : -3.0dB
Ref Spurs : 5.0dB
** Not compensated**

Figure 5: 10MHz Phase noise (refer to Test Nr. 3)



3235B Sn.25078
16 January 2025 16:46
SN : 07C00A0664 calibrated :08/05/2018
Phase
Kphi : 0.461
Loop BW : 1.1Hz
Tune Slope : 0.8Hz/V
Offset Ref : -3.0dB
Ref Spurs : 5.0dB
** Not compensated**

Figure 6: 5MHz Phase noise (refer to Test Nr. 4)

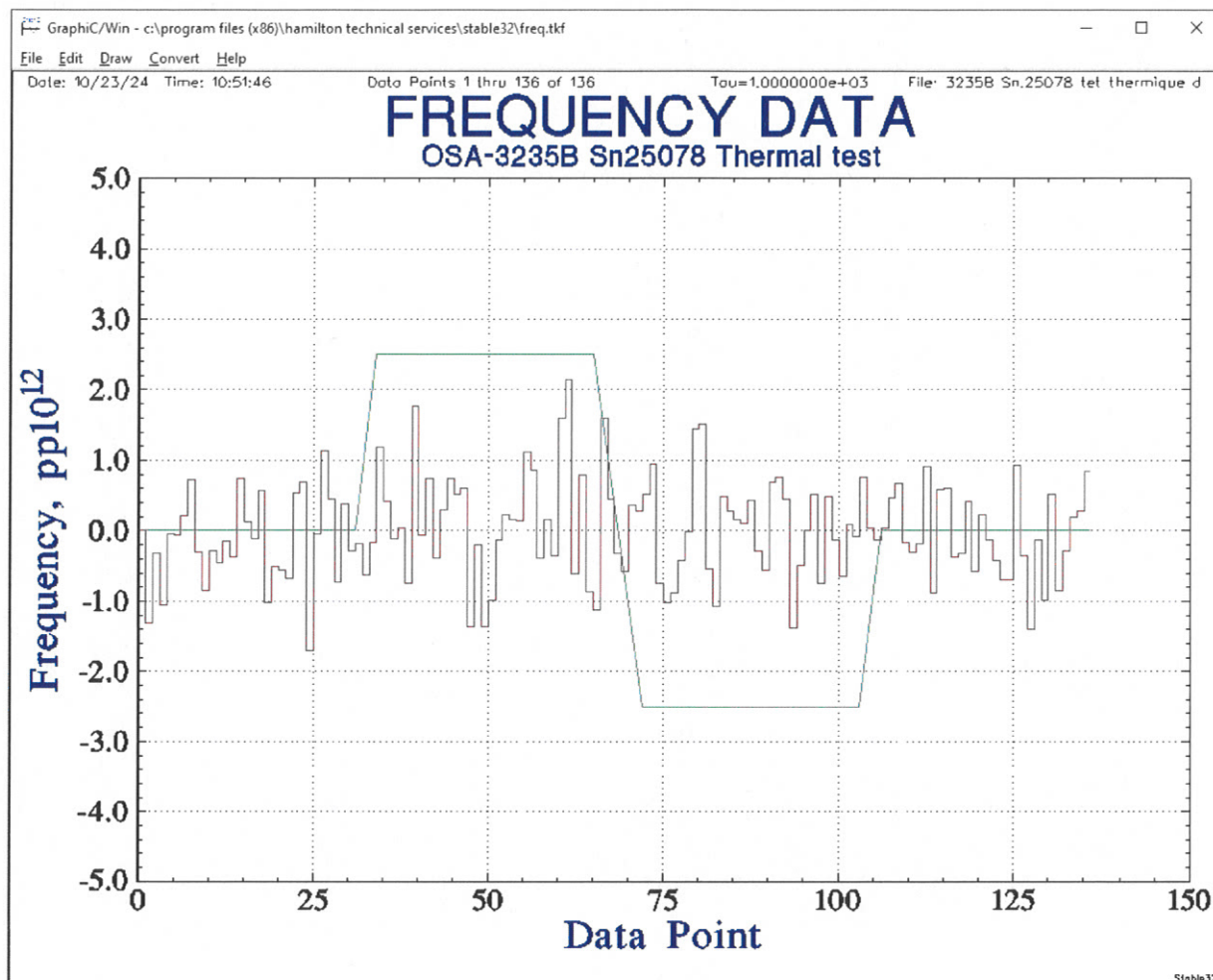


Figure 7: Fractional frequency deviation over temperature cycle compared to UTC (refer to Test Nr. 6)

Temperature	25 °C / 77 °F (9hours)	55 °C / 131 °F (9hours)	-5 °C / 23 °F (9hours)	25 °C / 77 °F (9hours)
Accuracy	-1.69e ⁻¹³	1.82e ⁻¹³	0.07e ⁻¹³	-0.68e ⁻¹³

Maximum average frequency difference: $ABS(Accuracy_{MAX} - Accuracy_{MIN})$

Inventory of Cesium	
File	
Title	Info
Equipment Type	OSA-3235B
Part Number	4047360002
Serial Number	N-4047360002-25078
Layout Version	3
Firmware Part Number	A016816
Firmware Version	1.12
Test Date	20241001
Oscillator Type	MV201
FPGA Version	3.03
Cesium Tube Type	A016282
Cesium Tube Serial Number	703416
FPGA Expansion Version	1.03
PSU Layout Version	4
PSU Firmware Version	1.02

Figure 8: RS232 port – Inventory request

OSCILLOQUARTZ SA

Add-on Factory Acceptance Tests Battery Tests

Model: OSA-3235B

S/N: N-4047360002-25078

<i>Oscilloquartz S.A</i>	Customer
Title: Lead Production Technician	Signature/Date:
Date: 15.01.2025	
Signature : Christophe Cristina	

1. Scope.

This document is an add-on of the Factory Acceptance Test for the OSA 3235B 19" Cesium Clock equipped with battery. The tests are performed according to the defined tests procedure, which are reported hereafter.

2. List of equipments.

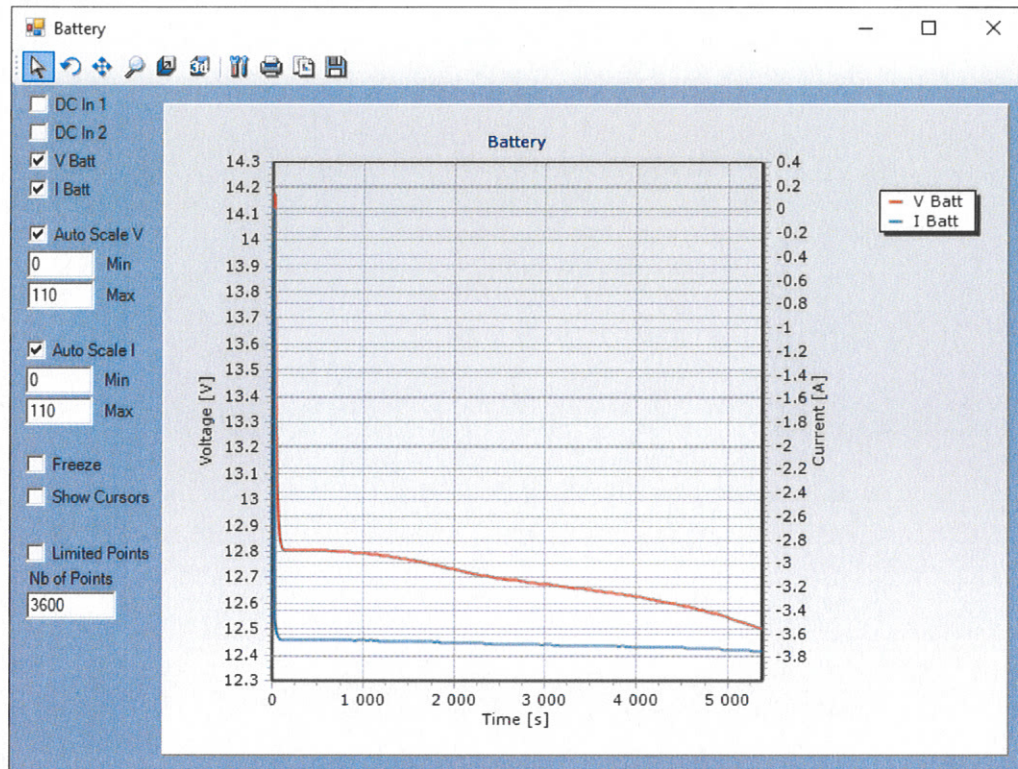
Equipment	Function	Model
CMSW	Monitoring Software	V 2.24 or Higher

3. Test results.

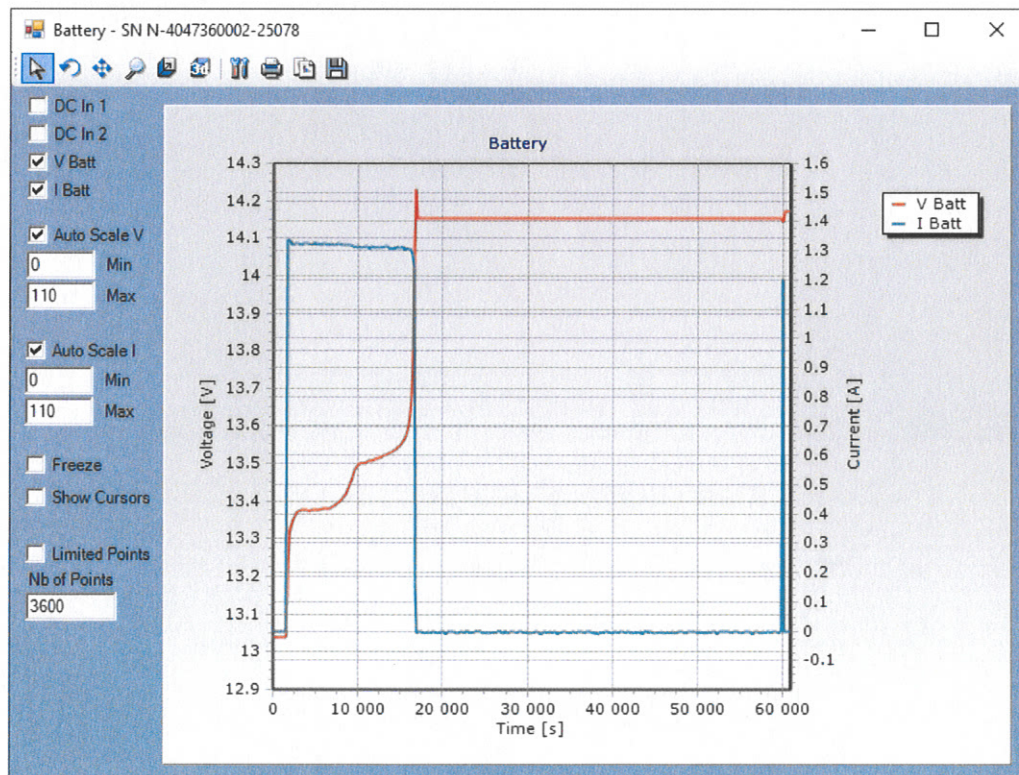
Test Name	Test procedure	Specification	Test result
Switch to battery	When PSU 1 and 2 disconnected from Cs Clock, Check that Clock switch immediately to battery power supply.	Switch with no shut down or signal degradation.	C
Discharge performance.	Record the current value/voltage value until full discharge and unit shutdown.	60 minutes.	90 minutes
Recharge-Discharge-Recharge Cycle.	Plug back PSU On clock Recharge-Discharge-Recharge.	No discharge / recharge failure.	C

4. Screen battery discharge/recharge.

5.



a. Full discharge.



b. Recharge-Discharge-Recharge cycle

Magnetic Cesium Clock Equipment



**THIS PRODUCT CONTAINS ELECTRO-STATIC SENSITIVE DEVICES.
DAMAGE CAN OCCUR IF INCORRECTLY HANDLED.**

1. When you receive the Magnetic Cesium Clock equipment:

Power ON the unit, It may take up to 50 minutes for the LED's to turn to a steady green.

If the LED's do not display green after 50 minutes perform the following:

Power OFF the unit and wait for 5 seconds and then power ON the unit again.

If the LED's do not display as a steady green within 50 minutes then contact the support group for assistance.

2. General maintenance

This product must not be stored without power for more than 2 months. If this Magnetic Cesium will be stored for more than 2 months then power should be applied every two months and remain powered on for at least 4 hours. All LED's should display a steady green light within 50 minutes as outlined above.

READ THE PRODUCT USER MANUAL SAFETY GUIDE AND INSTALLATION INSTRUCTIONS BEFORE INSTALLING THE PRODUCT OR CONNECTING POWER.



CAUTION

Check first that the packaging does not have any signs of rough handling such as dents or scratches, which might have occurred during transportation. Also inspect the equipment carefully for possible damage (broken knobs, bent handles, etc.). Should the equipment have suffered any damage, immediately notify the carrier and retain the packing material for inspection.



Recommendation:

We recommend saving the packing material for use in case of return shipment. Should you need to return the equipment, please do not hesitate to contact ADVA for help in obtaining appropriate packing material.



CAUTION

When handling the Magnetic Cesium Clock unit or spare cards, the operator must use grounded wrist straps.
