Commissioning and further development of cryogenic readout electronics for LAr-TPC applications

《New project proposal》

Dario Autiero[a], Ritsuya Hosokawa[b]

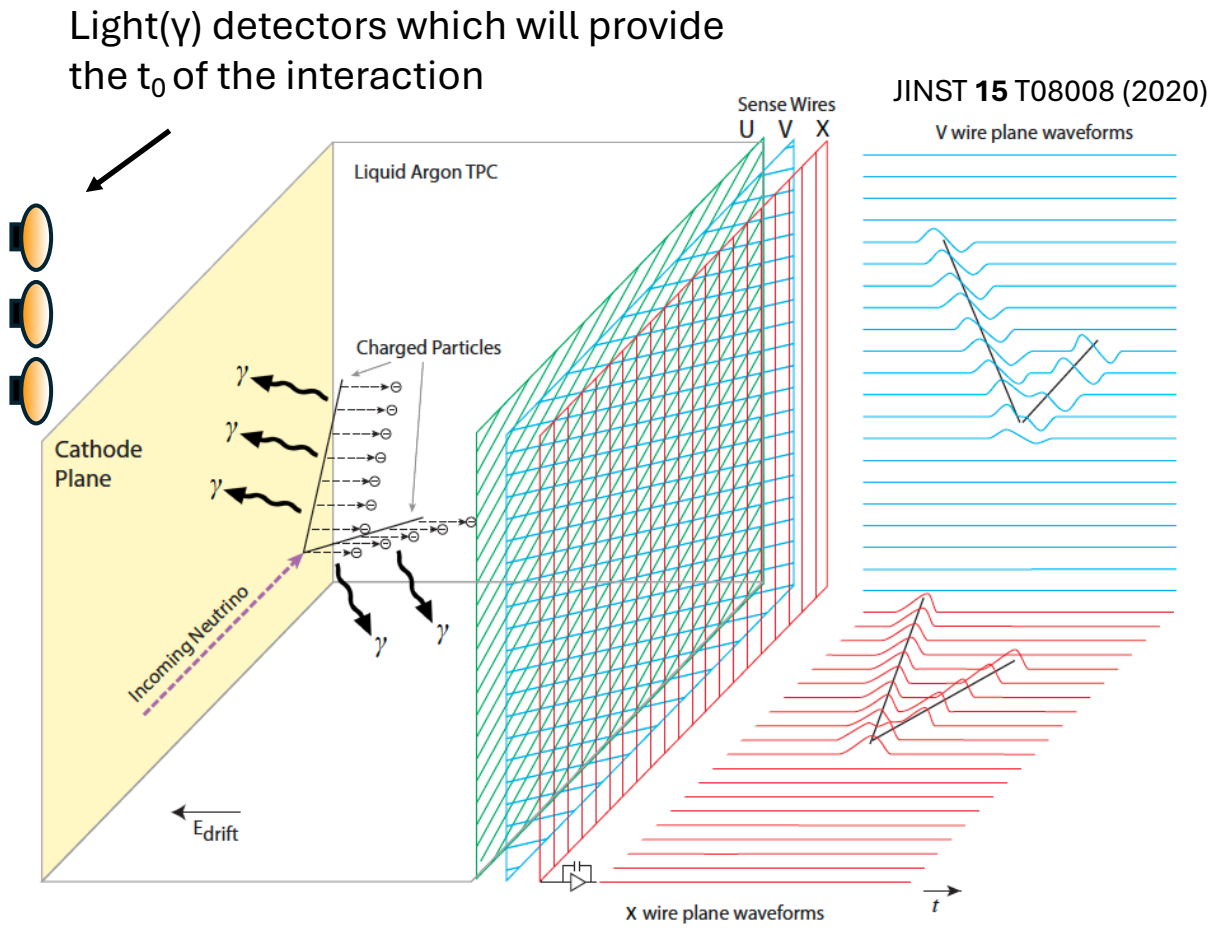
IP2I Lyon[a], France

Iwate University[b], Japan

LAr-TPC for neutrino measurements

- High-res (~ a few mm) 3 dimentional imasing of tracks
- Excellent capabilities on energy loss measuement and PID
- Liquid Ar (LAr) is relatively cheap (good for large-scale detector)

- The frontend equipments, such as frontend readout electronics, are exposed to cryogenic environment
  - Boiling point of LAr: ~87.3 K

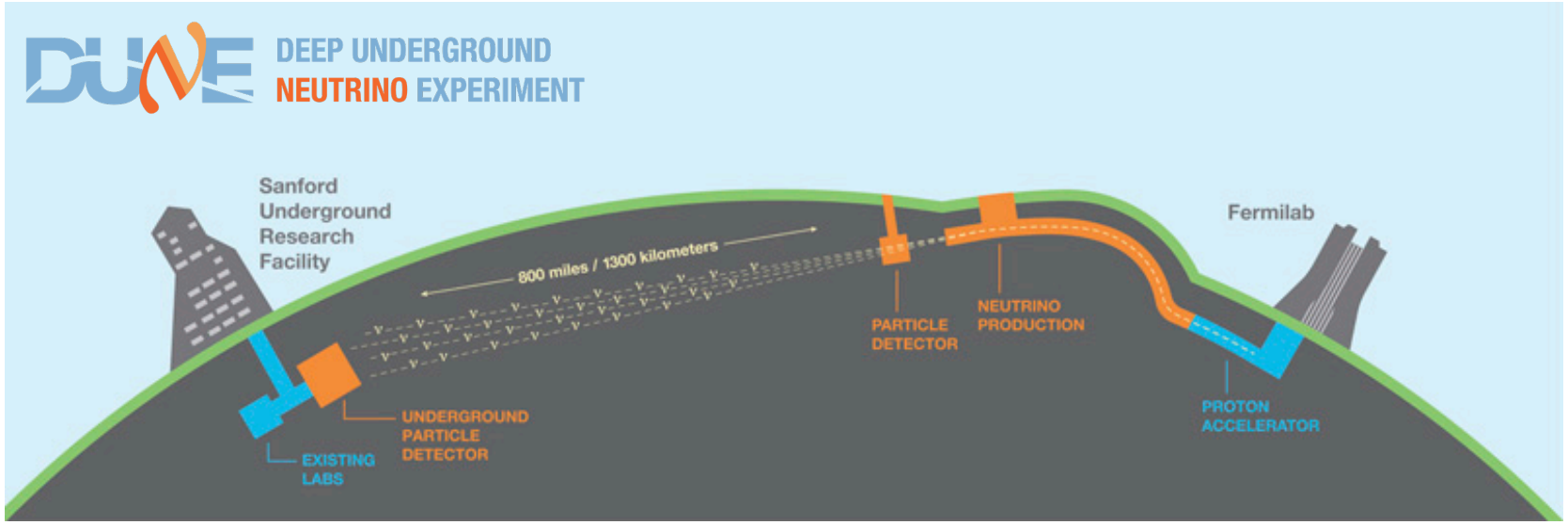


General operating principle of LAr-TPC

Stable operation of readout electronics in cryogenic environments is critical

The Deep Underground Neutrino Experiment (DUNE)

- A next-generation long-baseline neutrino oscillation experiment using the Fermilab accelerator facility and the SURF in USA
- Main physics goals:
  - Measurement of the neutrino mass hierarchy, the amount of CP violation in the leptonic sector
  - Detection of low energy neutrinos such as neutrinos from supernova bursts or the Sun
  - search for nucleon decay and other beyond the standard model phenomena
- Planning to construct ~40 kt scale LAr-TPC for the far detector
- Aiming to start the experiments at around the end of FY2029



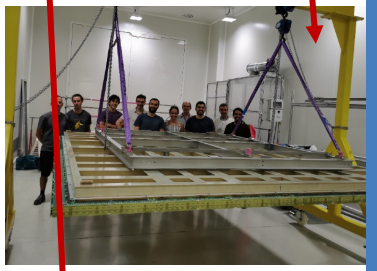
1st DUNE Far Detector Module: Vertical-Drift (**FD-VD**) :

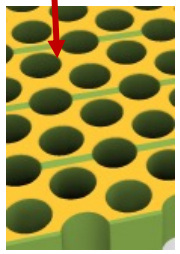
15 kton of active LAr volume

Japanese groups historically involved in the Top-Drift Electronics (TDE) Consortium in collaboration with IN2P3 groups

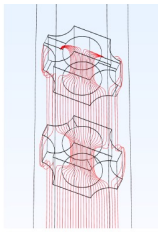
Top and bottom anode charge readout surfaces:

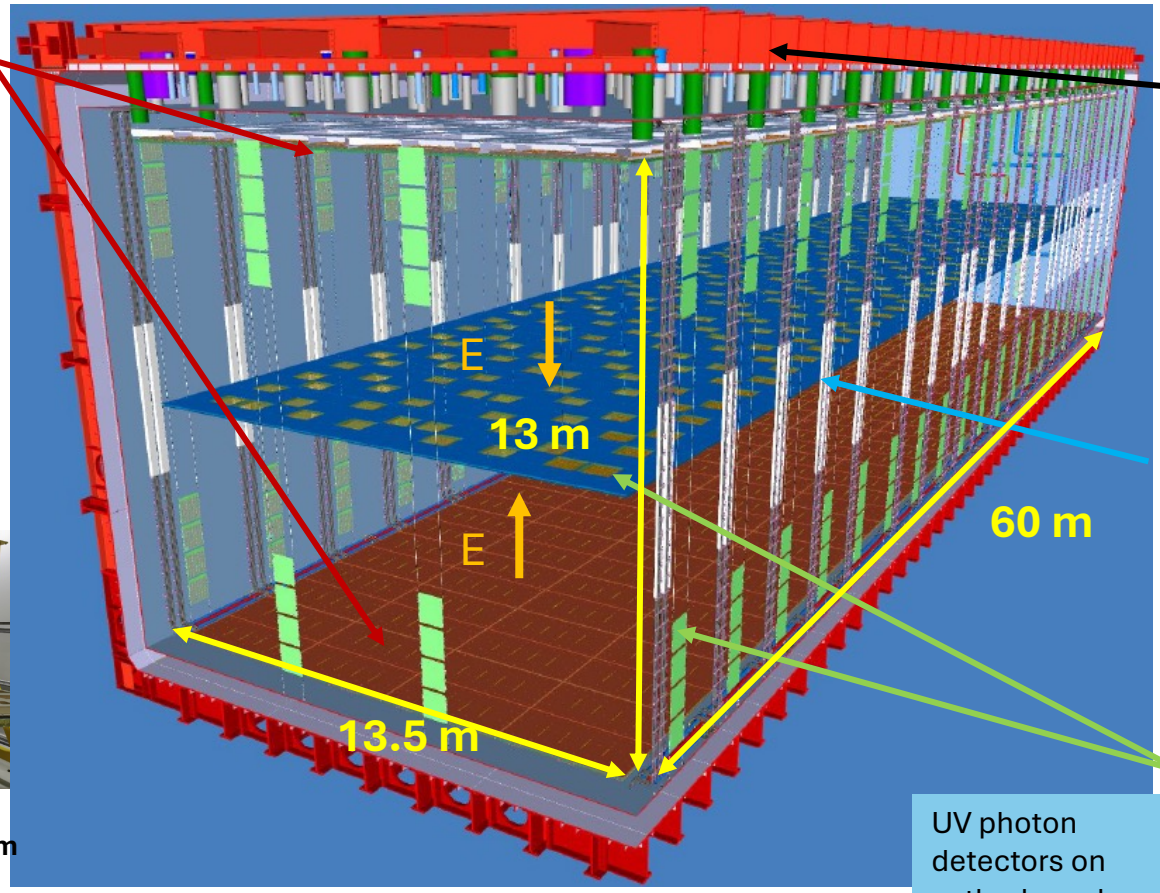
Made of 80+80 Charge Readout Plane units 3x3.375 m^2
Each unit: 2 stacked layers of segmented perforated PCBs



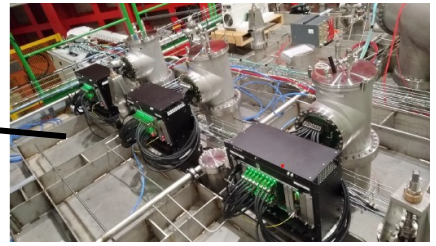


Strips 5 mm
Holes 2.4 mm





UV photon detectors on cathode and cryostat walls

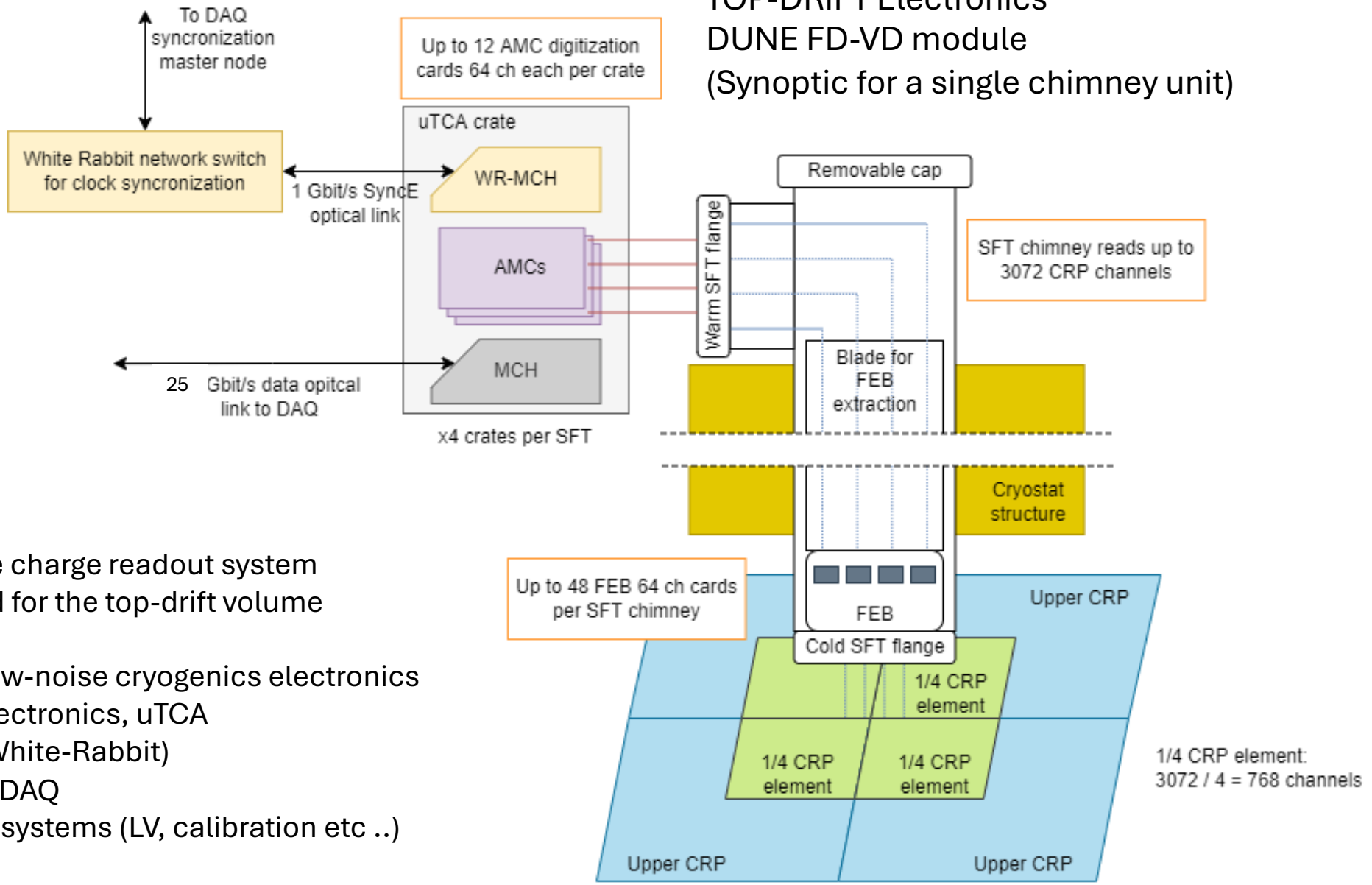


Cryostat roof with TDE Chimneys containing analog cryogenic FEB and μTCA digitization readout

Cathode surface at -300 kV
→ E~500V/cm

1/40 Prototype in CERN cryostat

TOP-DRIFT Electronics
DUNE FD-VD module
(Synoptic for a single chimney unit)



→ Complete charge readout system optimized for the top-drift volume

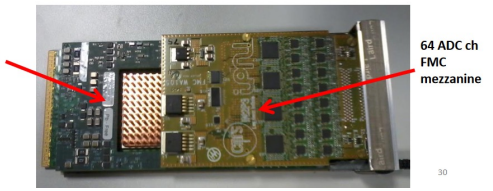
- Analog low-noise cryogenics electronics
- Digital electronics, uTCA
- Timing (White-Rabbit)
- Ethernet DAQ
- Ancillary systems (LV, calibration etc ..)

R&D at IP2I since 2006:

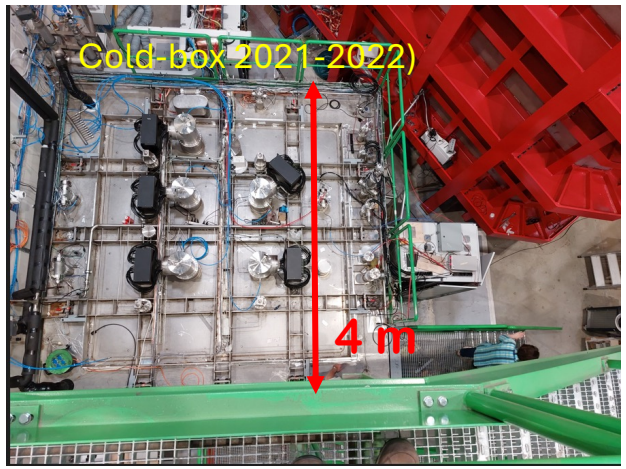
- Cryogenic ASIC amplifiers (first cryo-ASIC in the world in 2007)
- uTCA digitization
- ethernet DAQ
- Timing distribution; White Rabbit

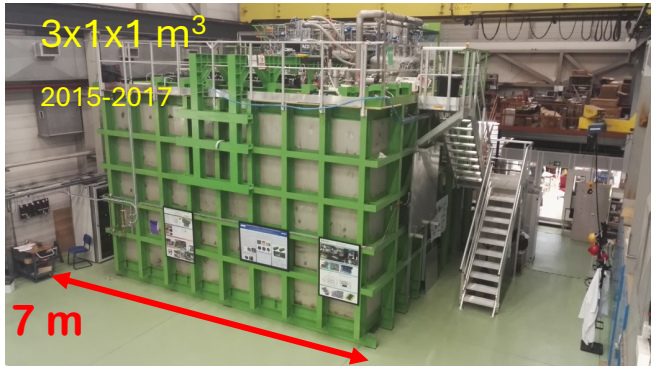
2009 first µTCA system with prototype digitization AMCs

AMC demonstrator 2014



Validation with large-scale applications and prototyping activities at the CERN Neutrino Platform
(EHN1 Hall and Bd 182) 2015-2023





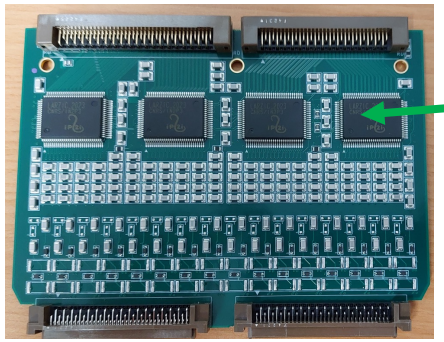
TDE Development activities completed in 2023

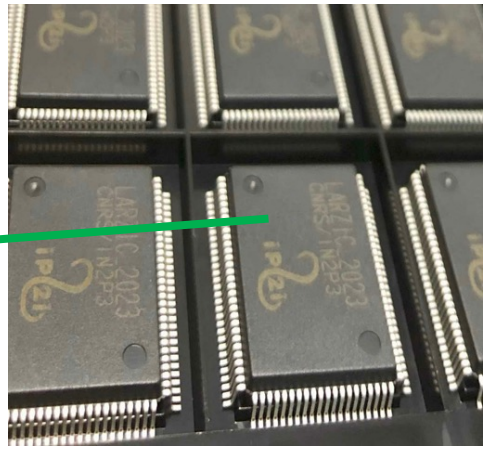
Production for FD-VD in progress since beginning of 2024 (see next slide)

Readout System for the top-drift volume of FD-VD
80 CRP, 3072 channels/CRP, 246k total channels

Nominal number of elements to be installed on FD-VD (production in progress 2024-2026):

- 3840 cryogenic FEB boards (64 channels) with ASIC 16 channels amplifiers





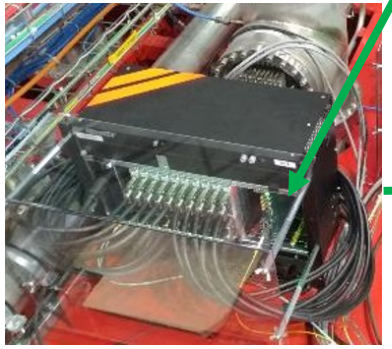
- LARZIC cryogenic ASIC amplifiers 15360 pieces

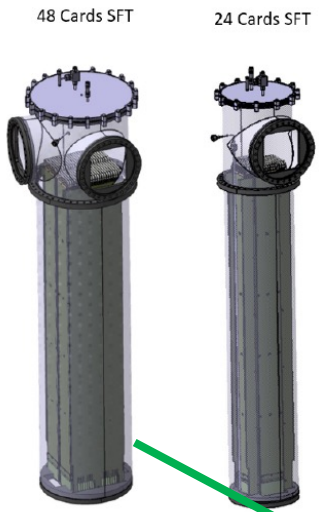
- 3840 AMC Digitization boards (64 channels)

Timing system White-Rabbit

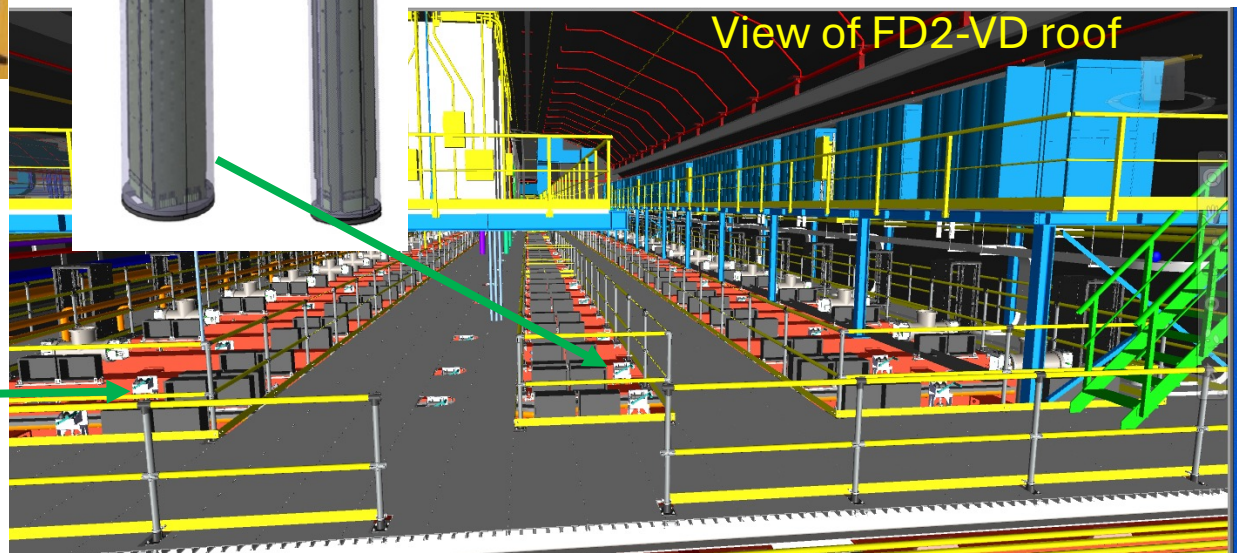
- 320 WR-MCH

- 320 µTCA systems with 25 Gbit/s MCH



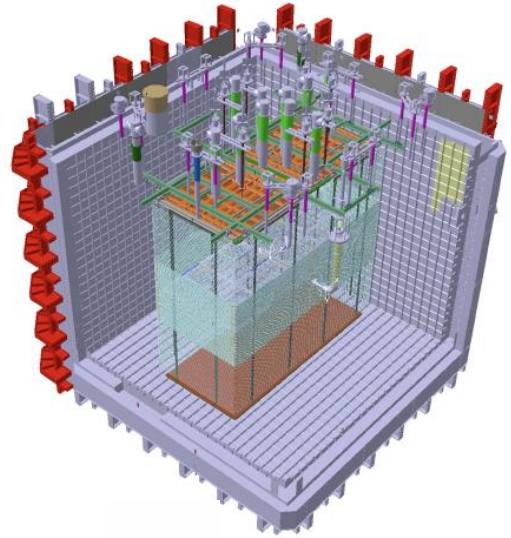


- 105 Chimenys hosting 48 or 24 FEB boards (Mechanics)



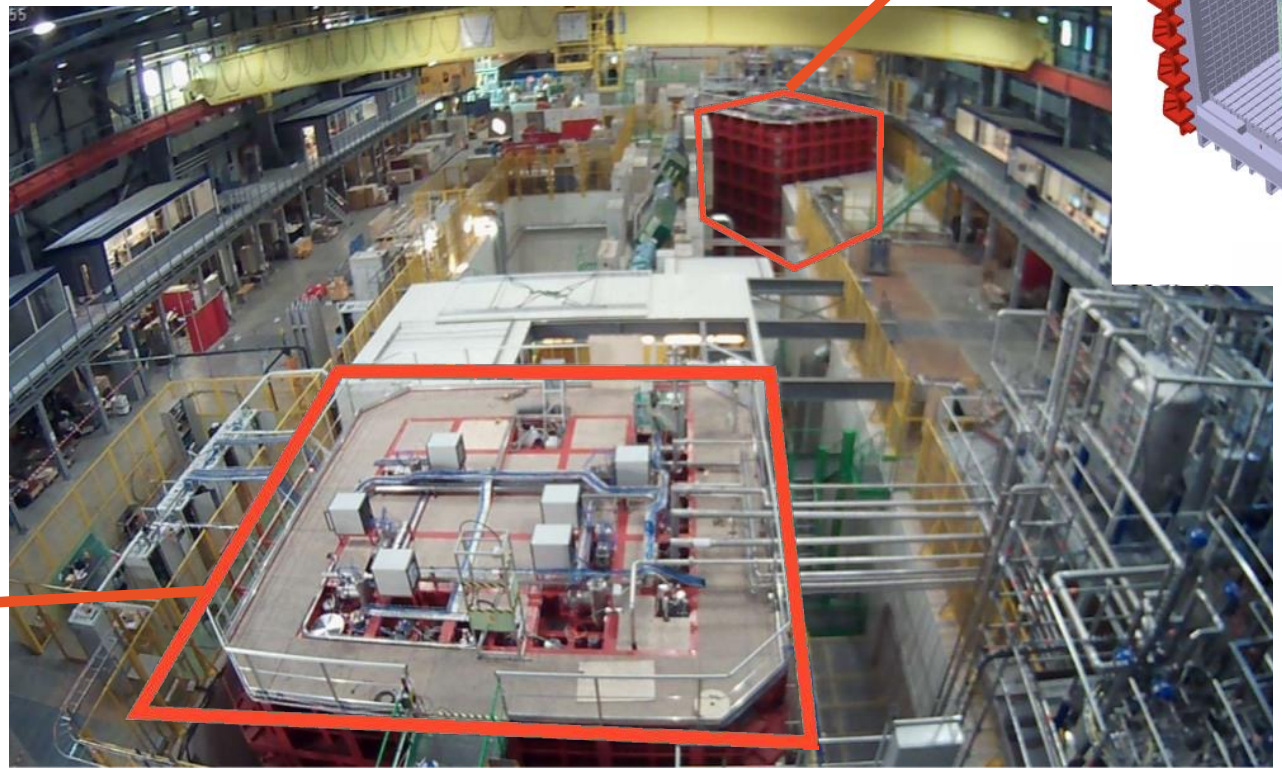
The DUNE prototype experiment (ProtoDUNE)

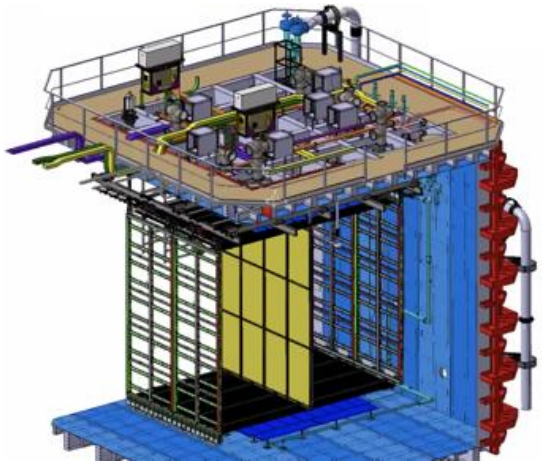
- Prototypes of the DUNE detectors are constracted and tested at the CERN neutrino platform
- Part of full size detectors (1 module)
  - Active volume: ~1 kt



NP02
VD

Figure: CERN Neutrino Platform.





NP04
HD
(Horizontal-Drift)

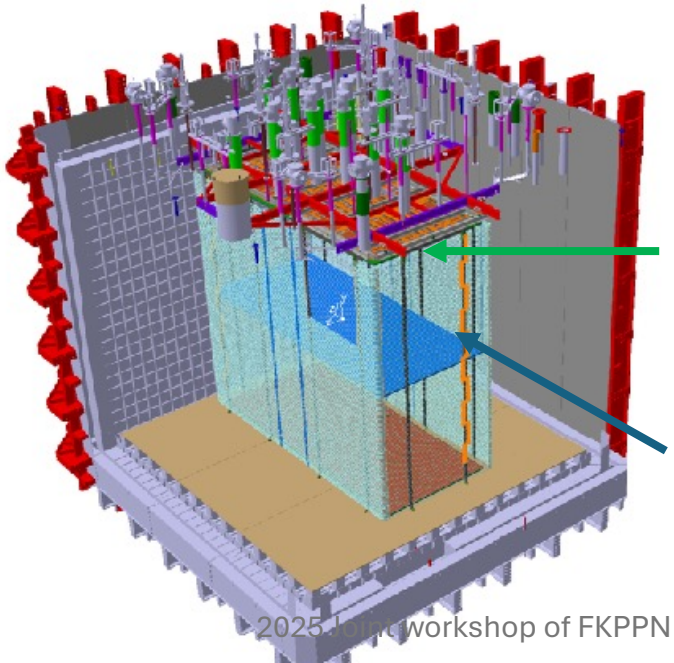
Module-0 VD assembly test in NP02 (2023)

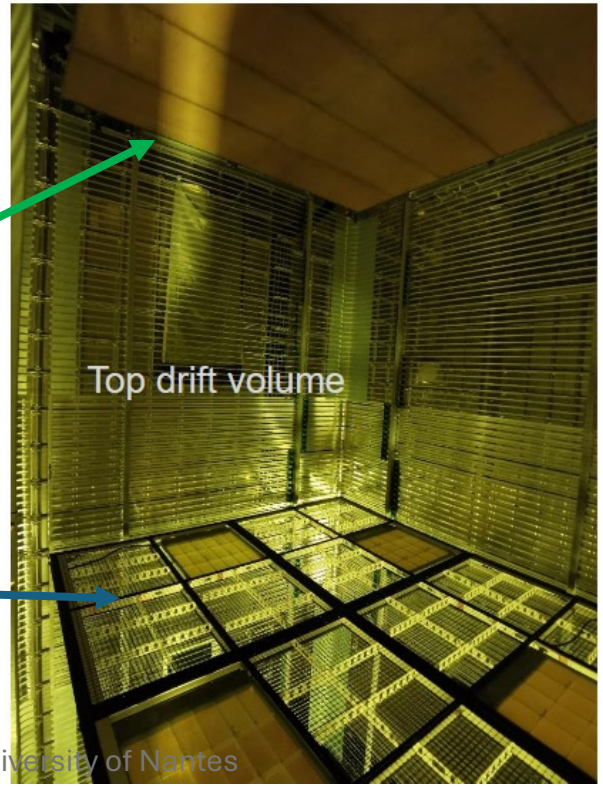
- Two final top-drift CRPs (CRP2 and CRP3) + TDE readout testing completed by October 2022 in Cold-Box

- 6144 readout channels (96 FEB boards and 96 AMC boards)
- Use of existing NP02 10 FEB chimneys → 10 uTCA crates with 10 AMC each
- Very high bandwidth readout system 400 Gbit/s network infrastructure

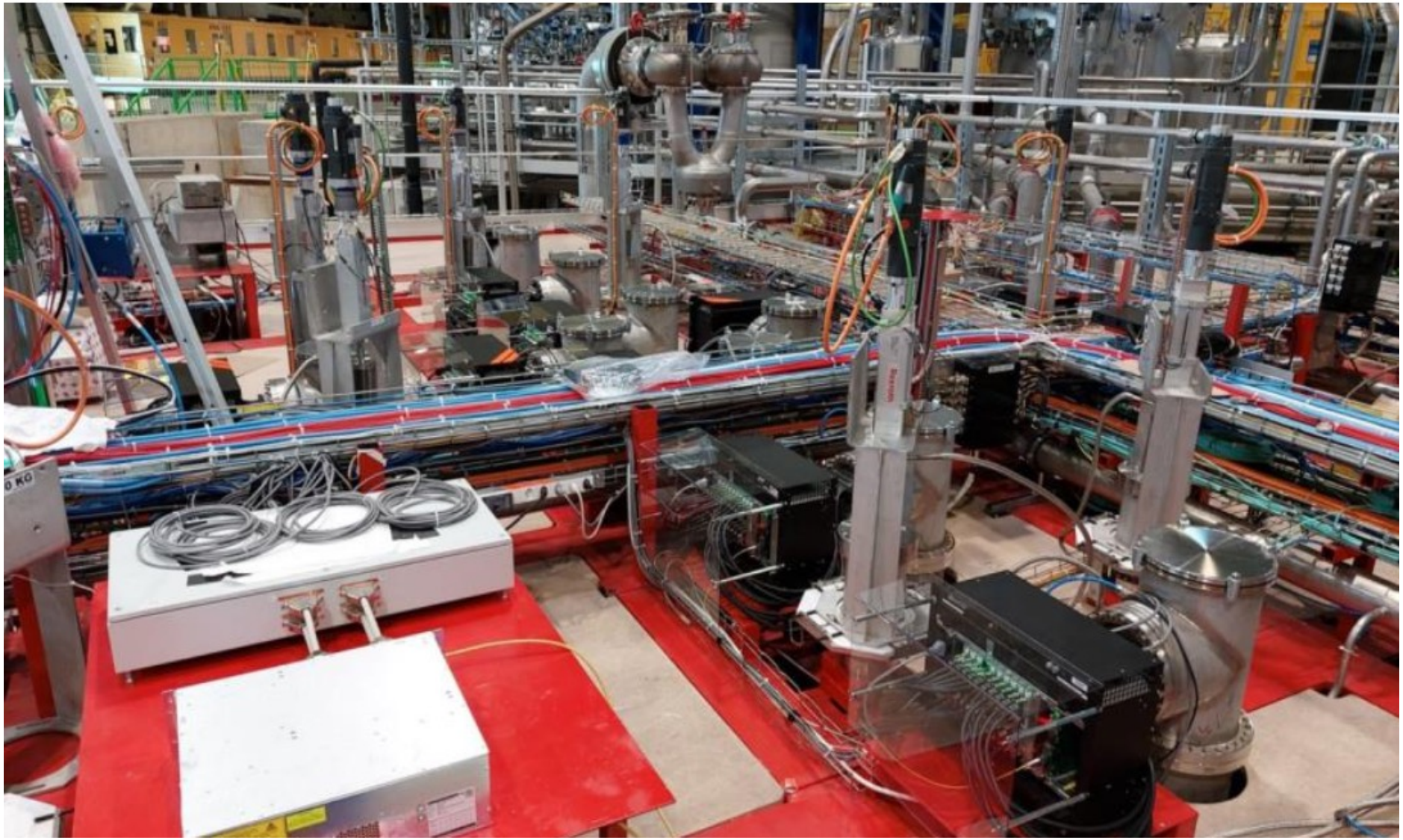
- **Module-0 integration successfully completed in June 2023**

- Detector filled with LAr at the end of 2024 and operational, foreseen detector exploitation with beam in summer 2025





Top Drift Charge Readout Electronics operating on the roof of NP02 ProtoDUNE Vertical-Drift at CERN after detector integration exercise completion (June 2023)



ProtoDUNE Vertical Drift will have the chance since summer 2025 of a long running period including also of a beam exposure of several weeks
→ unique opportunity, over an extended time period, to:

1) learn and improve the operation procedures of the first DUNE Far Detector module
2) have dedicated data in controlled conditions of injected particle types and momenta, useful to refine the reconstruction algorithms.
3) completing the developments of all the tools and the software interfaces to operate the detector and fully exploit its data and to validate their effectiveness and reliability.

This TYL-FJPPN project includes commissioning and development tasks, in particular on the TDE signal readout electronics for ProtoDUNE Vertical Drift and the associated DAQ system

- NP02 offers the possibility of to complete software developments to operate and control the TDE/DAQ and to process the readout data and to validate all integration and operation procedures → **complete the preparation for FD-VD installation and commissioning**

- Great opportunity to **improve the reconstruction and physics exploitation of the data** in view of effectively preparing for the operation of the Vertical Drift Far Detector since 2028.

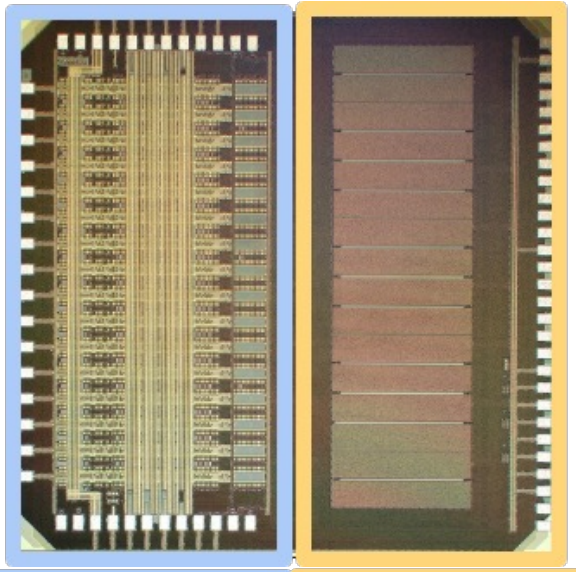
Low Temperature Analog Readout System (LTARS)

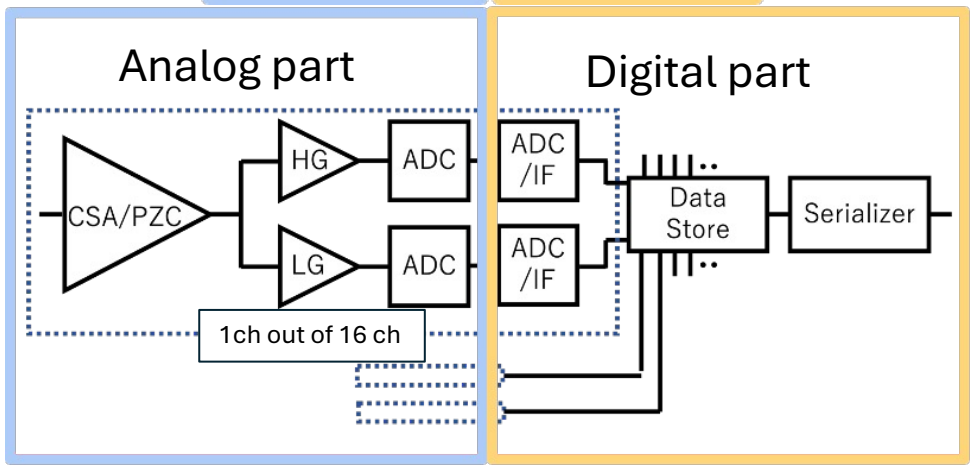
- A project of new signal readout cryo-ASIC is in progress
- The R&D has been led by Iwate-KEK group
  - The latest ASIC has amplifier and ADC on-a-chip

Current targeted design specifications

Parameter	High Gain (HG)	Low Gain (LG)
Peaking Time	1 us, 4us	
Conversion Gain	10 mV/fC	0.5 mV/fC
Dynamic Range	±80 fC	±1600 fC
ENC	<3000 e^-	<62500 e^-

The latest LTARS ASIC (LTARS16A)

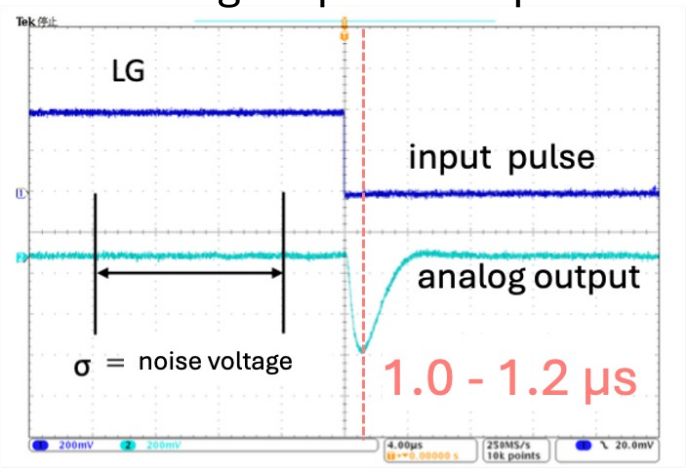




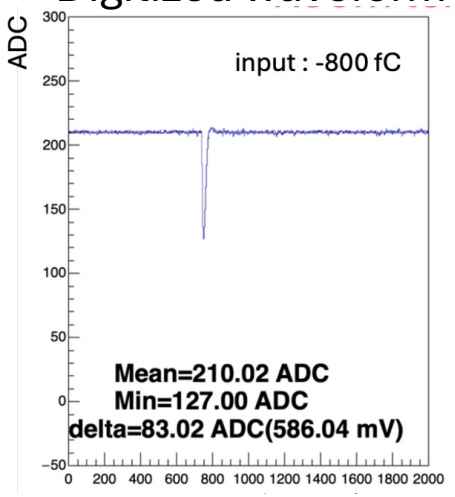
Operating characteristics at room temperature

- Operating characteristics are evaluated for the low gain(LG) with test pulse

Analog amplifier output

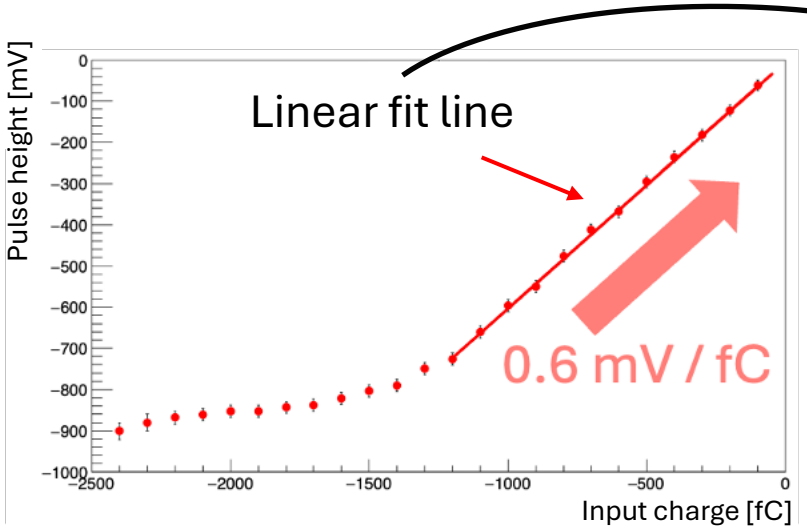


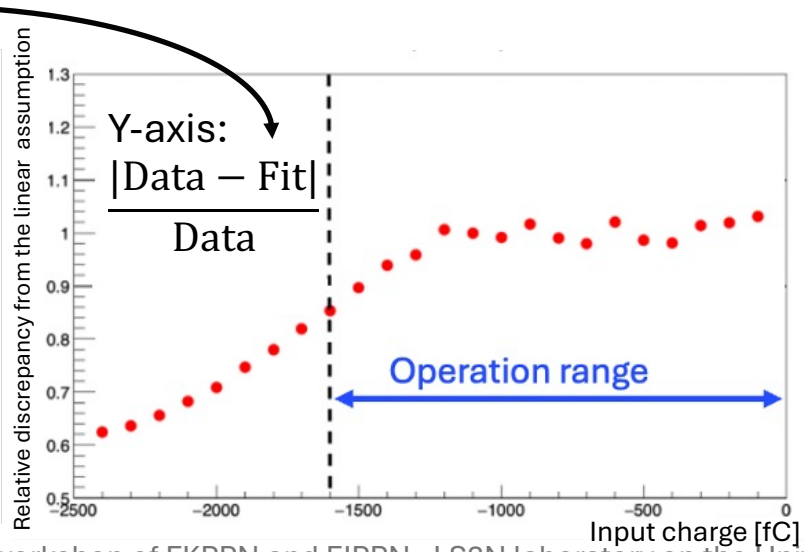
Digitized waveform

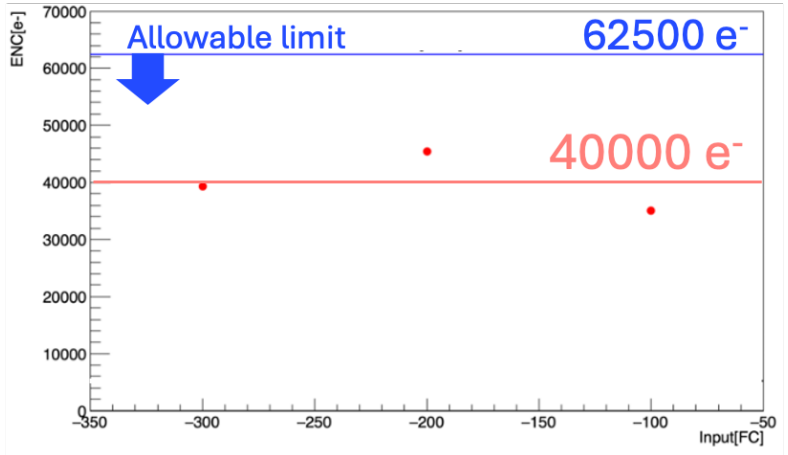


- ✓ Shaping time: ~1.0-1.2 μs
- ✓ Conversion gain: ~0.6 mV/fC
- ✓ Dynamic range: ~ -1600 fC
- ✓ Equivalent noise charge(ENC): ~40000 e⁻

Satisfies the LG specifications

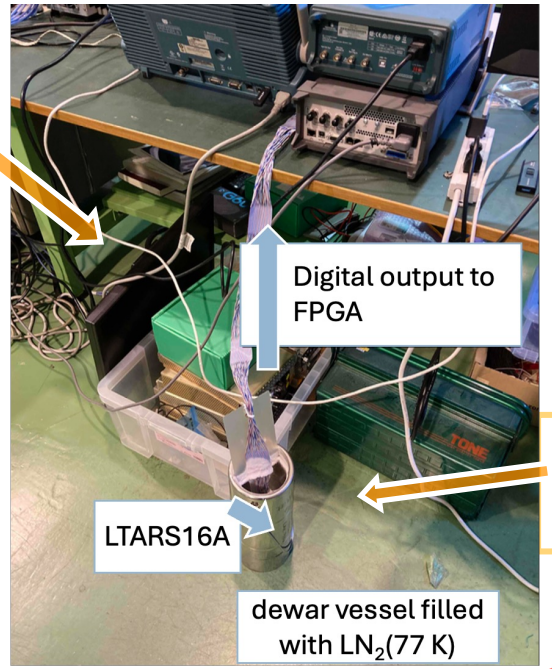






Cryogenic test with liquid nitrogen

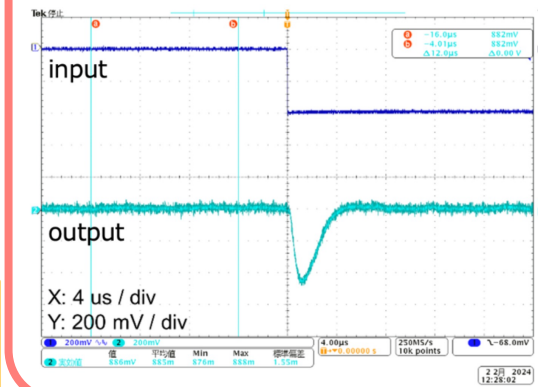
Input test pulse to the LTARS16A



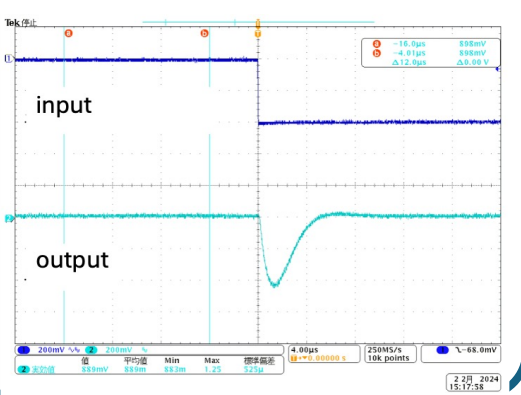
Immersed ASIC board in a dewar vessel

Analog signal waveform (LG)

Room temperature

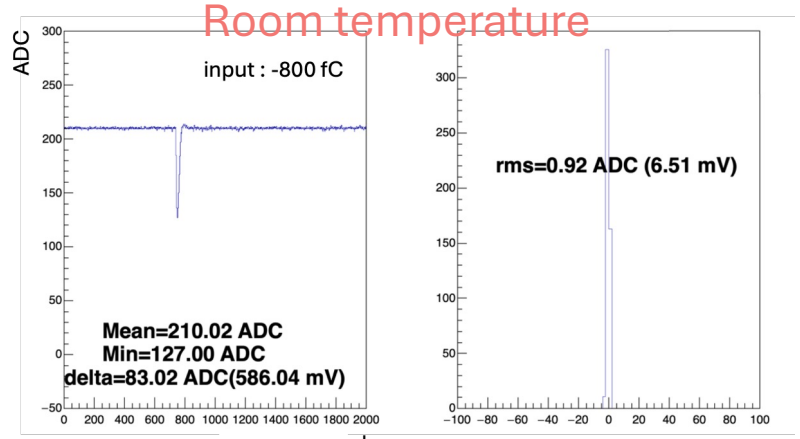


LN_2 temperature

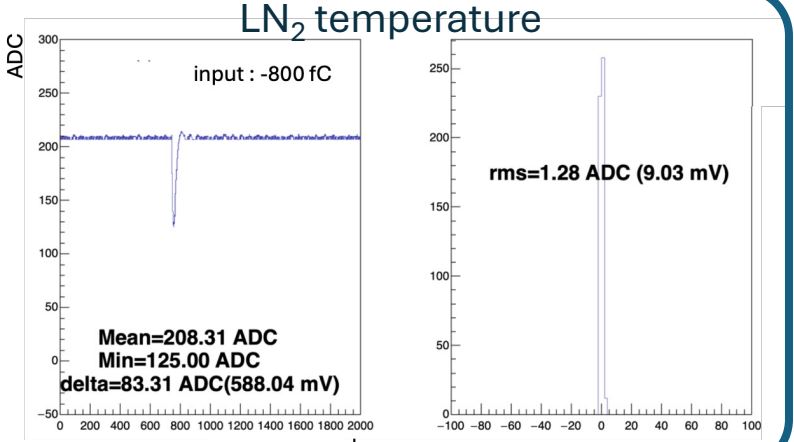


Digital signal waveform (LG)

Room temperature



LN_2 temperature

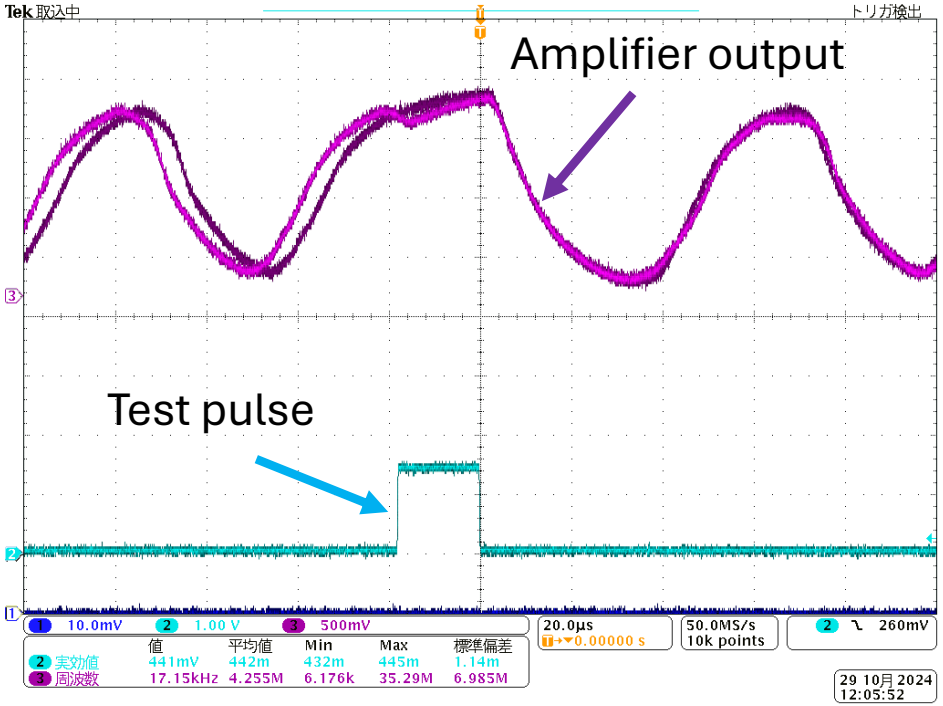


LTARS is successfully operated even in the cryogenic (77 K) environment and the LG signal shows almost same response as in the room temperature

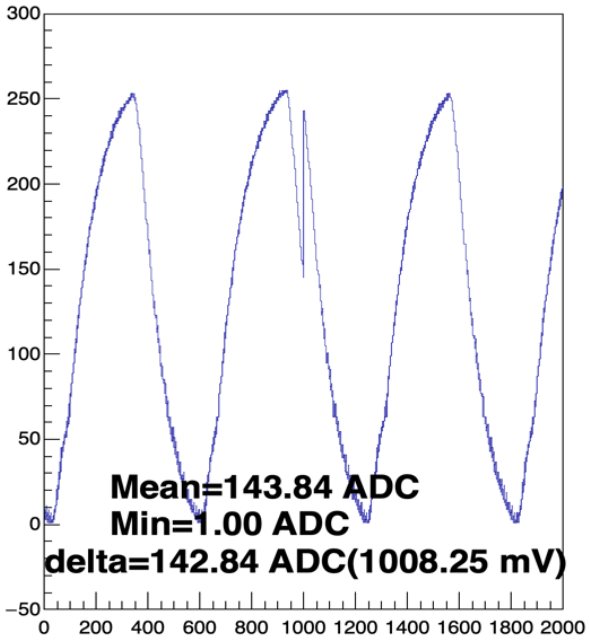
Current issue and prospects

✓ Output of high gain shaper amplifier shows oscillation

Analog amplifier waveform (HG)



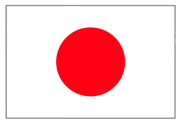
Digitized waveform



- Investigate on the problems on the current design and produce a new ASIC implementing countermeasure(s) to the oscillation problem
- Aim to design a more optimized ASIC for neutrino measurements based on experience with electronics operation and analysis of measured data at ProtoDUNE with technical exchanges among Japanese and French groups

Overview of the project in this proposal

- Technical exchange on the cryogenic electronics



IP2I Lyon group ⟷ Iwate-KEK group

- Technical supports on the TDE
- Human resouces

- Human resources

- Lead the R&D

ProtoDUNE-VD/DUNE project

Feedback from the TDE →

← Application to future upgrade?

LTARS project

Application to future experiments →

- Commisioning and operation of the TDEs
- Detector operation and data taking
- Calibration and data analysis for physical measurements

- R&D of the ASIC
- Integration tests with a LAr-TPC

New proposal: “Commissioning and further development of cryogenic readout electronics for LAr-TPC applications”

FJPPL (TYL) application 2025

Fiscal year April 1st 2025 – March 31th 2026

Please replace the red examples by the appropriate data in black

ID[1]:	Title: Commissioning and further development of cryogenic readout electronics for LAr-TPC applications					
	French Group			**Japanese Group**		
	name (Family name, First name)	**title**	**lab.[2]**	**name** (Family name, First name)	**title**	**lab.[2]**
PIs:	Autiero Dario E-mail: autiero@cern.ch	Dr.	IP2I Lyon	HOSOKAWA, Ritsuya E-mail: ritsuya@iwate-u.ac.jp	Dr.	Iwate Univ.
Members:	Slavic Galymov	Dr.	IP2I Lyon	NARITA, Shinya	Dr.	Iwate Univ.
	Edouard Bechetoille	Mr.	IP2I Lyon	SAKASHITA, Ken	Dr.	KEK
	Hervé Mathez	Mr.	IP2I Lyon	HAMADA, Eitaro	Mr.	KEK
				MORITA, Ayumi	Ms.	Iwate Univ.

Funding Request from France

Description	€/unit	nb of units	total (€)	requested to[3]
Visit to Japan	200/day	7 days	1400	IN2P3
Travel	1500	1 travel	1500	IN2P3
Total			2900	

Funding Request from Japan

Description	k¥/Unit	nb of units	total (k¥)	requested to[3]
Visit to France	20/day	30 days	600	KEK
Travel	300	2 travels	600	KEK
Total			1200	

Additional Funding from France			Additional Funding from Japan		
provided by/requested to[4]	**Type**	**€**	**provided by/requested to[4]**	**Type**	**k¥**
			Iwate Univ., will be provided by	Travel and consumable	1000
Total			Total		1000

Joint topics among the French and Japanese groups :

- Finalization of integration aspects of the TDE front-end electronics in the general DUNE DAQ system
- Development of tools and interfaces to monitor and steer the operation of the TDE front-end electronics and the associated DAQ processes
- Development and testing of the online DAQ triggering algorithms for the DUNE FD operation
- Developments and testing associated to the offline interfaces for the exploitation of the data
- QA/QC and data analysis of the data samples acquired under different running conditions (HV tests, purity, doping, coherent noise improvements etc..) and related to dedicated development tests
- Implementation and exploitation of dedicated calibration runs with the charge injection system or other means
- Physics exploitation of the cosmic and beam data sets and improvements of reconstruction algorithms
- Discussion and technical exchanges on a new cryogenic electronics R&D

- Japanese groups interested in contributing to these experimental activities on site at CERN and in part at IP2I Lyon by having travel exchanges involving young researchers for periods of several weeks travel time, 2-3 times per year.
- A new cryogenic electronics R&D will be conducted with technical exchanges between French and Japanese group by having travel exchanges involving IP2I Lyon stuffs for periods of a week, 1 time per year.

- Additional work can be performed remotely given the network access to the facility and the collaborative tools available.

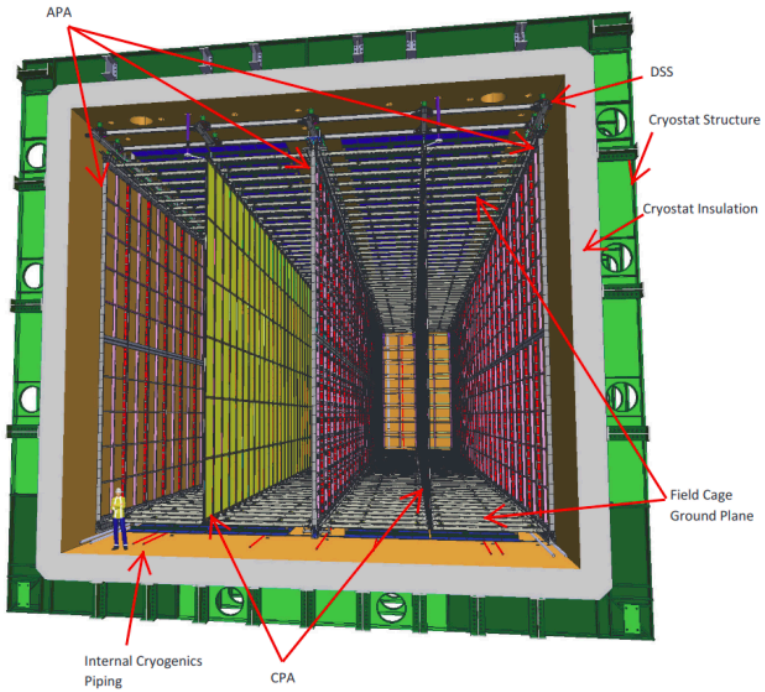
Thank you for your consideration!

Backup

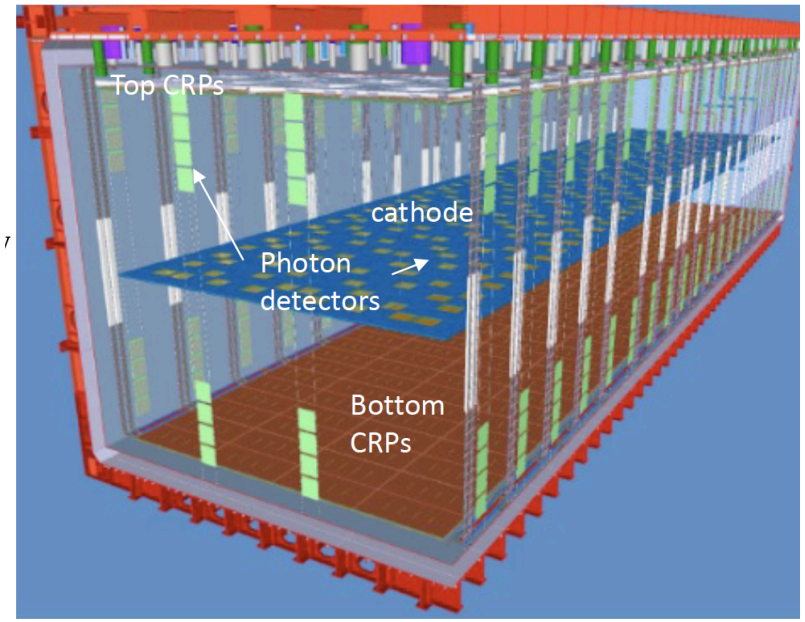
The DUNE Far Detector

➢ There are two detector concepts; DUNE FD1 and FD2

- FD1
  - Holizontal Drift (HD)
    - ✓ ~3.5 m drift length (drift voltage of 180 kV),
  - Active volume: ~13.66 kt
    - ✓ 4 drift volumes
  - Charge readout: 3 layers wire planes



- FD2
  - Virtical Drift (VD)
    - ✓ ~6.5 m drift length (drift voltage of 300 kV),
  - Active volume: ~14.19 kt
  - Charge readout: Charge Readout Plane (CRP) consists of perforated PCB, reducing overall costs to FD1



Requirements on the TDE

Label	Description	Specification (Goal)	Rationale	Validation
DP-FD-2	System noise	$< 1000\ e^-$	Studies suggest that a minimum of 5:1 S/N on individual strip measurements allows for sufficient reconstruction performance.	ProtoDUNE and simulation
DP-FD-4	Time resolution	$< 1\,\mu s$ ($< 100\,ns$)	Enables 1 mm position resolution for 10 MeV SNB candidate events for instantaneous rate $< 1\,m^{-3}ms^{-1}$.	
DP-FD-13	Front-end peaking time	$1\,\mu s$ ($1\,\mu s$ achieved in current design)	Vertex resolution; 1 us matches 3mm pitch and DP S/N ratio.	ProtoDUNE and simulation
DP-FD-14	Signal saturation level	7,500,000 electrons	Maintain calorimetric performance for multi-proton final state; takes into account an effective CRP gain of 20 in the DP signal dynamics.	Simulation
DP-FD-19	ADC sampling frequency	$\sim 2.5\,MHz$	Match $1\,\mu s$ shaping time.	Nyquist requirement and design choice
DP-FD-20	Number of ADC bits	12 bits	ADC noise contribution negligible (low end); match signal saturation specification (high end).	Engineering calculation and design choice
DP-FD-21	TPC analog cold FE electronics power consumption	$< 50\,mW/channel$	No bubbles in LAr to reduce HV discharge risk.	Bench test

Vertical Drift:

Noise< 1000 e-
Peaking time 1 us
Dynamics 500k e-
12 bit ADC
2 MHz sampling
< 50 mW/ch