BASHI :

Bootstraping mAps development in a Shared Investigation

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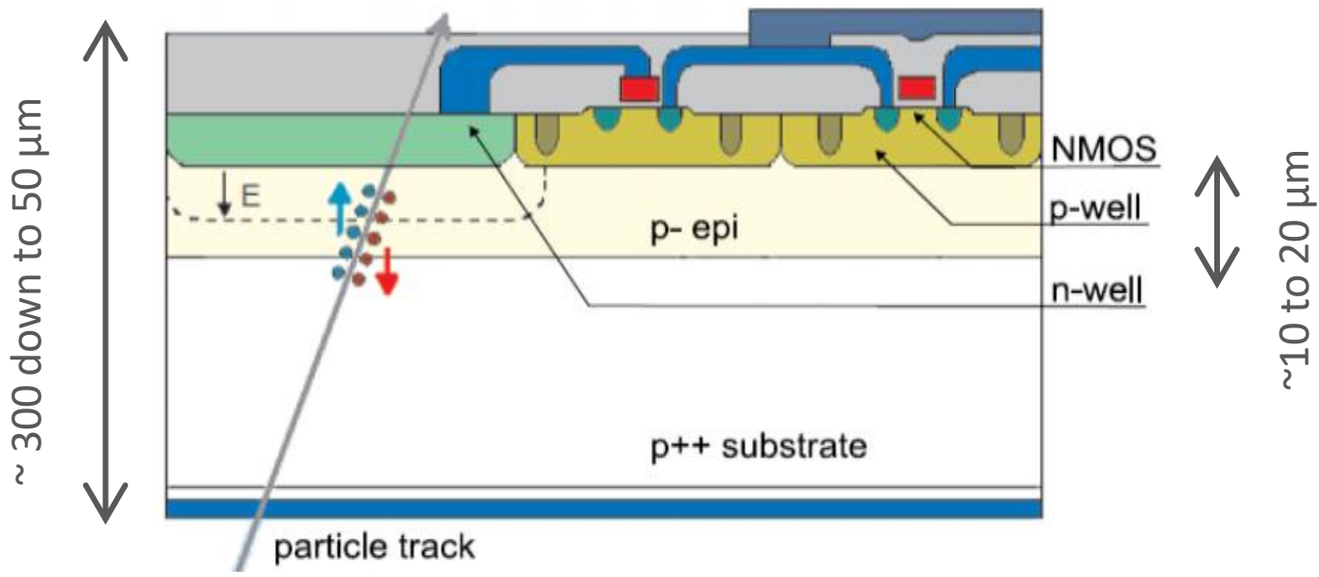
2025 Joint Workshop of FKPPN and TYL/FJPPN

BASHI project

- BASHI : Bootstraping mAps development in a Shared Investigation
  - A collaboration between two detector development centers, ITDC at KEK and C4Pi at IPHC, other groups to match the challenges of the development of CMOS monolithic active pixel sensors (MAPS) in the mid and long term.

- Goals
  - Development of OBELIX sensor (TowerJazz 180 nm) for Belle II vertex upgrade VTX
  - R&D in the development of intrinsic amplification by impact in the silicon for the monolithic technology
  - R&D on the new generation MAPS (TPSCo 65 nm) for ALICE ITS3 and future applications



Project institutes and members

- Tomoto Makoto
- Hanagaki Kazunori
- Enari Yuji
- Okazaki Yuta
- Togawa Manabu
- Nakamura Koji

KEK - ITDC

KEK - ATLAS

KEK - Belle II

- Nakamura Katsuro
- Chujo Tatsuya
- Inaba Motoy
- Gunji Taku

U.Tsukuba - ALICE

U.Tokyo - ALICE

- Yamaguchi Yorito

U.Hiroshima - ALICE

IPHC

- Baudot Jerome
- Besson Auguste
- Shamas Hasan
- Hu-Guo Christine
- El Biter Ziad
- Morel Frederic
- Senyukov Sergey
- Maire Antonin

LPSC

- Guernane Rachid

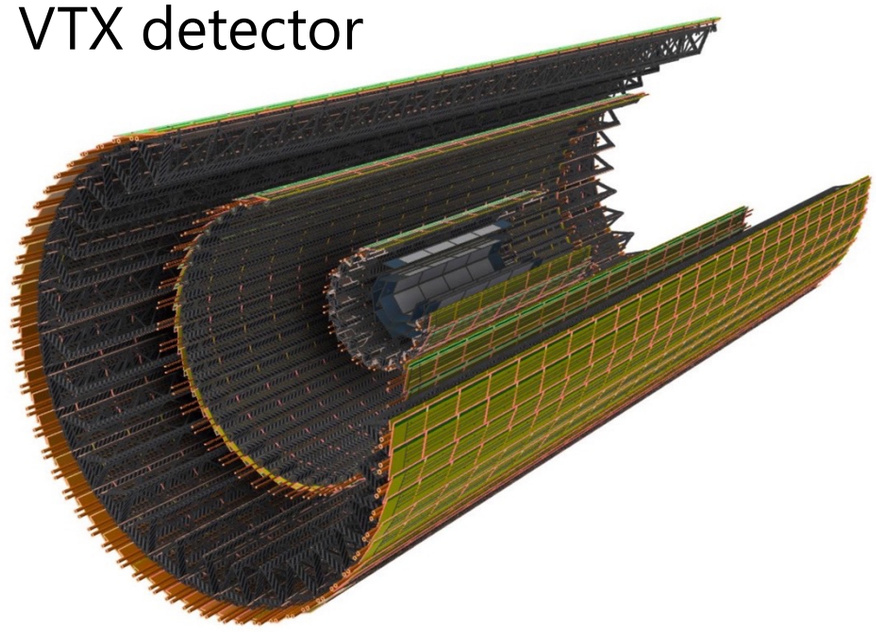
Belle II vertex detector upgrade

- New vertex detector VTX :
  Fully pixelated 5-layer detector
  using CMOS MAPS
  - Higher space-time granularity
  - Small material budget : ~ 2.4% X_0

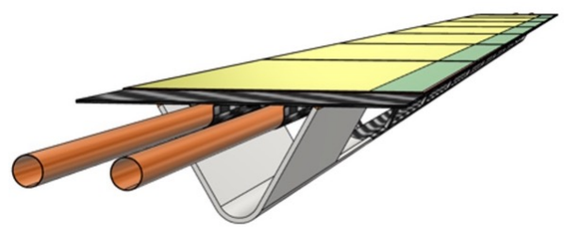
- Thin MAPS sensor :
  Optimized BELIe II pIXel chip (OBELIX)
  - New CMOS MAPS for Belle II vertex upgrade
  - Tower Jazz 180 nm

- OBELIX matrix is based on TJ-Monopix2 for HL-LHC ATLAS
  - Implementing new digital periphery and trigger logic for Belle II
  - Detailed performance characterization of TJ-Monopix2 is crucial for OBELIX design

VTX detector

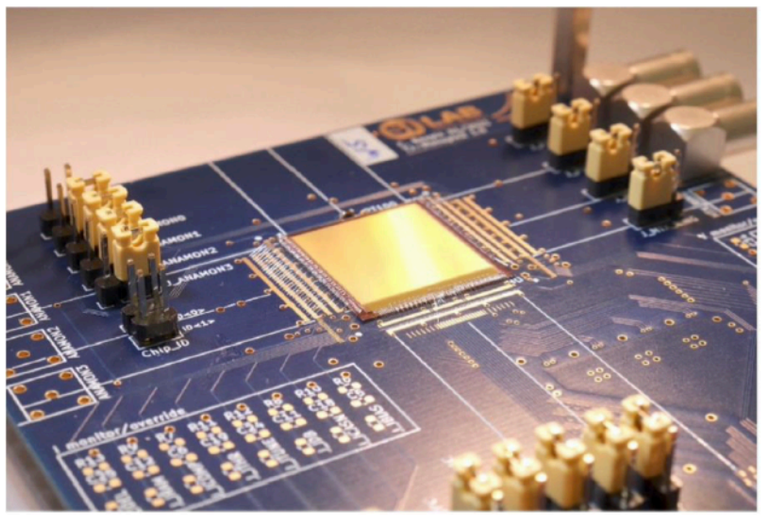


- Inner layer : L1/L2
  - Air cooling
- Outer layer : L3/L4/L5
  - Carbon fiber support
  - Water cooling



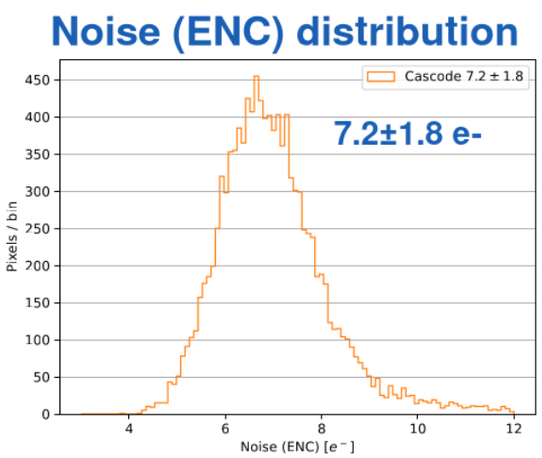
TJ-Monopix2 performance characterization

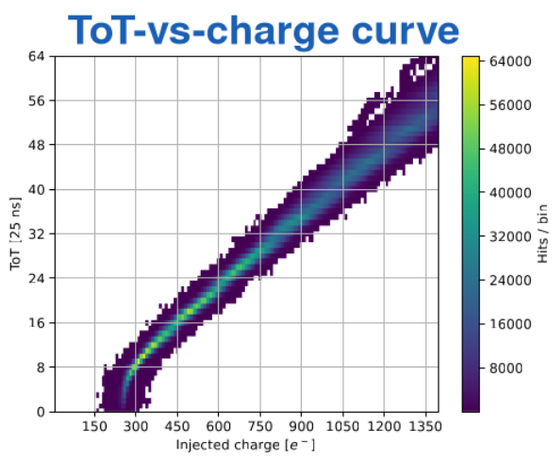
TJ-Monopix2

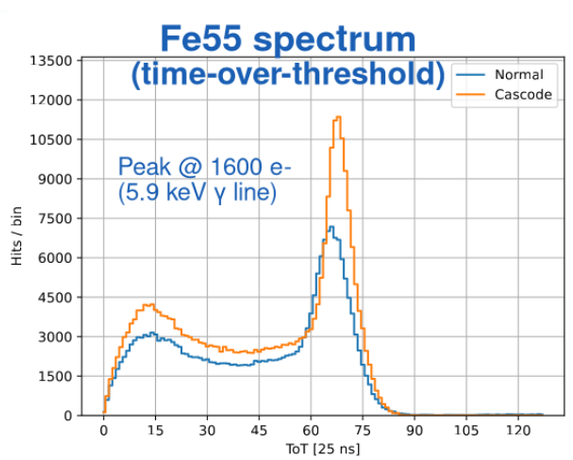


- Chip size : 2 cm × 2 cm
- Pixel pitch : 33 μm × 33 μm
- 512 × 512 ch
- ~ 1 μW/pixel (90 mW/cm^2)
- 25 ns time stamping

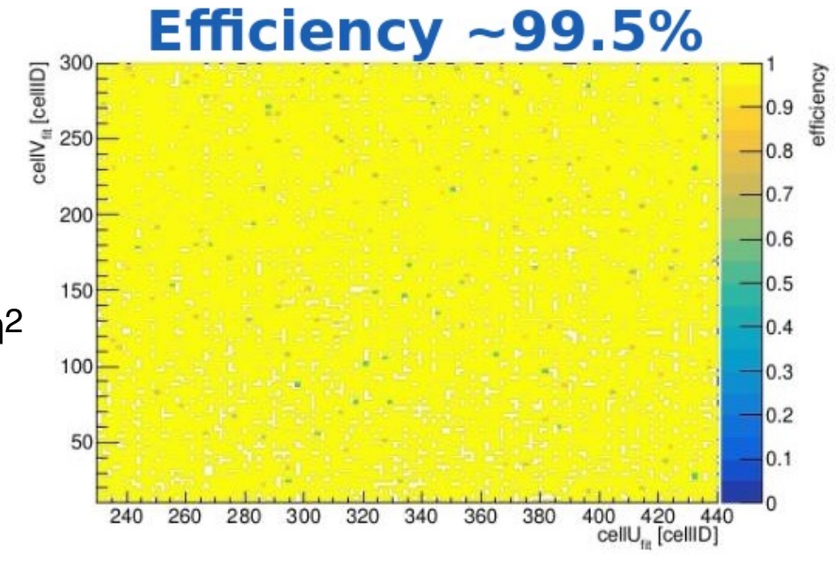
Lab-testbench measurements

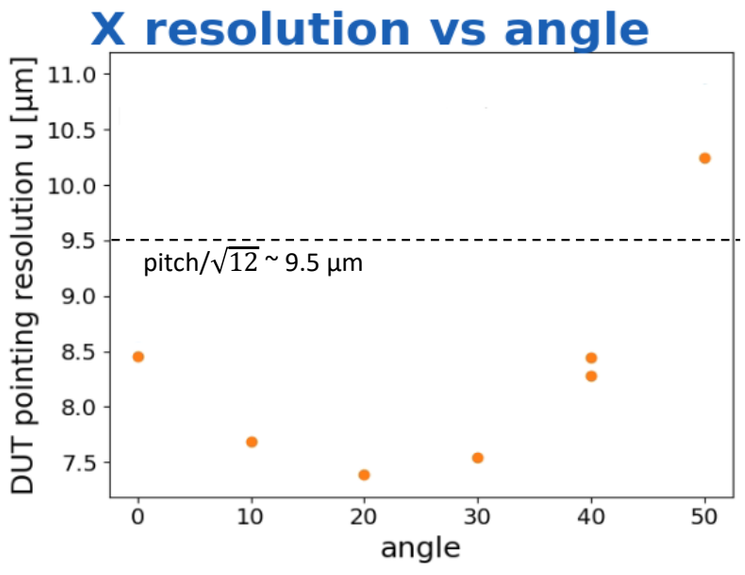






DESY electron beam measurements





Including irradiated samples

- High efficiency even w/ 5×10^{14} n_{eq}/cm^2

KEK PF-AR testbeam line

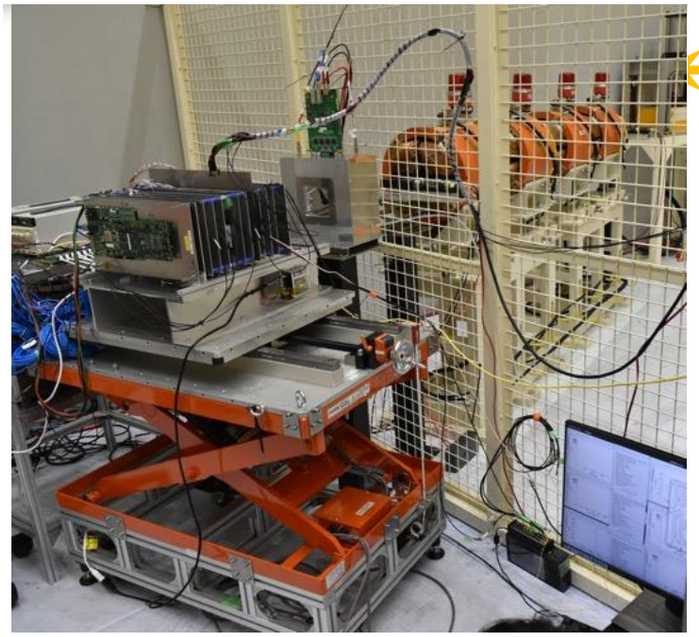
3 GeV electron beam with SOI telescope

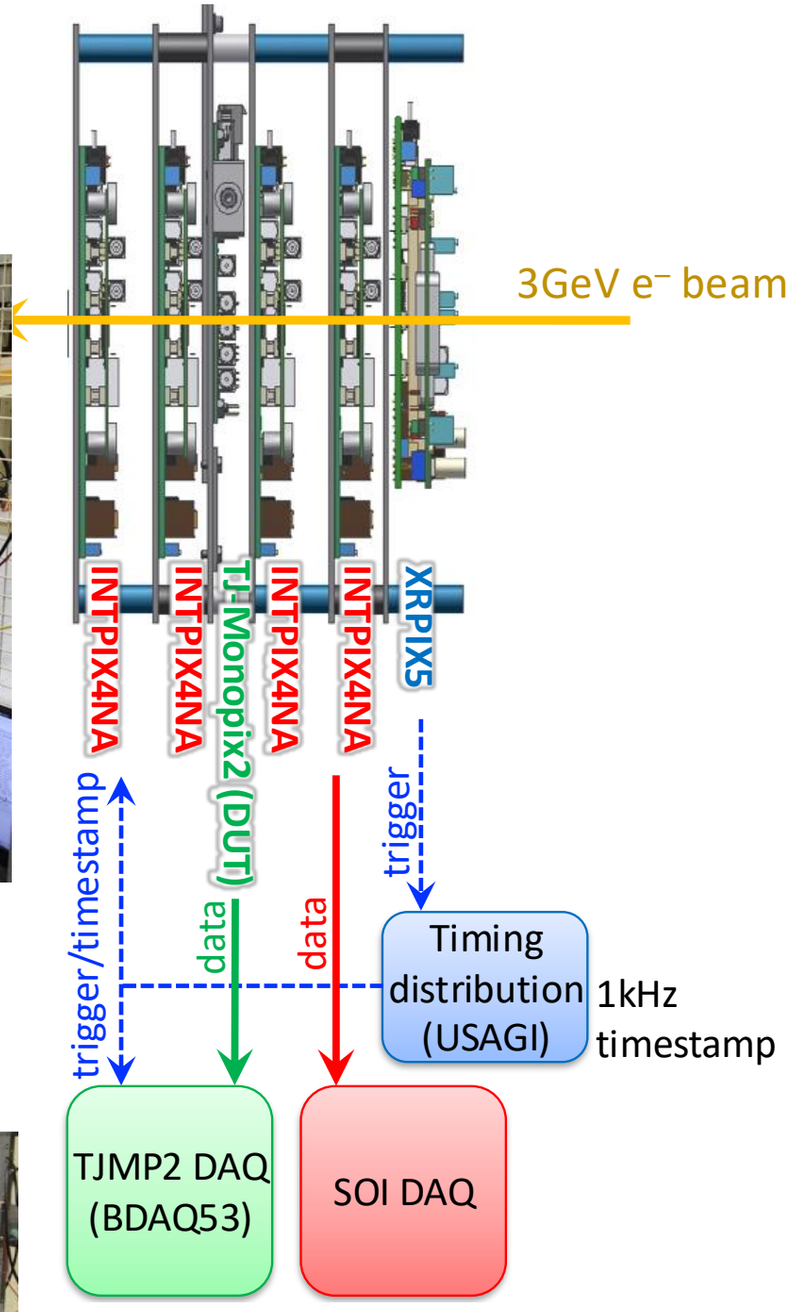
SOI telescope

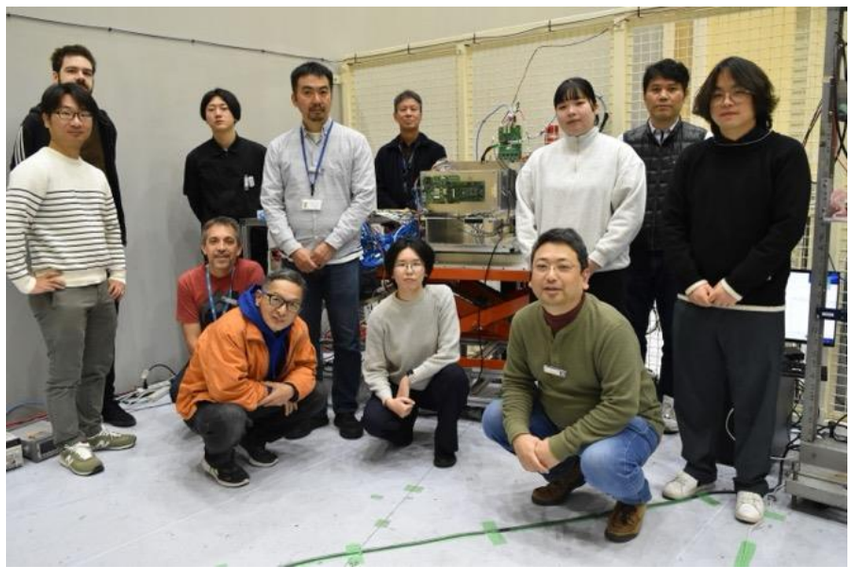
- 4 INTPIX4NA sensors : for tracking
  - Pixel pitch: 17 μm x 17 μm
  - ~300 μm thickness
  - ADC from all pixels are recorded
  - Select RoI to reduce the data size

- XRPIX5 sensor: for trigger
  - Pixel pitch: 36 μm x 36 μm
  - Trigger latency: a few 10 μm at most
  - No data stored in DAQ

- Reconstructed track rate on TJ-Monopix2:
  - roughly about 70-80 Hz/cm^2



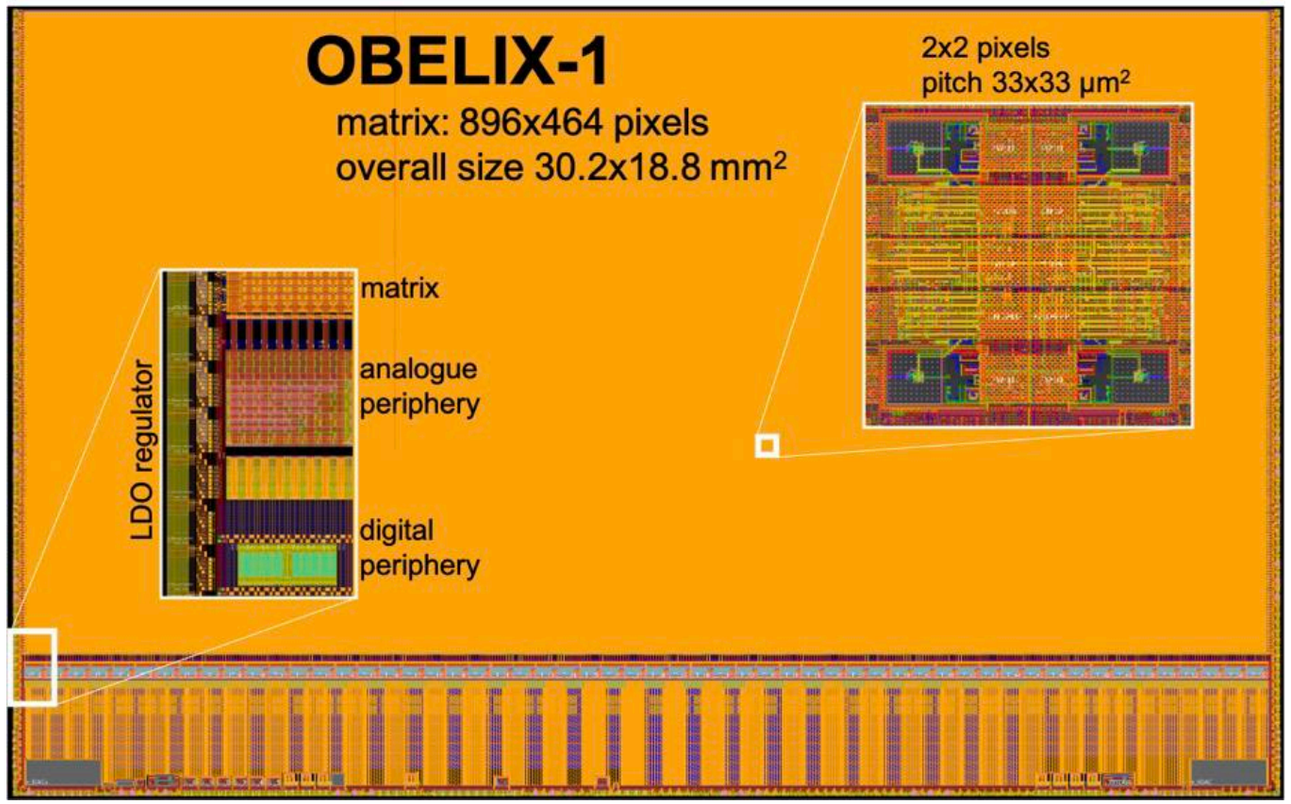




Preliminary results

- Efficiency is above 99%
- Position resolution : 12-14 μm

OBELIX prototype



IPHC group leads the overall design.

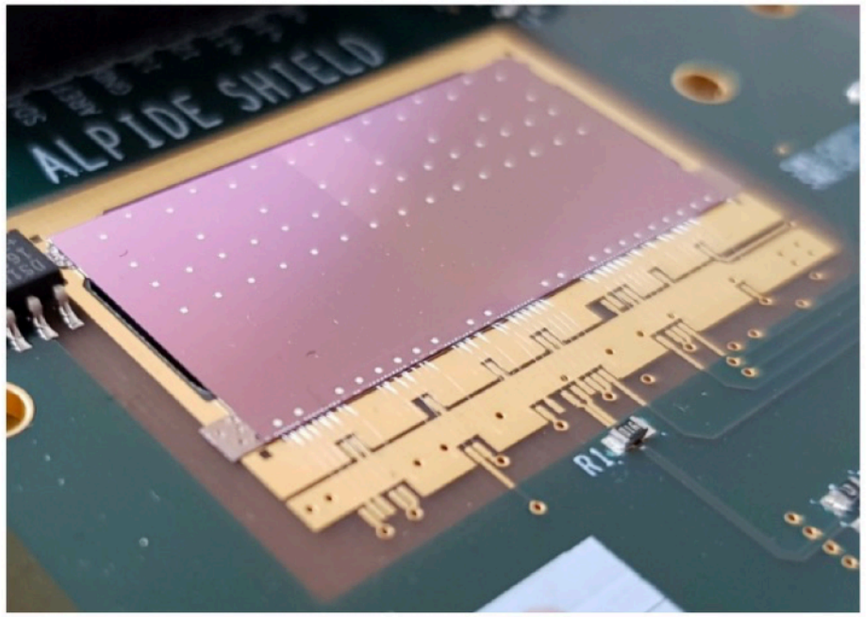
Ph.D student (Xiangyu) from KEK contributes the design of OBELIX-1 (LDO regulator part).

The design of the sensor is now achieved and simulations as well as verifications are on-going before its submission.

	TJ-Monopix2	OBELIX
Year	2020	2025
Pixel pitch	33 μm	33 μm
Sens. area	17× 17 mm^2	~ 30× 16 mm^2
Sens. thickness	25 - 100 μm	~ 30 μm
Integration	25 ns	25 - 100 ns
Bandwidth	320 MHz	320 MHz
Power	200 mW/cm^2	200~300 mW/cm^2 (depending on the hit rate)
TID fluence	0.1 MGy 10^{15} n_{eq}/cm^2	< 1 MGy < 5 ×10^{14} n_{eq}/cm^2

Next generation MAPS for ALICE

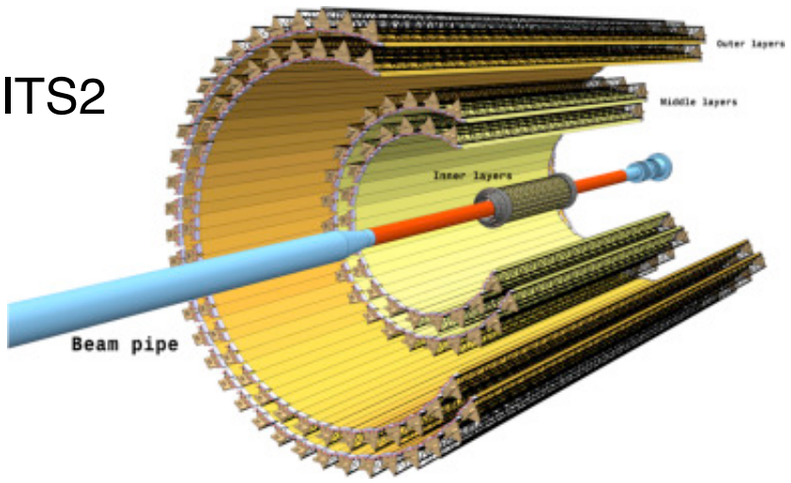
ALPIDE (ALice PIxel DEtector)



Used in ITS2

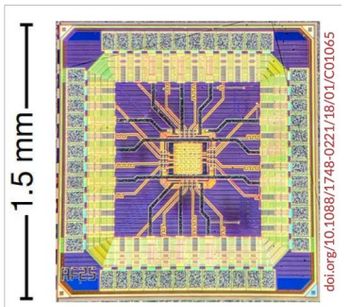
- TowerJazz 180 nm
- Pixel pitch : 29.24 μm × 26.88 μm
- 1024 × 512 ch
- 40 mW/cm^2
- Readout : Digital
- Process : Standard

ITS2



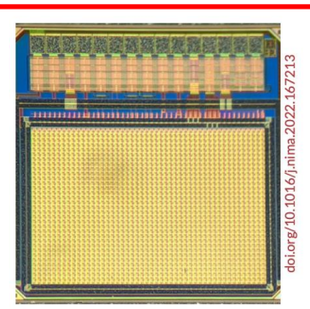
New MAPS for Inner Tracker System

- Using TPSCo 65 nm CMOS technology
- Prototype with a variety of key parameters
  - Pixel pitch (15 μm, 18 μm, 22.5 μm)
  - Matrix pattern (Square, Hex-Square)
  - Inner structure (STD, BLK, GAP)



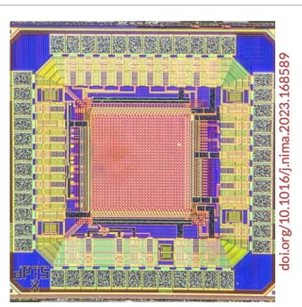
APTS

- 6x6 pixel matrix
- Direct analog readout from central 4x4



CE65

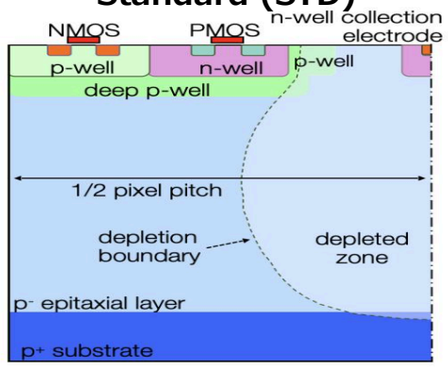
- 48x24 pixel matrix
- Rolling shutter analog readout



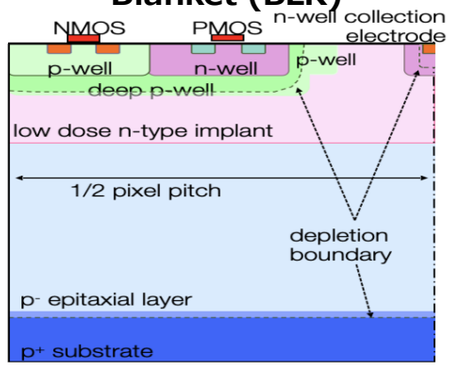
DPTS

- 32x32 pixel matrix
- Asynchronous digital readout

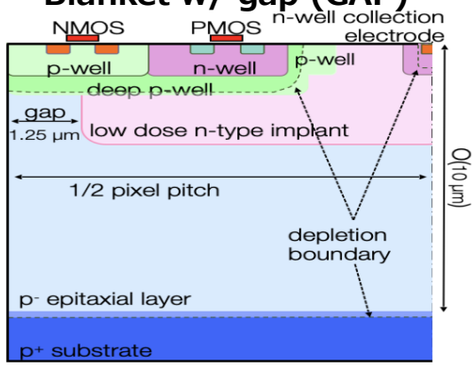
Standard (STD)



Blanket (BLK)

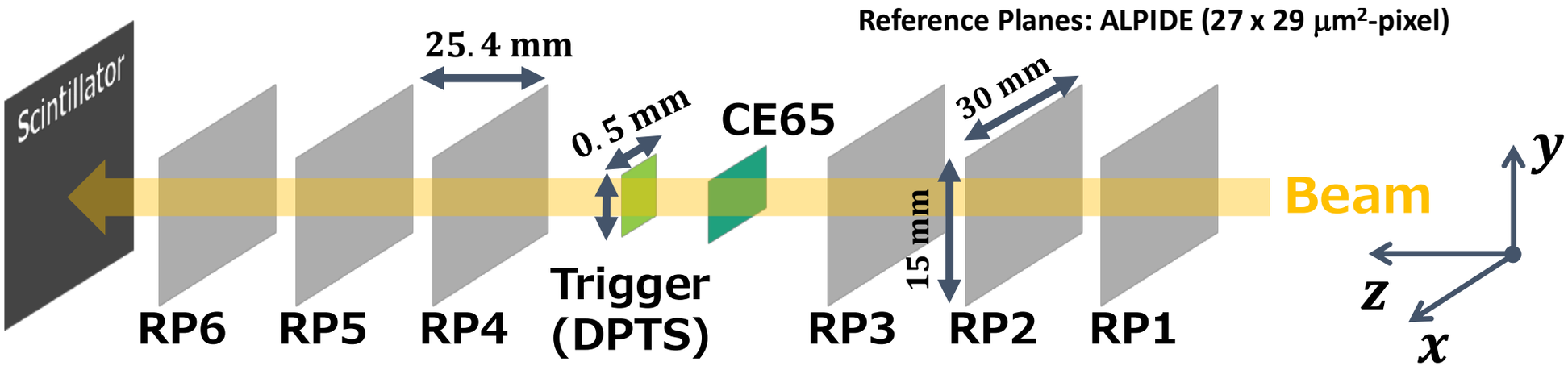


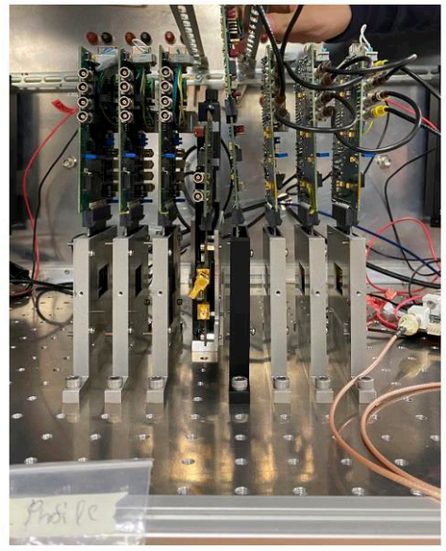
Blanket w/ gap (GAP)



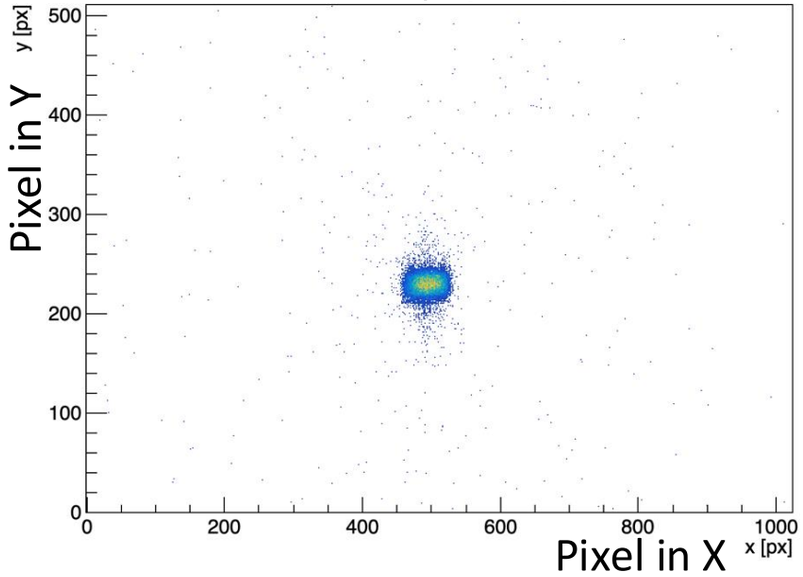
KEK PF-AR testbeam line

Setup

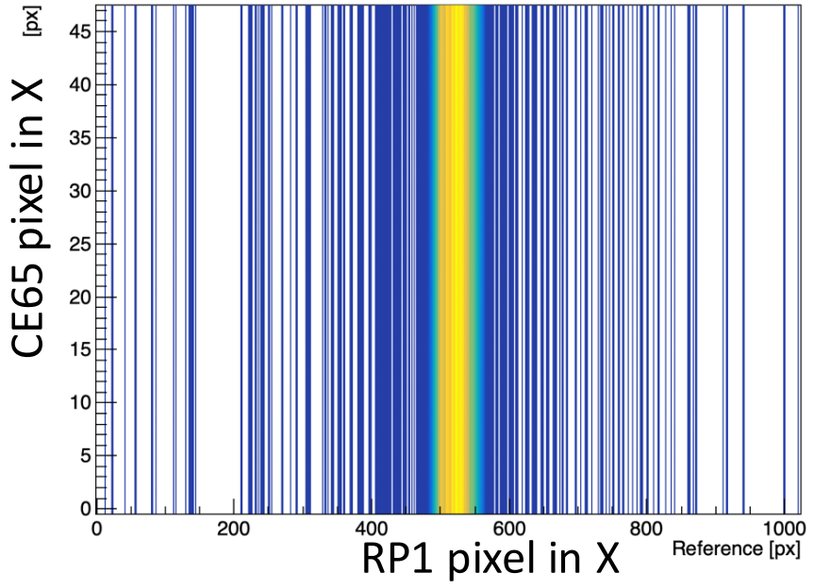




Hitmap (RP1)



Correlation of CE65 hits w/ RP1 hits



Analysis is on-going.

- Compare two inner structures (STD, GAP)

Collaboration with French and Korean group

MAPS with an amplification layer

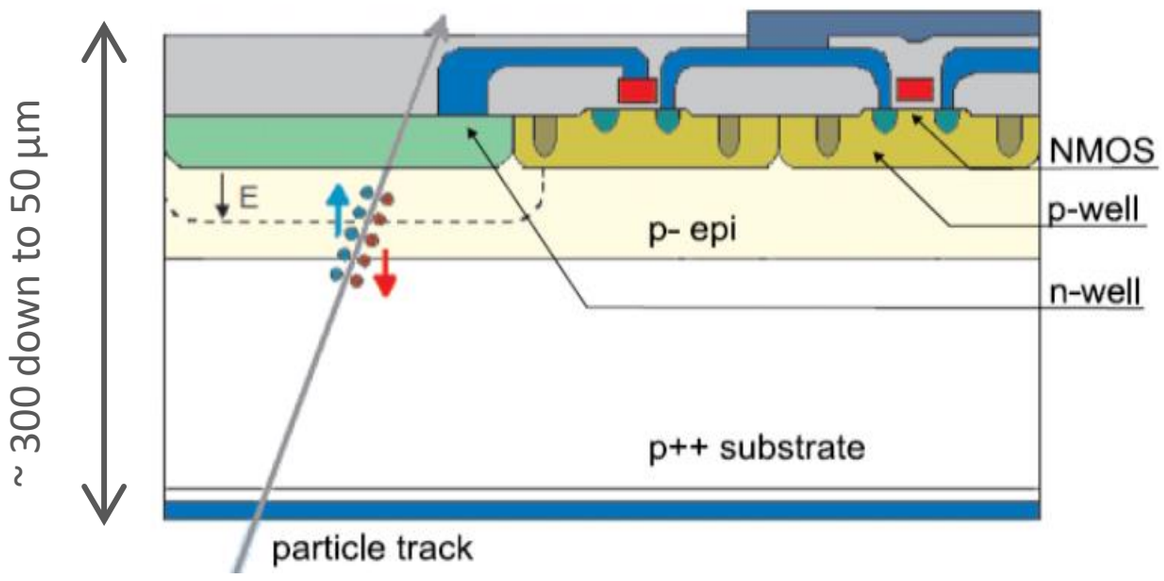
In near future particle physics experiments, silicon detectors are requested to provide precise time information for

- An accurate track reconstruction
- Particle identification
- Mitigation of beam-induced backgrounds

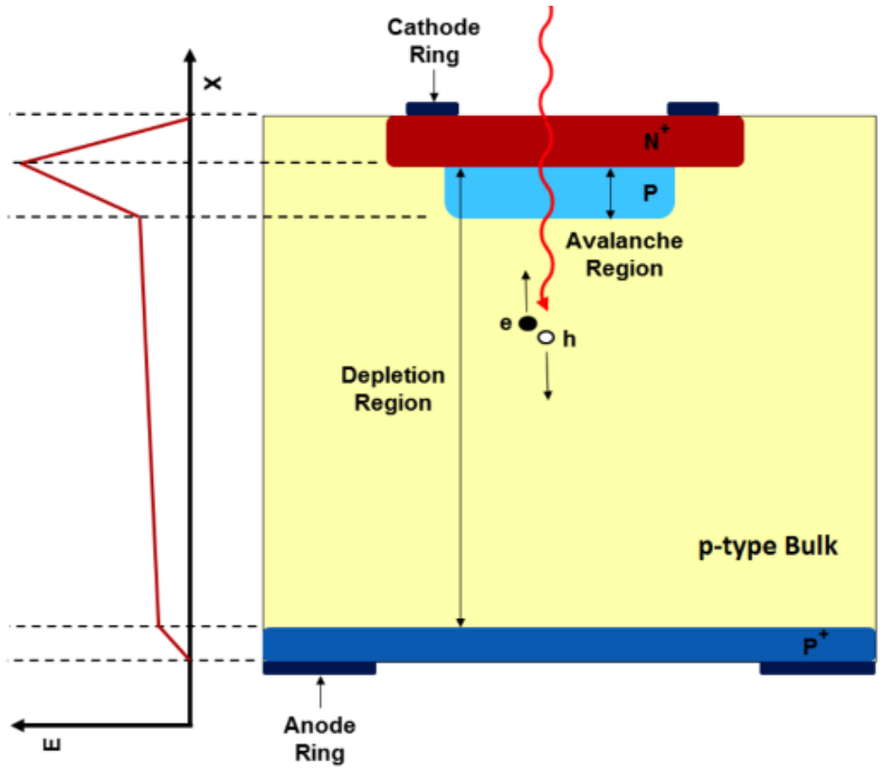
MAPS with an amplification layer has the potential to improve time resolution like LGAD.

- Signal is amplified by an avalanche of electrons in the high electric field
- LGAD has good time resolution (~30 ps)

MAPS



LGAD



APICS prototype

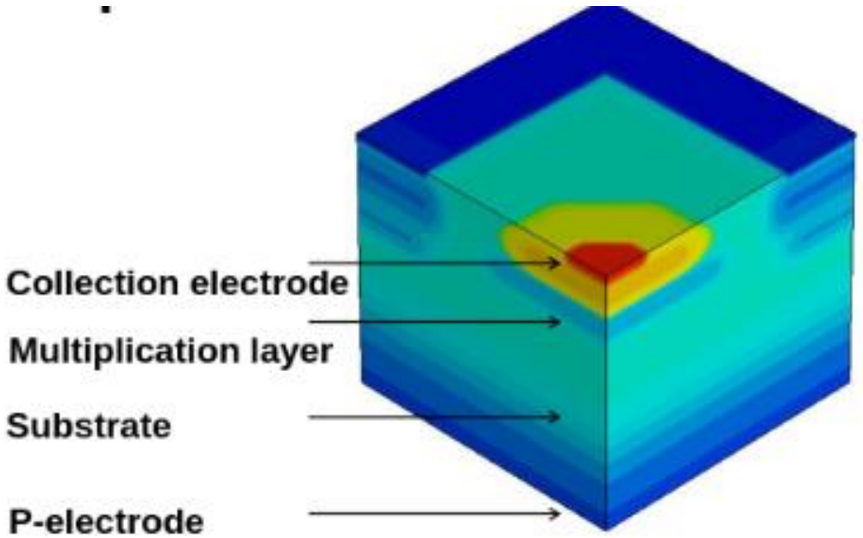
in DRD3 WG 1 project (CASSIA)

APICS (Impact Amplification with CMOS pixel Sensor) project

IPHC and KEK design prototype MAPS with an amplification layer.

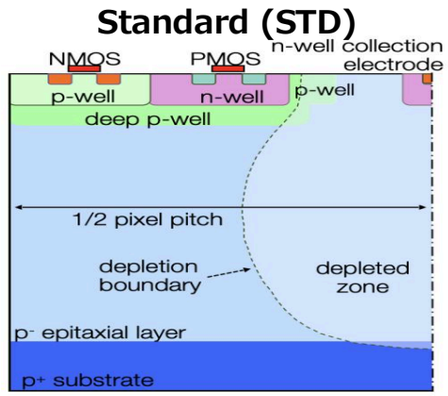
- Tower Jazz 180 nm
- To understand the characteristics with different structures
  - Doping concentration
  - Depth and size of amplification layer
  - Size of electrodes …

- I visited Strasbourg and we started working on a simulation with the same setup.



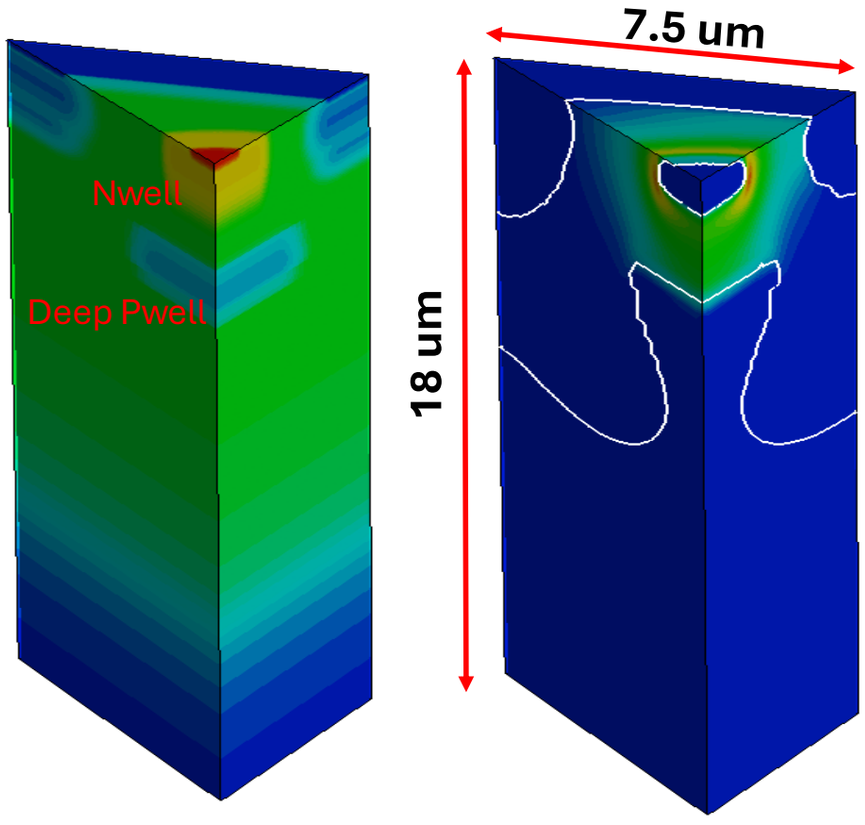
¼ of APD, pitch 15um

Simulation results

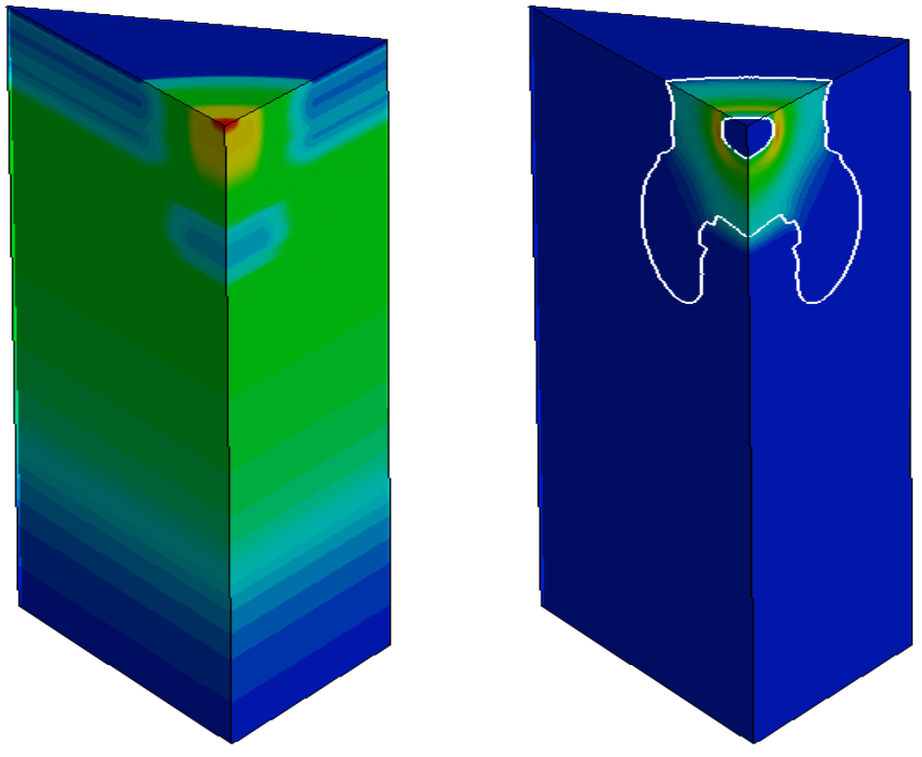


MAPS (Standard) with an amplification layer

Large electrode



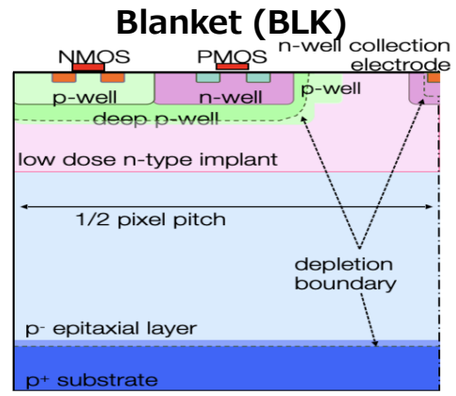
Small electrode



For the large electrode structure, optimized parameters of p-well are

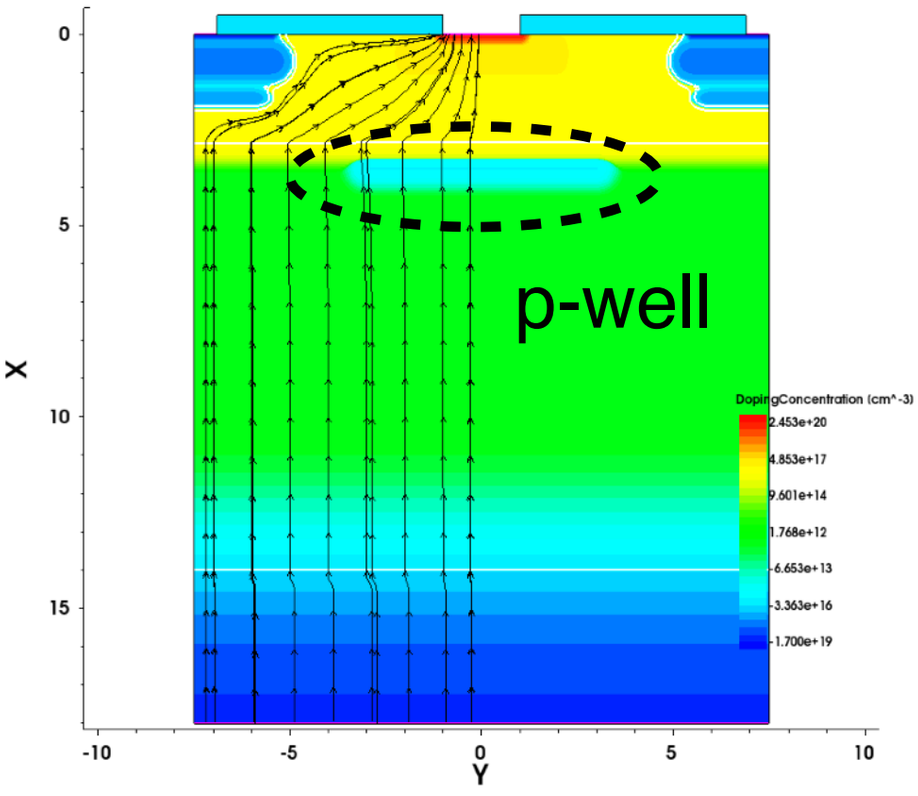
- ~ 1×10^{16} cm^{-3} doping concentration
- 1.5 - 2.5 μm depth

Simulation results

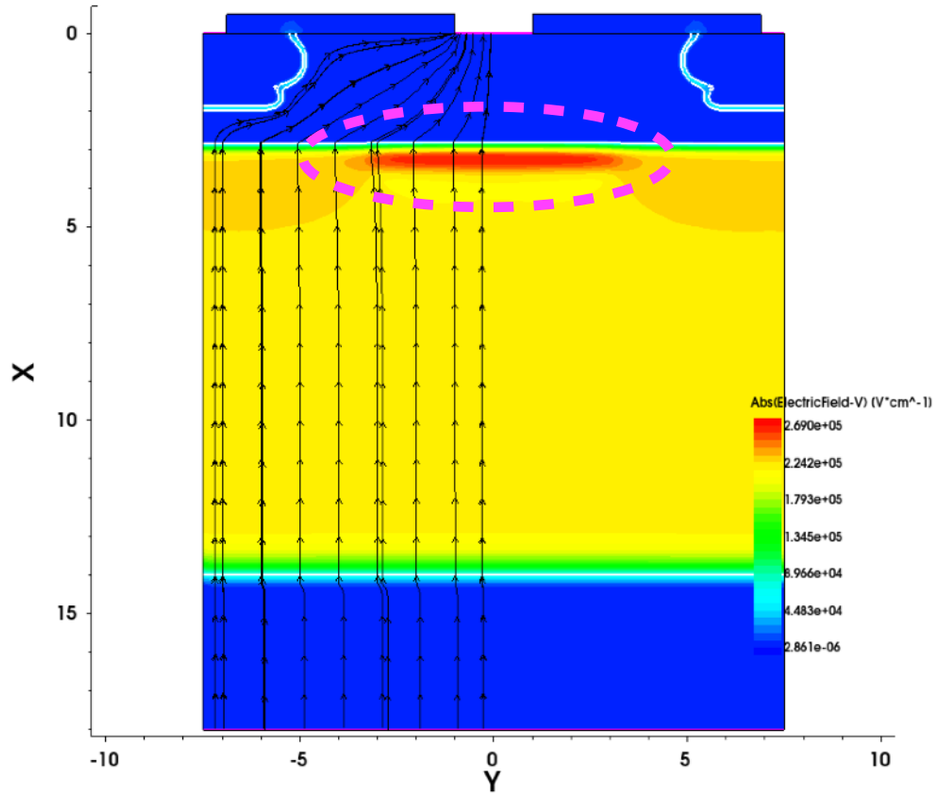


MAPS (Blanket) with an amplification layer

Structure



Electric field



The amplification region is only generated locally, and the gain and time resolution change depending on the hit position within the pixel.

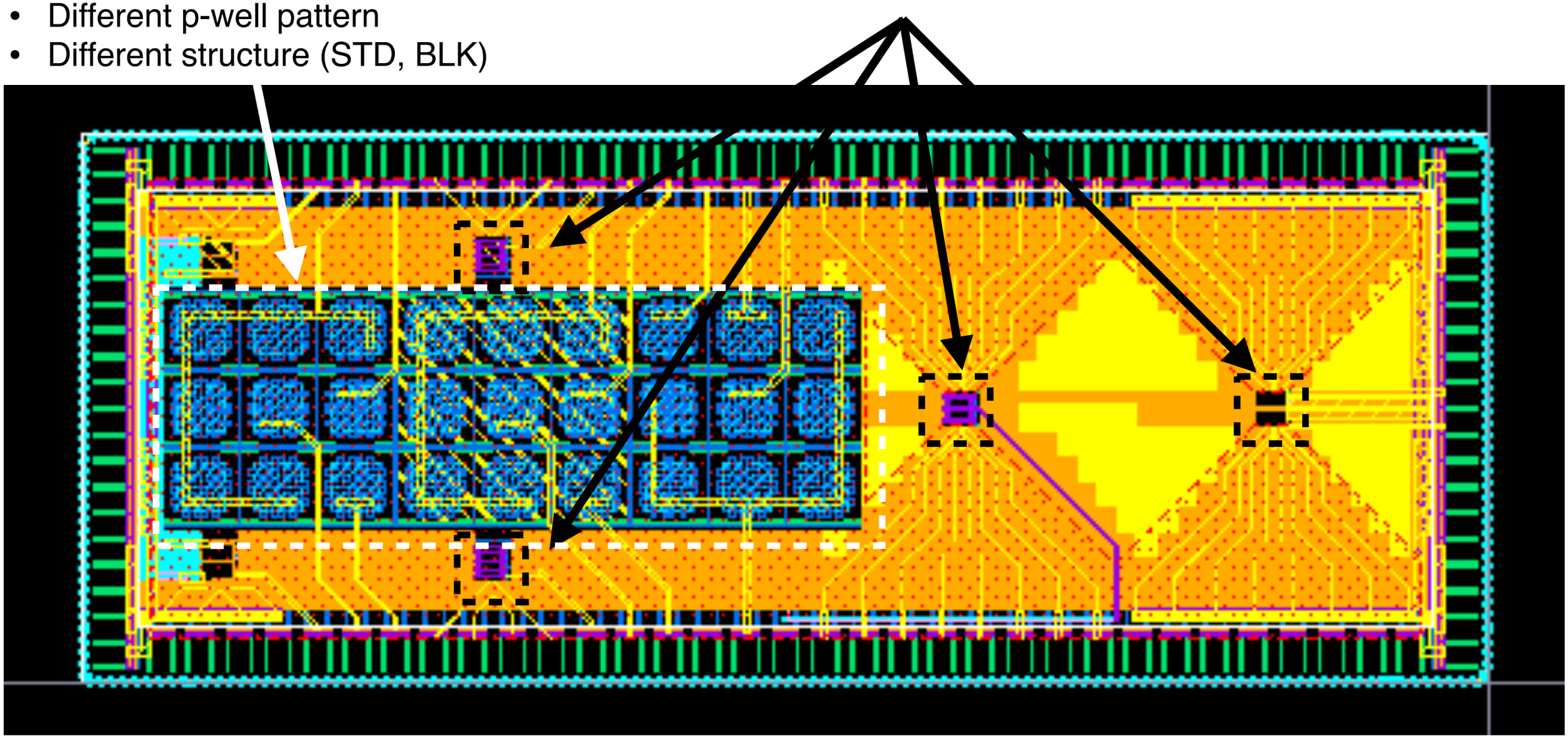
→ To reduce position dependency, the design is changed to implant p-well in the entire pixel area.

APICS prototype chip

Chip size : 5.5 mm × 2 mm

Simple diode (for measurements of characteristics)
- 300 μm × 300 μm pixel size
- 3 × 3 matrix
- Different p-well pattern
- Different structure (STD, BLK)

MAPS with an amplification layer
- 15 μm × 15 μm pixel size
- 8 × 8 matrix
- Different p-well pattern
- Different structure (STD, BLK)



The prototypes are to be sent in fabrication now.

Summary

- Goals of BASHI project
  - Development of OBELIX sensor for Belle II vertex upgrade VTX
  - R&D on the new generation MAPS
    - TPSCo 65 nm for ALICE
    - Internal amplification layer for future applications

- OBELIX sensor development for Belle II
  - TJ-Monopix2 characterization confirmed in lab, DESY and KEK PF-AR test beam line.
  - OBELIX prototype design is on-going.

- TPSCo 65 nm MAPS R&D for ALICE and future e^+e^- collider
  - Characterization of CE65 chips with different structures.
  - A beam test at KEK PF-AR test beam line. Analysis is on-going.

- MAPS with an amplification layer
  - TCAD simulation with different structure is done.
  - Prototype chip design is done.