FKPPL - TYL/FJPPN annual workshop
14-16 May 2025
https://indico.in2p3.fr/event/35664

New generation of MAPS-based telescope with the sensors planned for the Belle II upgrade

J. Baudot for
Miho Yamada (TMCIT)
Christian Finck (IPHC)

- Context of Franco-Japanese MAPS R&D
- Report on D-RD-24 () MAPS for Belle II upgrade
- New proposal focused on beam telescope

MAPS R&D between France & Japan

Science & R&D

Belle II

Vertex upgrade
with OBELIX sensor

ALICE

ITS upgrade
ALICE-3

- ***Other FJPPN talks***
  Y. Okazaki (D_RD_29)
  R. Guernane (nex)

DRD3

R&D for new MAPS generation
with TPSCo 65 nm

French groups

@ IN2P3

TYL / FJPPN

@ KEK

ITDC 測定器開発センター Instrumentation Technology Development Center

Japanese groups

Education

MAPS Academy

KEK, 23-30 July 2025
20 students Asia/America/Eu
https://wiki.kek.jp/display/mapschool/MAPS+Academy

Test facility

AR Test Beam Line

Partners in this collaboration

TMCIT

- Miho Yamada

IPNS/KEK

- Akimasa Ishikawa
- Tristan Fillinger (post-doc)
- Toru Tsuboyama
- Takehiko Takayanagi

Univ. Tsukuba

- Takumi Omori (PhD student -2023)

Nara Women's University

- Kenkichi Miyabayashi
- Emi Ozaki (Master student 2024-)

IPHC / TYL

- Jerome Baudot
- Auguste Besson
- Ziad El Bitar
- Mathieu Goffe
- Thomas Lauber (Master student)
- Mattéo MAUSHART (PhD student)
- Christian Finck

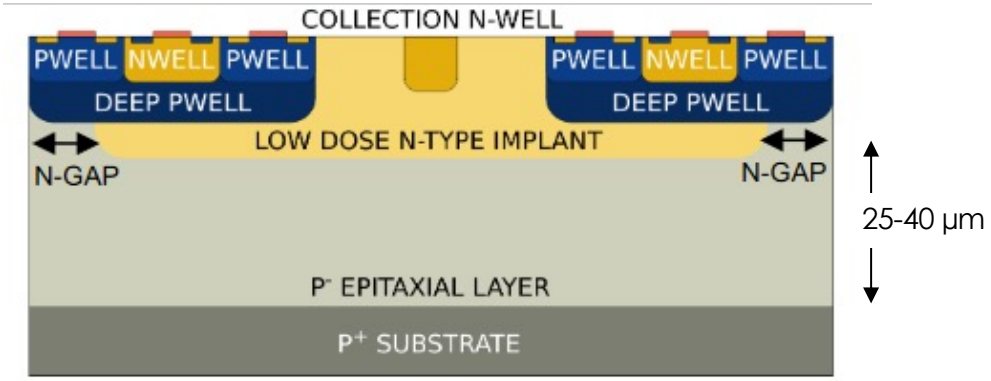
Recap of D_RD_24 project: 2021-2025

Context of Belle II vertex detector upgrade

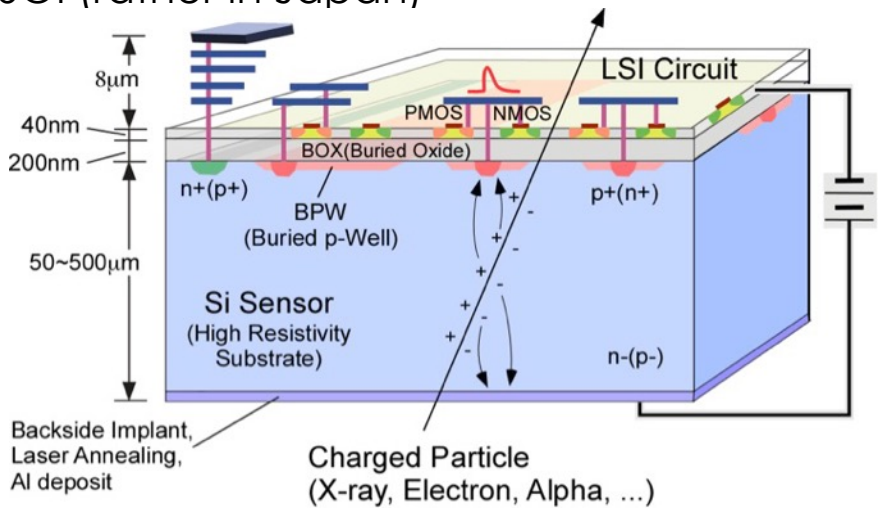
- Motivation: **more robustness against higher beam background** with higher lumi / current DEPFET and Strip sensors
- Proposed solutions: **single monolithic sensor & simple/light system**

2 technologies of monolithic sensors

- CMOS (rather in France)



- SOI (rather in Japan)



Franco-Japanese project to progress in parallel

- Initial phase: discussing specifications & exchanging expertise on sensor design
- **Final goal: common beam test with both technologies**

SOI Telescope

Tracking reference planes

- INTPIX4 SOI sensor
- Matrix (832x512) 14.1 x 8.7 mm^2
- Pixel pitch 17 x 17 µm^2
- Analogue (12 bits) read-out

} Benefit position resol. / Limit hit rate

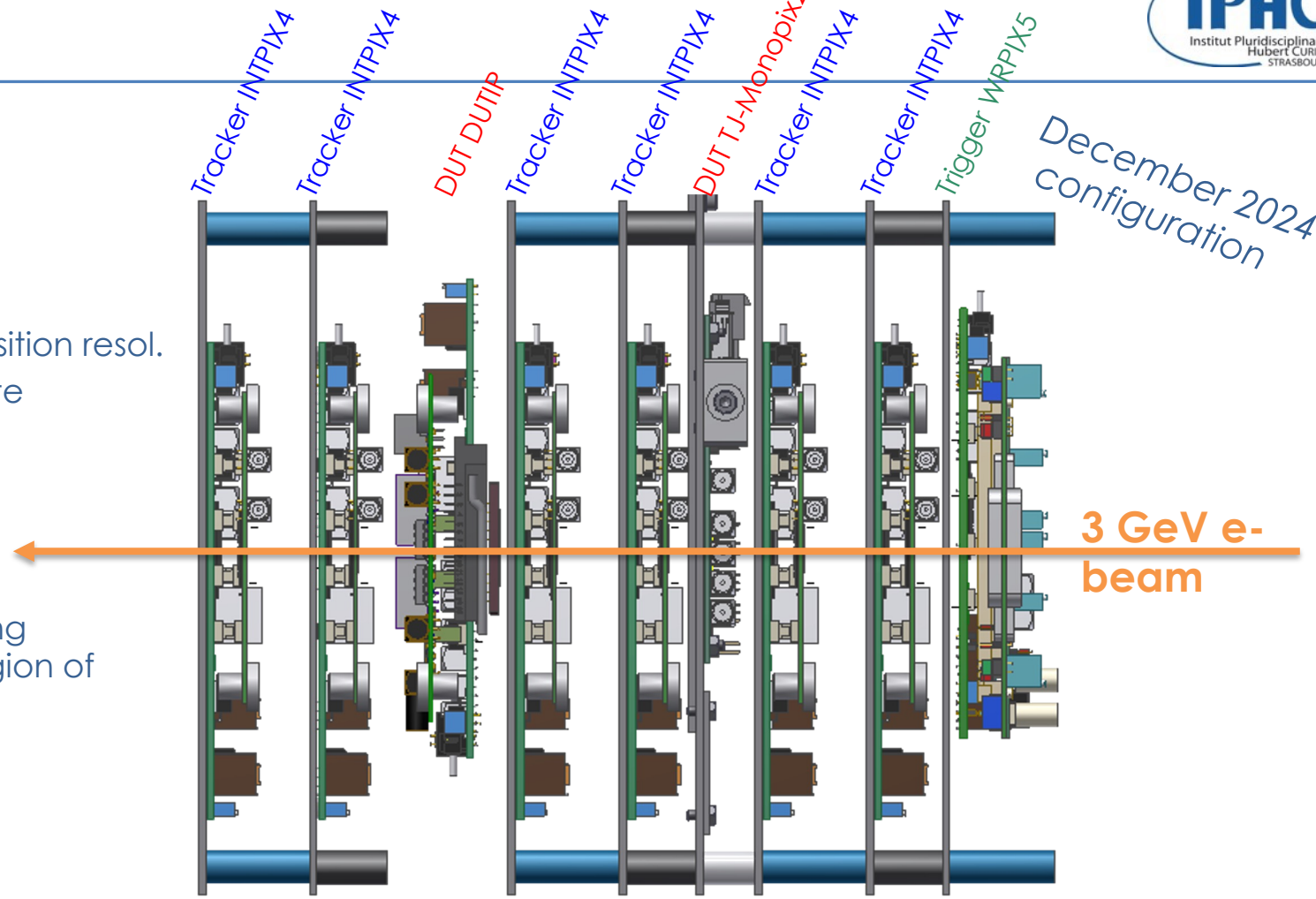
Triggering planes

- XRPIX5 sensor
- Matrix (608x384) 21.9x13.8 mm^2
- Pixel pitch 36 x 36 µm^2
- Binary read-out

} Triggering over region of interest

Device Under Test (DUT)

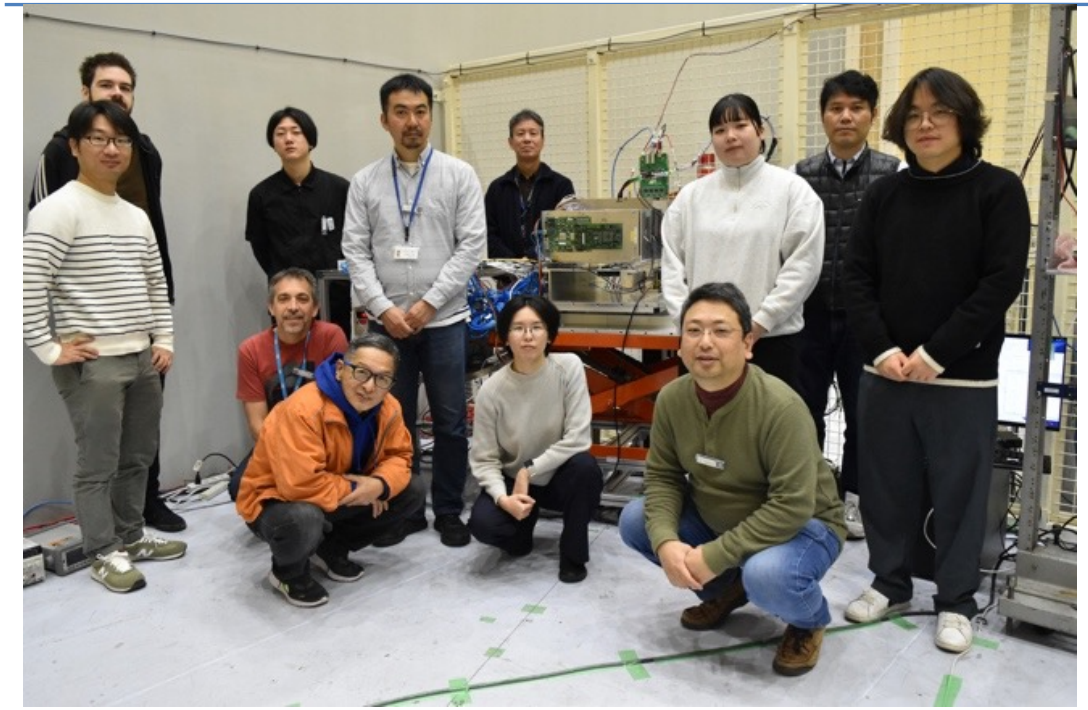
- DuTIP SOI sensor
- TJ-Monopix2 CMOS sensor

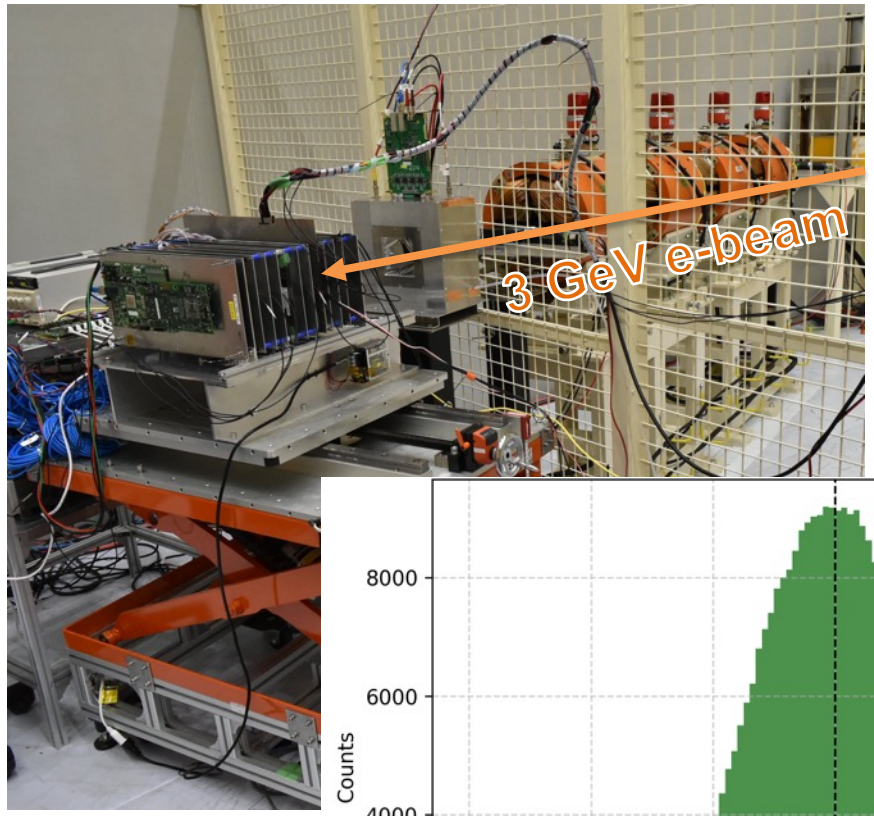


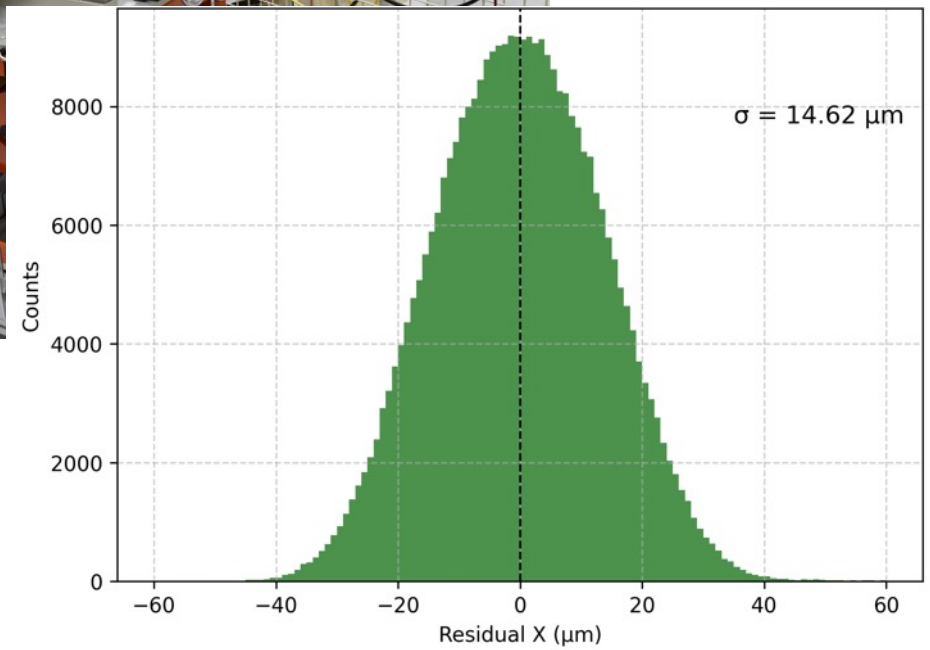
+ Newly developed trigger logic (USAGI) distributed to all boards

=> Typical track rate at DUT ~80 Hz

Common SOI-CMOS beam test 6-11 Dec 2025







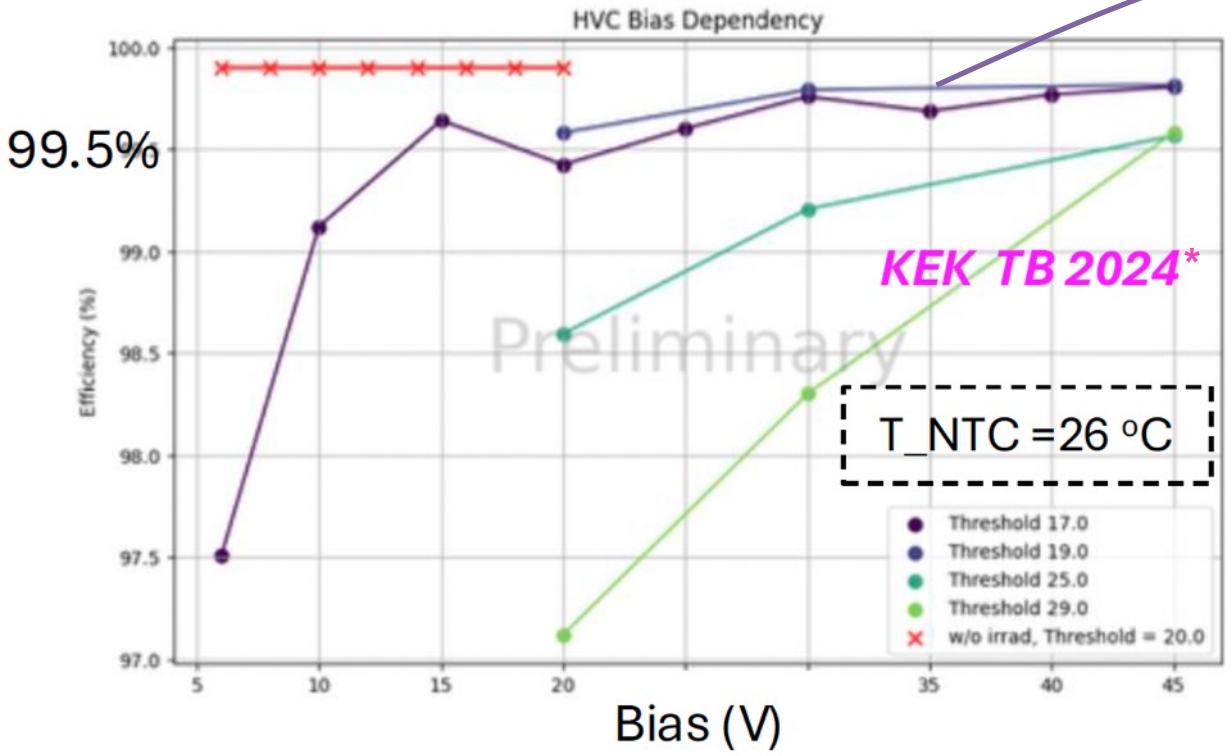
Telescecope-track position – DUT position

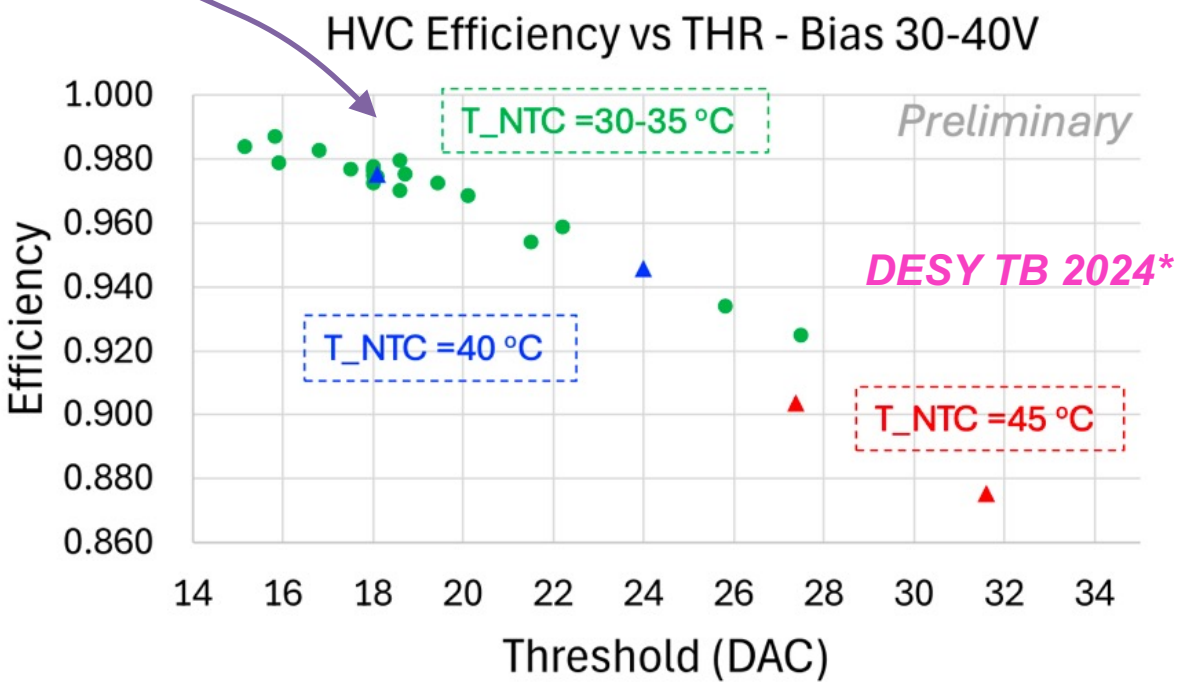
- Excellent operation of SOI telescope
- Results from TJ-Monopix2 already back
- Data from DuTiP sensor still in analysis

TJ-Monopix2 characterisation

- Key question: operation at room temperature after fluence $5x10^{14}$ n_{eq}/cm^2

- Result highlights on detection efficiency





* Analaysis for D_RD_29 project

* Participation of S.Wang (KEK) to DESY TB

Proposal for new project 2025-

- Principle investigators: Miho Yamada (TMCIT), Christian Finck (IPHC)

- New generation of sensors to characterise
  - CMOS: OBELIX-1 starting in 2026, OBELIX-2 at the horizon of 2028
  - SOI: DuTiP-2 starting in 2025
  - Re-use of SOI telescope => possible modification of trigger logic

- New generation of beam telescope
  - Exploit all features of OBELIX-1 for high hit-rate & track-triggering
  - Potential commissioning in 2027

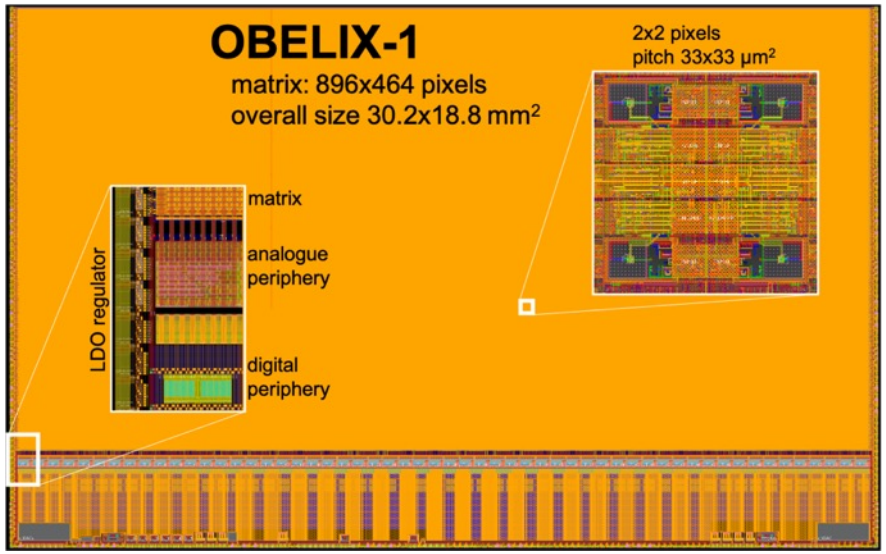
OBELIX (Optimized BELle II pIXel) sensor

	OBELIX
Pitch	33 µm
Signal ToT	7 bits
Integration time	50 To 100 ns
Time stamping	~5 ns for hit rate < 10 MHz/cm^2
Hit rate max for 100% eff.	120 MHz/cm^2
Trigger handling	30 KHz with 10 µs delay
Trigger output	~30 ns resolution with low granularity
Power (with hit rate)	120 to 200 mW/cm^2 (1 to 120 MHz/cm2)
Bandwidth	1 output 320 MHz

=> Large hit-rate

=> track-triggering

- Matrix core
  - Re-use of TJ-Monopix2
  - With some corrections
- New digital logic
  - Timing & triggering



- Current schedule
  - Design (layout) completed
  - Verification on-going
  - Tape-out this Summer 2025
  - OBELIX-2 in 2027

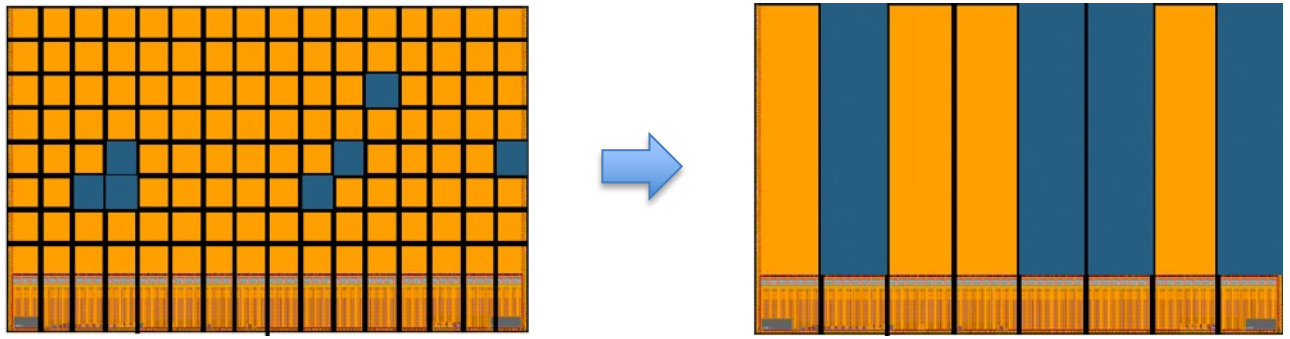
=> Large test campaign required

Track-triggering with OBELIX

- Preliminary work by Mattéo MAUSHART (TYL Master student in 2024)

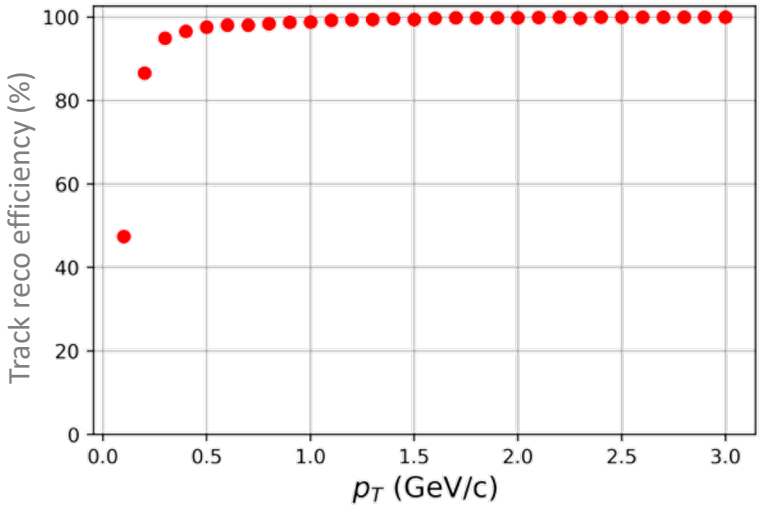
A software estimation

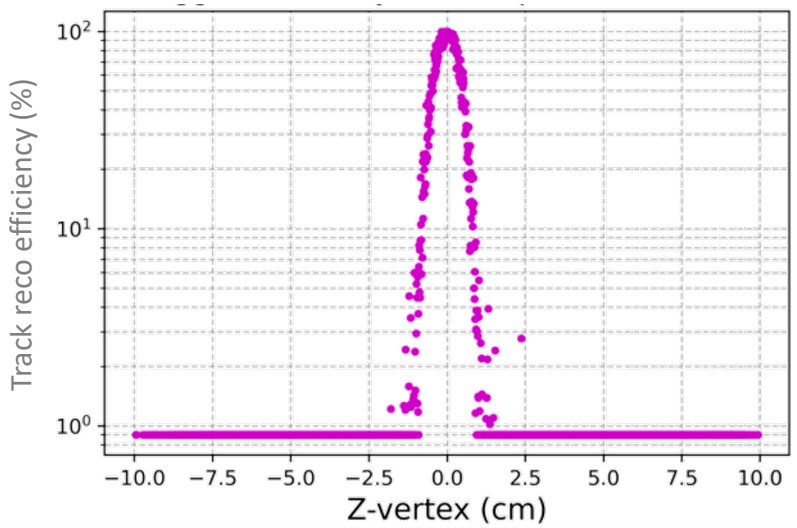
- Exploit 5 layer geometry full simulation
- Granularity reduced to 8 striplets/sensor
- 30 ns integration, used in simulation



Track reconstruction

- Training: store track hit-patterns in Look-up table
- Reco: search hit-pattern in table => track

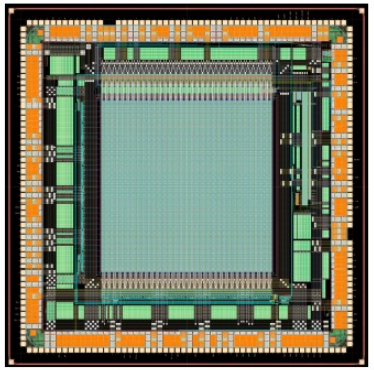




- Excellent standalone efficiency
- But large fake track rate at high rate (not a concern for telescope)

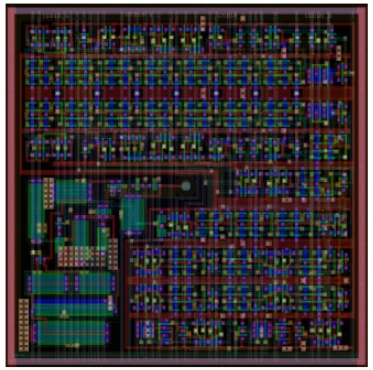
DuTiP series

DuTiP1 (2020—)



6 × 6 mm²

DuTiP1 Pixel

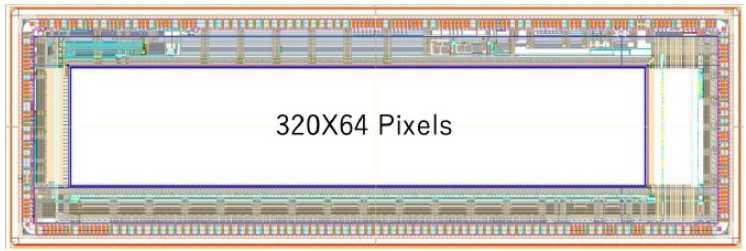


45 × 45 µm²

Pixel
- Pre. amplifier (ALPIDE type)
- Shaper
- Comparator
- Dual down time counters (7 bit)
- Timing memory (Previous/Current)

Readout
- Row address (5 bit)
- Column address (5 bit)
- 2 bit hit (Previous/Current)
- CMOS in/out

DuTiP2 (2021—)



18.4 × 6 mm²

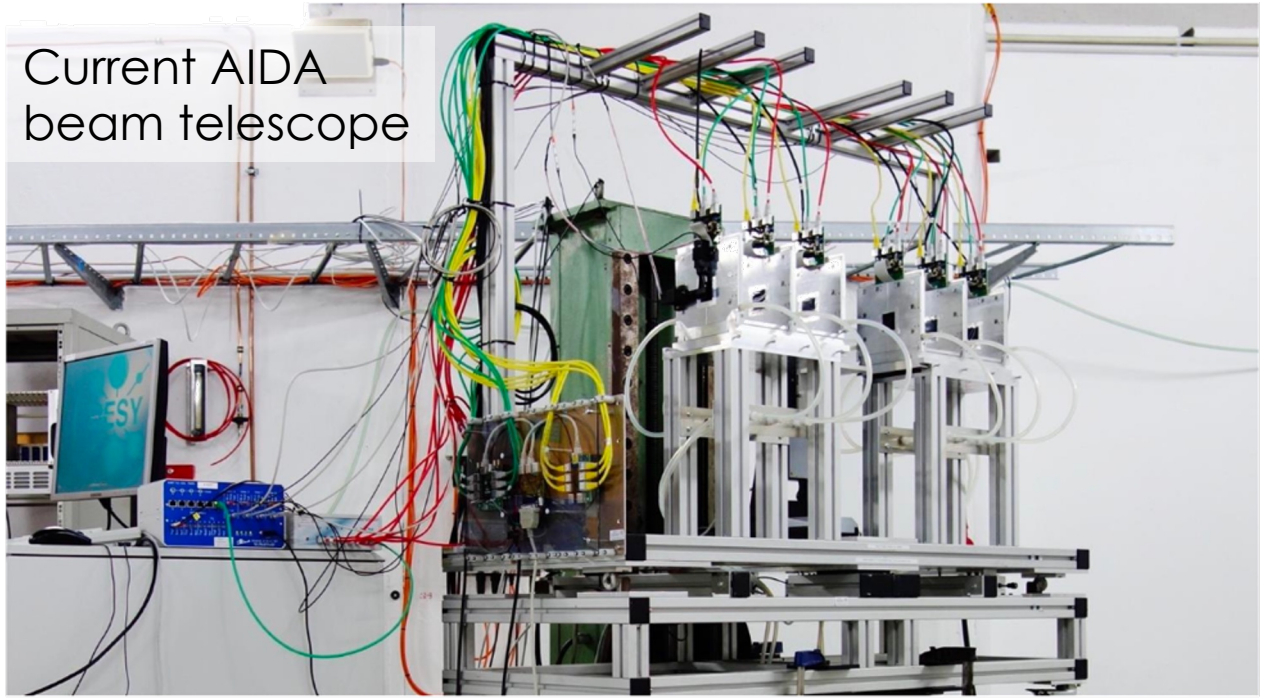
Design
- Dec. 2021 submitted → deliver in Spring 2022
- Pixel design is almost completed by DuTiP1
- Row 320 pixels (Full size for Belle II) for design of large-area sensor
- FIFO, LVDS in/out, DAC

DuTiP3 (2023—)

Design
- June 2023 submitted, February 2024 delivered

Still significant amount of tests needed

Plan for OBELIX-based beam telescope



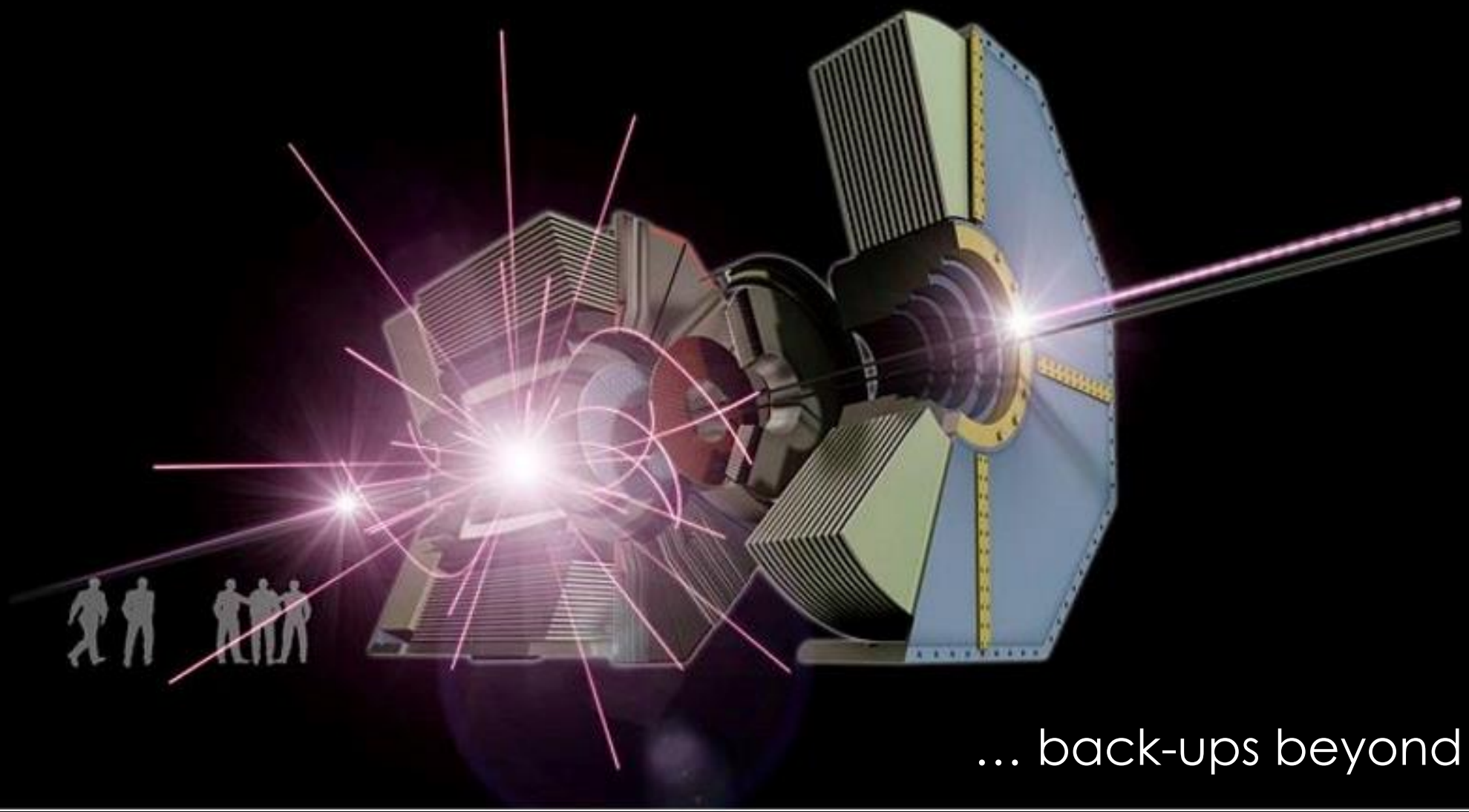
- New facility proposed in DRD3
  - Various European partners
  - Replicas of same telescope in CERN, DESY, KEK
  - 6 large area high-resolution / high-rate detector planes for tracking & triggering
  - DAQ & control, similar to Belle II-VTX system
  - Operated through standards (EUDAQ, Corry)

=> Proposed innovation:
track-trigger on beam particles

=> Major opportunity to
- Experience long period of data taking with OBELIX & associated system
- Enhance test facilities

- Starting phase 2025-2026
  - Sensor = OBELIX-1
  - DAQ = current BDAQ53 lab-system

Thank you …

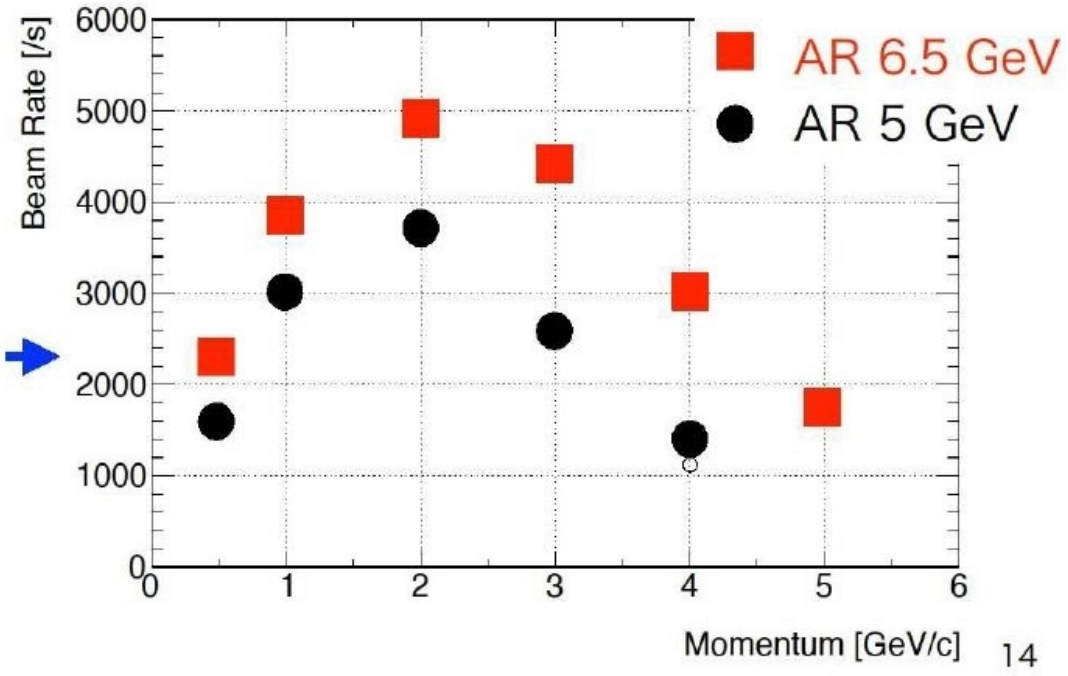


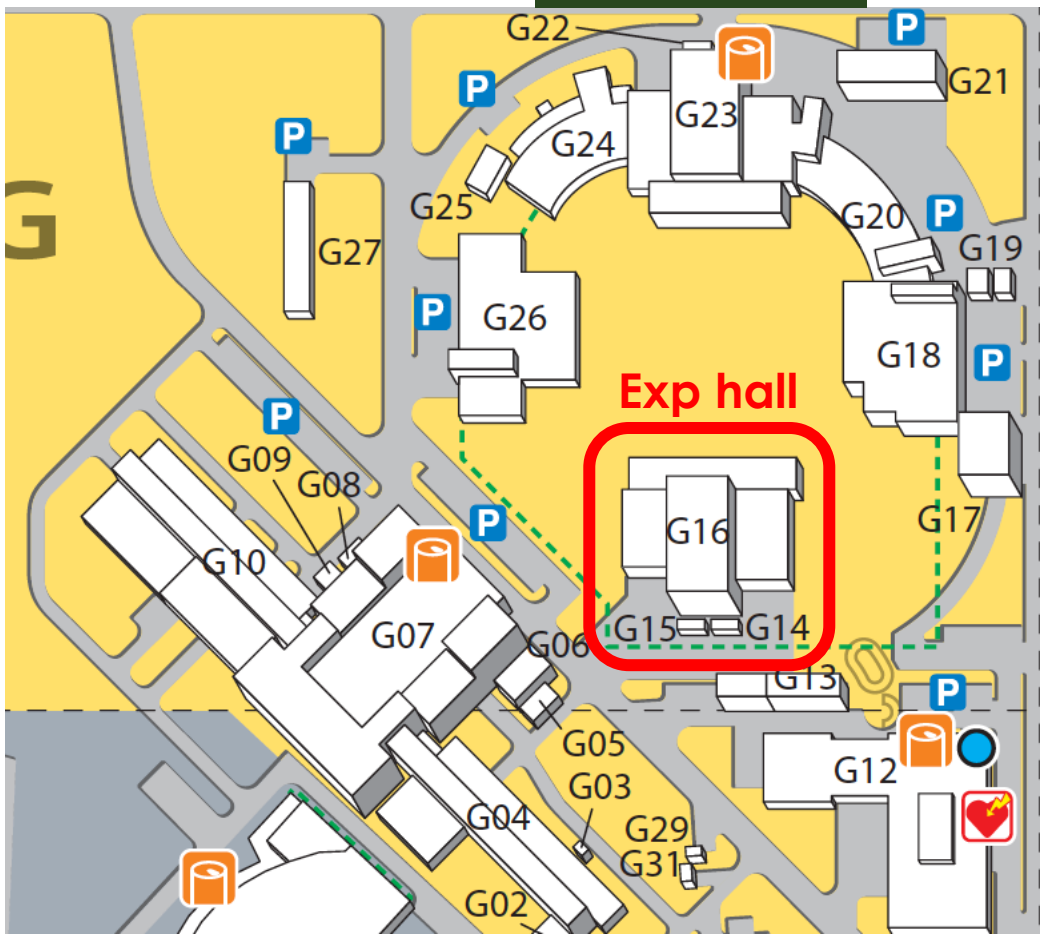
… back-ups beyond this point

KEK ITDC PF-AR test e- beam line

- https://itdc.kek.jp/testBeamLine/index.html
- K. Hanagaki, JPS 2020 Autumn Meeting https://kds.kek.jp/event/35569/

- Current max rate ≲ 1 kHz

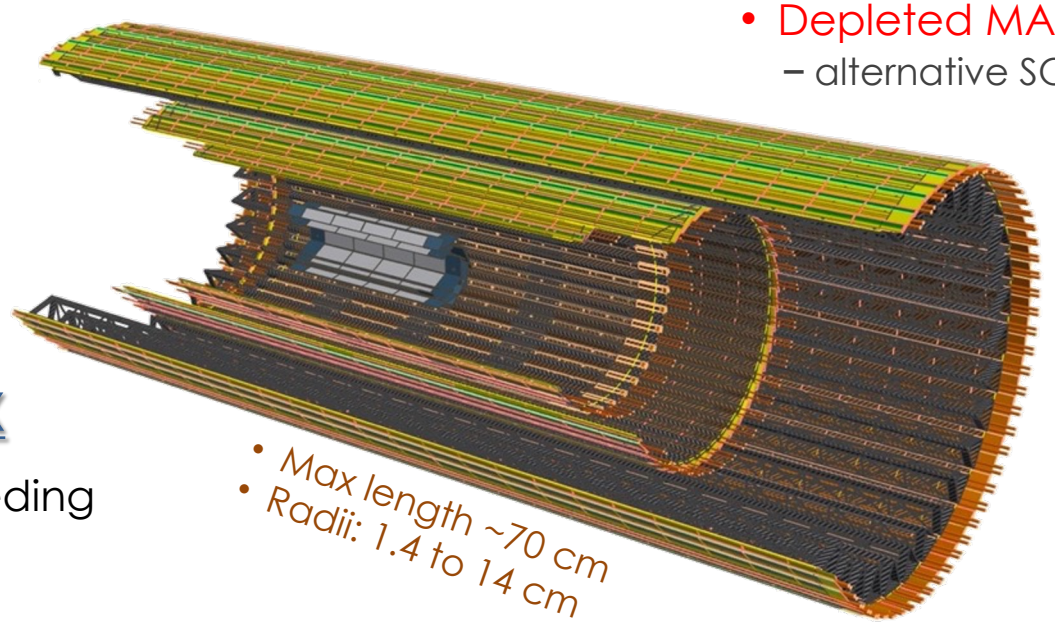




VTX main concepts

- **2 inner layers: iVTX**
  - "On" beam pipe for IP resolution
  - Full-silicon concept:
    - material ≲ 0.2 % X_0 / layer
    - single-side connexion

- **Same sensor everywhere**
  - Space & time granularity => occupancy ≪ 1%
  - Depleted MAPS: **OBELIX**
    - alternative SOI: DuTIP



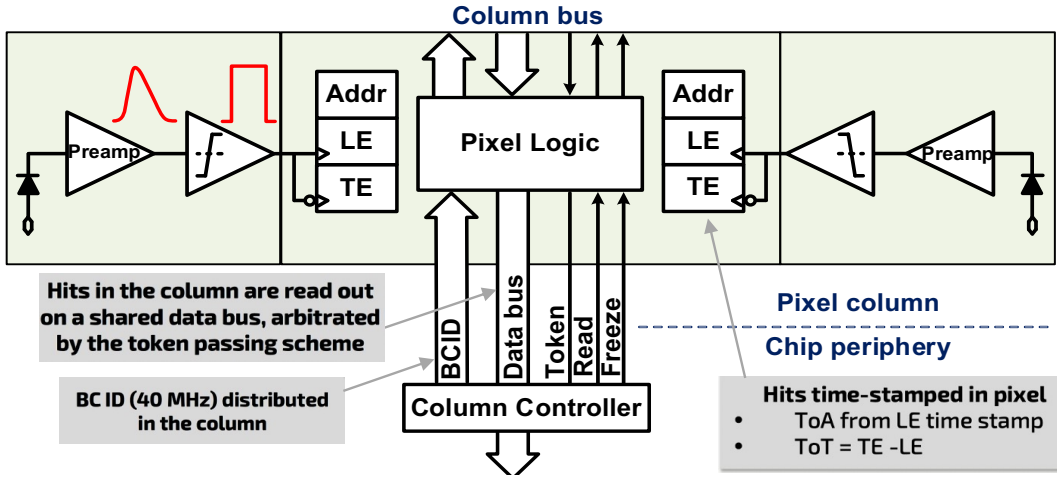
- **3 to 4 outer layers: oVTX**
  - at least 3 points for track seeding
  - Light & thin support:
    - material ≲ 0.8% X_0 / layer
    - single-side connexion whenever possible
  - Straight sections => adaptable to any IR

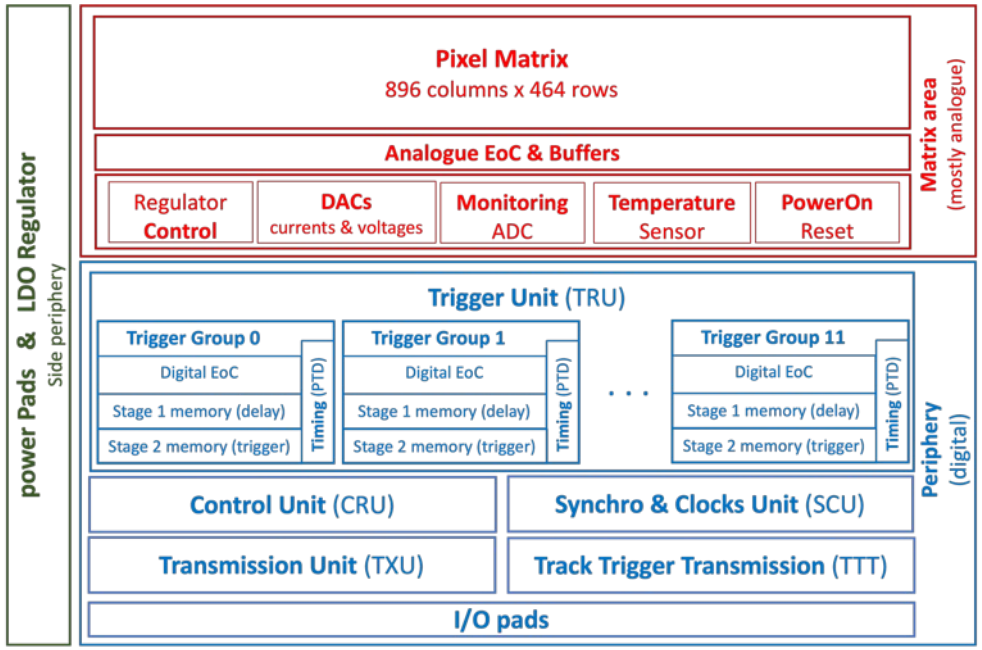
- **System**
  - Optical links asap

- **Fast track reconstruction**
  - Full resolution for High Level Trigger
  - Reduced granularity for L1 trigger

Framework Conceptual Design Report arXiv:2406.19421 [hep-ex]

Design of OBELIX-1





Matrix design

- Extended copy of TJ-Monopix2
- 2 front-end falvours: **DC- and AC- casocode**
- Clock for time-binning slowed down: 100ns

Powering

- LDO regulator for easier voltage distribution
- Overall power depends on hit rate: 200-300 mW/cm^2

Trigger Unit

- Simulated with realistic inputs: 120 MHz/cm^2
- Can sustain 800 MHz/cm^2 for 0.5 µs

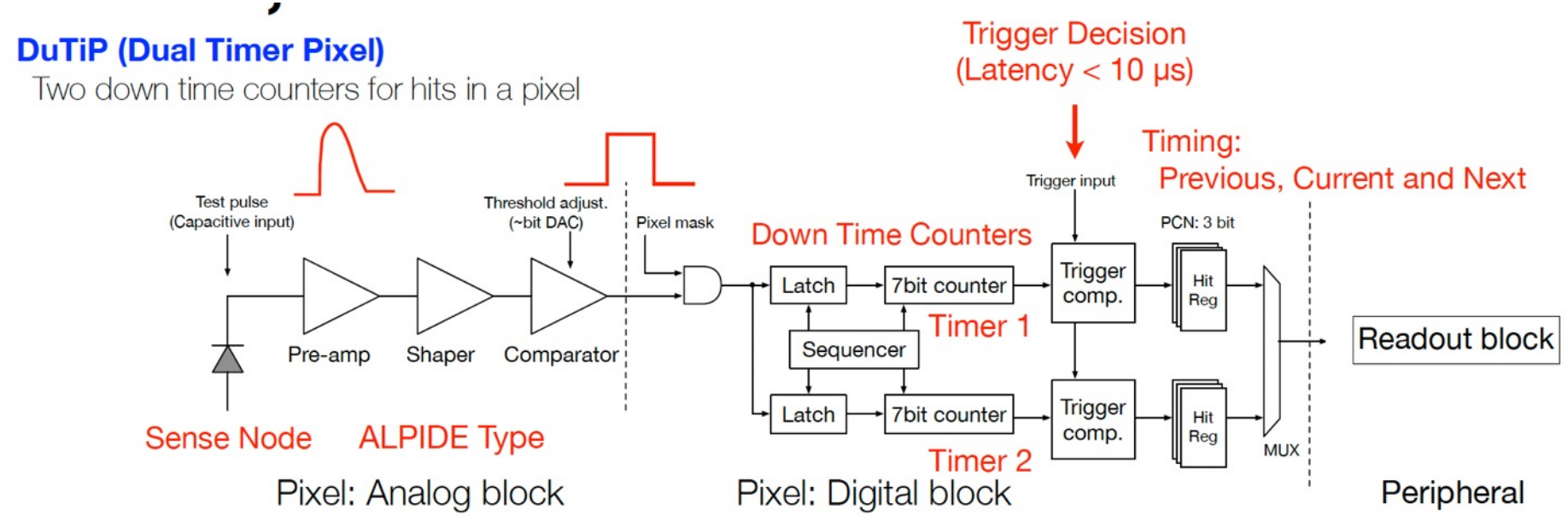
Fine time stamping

- 6 ns achievable with end-of-column fast clock
  - Limited to hit rate <^ 10 MHz/cm^2

Track trigger

- Reduced granularity to 8 striplets (~4 x18 mm^2)
- Increased transmission rate: 33 MHz

DuTiP concept



Analog block: Usual configuration for the binary detector
Hit memory: Timing of Previous, Current and Next collision
Signal: Coincided with event trigger ← Down time counter corresponds to trigger latency
Background: Random, out of time window ← Suppressed by coincidence
Multiple hits in trigger latency: Multiple timer and memory are controlled by Sequencer