

## CALOROC status

Feb 21 2025

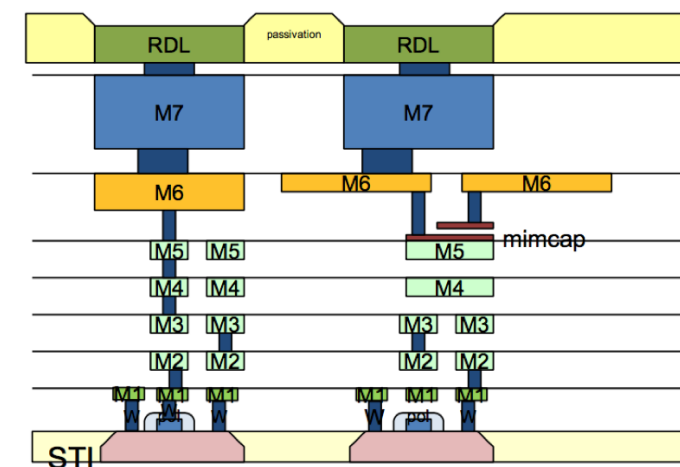
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# CALOROC development and test plans

- ❑ CALOROC submission process initiated with request of
  - ❑ 5 wafers (for wire-bonding)
  - ❑ 2 wafers (with C4 bumps) → **CALOROC** are here ~160 pieces total
  - ❑ 1 wafer on hold
  - ❑ Waiting for quotation, then payment

- ❑ CALOROC back-end ready on GIT available at:

- ❑ <https://gitlab.in2p3.fr/eic/calodigglobal>
- ❑ Distributed to LLR and ORNL (then to ppl who really needed it)



- ❑ Quotation for the CALOROC interposer requested

- ❑ Aka substrate, mandatory for packaging in BGA
- ❑ ~ 3 month of fabrication

- ❑ CALOROC testboard (based on HK digitizer from LLR)

- ❑ Testboard = ASIC characterization
- ❑ Trying to find how to manage/design it

