# Contributions to DRD3/WP2-WP4

## LGAD Sensor development
## Novel interconnection technologies for pixel detectors

# Development of TI-LGAD for 4D tracking

## Project in DRD3/WP2

LPNHE / IJCLab

# DRD3 WP2: Context for high-resistivity

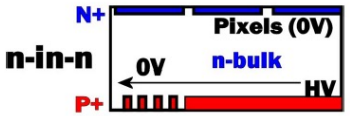
## Expertise in high resistivity sensor design and development at IN2P3

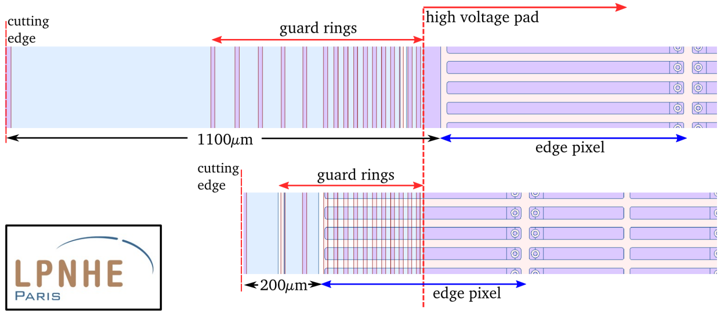
In the last decade applications to High Energy Physics in particular for LHC experiments

- early upgrades (example: ATLAS IBL)
- HL-LHC upgrades

## Examples of complete contributions, from the sensor conception and gds to the final modules

### ATLAS IBL




Existing B Layer

IBL approved

LPNHE Paris

IJCLab Irène Joliot-Curie

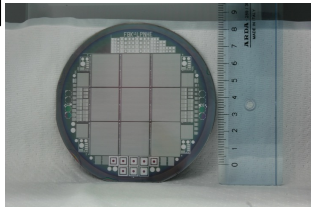
Work to improve the design of the GR region
Distance of last pixel from the edge reduced now to 200um in the IBL, was ~1mm before !

### Developments to achieve ATLAS ITk final design (n-in-p proof!)

LPNHE Paris

IJCLab Irène Joliot-Curie

2014 – PAE1



4'' 200um wafers
50x400 and 50x250 pixels with and without active edges

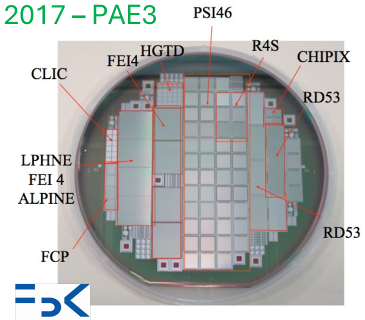
FBK Fondazione Bruno Kessler

2016 - P2 standard edge


6" 100-130 µm thick n-on-p
50x250 (FE-I4)
Dedicated test structures (first FBK 6'' production) in preparation of PAE3

Shared production ATLAS-CMS

2017 – PAE3




FBK Fondazione Bruno Kessler

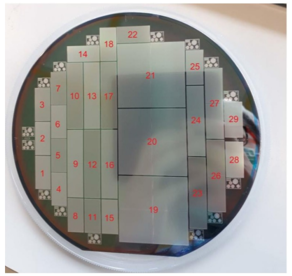
6'' 100 and 130um

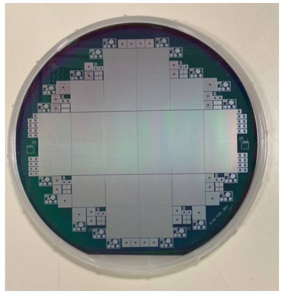
ATLAS pixels
50 x 250 (FE-I4)
50x50, 25x100 (RD53)
Active Edge devices
More devices added for other collaborations

ATLAS-CMS

LPNHE Paris

6'' 150, 100, 50um (ITk preprod and prod)





FBK Fondazione Bruno Kessler

ITk final quad sensors
Structures for hybridization QC
LPNHE responsible for final design at FBK

## Willing to maintain the expertise for many future applications

# Applications of high-resistivity for future devices

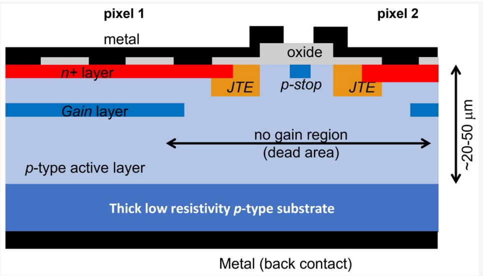
## Most of the applications are based on time resolution

- replacement of HL-LHC (Phase-II) components
- timing layers at 30-50 ps for LHC experiments
- TOF large area layers (example EIC)
- 4D tracking

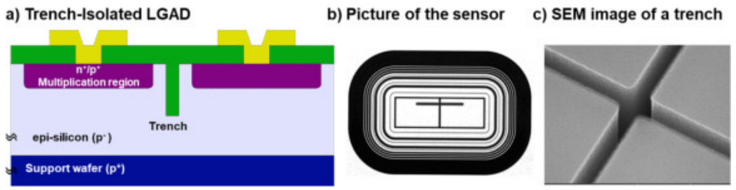
## An excellent solution to match these requirements is given by LGAD

Very intense activity on LGAD in the sensor community in the last 5 years

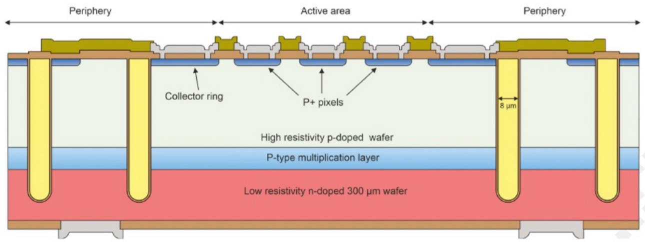
Improve layout by suppressing Junction Terminations



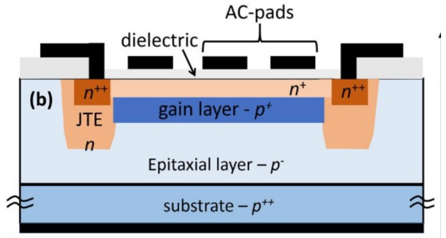

Need to suppress JTEs




Trench isolated LGAD



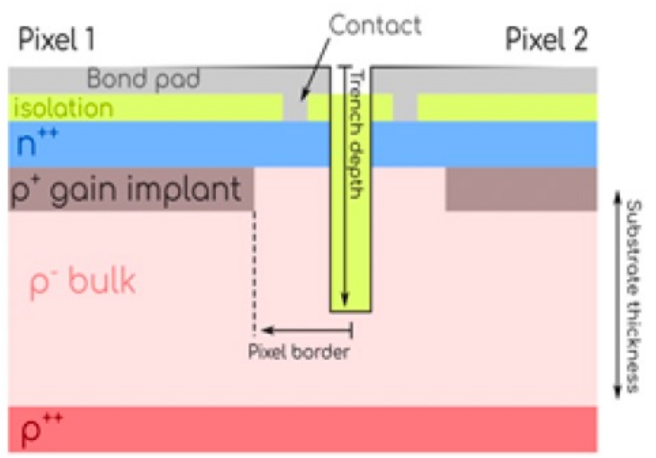

Inverted LGAD




AC LGAD

Improve radiation hardness with carbon or compensating implantations

# Our project in DRD3/WP2

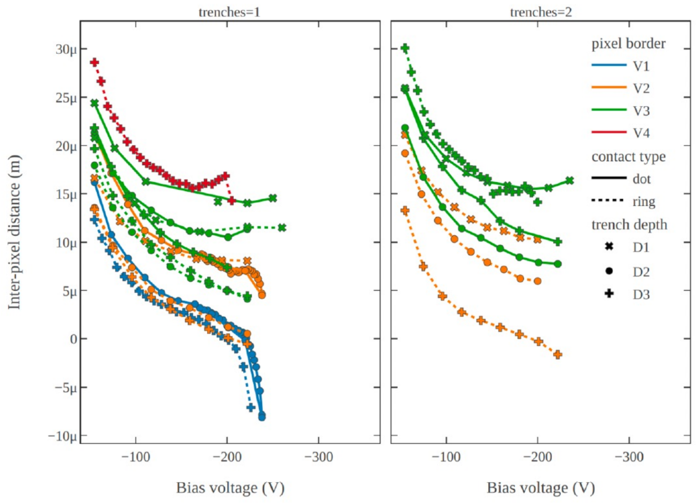



## Work on improvement of present TI LGAD designs

Start from two existing TI-LGAD production (RD50 and AIDAInnova) and complete the characterization
Proceed at one or two new submissions based on results, with optimized pixel layout, trench depth and carbon implantation

## Main axes:

- Study the possible parameter of carbon implantation and optimize the radiation hardness to $5x10^{15}$ $n_{eq}$/cm2
- Achieve an Inter-Pixel distance of a few microns (<5 µm) before and after irradiation, through an optimization of the design and of the process
- Ensure a good yield for sensor structures compatible with read-out chips of a few $cm^2$ and pitches of the order of 50×50 $µm^2$
- Achieve a time resolution per hit around 30-40 ps




- Prototype sensors for upgrades of the **ATLAS HGTD** and possible upgrade of the **CMS TEPX** with 4D pixels, interest for **very forward proton detectors close to ATLAS and CMS**
- Explore the feasibility of implementing TI-LGAD sensors for TOF and particle identification in the **outer layers of trackers for experiments at FCC-ee**.

# Participants in the project

| Institute | Contact | Main areas of contribution |
|---|---|---|
| National Technical University of Athens (NTUA) | I. Kopsalis | Testing M1, M4, M6 |
| University of California (UCSC) | S. Mazza | Testing M1, M5, M7 |
| CERN | D. Dannheim | Hybridization M5, M7 |
| CSIC | I. Vila | Testing M1, M5, M7 |
| FBK | M. Boscardin | Production, simulations D1, D2 |
| GSI Darmstadt | J. Pietraszko | Characterization, exchange of samples from a dedicated strip TI-LGAD production M5, M7 |
| Hamburg University | J. Schwandt | Testing, simulations M1, M2, M5, M7 |
| IJCLAB | A.Torrento | Testing M5, M7 |
| IPE KIT | M. Caselle | Testing, Hybridization, Photonics applications M5, M7 |
| JSI Ljubljana | G. Kramberger | Testing, irradiations, M5, M7 |
| LIP Lisbon | J. J. Hollar | Testing, irradiations, simulations M1, M5, M7 |
| LPNHE Paris | G. Calderini | Testing, Hybridization with ACF/ACP M5, M7 |
| University of Montenegro | G. Medin | Testing M1, M5, M7 |
| ORNL | M. Benoit | Testing, Hybridization, Irradiation M5, M7, D1 |
| National Accelerator Center, Seville | Mª Carmen Jiménez Ramos | Ion Beam characterization M5, M7 |
| Torino University | V. Sola | Simulations, Testing M1, M5, M7 |
| Zurich University | A. Macchiolo | Testing, DAQ M1, M5, M7 |

# Project structure

**Project Work Package 1: Simulations and processing**
Task 1: Sensor Optimization / TCAD simulations (collaboration with WG4)

Task 2: Processing at FBK of consecutive productions

Task 3: Physics Performance / Geometry Optimization

**Project Work Package 2: Data acquisition and feedback to ASIC designer (collaboration with DRD7)**
Task 1: Development of PCB boards to read-out test-structures / Read-out systems for timing chips

Task 2: Collection of requirements from the sensor side for the design of ASIC in 28 nm; link with DRD7 activities

**Project Work Package 3: Testing & Characterization**
Task 1: Characterization of the sensors in the lab with TCT and radioactive sources

Task 2:Testing of the sensors with beam tests, to derive spatial and timing resolution before and after irradiation

**Project Work Package 4: Irradiations**
Task 1: Organization of irradiations (protons and neutrons) of the two TI-LGAD productions

**Project Work Package 5: Hybridization**
Task 1: Organization of hybridization for the two TI-LGADs production

# Milestones / Deliverables

| Number | Deliverable/Milestone Title | WP project # | Lead | Type | Dissemination Level | Due Date |
|---|---|---|---|---|---|---|
| M1 | Report on radiation hardness studies of TI-LGAD structures from RD50 (no-carbon) and AIDAinnova runs (w/ carbon) | 3 | Santander, Ljubljana? | Report | DRD3 report | Month 12 (Q4 2025) |
| M2 | Comparison of observed performance with TCAD simulations | 1, 3 | UHH, Torino | Report | DRD3 report | Month 18 (Q2 2026) |
| M3 | Design of the first TI-LGAD production within DRD3 | 1 | FBK | Layout | DRD3 report | Month 12 (Q4 2025) |
| D1 | First production of small area TI-LGAD structures, to optimize radiation hardness, timing and yield | 1 | FBK | Prototype | Publication | Month 18 (Q2 2026) |
| M4 | Design and production of a multi-pad PCB board for the read-out of LGAD test-structures | 2,3 | KIT | Board | DRD3 report | Month 18 (Q2 2026) |
| M5 | Characterization of the devices of first production before and after irradiation | 3,4,5 | UZH, Torino | Report | Publications/ DRD3 report | Month 30 (Q2 2027) |
| M6 | Design of second production of TI-LGAD structures compatible with full scale timing ASICS. | 1 | FBK | Layout | DRD3 report | Month 36 (Q4 2027) |
| D2 | Second production of larger area TI-LGAD structures, compatible with full scale ASICs | 1 | FBK | Prototype | Publication | Month 42 (Q2 2028) |
| M7 | Characterization of the devices of first production before and after irradiation | 3,4,5 | LPNHE / IJCLab (proposed; subject to Review) | Report | Publications/ DRD3 report | Month 48 (Q4 2028) |

# Personnel in France

| Person | | FTEs (total months) |
|---|---|---|
| **LPNHE** | | |
| G. Calderini | DR | 4 |
| R. Camacho | CR | 4 |
| Non-permanent (AIDA) | Post-doc | 6 |
| F. Crescioli | IR | 4 |
| **IJCLab** | | |
| A. Torrento | IR | 6 |
| … | | |
| | | |

Premiere estimation des demandes budgetaires (à definer mieux dans la suite)

In total, over the experiment (2025-2027)

~ 20K contribution to productions + 10K hybridization

~ 5K small equipment

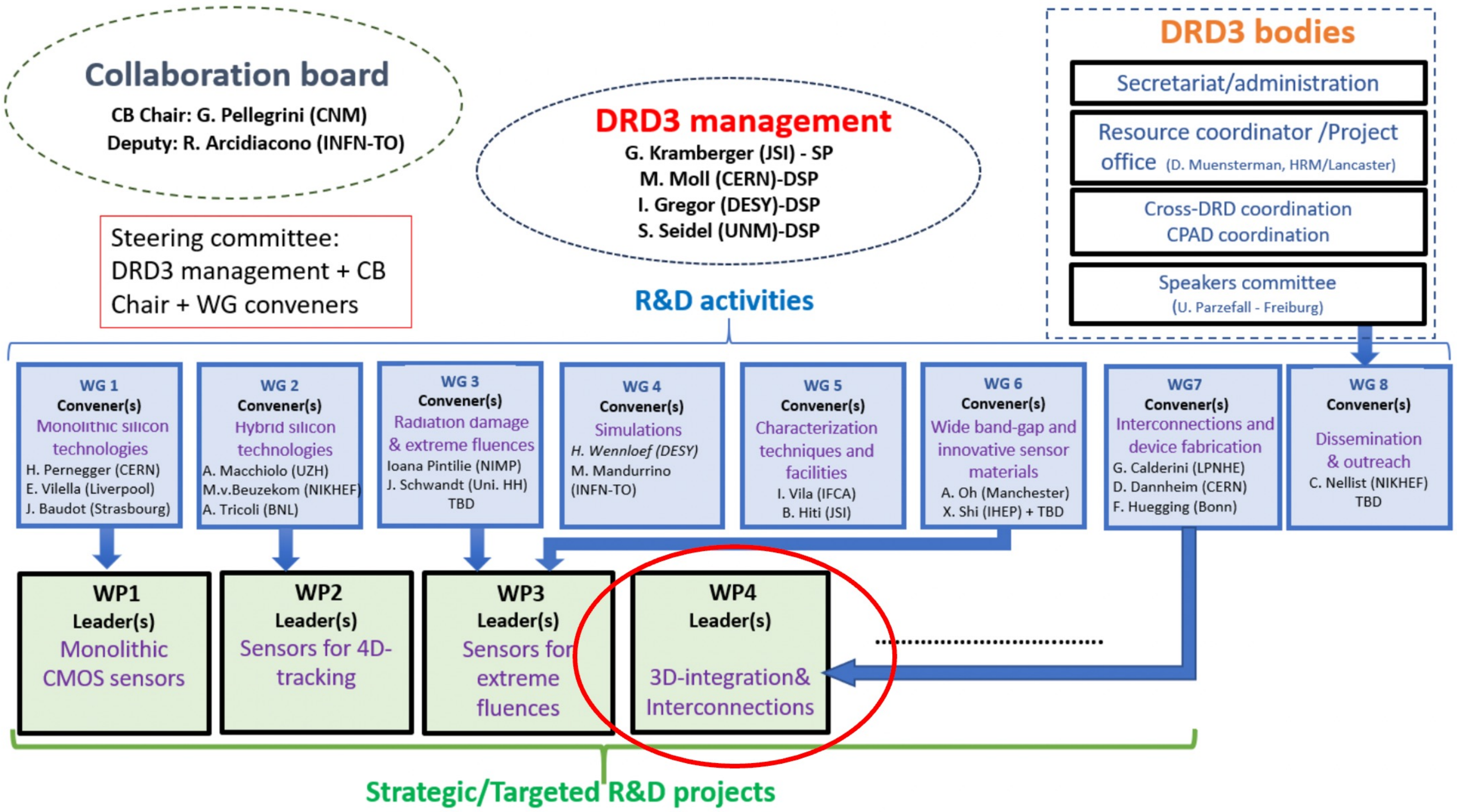
~ 5K consommables

~ 6K missions (2025-27)

# In-house plating, hybridization and module integration technologies for pixel detectors

Project in DRD3/WP4

# DRD3 WP4: Interconnections technologies




One of the four ECFA strategic axes for solid state detectors, translated in the 4 WP of DRD3

# DRD3 WP4: Context for interconnections

Need to provide fast, cheap and reliable interconnection technology (pixel die-to-die but also die-to-flex)

This will boost the R&D in laboratories

Advantages:

- Single die processing
- Adaptable to the application
- Low temperature process
- Maskless
- In-house (short turnaround time, quick adjustments)
- Cheap

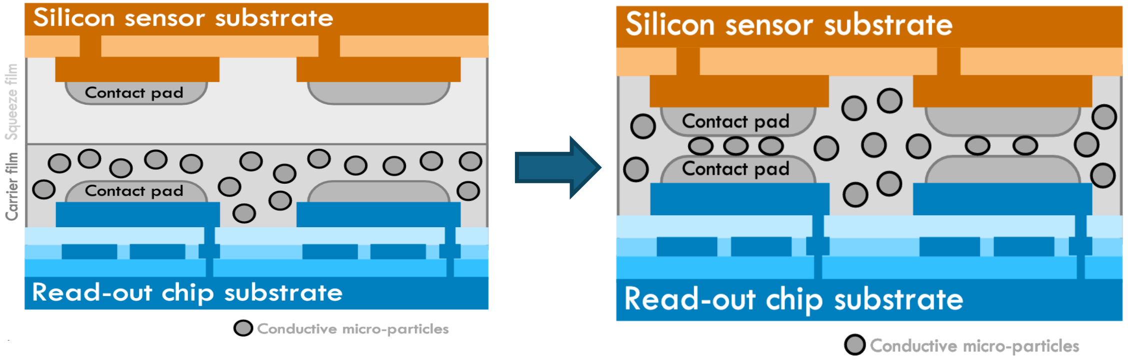
Some possible solutions

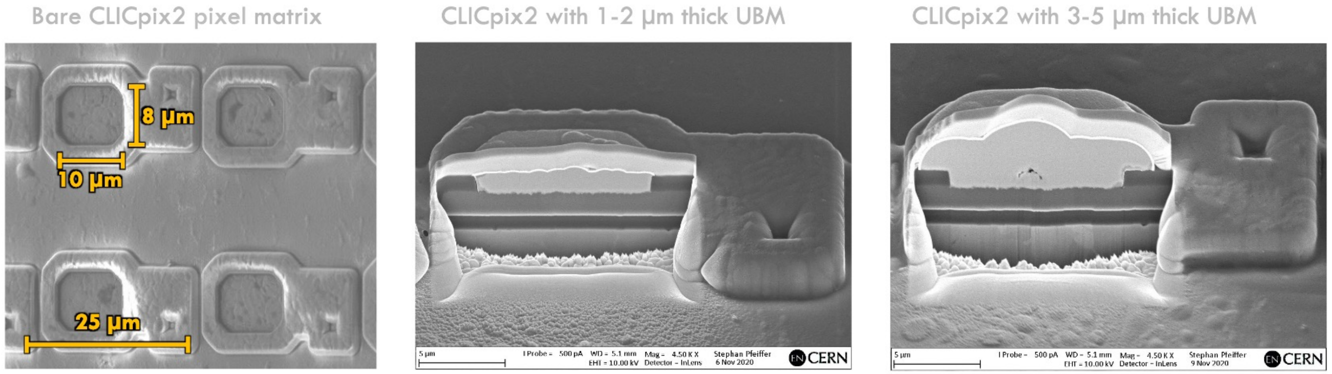
- Use of Anisotropic Conductive Films (ACF) or Pastes (ACP)

  UBM is still required to obtain the particle adhesion, but it is a wet chemical deposition of Ni and Au (maskless process, low cost)
- Interconnection via gold stud deposition

# ACF/ACP

## Existing activity to use ACF/ACP in the framework of AIDAInnova (and now DRD3 project)




See: P. Svihra,
https://indico.cern.ch/event/1104064/contributions/4789884/attachments/2416826/4135907/svihra_AIDA2022_ACF_update.pdf
or A. Lale et al. "Pixel detector hybridization with anisotropic conductive adhesives" PIXEL 2024, Strasbourg, 18-22/11/2024
https://indico.in2p3.fr/event/32425/contributions/142775/

In-house post-processing of devices: Nickel-Gold (ENIG), mask-less

Deposition of epoxy film or compound with small (3-5µm) conductive particles

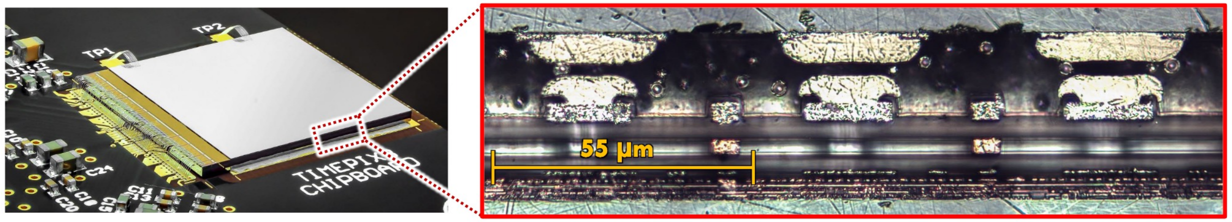
Film or paste produced by company; can be optimized depending on the device

Thermo-compression: 150C, 500N/cm2

Being demonstrated in AIDAInnova but only preliminary results

Need full process optimization and validation in real conditions

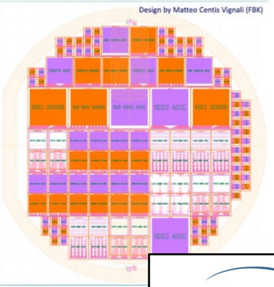
(mechanical and thermal stress, radiation hardness)

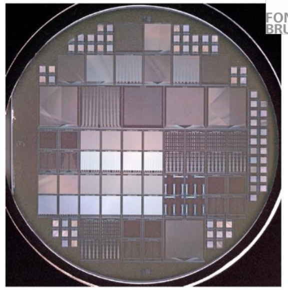


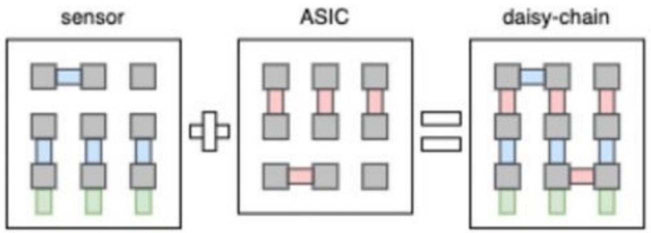
# Characterisation tools

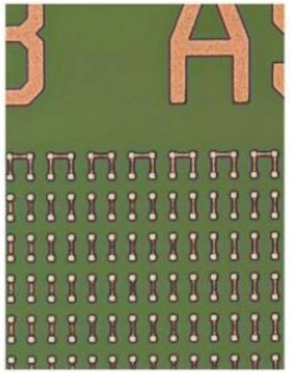
## Yield optimization depending on device characteristics (pixel pitch, device size etc)

Wafer layout with different sensor types has been designed at LPNHE in collaboration with FBK which then produced it; system of conductive chains to measure the interconnection reliability and yield

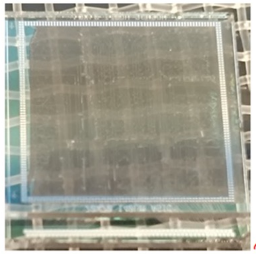


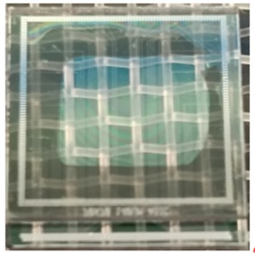


| | pitch | size in mm | connections | per wafer | type |
|---|---|---|---|---|---|
| 160x160 20um | 20 um | 3.2 x 3.2 | 25600 | 36 | grid |
| CLICpix2 | 25 um | 3.2 x 3.2 | 16384 | 34 | grid |
| 400x400 25um | 25 um | 20 x 20 | 640000 | 5 | grid |
| Timepix3 | 55 um | 14 x 14 | 65536 | 4 | grid |
| Timepix3 islands | 55 um | 14 x 14 | 65536 | 4 | grid |
| RD53 | 50 um | 20 x 20 | 160000 | 4 | grid |
| RD53 islands | 50 um | 20 x 20 | 160000 | 2 | grid |
| 70x70 140um | 140 um | 20 x 20 | 2112 | 3 | peripheral |
| 10x10 1000um | 1000 um | 20 x 20 | 400 | 3 | grid |
| 3x3 4500um | 4500 um | 20 x 20 | 36 | 1 | grid |



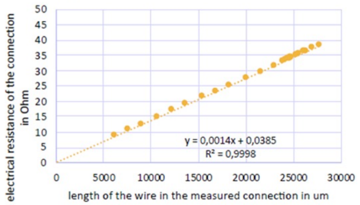
3 µm particles



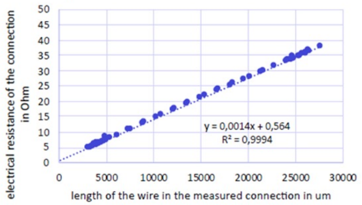
3 µm particles


4 µm particles

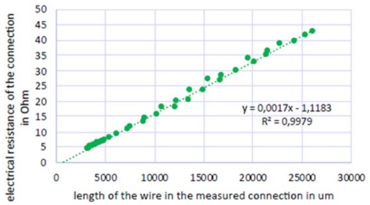
18 µm ACF – resistance measurement




14 µm ACF – resistance measurement




ACP – resistance measurement



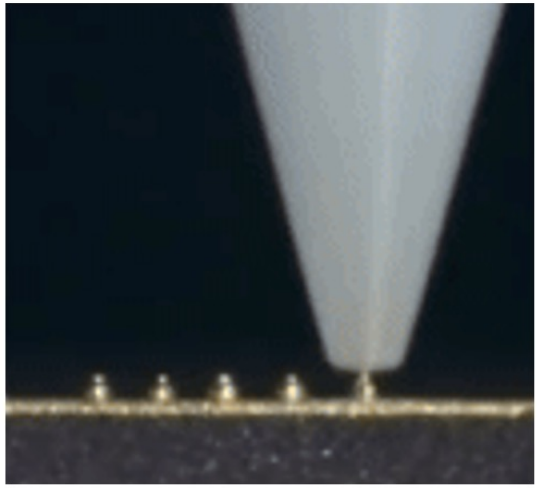

Preliminary measurements on the very first prototypes indicate very good conductivity (connection resistance <1 Ohm ) and yield between 98 and 99%

To be studied more systematically

# Gold stud hybridization test

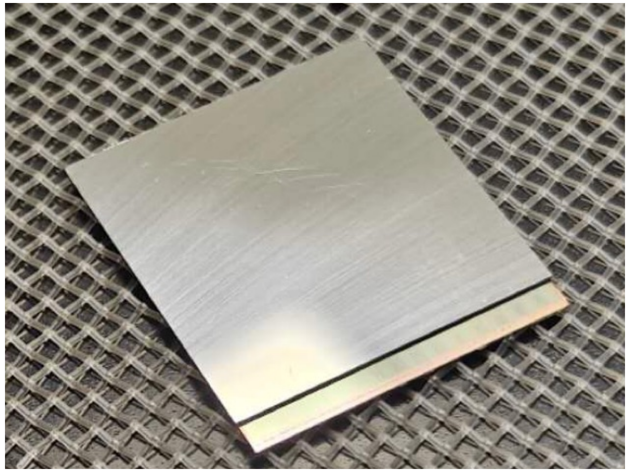
## ALTIROC3/A and LGAD sensors from ATLAS High Granularity Timing Detector (HGTD)

- Single and stacked double gold studs used for the connections between the chips, epoxy underfill for bonding

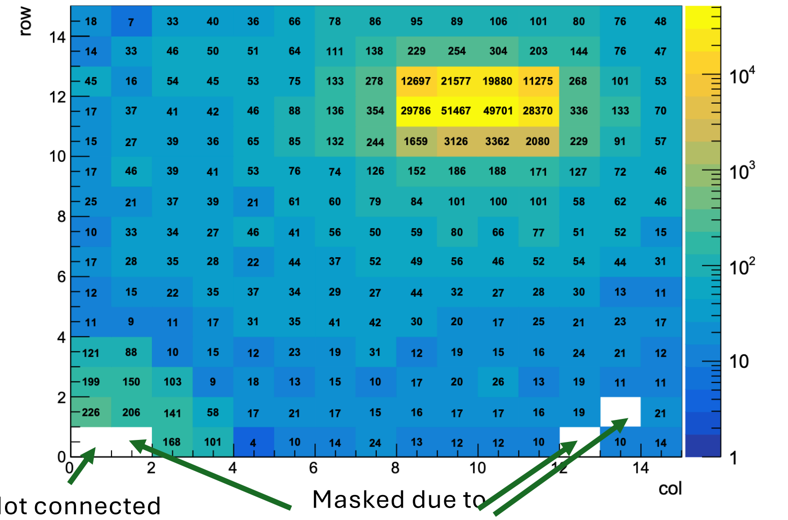


Gold studs are deposited one by one

ALTIROC/LGAD Hybrid
Flip-chip done with NCP (Araldite 2011)

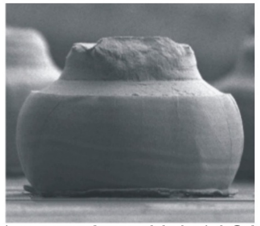


Test-beam occupancy map of ALTIROC with double gold studs + irradiated LGAD sensor



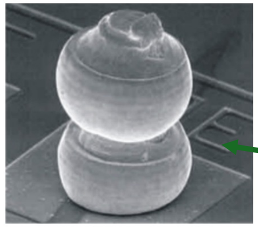

Confirmation of good inter-connection with occupancy map (≈ 100%)

Gold stud



Pictures from Hybrid SA

Stacked Gold studs



Preferred this solution to increase the gap between ASIC and sensor from 20 μm to 35 μm and thereby decrease coupling between them

- High connection yield, reproducibility, low temperature process
- Only for large pitch (>100μm), large pads (>80μm) chips

# Our project in DRD3/WP4

This project targets the development of scalable and cost-effective in-house plating, hybridisation and module-integration technologies. The main development objectives in the different technology areas are:

- Development of an in-house Ni/Au plating process suitable for single dies and a wide range of interconnect pitches (25 microns to several mm) and interface topologies
- Development of very thin hybrid pixel modules using alternative in-house interconnection technologies such as Anisotropic Conductive Films (ACF) or Pastes (ACP), nanowires, solder-jet printing, gold-stud bonding;
- Study of die-to-die 3D interconnection techniques to achieve highly integrated modules, using RDLs (Redistribution Layers) and other enabling interconnection techniques such as mentioned above; validation in a first phase for general R&D and demonstrator-module building using monolithic chips or hybrid assemblies from the participating sensor and ASIC R&D projects;
- Integration of modules for hybrid and CMOS pixel detectors for low mass large-area detectors; studies to combine electrical and mechanical connections to achieve a compact module layout; studies to integrate optical data transmission using existing developments from collaborating projects;
- Characterization of produced test devices in terms of interconnect yield and quality: mechanical (cross sections) and functional (radioactive sources, particle beams) tests.
- Reliability testing of produced test devices: accelerated ageing / thermal cycling, radiation hardness; mechanical (delamination) and functional tests.

# Participants

| Institute | Contact | Main areas of contribution |
|---|---|---|
| LPNHE Paris | G. Calderini | Testing, development of test devices |
| FBK Trento | M. Boscardin | Development of test devices, hybridisation, flex developments |
| CERN | D. Dannheim | Plating, hybridisation, module integration, flex developments, testing |
| University of Geneva | M. Vicente | Hybridisation, module integration |

(CONPART, Norway, partner commercial)

(everybody interested is welcome to join!)

# Project structure

## Project Work Package 1: Plating

- Task 1: ENIG plating for different test chain devices and process optimisation for different pitches, pad sizes and matrix areas
- Task 2: ENIG plating for functional sensor, ASIC and PCB samples from the collaborating projects

## Project Work Package 2: Hybridisation

- Task 1: Evaluation of different hybridisation processes using chain devices
- Task 2: Hybridisation of functional samples from different projects
- Task 3: Design and production of dedicated chain devices for plating and interconnect tests

## Project Work Package 3: Module integration

- Task 1: Demonstration of flip-chip module integration with suitable ASICs and test boards
- Task 2: Development of flex-PCB for multi-chip module integration demonstrator
- Task 3: Integration of silicon photonics integrated circuits from collaborating projects to build demonstrator modules and study their integration

## Project Work Package 4: Testing

- Task 1: Electrical and functional testing of produced chain devices, functional hybrids and module demonstrators
- Task 2: Thermal-cycling and mechanical robustness studies with chain devices, functional hybrids and module demonstrators
- Task 3: Radiation-hardness testing of functional hybrids and module demonstrators

# Milestones / Deliverables

| Number | Deliverable/Milestone Title | Project WP # | Lead | Type | Dissemination Level | Due Date |
|---|---|---|---|---|---|---|
| M1 | Characterisation of existing interconnect-test devices | 4 | LPNHE, CERN | Report | DRD3 report or publication | Month (Q2 2025) |
| D1 | New interconnect test devices produced | 1, 2 | FBK, LPNHE | Prototype | DRD3 report or publication | Month 30 (Q2 2026) |
| D2 | Optimised plating process developed | 1 | CERN | Report | DRD3 report or publication | Month 48 (Q4 2026) |
| M2 | Characterisation of assemblies with new interconnect-test devices | 2, 4 | LPNHE, CERN | Report | DRD3 report or publication | Month 42 (Q3 2027) |
| D3 | Single-die hybridisation process developed | 2 | UNIGE, CERN | Report | DRD3 report or publication | Month 48 (Q4 2027) |
| D4 | Module flex developed | 3 | CERN, FBK | Prototype | DRD3 report or publication | Month 48 (Q4 2027) |
| D5 | Reliability testing | 4 | LPNHE, CERN | Report | DRD3 report or publication | Month 48 (Q4 2027) |

# Personnel

| Person | | FTEs (total months) |
|---|---|---|
| **LPNHE** | | |
| G. Calderini | DR | 4 |
| B. Laforge | PR | 4 |
| Non-permanent (AIDA) | Post-doc | 6 |
| F. Crescioli | IR | 4 |
| N. Garroum | IR | 4 |
| Y. Orain | AI | 4 |

Premiere estimation des demandes budgetaires (à definer mieux dans la suite)

In total, over the full experiment (2025-2027, and considering some tens of KE from AIDAInnova in 2025)

~ 12K contribution ACF/ACP
~ 5K small equipment
~ 6K consummables
~ 9K testbeams/irradiations
~ 6K missions (2025-27)

# Next steps for the two projects

- Finalization of participants' names and contributions
- Update of Fiches Projet with the common template
  (almost finished)
- Consolidation of synergies with other DRD projects