R&D on Monolithic CMOS sensors and DRD3 projects

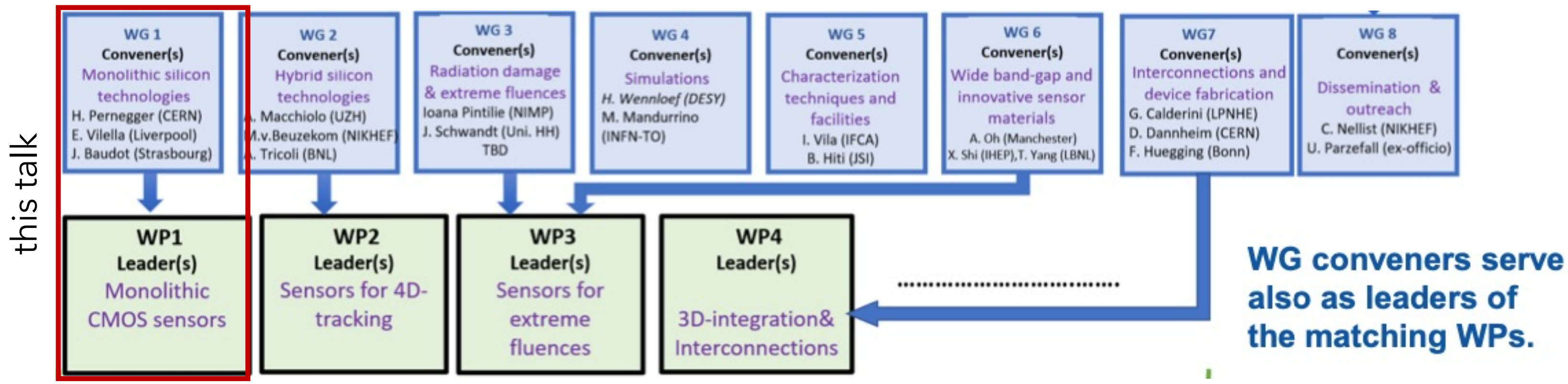
Workshop DI2I, March 4 – 2025

A. Besson (IPHC), M. Barbero (CPPM), M. Bomben (APC), G. Calderini (LPNHE), D. Contardo (IP2I)

Contributions to DRD3 WP1 – overview

- Participating institutes: APC, CPPM, IPHC, IPI2I, LPNHE
- Responsibilities in DRD3 (solid state detectors) and related in DRD7 (electronics)
  - J. Baudot co-convener of WG1//WP1 « Monolithic CMOS »
  - J. Baudot member of the DRD7 steering committee (elected)

  } ensuring good interface between DRD3 & DRD7
  - G. Calderini co-convener of WP4/WG7 « Interconnection »
  - M. Barbero co-convener of DRD7 WP6 « Complex imaging ASICs and technologies »
- Scientific contributions target the FCC-ee project
  - ➢ 4 projects in WP1 on MCMOS for Vertex Detector, Tracking and Particle Identification layers
  - ➢ Technology TPSCo 65 nm



DRD3 Work Packages* and Working Grourps organization

Contributions to DRD3 – overview continued

- Projects are spanning DRD3 and DRD7
  - DRD3 WP1 developing the sensors and readout architectures
  - DRD7 WP2 « Virtual Electronic System Prototyping » modelling from particle interaction to digital readout, WP3 « 4D and 5D techniques » preparing shared IP blocks, WP6 « complex imaging ASICs and technologies » providing access to foundries (PDK)*, design and characterization methodologies, investigating 3D interconnection techniques (see M. Barbero)
  - ➢ The present projects cover a 1st DRD phase of ≃ 3 - 4 years (approved by the CERN Research Board)
    - Technologies evaluation that should collapse in a 2nd phase to more specific processes and designs, possibly implementing new techniques brought by DRD7
- Status of preparation of MoU resource agreements (personnel and finding allocated to WPs**)
  - DRD3 still preparing list of deliverables, expected to converge by end of March
    - assumed to be formulated in foundry submissions (where the funding will go)
  - DRD7 collecting initial proposal for resources (see M. Barbero)
  - Ongoing discussion between DRDs/FAs/CERN management on fees/Common Fund

* C4PI IPHC provides community access to TJ 180nm Multi Project Runs, this is part of GRAM and DRD7 WP6 (see M. Barbero)

*** WPs contain the deliverables with allocated resources (subject to MoUs), matériel (components/systems), modelling and/or characterization tools available to the community, design simulations & characterization of components/systems; not include in MoUs local equipment & running budgets*

Contribution to DRD3 WP1 - « Octopus »

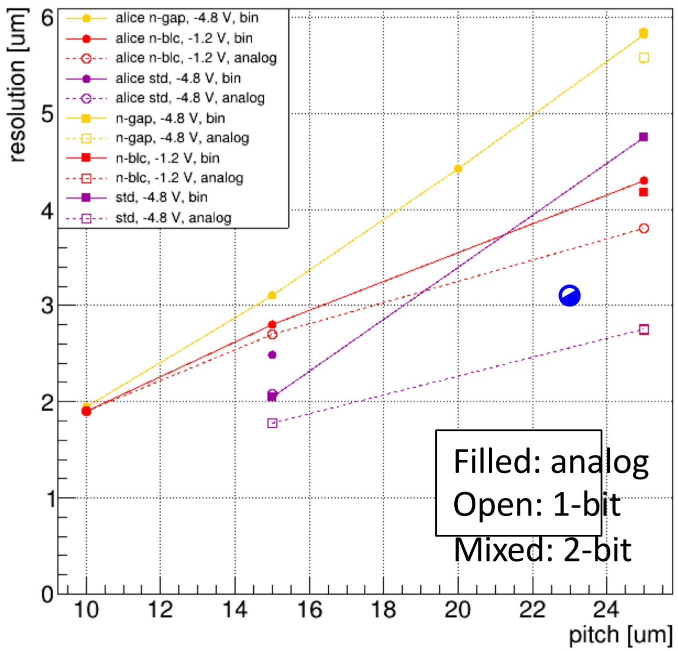
D. Dannheim S. Spannagel

APC, Bonn Uni., CERN, CPPM, DESY, ETH, FNSPE, GSI, HEPHY, IPHC, Oxford Uni. Zurich Uni.*

Goal to develop « Optimized CMOS Technology fOr Precision in Ultra-thin Silicon »
for FCC-ee application - TJ TPSCo 65 nm process

Spatial resolution per layer	$\simeq 3$	μm
Pixel pitch	14-20	μm [1]
read-out time	$\simeq 500$	ns [2]
Power dissipation	$\simeq 20 - 50$	mW/cm^2
Sensor thickness	$40 - 50$	μm [3]
Safety factor on particle rate	3	[4]
Maximum Hit rate	75 / 25	MHz/cm^2 [5]
Maximum Hit rate	22.5×10^{-3} / 7.5×10^{-3}	$hits/mm^2/BX$ [5]
Assumed cluster multiplicity	5	
Fired pixel rate	375 / 125	MHz/cm^2 [5]
Fired pixel rate	0.33 / 0.11	$fired\ pixels/mm^2/BX$ [5]
Occupancy/pixel/read-out	3.45×10^{-3} / 1.15×10^{-3}	$/pixel/readout$ [5]
Ionising radiation (1^{st} layer)	30 / 10	$MRad/year$ [5] [6]
Corresponding Fluence	$\simeq 1.8 \times 10^{14}$ / 6×10^{13}	$n_{eq(1\ MeV)}/year$ [5] [7]

[1] Depending on charge sharing/encoding
[2] Compromise between power dissipation and pile-up at $\sqrt{s} = 91\ GeV$
[3] To allow bending
[4] due to beam background uncertainties estimates
[5] With / without safety factor
[6] assuming beam running 180 days/year, and average incident angle of $\simeq 70^o$.
[7] assuming NIEL factor of 5×10^{-2}

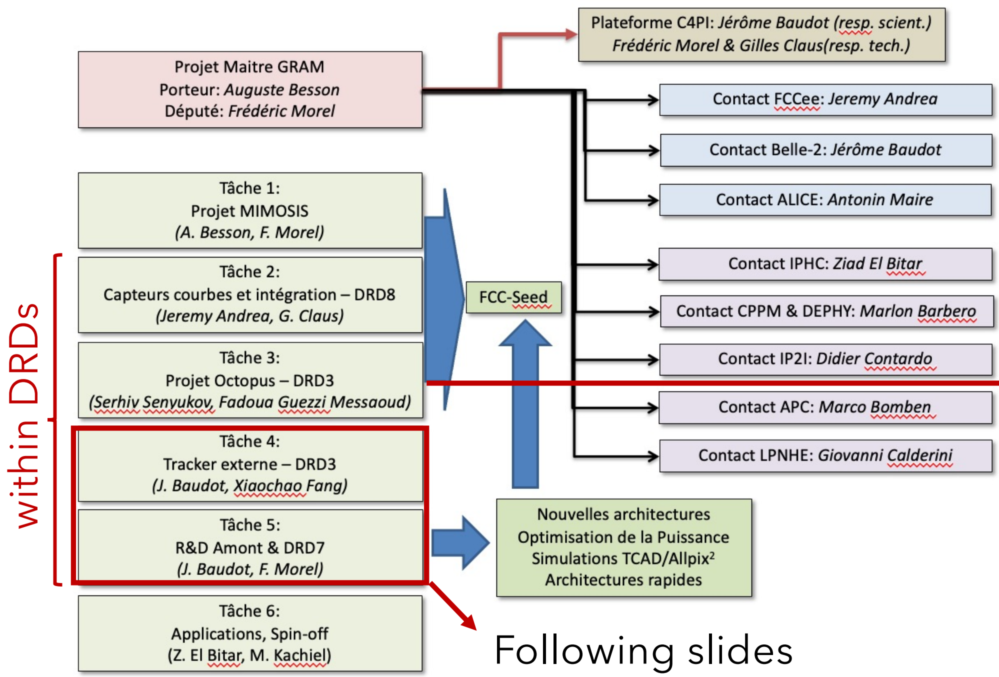


* IP2I and LPNHE considering possible contributions respectively to common aspect in redout architecture design and characterization of samples

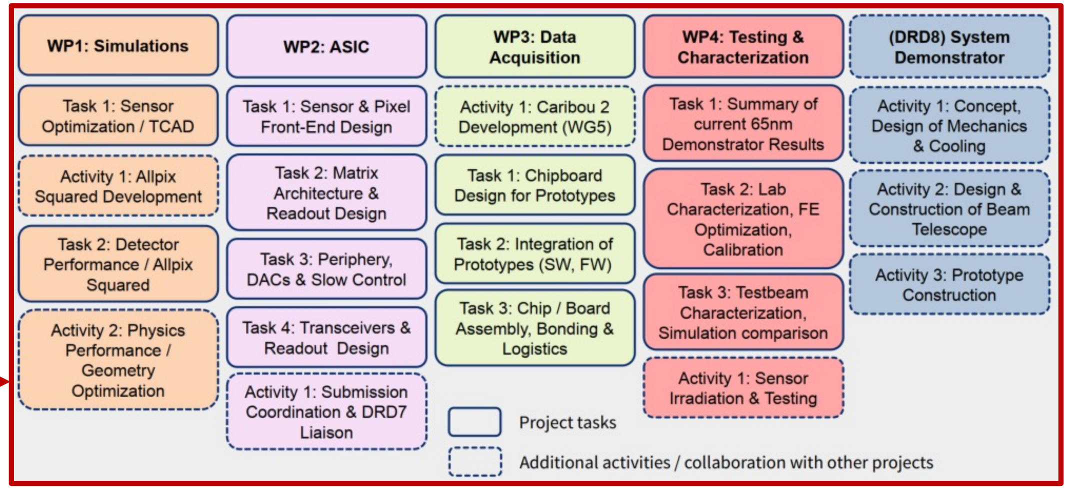
« Octopus » project description

application SEED EoI for Vertex Detector at FCC-ee

Master Projet GRAM (Auguste Besson)



Octopus Work Packages and tasks



Proposed leading commitments:

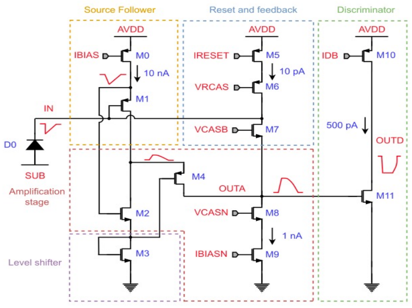
- WP2 ASIC design - conveners F. Guezzi. S. Senyukov
- WP4 Testing and Characterization

« Octopus » technical proposal

- Challenges
  - Accommodate high density for spatial resolution (small pitch) & read-out architecture footprint
  - Power optimization for gas flow cooling
  - Data flow / radiation tolerance not negligible at FCCee

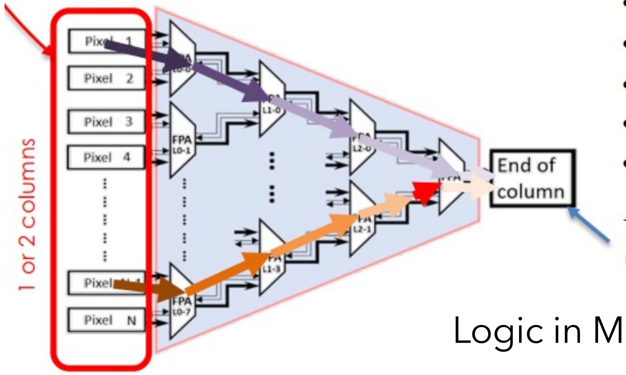
➢ Versatile architecture which can adapt to different data flows/time resolution/power consumption
  - Asynchronous readout: priority arbiters already explored by C4PI through SPARC
  - SPARC to be submitted in ER2 (ALICE ITS3 run imminent)

➢ Possibly decouple pitch & spatial resolution with charge encoding over few bits for charge sharing
  - Explored in CE_65 chips (PICSEL+C4PI and collab.)



DPTS FE as baseline
from ER1/ER2

Cascade of asynchronous arbiters



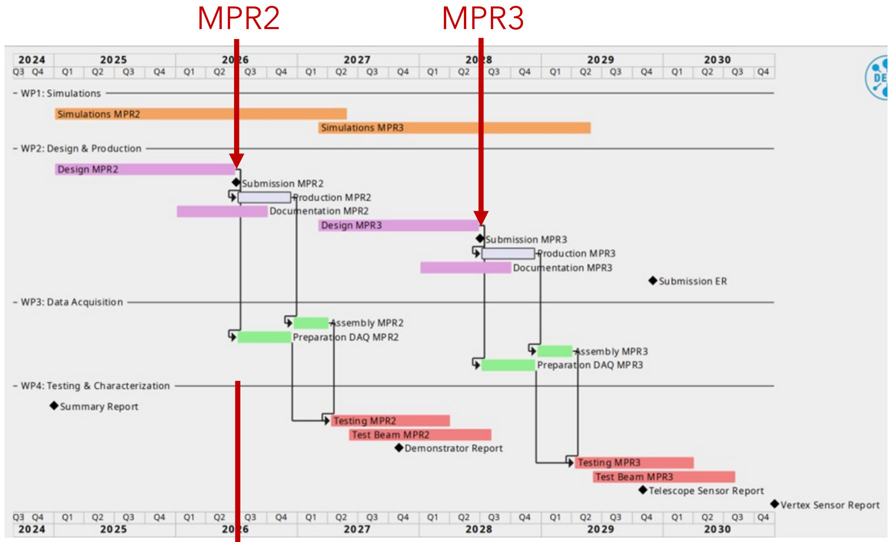
- Chiplet in ER2 (ALICE ITS3)
- 28 x 32 pixels / 1.5 x 1.5 mm²
- Pitch 24.1 x 16.0 µm²
- PhD thesis of Jean Soudier
- Design: IPHC, ICUBE, IRFU

Time-stamping here
(no clock in matrix)

Logic in Matrix ER2

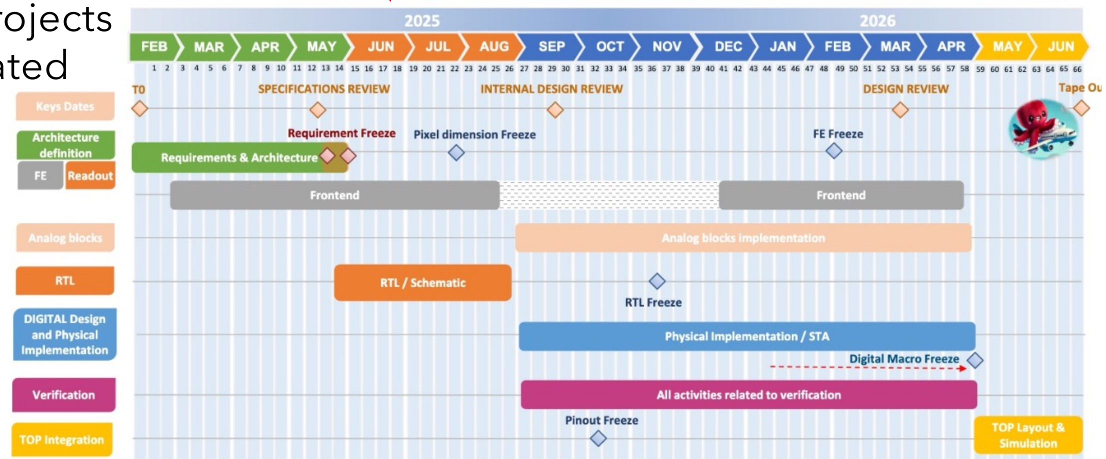
« Octopus » project planning

Number	Deliverable/Milestone Title	WP project #	Lead	Type	Dissemination Level	Due Date
M1	Report on Demonstrators	4	DESY	Report	DRD3 report	Month 9 (Q1 2025)
D1 **MPR2**	Beam Telescope Demonstrator Matrix Submission **3 µm**	1, 2	IPHC	Prototype	Manual / Presentation **Full column height**	Month 24 (Q2 2026)
M2	Report on Demonstrator Matrix Characterization	3, 4	DESY	Report	Publication	Month 36 (Q2 2027)
D2 **MPR3**	Full Beam Telescope Sensor Submission	2, 3	IPHC	Prototype	Manual / Presentation **≥ 2cm² sensor**	Month 48 (Q2 2028)
M3	Report on Beam Telescope Sensor Performance	3, 4	DESY	Report	Publication	Month 60 (Q2 2029)
D3 **ER**	LC Vertex Sensor Demonstrator Submission	1, 2	IPHC	Prototype	Manual / Presentation	Month 66 (Q4 2029)
M4	Report on LC Vertex Sensor Demonstrator Performance	3, 4	DESY	Report	Publication	Month 78 (Q4 2030)



MPR2 - MPR3 are common submissions to all projects
cycles of 18 months schedule to be consolidated
ER is part of 2nd phase of DRD3

WP2 MPR2 typical workflow for ASIC design
it aplies to other projects presented in this talk



« Octopus » project personnel

APC, CPPM, IPHC : ≃ 160(IT) + 30(Phy) ETP.mois (2027-2028) - ≃ 8 IT with significant involvement

Prénom Nom	Statut/Métier	expertise/compétence	Tâches dans le projet	ETP.mois 2025	ETP.mois 2026	ETP.mois 2027	ETP.mois 2028	ETP.mois total	DRD3_WP1_D1 ETP.mois (total)	DRD3_WP1_D2 ETP.mois (total)
J. Baudot	**PR**	coordination scientifique	**WP1**	**0,6**	**0,6**	**0,6**	**0,6**	**2,4**	**1,2**	**1,2**
A. Besson	**MCF**	coordination scientifique	**WP1**	**0,6**	**0,6**	**0,6**	**0,6**	**2,4**	**1,2**	**1,2**
M. Bomben	**MCF**	**simulations**	**WP1.2**	**0,6**	**0,6**	**0,6**	**0,6**	**2,4**	**1,2**	**1,2**
M. Barbero	PR	coordination scientifique	WP1	**0,6**	**0,6**	**0,6**	**0,6**	**2,4**	**1,2**	**1,2**
tbd/tbc	post-doc	analyses tests	WP1.3		**3**	**10**	**7**	**20**	**3**	**17**
total physiciens (FTE)				**2,4**	**5,4**	**12,4**	**9,4**	**29,6**	**7,8**	**21,8**
total physiciens (nb)				**5**	**5**	**5**	**5**			
Fadoua Guezzi	IR	ASIC desig, Responsable Technique, convener WP2 in octopus	WP1.1	10	10	10	10	**40**	**20**	**20**
Serhiy Senyukov	IR	Responsable Technique, convener WP2 in octopus	WP1.1, WP1.3	5	5	5	5	**20**	**10**	**10**
Frédéric Morel	IR	ASIC design, coord technique	WP1.1	1,2	1,2	1,2	1,2	**4,8**	**2,4**	**2,4**
Andrei Dorokhov	IR	ASIC design	WP1.1	4	4	4	4	**16**	**8**	**8**
Isabelle Valin	IR	ASIC design	WP1.1	3	4	4	4	**15**	**7**	**8**
Gregory Bertolone	IR	ASIC design	WP1.1	4	4	4	4	**16**	**8**	**8**
Liana Wassouf	IR	ASIC design	WP1.1	3	7	7	7	**24**	**10**	**14**
Olivier Clausse	AI	microtech.	WP1.3	0	0,05	0,1		**0,15**	**0,05**	**0,1**
Christophe Wabnitz	AI	microtech.	WP1.3	0	0,3	0,3		**0,6**	**0,3**	**0,3**
Gilles Claus	IR	test/caracterisation	WP1.3	0	0,75	0		**0,75**	**0,75**	**0**
Mathieu Goffe	IE	test/caracterisation	WP1.3	0	0,75	0		**0,75**	**0,75**	**0**
Kimmo Jaaskelainen	IE	test/caracterisation	WP1.3	0	0,75	0		**0,75**	**0,75**	**0**
Matthieu Specht	IE	test/caracterisation	WP1.3	0	3	0,75		**3,75**	**3**	**0,75**
Mohsine Menouni	IR	ASIC design	WP1.1	2	2	2		**6**	**4**	**2**
Pierre Barrillon	IR	test/caracterisation	WP1.3	1	1	1		**3**	**2**	**1**
D. Fougeron/P. Breugnon	IR	test/caracterisation	WP1.3	2	2	2		**6**	**4**	**2**
Patrick Pangaud	IR	ASIC design	WP1.1	1	1	1		**3**	2	1
total IT (FTE)				**36,2**	**46,8**	**42,35**	**35,2**	**160,55**	**83**	**77,55**
total IT (nb)				**12**	**12**	**12**	**12**	**12**	**12**	**12**

R&D « amont » IPHC - contributions to DRD7

on going activities, TCAD simulation, prospective for new developments, access to TJ 180 nm

IPHC : ≃ 60(IT) + ≃ 70(Phy) ETP.mois (2027-2028) strongly supported by PhDs

task	name	2024				2025				2026				2027				2028				total ETP (mois)
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	
Coordination scientifique	Jérôme Baudot	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	3
Coordination technique	Frédéric Morel	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	6
Coordination technique	Andrei Dorhokov	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	6
Coordination technique	Maciej Kachel	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	6
R & D amont	Andrei Dorhokov	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	3
	Luca Federici	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	6
	Hung Pham	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	6
	Abdelkader Himmi	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	6
	Rachid Sefri	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	6
PhD	Jean Soudier	100%	100%																			6
PhD	Elio Sacchetti	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%											30
PhD	Hasan Shamas	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%											30
fabrication (ER2)	Gregory Bertolone					10%																0,3
sparc microtec	Christophe Wabnitz								10%													0,3
PCB	Matthieu Specht							30%														0,9
test SPARC	Gilles Claus					10%	10%		10%													0,9
	Mathieu Goffe								30%													0,9
	Kimmo Jaaskelainen																					0
	Matthieu Specht					20%	20%		10%													1,5
	Willy Perrin					100%	100%		100%													9
TOTAL		380%	380%	280%	280%	420%	410%	310%	440%	280%	280%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	127,80

Contribution to DRD3 WP1
« A versatile pixel matrix in TPSCo 65 nm for future trackers »

J. Baudot
CPPM, Bergamo, GSI, Heidelberg, IFIC, IGFAE, IPHC, IP2I, IRFU, HEPHY, LPNHE, Munich, Pavia*

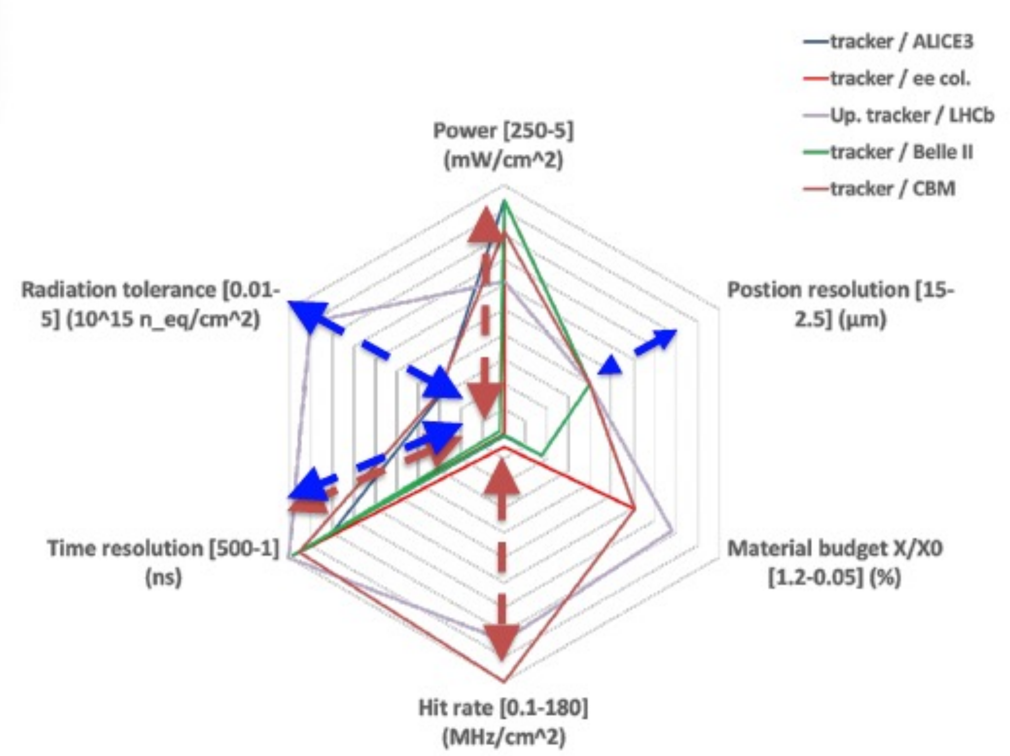
Goal to develop a readout architecture for tracking systems with configurability and ability to accommodate performance requirements of several applications

	ALICE3 OT	Belle II trk	CBM trk	LHCb UT	FCCee trk
Position resolution	~10 µm	<15 µm	~10 µm	<10 µm	<10 µm
Pixel pitch (µm)	50	50	~30	50	50
Hit rate (MHz/cm^2)	0.05 to 2	<1	60/180	160	<10
Data rate (Gb/s)			8	20	
Time figure (ns)	100	~1	25	~1 (<25)	20 to 1000
Triggering	no	yes	no	no	?
Power	~20	<50	~50	<100	~20?
TID (kGy)	50	10?	~10	2400	10?
NIEL	10^{14}	10^{11}?	few 10^{14}	3×10^{15}	10^{11}?

J. Baudot - Versatile pixel matrix in TPSCo 65 nm - Vertex detector discussion meeting - DRD3 week, 17-21 June 2024, CERN

* *Other potential interests in Japan and US*

« A versatile pixel matrix in TPSCo 65 nm for future trackers »
Project description : versatility/configurability



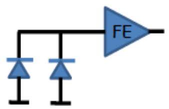
- **Fabrication process variants:**
  - Standard process: more q-sharing
  - Modified process: faster collection
- **Pixel front-end:**
  - Tunable main bias current: speed vs power
  - Two stages for pixel grouping:
    - excellent detection efficiency
    - power-saving

« A versatile pixel matrix in TPSCo 65 nm for future trackers » Technical proposal

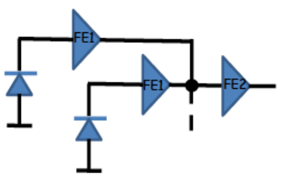
Front-End

- **Pixel grouping**
  - use front-end with two stages
    - Pre-amplify signals with FE1 for each diode
    - sum up N nodes into FE2 for discrimination
  - Analogue pixel power = n*FE1 + FE2
    - std situation = single FE with power P
    - assuming $P \sim P_{FE1} + P_{FE2} = P_1 (1 + P_2/P_1)$
    - power density with grouping = $P_{FE1} + P_{FE2}/N$
- **Status**
  - First ideas implemented in TJ 180 nm
  - In translation to TPSCo 65 nm

Standard situation

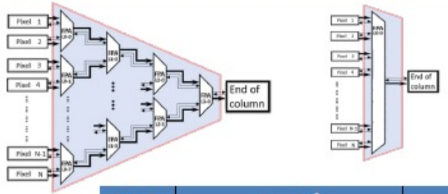


Pixel grouping



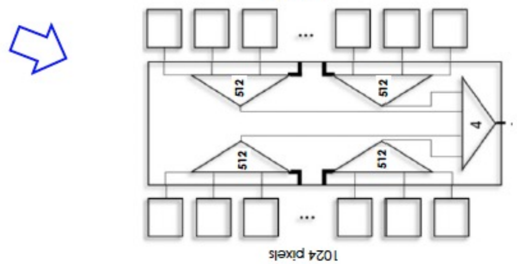
Digital architecture (same logic in matrix as in octopus)

- **Asynchronous logic**
  - cascade of N:1 arbiters
  - see Doi: 10.1016/j.nima.2024.169663
  - 1st prototype SPARC submitted in (ITS3-)ER2
  - timestamping 25-100 ns doable



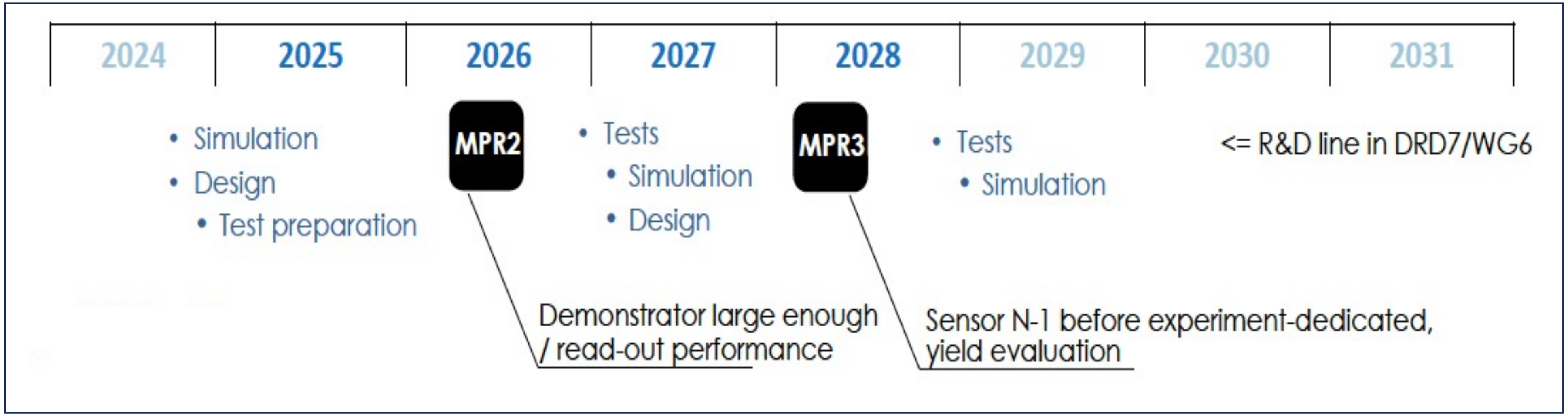
Controller size	1 MHz/cm² mean time	1 MHz/cm² 99.9% time	1 MHz/cm² digit. power	200 MHz/cm² mean time	200 MHz/cm² 99.9% time	200 MHz/cm² digit. power
2:1	20 ns	64 ns	3 mW/cm²	22 ns	65 ns	9 mW/cm²
512:1	15 ns	63 ns	1 mW/cm²	17 ns	> 100 ns	5 mW/cm²

- **Implementation for tracker sensor**
  - Assuming column length ~24 mm (reticule height) => 1024 pixels of 23.4 µm
  - Possible cascade for double-column
    - Mix 512:1 & 4:1 controllers
  - Possible prototype size
    - pitch 23.4 µm and one full functional region ~ 128 columns X 1024 rows ~ 0.3 x 2.4 cm2



« A versatile pixel matrix in TPSCo 65 nm for future trackers »
Project planning

MPR2 and MPR3 common timeline foreseen for submissions in TPSCo 65 nm
detailed task sharing to be developped with partners



« A versatile pixel matrix in TPSCo 65 nm for future trackers » project personnel

IPHC : ≃ 55(IT) + ≃ 10(Phy) ETP.mois (2027-2028)

task TRACKER	name	2024				2025				2026				2027				2028				total ETP (mois)
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	
Coordination scientifique	Jérôme Baudot	0%	0%	0%	5%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	4,95
Coordination technique	tbd				0%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	4,80
Coordination technique					0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0,00
design tracking	Xia Chao					50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	24,00
	Luca Federici					10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	4,80
	Andrei Dorokhov					10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	4,80
	Isabelle Valin					20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	9,60
fabrication (MPR2)	Gregory Bertolone											10%	10%									0,60
microtec.	Olivier Clausse													10%								0,30
	Christophe Wabnitz													10%								0,30
Tests	Mathieu Goffe													5%								0,15
	Matthieu Specht													5%								0,15
	Gilles Claus													5%								0,15
	Kimmo Jaaskelainen													5%								0,15
TOTAL		0%	0%	0%	5%	110%	110%	110%	110%	110%	110%	120%	120%	150%	110%	110%	110%	110%	110%	110%	110%	54,75

Contribution to DRD3 WP1
« A pixel matrix for tracking and timing »

D. Contardo

to be merged with « versatile pixel matrix » project

Goal to develop a readout architecture with both tracking and timing for Particle ID application at FCC-ee in tracker outer layer(s)* - possibly extending to intermediate radius

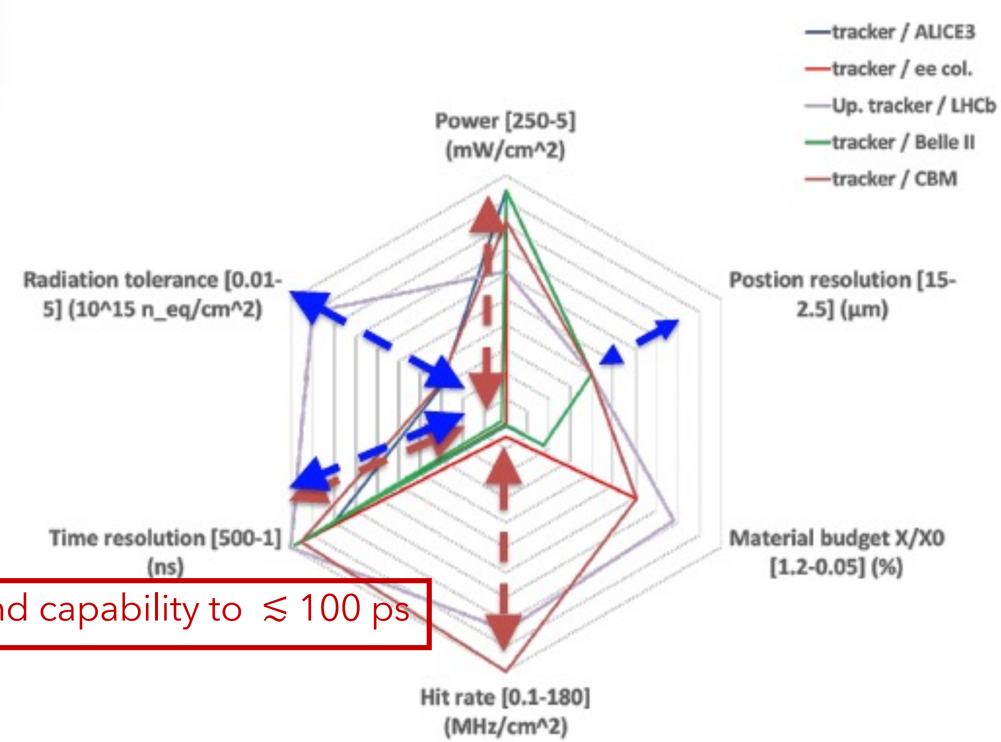
	ALICE3 OT	Belle II trk	CBM trk	LHCb UT	FCCee trk	FCCee TK/PID
Position resolution	~10 µm	<15 µm	~10 µm	<10 µm	<10 µm	≲ 10 µm
Pixel pitch (µm)	50	50	~30	50	50	25
Hit rate (MHz/cm^2)	0.05 to 2	<1	60/180	160	<10	< 0.5
Data rate (Gb/s)			8	20		
Time figure (ns)	100	~1	25	~1 (<25)	20 to 1000	≲100 ps
Triggering	no	yes	no	no	?	
Power	~20	<50	~50	<100	~20?	?
TID (kGy)	50	10?	~10	2400	10?	
NIEL	10^{14}	10^{11}?	few 10^{14}	$3x10^{15}$	10^{11}?	

low rates & reduced power (X/X_0) constraints at large radius

J. Baudot - Versatile pixel matrix in TPSCo 65 nm - Vertex detector discussion meeting - DRD3 week, 17-21 June 2024, CERN

* *Expression of Interest submitted to ESSP-2025 IP2I - CEA/IFRU, layers of PID could also be deployed in a Si/W electromagnetic calorimeter*

« A pixel matrix for tracking and timing »
Project description : extension of the « Versatile… » project



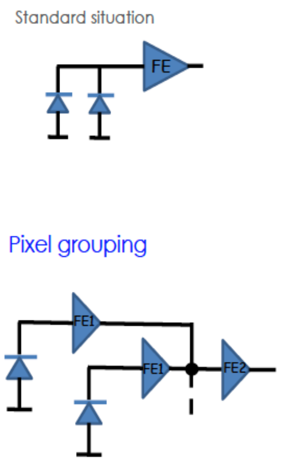
extend capability to $\lesssim$ 100 ps

- **Fabrication process variants:**
  - Standard process: more q-sharing
  - Modified process: faster collection
- **Pixel front-end:**
  - Tunable main bias current: speed vs power
  - Two stages for pixel grouping:
    - excellent detection efficiency
    - power-saving
- Pixel digital part
  - Implement precise TDC

« A pixel matrix for tracking and timing » Technical proposal

Front-End

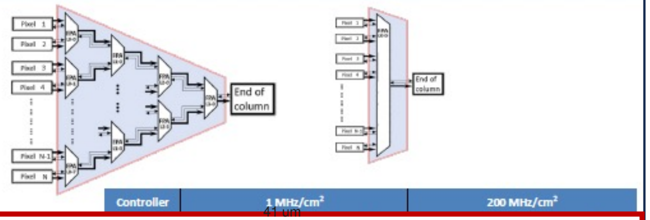
- **Pixel grouping**
  - use front-end with two stages
    - Pre-amplify signals with FE1 for each diode
    - sum up N nodes into FE2 for discrimination
  - Analogue pixel power = n*FE1 + FE2
    - std situation = single FE with power P
    - assuming $P \sim P_{FE1} + P_{FE2} = P_1 (1 + P_2/P_1)$
    - power density with grouping = $P_{FE1} + P_{FE2}/N$
- **Status**
  - First ideas implemented in TJ 180 nm
  - In translation to TPSCo 65 nm



consistent with timing goals

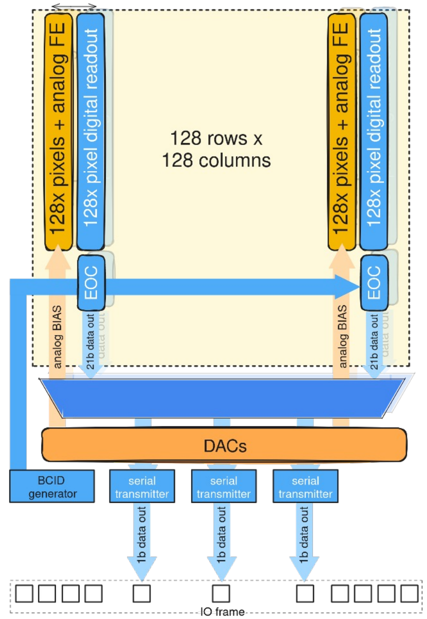
Digital

- **Asynchronous logic**
  - cascade of N:1 arbiters
  - see Doi: 10.1016/j.nima.2024.169663
  - 1st prototype SPARC submitted in (ITS3-)ER2
  - timestamping 25-100 ns doable



ex. DOTIIX TJ 180 nm IPHC –IP2I

- top-to-bottom priority column drain
- asynchronous readout at EoC
- ToT with 4b timestamp in pixel memory at Leading or Trailing Edge with 10b extension at the EoC level
- LE and TE timestamps are serialized in three 160 Mbps output links
- ➢ include TDC in matrix or at EoC
  - vernier ring oscillator/delay line
- ➢ cascade arbiters concept to be considered wrt timing precision



« A pixel matrix for tracking and timing » Project planning

to be merged with « versatile pixel matrix » project

- MPR2 1st high precision timing digital implementation in 128 x 128 pixel matrix
- MPR3 high precision demonstrator reticule size
  - implementing analog (sensor and FE) part with targeted timing performance*
  - ➢ CASSIA considered for analog part (see next slides)
  - ➢ CACTUS in LF150 nm (CEA IRFU, P. Schwemling) can also evolve to TPSCo 65 nm
  - power consumption optimization

➢ 2eme R&D phase (not covered in the FP)
  - large size demonstrator (« stitching » technique)
  - possibly 3D interconnexion - « Wafer Stacking »
  - other improved IP blocks through DRD7

Work Packages Tâches/livrables	Description	2025				2026				2027		
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
WP1	**Simulation**											
WP1.1	développement software collection de charge (Allpix2)											
WP1_D1	**performance variantes de configuration des électrodes**				★							
WP1.2	développement software numérisation signal aux conditions FCC-ee (Key4HEP)											
WP1_D2	**simulations évènements de physique, fichiers de données input électronique**				★							
WP2	**Architecture de lecture : PMaTT_V1 - démonstrateur numérique 128x128 pixels**											
WP2.1	choix de configurations d'électrodes[1)]											
WP2.2	choix de l'étage de prémplification - discriminitation[1)]											
WP2.3	étude/choix des blocs d'architecture numérique dans la matrice et péripherie											
WP2.4	description RTL de l'architecture numérique (System Verilog)											
WP2.5	routage/layout de composants numériques (DoT)											
WP2.6	développement banc test et validation description (RTL) et post-layout (UVM)											
WP2.7	assemblage "top level" des blocs analogiques et numériques, validation, fichiers GDS											
WP2_D1	**Soumission en fonderie : PMaTT_V1**							★				
WP3	**Caractérisation PMaTT_V1**											
WP3.1	conception cartes de test											
WP3.2	caractérisation électronique											
WP3.3	développement DAQ											
WP3.4	caractérisation avec source ou faisceaux , performance physique du senseur											
WP3_D1	**rapport/publication PMaTT_V1**								★		★	

* ≃ 70 ps intrinsic sensor resolution was reached in TPSCo first ER submissions, CASSIA and CACTUS aim to introduce gain below the electrodes to improve signal to noise ratio for improved timing resolution, development of fast FE with low power is another challenge

« A pixel matrix for tracking and timing » project personnel

IP2I : ≃ 128(IT) + ≃ 30(Phy) ETP.mois (2027-2028) - ≃ 4 IT with large involvement*

Prénom Nom	Statut/Métier	expertise/compétence	Tâches dans le projet	ETP.mois 2025	ETP.mois 2026	ETP.mois 2027	ETP.mois 2028	ETP.mois total	DRD3_WP1_Dl ETP.mois (total)	DRD7_WP6_Dz ETP.mois (total)
Gaelle Boudoul	CR	Simulation physiques	WP1.2	3	3	3	3	**12**		
Didier Contardo	DR	Responsable Scientifique		6	6			**12**	1,5	1,5
Jessy Daniel	Postdoc	Simulation physiques	WP1.2	6	6			**12**		
total physiciens				**15**	**15**	**3**	**3**	**36**	**1,5**	**1,5**
Luigi Caponetto	IR µ-élec.	Responsable Technique Concepteur ASIC	WP2.3, WP2.5, WP2.7, WP3.2, WP4.3, WP5.1	9	9	9	9	**36**	24	12
Benedetta Nodari	IR µ-élec.	Concepteur ASIC	WP2.6, WP3.2, WP4.3, WP5.1.	9	9	9	9	**36**	24	12
Mokrane Daoumane	IR µ-élec.	Concepteur ASIC	WP2.3, WP2.5, WP3.2 WP4.3, WP5.1	6	6	6	6	**24**	12	12
Xiushan Chen	IR eDAQ	Concepteur RTL	W2.4, WP3.2, WP4.3, WP5.1	6	6	6	6	**24**	24	
tbd	IE eDAQ	Concepteur PCB	WP3.1, WP5.1	2	2	2	2	**8**	8	
total IT				**32**	**32**	**32**	**32**	**128**	**92**	**36**

* *Approval process ongoing at IP2I*

Similar to « Octopus » joining effort with « versatile pixel matrix »
LPNHE considering to join by 2026, ≃ 2 x 20% (IT) + 10% (PHY) ETP
interest for characterization & asic design in relation with WP2

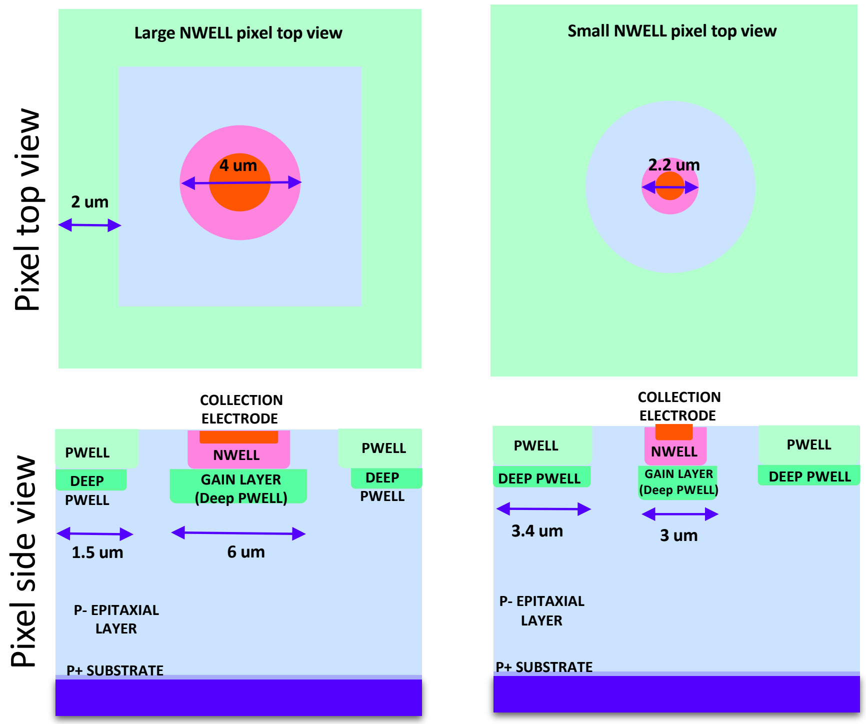
Contribution to DRD3 « CASSIA » goals

H. Pernegger (PI)
CERN, CPPM, GSI, IPHC, IIT Madras, KEK, Athens, Bonn, Glasgow, Kyushu, Tsukuba, Zagreb

Goal to develop process for implants providing internal gain for increased pixel density and/or reduced power dissipation, also enabling high precision timing ≲ 30 ps

Description – Technical proposal

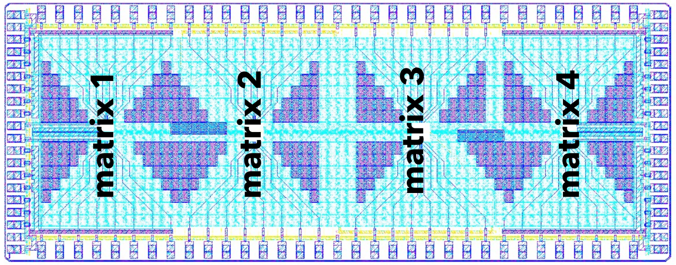
- Study depths and doping concentrations with different electrode configurations in TJ 180 nm
  - Thickness 18 μm
  - Pixel pitch 15 μm
  - DC and AC + Buffer output
- IPHC & CPPM contributions - ANR APICS 2024-2027
  - TCAD/Allpix2 simulation, sensor design, irradiation, characterization in lab and in beam



« CASSIA » Project planning and resources

Design tests in two TJ submissions in 3 years - upon success evolve to TPSCo 65 nm process

1st submission : 4 matrices, 22 x 33 pads



Matrix	Collection electrode	Gain layer	Circuit
1	Nwell, r=4um	deep Pwell	AC+BUF
2	Nwell, r=4um	deep Pwell	DC
3	Nwell, r=2.2um	p-diffusion	DC
4	Nwell, r=2.2um	p-diffusion	AC+BUF

2nd submission : 2 matrices with n-implants, optimized FE

Resources at IPHC from ANR 75 k€ : 1 PhD, submissions, test equipment

- CPPM 30% (IT) + 30% (PHY)
- IPHC 70% (IT) + 30% (PHY)

Overview of budget for MCMOS projects

- Budget outside of DRD MoUs
  - Equipment for tests : ≃ 20 k€ per year
    - PCB dedicated test cards and DAQ based on the CARIBOU DRD3 system ≃ 5 k€ x 4 institutes
  - Missions : ≃ 40 k€ per year (10 - 20 k€, # of participant/institutes, responsibilities)
    - DRD3 week, Working meetings, Test beams, Workshop and conferences
- Foundry 2 submissions ≃ 160 k€ (2025-2028) in DRD MoUs
  - Mutualized for all TPSCo 65nm projects ≃ 40 k€/year – eg 80 k€/submission

➢ More details in FPs, ventilation between DEPHY and GRAM to be defined

➢ Budget increase
  - New institutes (APC, IP2I) ≃ 20 k€/year, LPNHE not yet included*
  - TPSCo submissions 40 k€/year

** To be consolidated in relation with WP2 and WP4 activities*

Other requested information

- Inter-dependance within and across DRD3 and DRD7
  - foundry submissions are common to DRD3 and DRD7 for all projects - defining planning
  - access to technologies is provided by CERN through EPSE team / DRD7
  - ensuring sharing of experience and IPs is cross-cutting to DRD3 & DRD7
  - 3D interconnection is cross-cutting to DRD3 & DRD7 (could be a game changer in a 2^{nd} R&D phase)
- IP confidentiality
  - PDK access driven by foundry rules
  - IP bloc sharing is expected to be open to all participants
  - Discussion ongoing in MoU framework between CERN and Funding Agencies
- Risks are not specific to DRDs
  - contributors failing to deliver – re-orient task sharing, descope project
  - difficulties to meet international submission schedules – descope project towards next submission
  - performance target not achieved – re-orient technology choices
  - …

Outlook

- Projects are addressing DRD goals
  - performance expressed in ECFA Detector Development roadmap
  - strategic projects applications medium and longer term identified in ESPP-2020
  - approach is coherent in coherent to consider all technology performance parameters
  - commonalities in modelling and design of sensor analog and digital variants are considered
  - gathered IN2P3 competences cover all aspects (modelling/simulation, design, characterization…)
- FPs are being updated for the KDP1 review of Apr. 23-24
  - covering 1st R&D period of 3 – 4 years
    - ➢ participation in DRD3 are mostly in WPs (were resources are allocated)
  - will be grouped under the umbrellas of the DEPHY and GRAM MP
  - will include tables to match resources to tasks & deliverables within MP & DRDs
    - ➢ this may not yet reflect final sharing of work and resources from external contributors

➢ Medium term funding is expected to increase with new participants and TPSCo submissions
  - Comparison with current MP fundings no yet fully available
  - Possible fees/Common Fund in DRD3 10 k€/year (for 5 institutes)

➢ Ramp-up of funding can be anticipated through 2nd R&D phase toward large size) prototypes

➢ Continuous support for PostDocs/PhDs (part time) crucial for simulation and characterization