





# **Phase 2 Power Supply and Mechanics**

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# **Outline**

- Phase 2 Power Supply Status
  - Design review
  - Backplanes
- Phase 2 Mechanics Status
  - Design
- System Test
- Production status

# Phase 2 Power Supply





## V2 PSU Design

### **Features**

### Input

- 48V (3.1 A max), Isolated GND Outputs with isolated GND from input
- 3.3V (20 A) for Digiopt12
- 5 V (20 A) for PACE
- 3.3V (0.7 A) for PACE Boot and SC FPGAs
- 2.2 V (5A) for DigiOpt12
- 4 Temperature sensors (T1..T4)

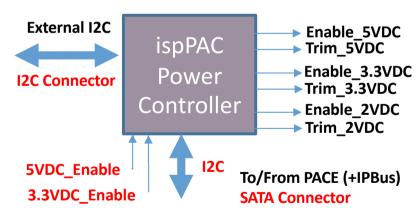
### **V2 PSU Dimensions**



90 x 65 mm<sup>2</sup>

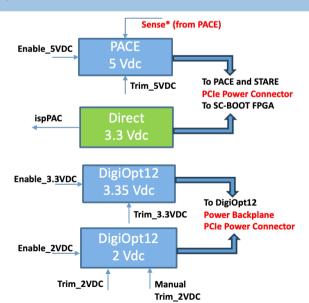
- 51% less than Ph1 PSU

### **V2 PSU Slow Control**



### DC/DC Enabling

- Manual (jumpers)
- External (I2C, PACE)



# Phase 2 Power Supply

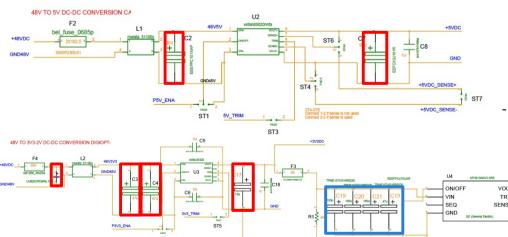


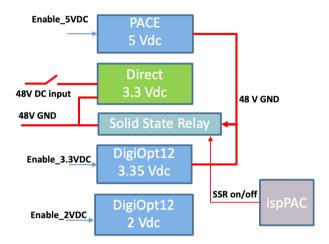


### **PSU V2 versions**

### **Design modifications**

- V2.5 (prototype t12.2 rev2)
- Modify de 2V trace to increase current capacity for future demand of DigiOpt12 boards
- Fix DC/DC drill diameters to fit different models for component obsolescence/availability
- First production batch of 50 units
- V2.6 (prototype t13\_rev1)
- Design modified due to obsolescence/availability
- Improve DC/DC stability









V2.5 (prototype t12.2\_rev2)

# Phase 2 Power Supply

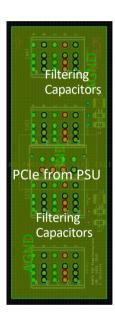




## **Backplanes**

#### **POWER BACKPLANE**

- Distributes +3.3V and +2V to DigiOpt12
- Capacitors for additional filtering





#### **SIGNAL BACKPLANE**

- Distributes to CLKs, SynPat, SPI, I2C to DigiOpt12
- FireFly connection to PACE
- Additional local I2C Access
  - Through I2C bridge
- SIGNAL BACKPLANE redesigns

#### V2\_t11

Missing Enable connection for i2C bridge Improved SILKSCREEN information

#### V2.4

Firefly connector wrong pinout affects DigiOpt12 SYNC\_PATTERN & CLOCK signals

#### **V2.5 production**

Firefly cable crosses signal pins. Corrected





Firefly from PACE

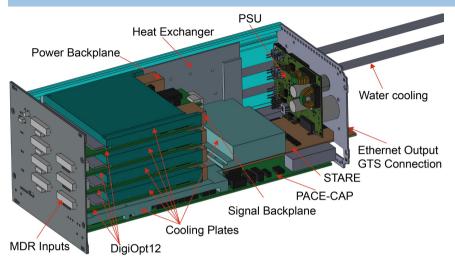
i2C Bridge

# Phase 2 Mechanics





## Design

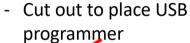


## **Modifications to control temperature**

- New Heat Exchanger for better cooling

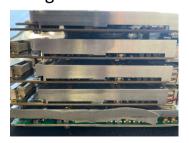


 Fan in PACE cooling block to lower temperature around DC/DC converters.
70,000 hours lifetime.





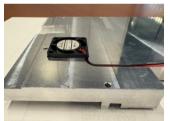
- Increase heat dissipation using box sides



 Thermal Pads on top and bottom layers. Use bottom plate as heat spreader

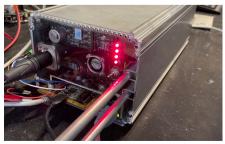








Fan at rear panel to lower PSU temp



# Phase 2 Mechanics





## Design

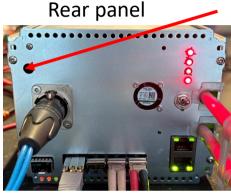
### Front and rear panels

Front panel



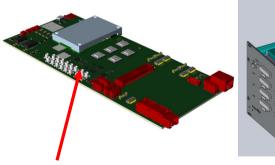
Aluminium prototype

# Trigger connector



**Steel** prototype

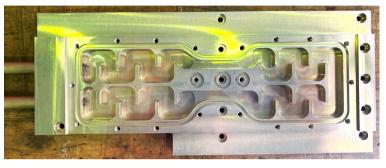
## **PACE cooling block modifications**



Area to modify block to connect the

Cutout of PACE cooling block to connect the external trigger signal

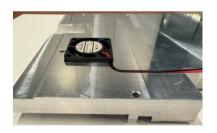
## **Heat exchange modification**



Alodine treatment to prevent corrosion



PACE modified cooling block



Groove for fan cabling

# System test





## Thermal tests

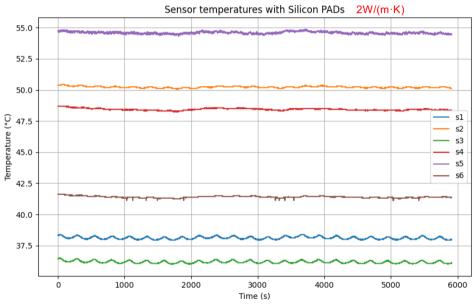
## Tests with box closed (PACE prod. t58)

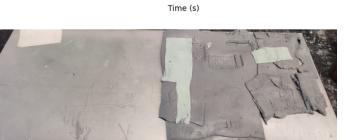
Vcc =48 V, Icc = 1.99 A

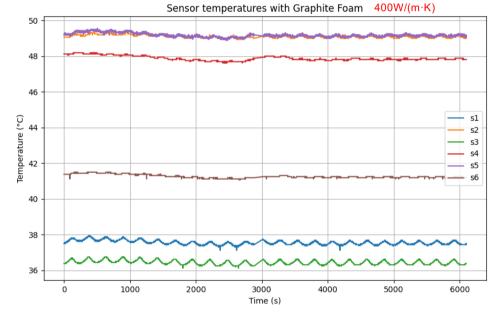














# System test





### Thermal tests

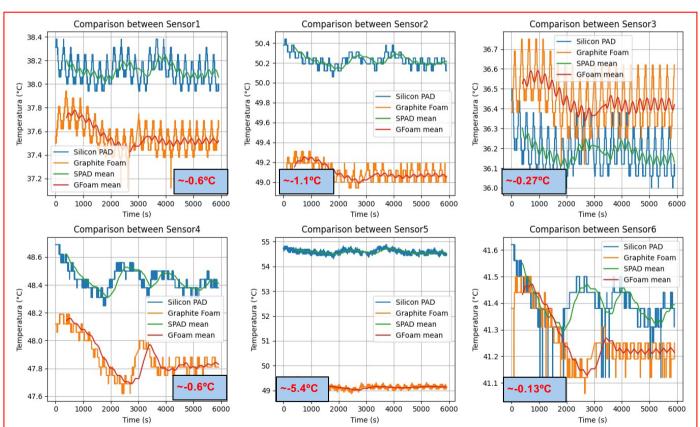
## Tests with box closed (PACE prod. t58)

- Vcc =48 V, Icc = 1.99 A









| PACE | PACE SC temp **49:** 45.81 °C 47.56 °C (**S4**) 4D: 48.62 °C (S5) **4E:** 40.94 °C (**S6**)

Running from September 10th

# **Production status**





#### **PCBs**

- Power backplane: 52 + 25 units

- Signal backplane: 60 + 25 units (expected)

- PSUv2.5: 50 units under CAT. Only minor change of resistor value to increase 2V output voltage

- PSUv2.6 (t13 rev1): board available end September

#### **Mechanics**

- Boxes: 90 units

- Crates: 90 units

- Cooling plates + heat exchangers:

- 28 PACE cooling blocks (+8 to be update to new design)

- **78** STARE cooling blocks

- **240** Digitopt12 cooling blocks

- **59** Heat exchanger

- 2 Frontal panels -> Minor redesign to help in the assembly process

- 1 Rear panel -> Minor redesign to help in the assembly process

#### **Cables**

- Firefly, HDMI, PCIe and SATA completed for at least 50 units







Thank you for your attention