

Time Distribution System Proposal for the Hyper-Kamiokande Experiment's Far Detector and J-PARC sites

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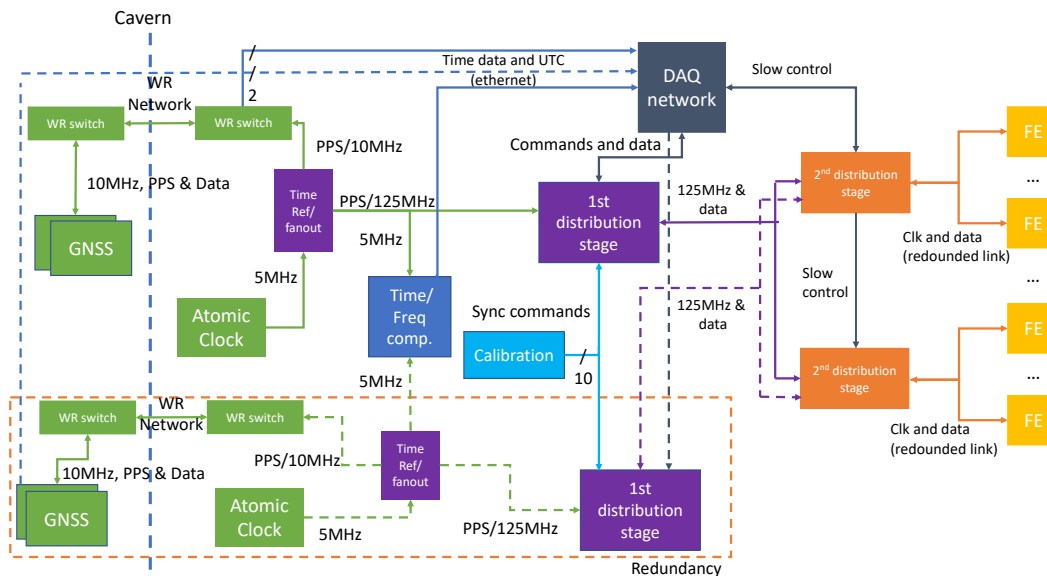


Figure 1: The proposed time distribution block scheme. The green boxes are part of the clock generation and UTC tagging described in section 2. The purple elements constitute the first distribution stage described in section 3, the orange ones are for the second distribution stage described in section 4, while the yellow ones refer to the time distribution endpoint, part of the front-end, described in section 5.

Introduction

A piece of crucial information to reconstruct the Cherenkov ring(s) associated with an event in the Hyper-Kamiokande experiment is the arrival time of the light emitted in water on the detector’s PMTs. To achieve this goal a reference time must be established and distributed to all the PMT front-end (FE) modules’ readout electronics.

The time synchronization precision is directly related to the event’s reconstruction accuracy; therefore, great care must be devoted to this task to control all sources of errors and inaccuracies. The Hyper-Kamiokande experiment requires a time distribution jitter smaller than 100 ps RMS and the clock skew between front-end boards to be constant over any power-on and reset.

The time tag of each particle interaction needs to be in a format that allows its correlation with data collected by other experiments worldwide; for this reason, the generated local time base has to be associated with the Coordinated Universal Time (UTC) with an accuracy better than 100 ns. This absolute time tagging will also be used to identify the events generated in the detector by the particles sent from the J-PARC accelerator. Along with the time synchronization, some “critical information” like slow control data have to be transmitted by this subsystem hence a 100 Mbps or greater bandwidth bidirectional data channel must be provided.

The full block scheme of the proposed system is depicted in Fig. 1. It can be subdivided into 3 main parts, as shown in the conceptual diagram reported in Figure 2 which highlights also its sub-constituents and their envisioned positions.

To guarantee the most stable and precise reference, the local time base originates in an atomic clock working in free-running mode. It generates a 5 MHz frequency that is sent to a time reference fan-out board. Here the 125 MHz reference clock is generated and sent to the distribution network along with a PPS (Pulse Per Second) “counted” using the 5 MHz time base. The 125 MHz frequency is distributed over different branches by means of time distribution modules and delivered to all the leaves represented by the FE modules using the so-called Time Distribution Endpoints or TDE. A 10 MHz clock is also generated and sent to a GNSS (Global Navigation Satellite System) along with the PPS. Here the time distance between the local PPS, the GNSS time and, in turn, a UTC prediction is measured and sent to the data acquisition computer infrastructure via Ethernet protocol where it is used to convert the event’s local time tag to it.

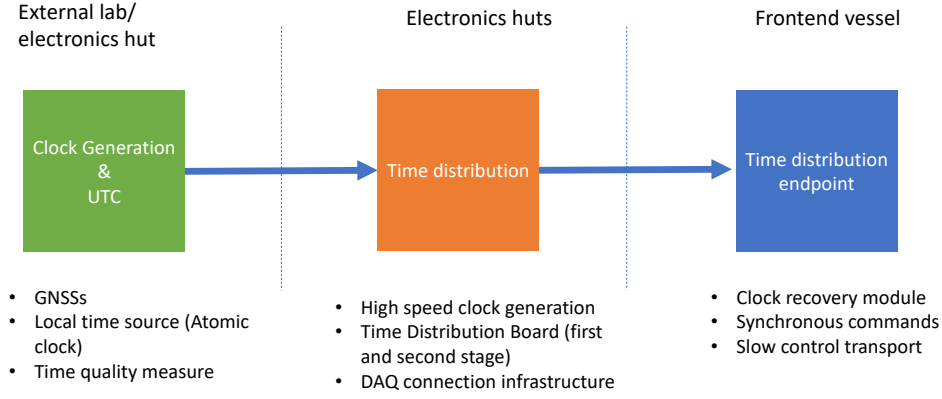


Figure 2: The block scheme that describes the 3 main time distribution sub-systems.

The HK R&D program has been carried out by LPNHE, INFN, and IRFU, but this document concerns mainly the contribution provided by the LPNHE group to meet the experiment’s requirements summarising all the efforts made over the last 3 years and presenting the envisioned solution for the Hyper-Kamiokande far detector.

The document starts by presenting the experimental requirements and then describes the proposed design in 3 main parts, following the block scheme reported in Figure 2. Section 2 describes how the HK far detector clock is generated and accorded to UTC. Details about the different instruments used (green boxes in Figure 1), their tested performances, and calibration are highlighted with the strategy to mitigate failures and enhance the system’s reliability. Section 3 is devoted to the first part of the clock distribution network, receiving the base cadence, generating the main reference clock, and distributing it to the second layer along with synchronous commands. This part corresponds to the purple boxes in Figure 1. As visible in the block diagram, it is connected to the data acquisition network (gray box) and the calibration system. In section 4 the second part of the distribution network (orange boxes of Figure 1) is described. It receives the clock and data from the first distribution stage and passes them to the front ends via optical fibers. On this bidirectional link, the FEs move some slow control data to the DAQ. This is the reason why the second distribution stage is connected to the data acquisition network via standard Ethernet links. Specific reliability considerations designed to prevent synchronous link interruptions are described at the end of this section. Some preliminary results devoted to testing the clock and data transmission concept are presented as well. Section 5 contains the description of the time distribution elements included in the front-end module to handle the synchronous data and clock and broadcast them to all the concerned modules. This part is implemented as a logic element integrated into the FE electronics depicted as the yellow boxes in the diagram of Figure 1.

The document ends with a section that describes our estimation of the cost and human resources required to produce the system along with a detailed schedule and a risk analysis.

1 Experiment’s Requirements

The full list of the experiment’s requirements relative to the time distribution system is reported below:

1. A high-speed reference clock must be distributed to all the FEs with a jitter of 100 ps RMS (measured on 10.000 cycles). The clock stability must be, at minimum, of 10^{-11} @ 1 s and 10^{-12} @100 s. At the present time, the selected frequency is 125 MHz but it could be changed to a different value in case it would better fit the digitizer’s needs. The proposed method to fulfill these requirements is presented in section 4.
2. The distributed clock absolute time difference between any two FEs must be kept within 10 ns. This means that the different cable lengths, due to the different FE positions in the detector, must be compensated by the time distribution system. The requirement is then met if any two FEs

receive the synchronous data stream within 10 ns (according to the measured cable delay) and each of them has a jitter smaller than 100 ps on the distributed reference clock (see requirement 1). An online phase difference measurement can be performed only if it doesn't require any extra hardware. An online phase compensation is not required. The clock distribution description is in section 4.

3. The time distribution system must provide a synchronous and phase deterministic communication link to each FE with a bandwidth equal to or greater than 100 Mbps. The link from the FEs to the time distribution and DAQ doesn't need to be phase deterministic. The proposed protocol description is presented in section 4.
4. The time distribution system must provide a TDCs synchronous reset every N periods of the 125 MHz distributed reference clock to all the FEs. In the actual configuration, N is 2048, which corresponds to a reset frequency of 61.03 kHz. As for the first requirement, also this aspect could be re-evaluated once the digitizer's design will be finalized. The method used to generate this signal is discussed in section 3.
5. A coarse counter is needed to extend the TDC's range. It must be common to all the FEs, generated from a single point and 32-bit long incremented at steps of $N \cdot 8$ ns (see requirement 4). The implications of the counter wrapping are dealt with outside of the time distribution system. Each FE will count the TDC resets and will check the received global coarse counter against that. The way the TDC reset is formed and distributed is presented in sections 3 and 4.
6. Two kinds of synchronous commands must be issued from various far detector subsystems to all the FEs via the time distribution system. The first is a so-called acquisition veto. The time distribution system must provide an interface to receive this command from up to 10 different sources and send it embedded in the sync packet in the trigger field (see requirement 7). The described transport method implies that the time difference between its reception at the time distribution system and its broadcast to FEs can be as high as 10's of microseconds since it could be issued in the next available sync packet (see requirement 4). The second kind of synchronous command is an emergency stop issued by one entity. Its interface is still to be decided. The system that handles the synchronous commands is presented in section 3.
7. The TDC reset, the global coarse counter, and the trigger register must be sent periodically in the same order forming a so-called synchronization packet. It is described in section 4.
8. The 1 Pulse Per Second (PPS) and a time code must be provided by the time distribution system to the multi PMT (mPMT) along with the synchronous packet. The PPS will be dispatched in a time-deterministic manner to all the FEs as soon as it is generated. The method used is presented in section 4.
9. The local time base used to generate the distributed reference clock must be accorded to UTC within 100 ns at least. An accord is also required to the J-PARC time base. All the details of the local time base and the GNSS system are given in section 2.
10. The GNSS system (composed of 2 GNSS receivers, at least) must be monitored using a local clock to detect any possible time jump.

2 Clock Generation and UTC

2.1 General Concept

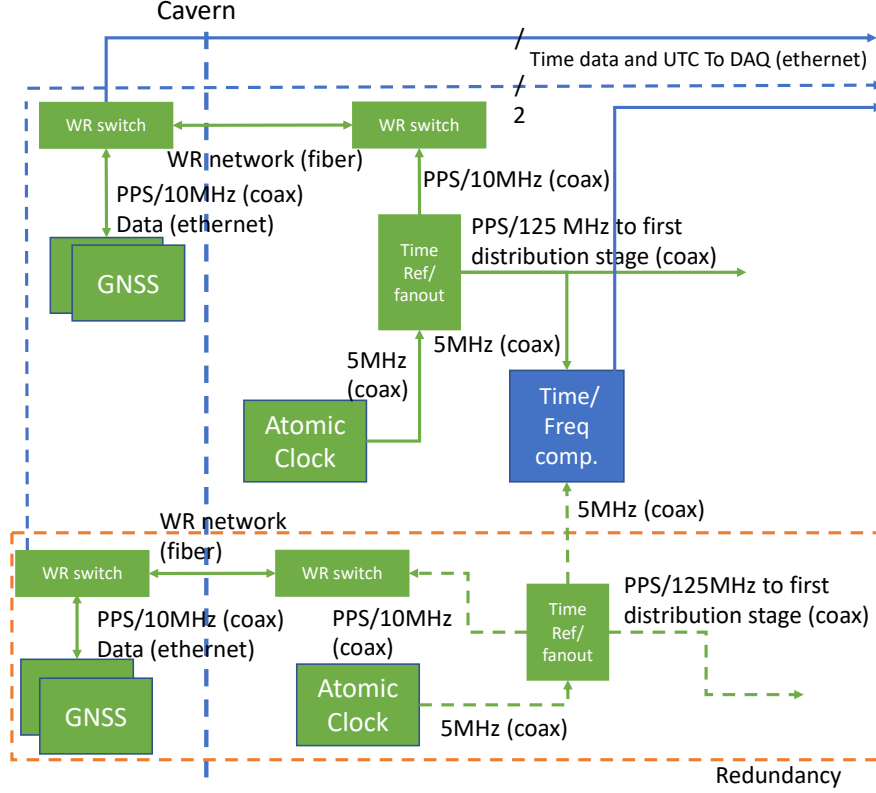


Figure 3: Detailed scheme of the clock generation section. The green boxes represent the clock and time generation instruments, the dashed orange box contains the hot spare clock generation chain while the blue box represents the subsystem used to monitor the time distance between the main and spare system.

The base clock represents the foundation of the cadence delivered to all the detector electronics elements; therefore it must be very stable and precise to guarantee, at each end-point, a signal that still meets all the requirements despite the deterioration due to the distribution process. To achieve this goal, many elements must work together as shown in the block scheme of Figure 3. As visible from it, the time origin is the atomic clock which delivers a stable 5 MHz clock cadence to the time reference/fanout element, physically embedded in the first distribution stage as described in section 3. Here the basic cadence is used to build all the needed clocks. The 125 MHz reference and the PPS (in accordance with requirements number 1 and 8) are sent to the first distribution stage while a 10 MHz frequency and a PPS are broadcast to the GNSS receivers via the White Rabbit (WR) which guarantees synchronicity and phase alignment over long distances. The Navigation satellite systems use these two periodic signals to measure the time distance between the Hyper-Kamiokande local time and the GNSS time giving a projection to the UTC fulfilling requirement 9. This information travels over the Ethernet link established by the WR network to the data acquisition system which converts the local time tag, recorded by the front end, to UTC. A second identical chain is proposed to enhance the total system reliability. The time reference/fanout entity serves also as a reference point for calibration and to check the time distance between the main and spare clock generation blocks.

This section describes in detail all the elements of the proposed scheme, their interconnections and the characterization tests already performed on them. Reliability and risk mitigation considerations are given at the end of the section.

2.2 Atomic Clock and time reference point

The cadence generator technology that guarantees the best performance is the atomic clock, but, currently, on the market, there is a vast range of instruments with different noise levels, stability characteristics, and prices. The two candidate technologies proposed for Hyper-Kamiokande are the Passive Hydrogen Maser (PHM) (microwave amplification by stimulated emission of radiation) and the Rubidium (Rb) standard. The models under consideration are the rubidium clock FS725 from Stanford Research (SRS) [1] and the T4Science pHMaser 1008 [2]. Both output a PPS, a 5 MHz and a 10 MHz, and, the selected rubidium clock, has also a PPS input used as a reference for its internal PLL. In other words, the clock’s output frequencies can be periodically calibrated using the PPS input. This option could be used to mitigate the instrument’s drift measured at 10^{-11} over 1000 s. The proposed PHM doesn’t have this feature.

The main characteristics of the two devices are summarised in Table 1¹.

Technology	pHMaser 1008	SRS SF725
Frequency stability	$\sim 5 \times 10^{-13}$ @ 1 s	$\sim 2 \times 10^{-11}$ @ 1 s
Equivalent jitter	0.5 ps	2 ps
Frequency drift	$\sim 5 \times 10^{-15}$ @ 1 day	$\sim 1.6 \times 10^{-12}$ @ 1 day

Table 1: Passive Hydrogen Maser pHMaser 1008 and Rubidium atomic clock SRS SF725 characteristics.

Atomic clocks performance As evident from Table 1, the Passive Hydrogen Maser shows much better performance that goes up to 2 orders of magnitude with respect to the Rubidium, both at short and long timescales. These values have been verified in an extensive test campaign conducted in collaboration with the colleagues of the SYRTE laboratory, part of the Observatoire de Paris (OP) [3], one of the institutes that concur to the UTC definition. A more visual comparison involving Allan Standard Deviation (ASD) [4] can be found in Figure 4. The time at which the curves reach the minimum indicates the time at which long-term frequency drifts become dominant over the short-time fluctuations. The difference in the performance of 2 orders of magnitudes between the PHM and Rb technologies is evident also in this plot where the green line is constantly and consistently below the others.

Time base system configuration Considering the far detector’s need to synchronize all the front-ends in a very tight manner, we plan to use the atomic clocks in the so-called “free-running” mode, so without steering the output using a PPS input coming from a GNSS receiver. Instead, the 5 MHz from the atomic clock is sent to the entity that generates the FE reference clock. The same entity also counts the number of cycles to reach one second and generates a local PPS. It then becomes the time distribution reference point as represented in Figure 3. It serves also as a fan-out providing a very stable 10 MHz frequency and the PPS to the GNSS receivers to phase align their outputs overriding the instruments’ internal oscillators. As described in the next section, this logical entity will be integrated into the first distribution stage board for practical reasons. The Septentrio GNSS receivers measure the time distance between the PPS input and UTC. This information is then sent to the DAQ via Ethernet links and is used to convert the local time tag to UTC. We prefer this scheme to the one where the atomic clock is steered by the GNSS PPS for, at least, 3 reasons:

- The free-running scheme gives the control of the atomic clock drift while, in the other mode, the atomic clock’s internal PLL follows the GNSS and won’t be as precise as a post-processing correction. Moreover, according to the manual [1], the steering procedure is mainly intended for instrument calibration.
- working in free-running mode allows also to avoid corrections on the atomic clock output frequencies that could bring possible errors due to GNSS receiver malfunction or satellite data misconfiguration. Configuring the atomic clock in steering mode could bring clock jump or excessive jitter on the output cadence if the PPS input from the GNSS receiver would jump out of the internal PLL adjustment range.

¹The Passive Hydrogen Maser also provides a 100 MHz clock output.

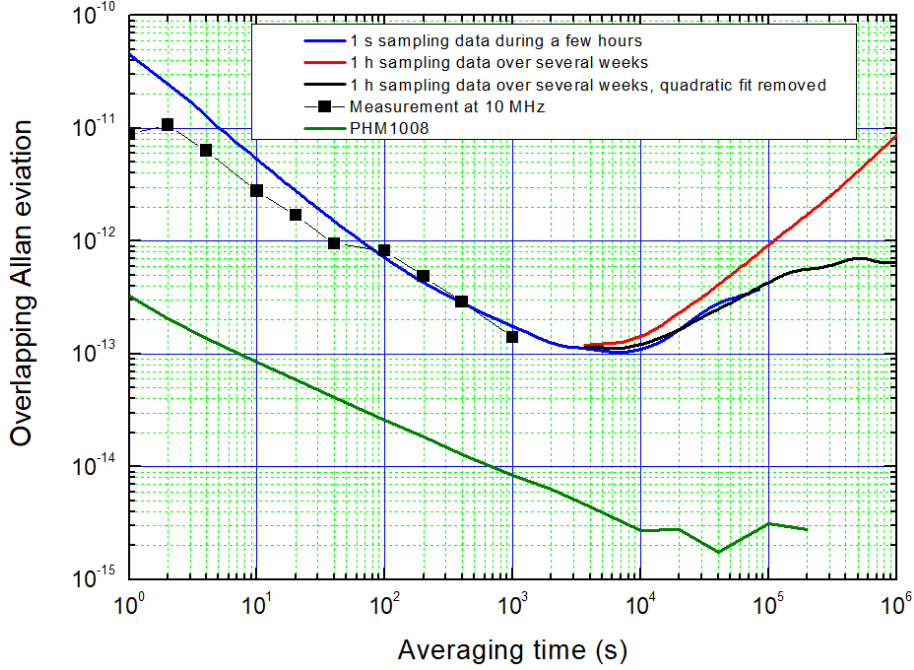


Figure 4: Allan Standard Deviation of the rubidium atomic clock calculated using different sampling times compared with the Passive Hydrogen Maser (green curve).

- The free-running clock configuration facilitates the use of multiple GNSS receivers giving the possibility to select the UTC time reference to use (see below).

It is also worth mentioning that any atomic clock drift, no matter its value, will affect all the detector's FEs equally then it will be invisible on the relative time tagging.

The conversion values to transform the local time tag into UTC (and fulfill requirement 9) will be calculated periodically by the GNSS receivers and sent to the data acquisition system via Ethernet in a CGGTTS (Common Generic GNSS Time Transfer Standard) file [5]. The validity period of each conversion factor depends on the atomic clock performance and in particular on its drift, evaluated by comparing its Allan standard deviation to the one of the GNSS receivers system. We have already performed this measurement on the purchased SF725 rubidium clock and the corresponding plot is reported in Figure 5. As visible from the purple curve, obtained comparing our atomic clock to the SYRTE UTC implementation called UTC(OP), it starts showing an evident drift at about 10^4 seconds after the GNSS alignment and this is the time when a new conversion value would be needed. A similar analysis can be done on the PHM atomic clock but, according to the datasheet and previous experiences, we are expecting to see a drift at a day scale consequence of a much more stable generated clock that implies a local PPS to UTC conversion factor rate of once per day.

To compute the conversion factor we are planning to use a time transfer method based on the information included in the CGGTTS file produced by the GNSS receivers. According to the standard, each satellite receiver calculates the time distance between the local PPS and the GNSS system time at intervals of 16 minutes in which the measurements are performed every 30 seconds for a total time of 13 minutes. The choice of these specific numbers has historical reasons and comes from the time when a receiver needed 13 minutes to acquire the full satellite navigation message and extra 3 minutes were foreseen to track the following scheduled satellite. In spite of an almost 20% inefficiency, the CGGTTS standard still uses these numbers to guarantee retro-compatibility with older systems. Every GNSS receiver then performs some corrections to take into account the signal's distortion due to the propagation in the atmosphere and the internal equipment delays, it computes a linear fit on the 26 acquired values and gives a time distance using the fit estimation at the 13 minutes midpoint. The data will be further processed with a specific algorithm to compute the conversion factor to the

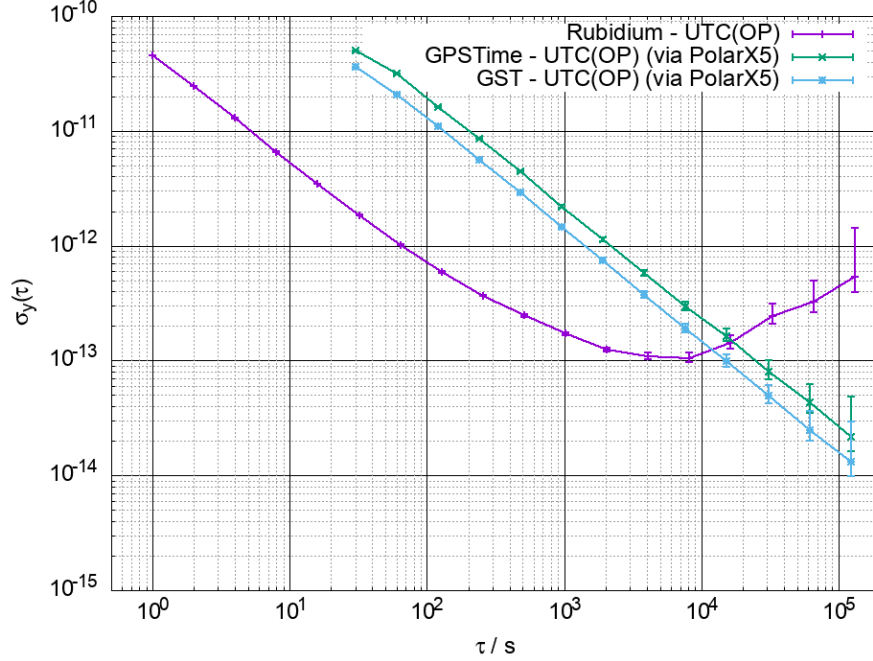


Figure 5: Allan standard deviation comparison between the SRS FS725 rubidium atomic clock and the GPS and GST (Galileo Standard Time) to the UTC definition of the Observatoire de Paris (UTC(OP)).

data acquisition system as explained in the paragraph below. An example of the CGGTTS file and some other details are given in Appendix A.

2.3 Global Navigation Satellite System (GNSS)

As already mentioned, the GNSS will be used to correlate the local time base with the universal coordinated time, or one of its implementations, by means of the information included in its data stream. To guarantee accuracy at the level of 100 ns or better (as reported in requirement number 9), many parameters must be taken under control and corrected, if needed. Some of them are related to the satellites, e.g. the position of each transmitter at any given time. This implies that each satellite's orbit must be known with a precision that sometimes goes beyond the one included in the data stream. Some other elements are relative to the receiver and concern the electromagnetic signal that reaches the antenna, the interference, and the reflection to which it is subjected. To improve the first kind of uncertainty, correction algorithms will be implemented on the received data by means of a computer infrastructure that elaborates information coming from the UTC consortium. This consortium is composed of many laboratories spread around the world working together on the UTC definition, as described in Appendix B. As part of their duty, they publish a weekly report that includes parameters needed to reconstruct the universal time at “state of the art” precision. The uncertainty related to the local equipment can be mitigated by performing an accurate calibration of the receiver, the associated antenna, and the connection cable against a cadence generated by a so-called group 1 laboratory, like SYRTE, able to guarantee a resolution below 5 ns.

After an extensive R&D study, the Septentrio PolaRx5 multi-frequency multi-constellation timing/reference receiver associated with a multi-frequency B3E6 choke ring antenna [6, 7] has been selected. A calibration procedure has been conducted on the first purchased set, presented in Figure 6, and the results are reported in the tables below:

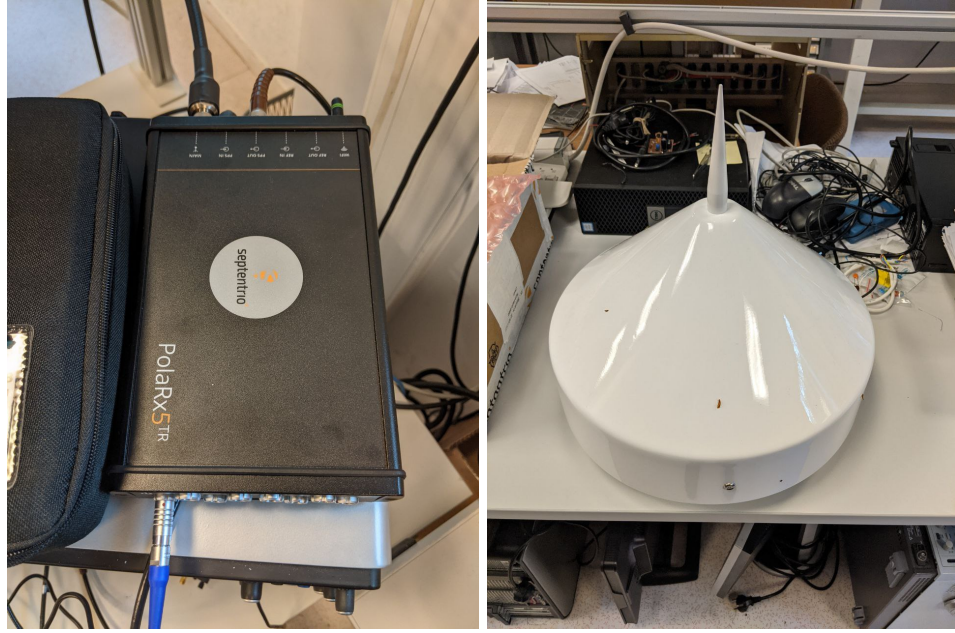


Figure 6: The Septentrio PolaRx5 GNSS receiver and the associated antenna.

Table 2: GNSS calibration equipment description.

Institute	Equipment status	Measure MJD	Receiver type	BIPM code	RINEX name
OP	Traveling	NC-NC	Septentrio PolaRx5TR	LPN1	LPN1
OP	Group 1 reference	59508 – 59514	Septentrio PolaRx5TR	OP73	OP73

Table 3: GPS calibration table. All values are in ns.

Receiver	Reference	Measure's MJD	REFDLY	CABDLY	P1 DLY	TDEV	P2 DLY	TDEV
OP73	Ref	59508 – 59514	85.2	129.6	29.500	NC	26.30	NC
LPN1 1	OP73	59508 – 59514	88.3	127.1	25.832	0.024	22.871	0.022

Table 4: Galileo calibration table. All values are in ns.

Receiver	Reference	Measure's MJD	REFDLY	CABDLY	E1 DLY	TDEV	E5a DLY	TDEV
OP73	Ref	59508 – 59514	85.2	129.6	31.700	NC	31.300	NC
LPN1 1	OP73	59508 – 59514	88.3	127.1	28.242	0.040	25.431	0.034

The presented calibration will be done on all the used receivers before the deployment and the measured delay values will be stored in their configuration system. The values will be checked every 5 years using a portable device called “traveling station”. This mobile station will be compared against

all HK’s GNSS receivers and with the one at the UTC consortium lab to align all the systems without moving them.

To achieve the best performances and use multiple devices together, each GNSS receiver will be provided with a 10 MHz and a PPS input cadence generated from the atomic clock. The 10 MHz frequency will be used to override the internal receiver’s oscillator, as it has a more stable and precise clock for the internal logic. The PPS input will be used at start-up to synchronize multiple receivers’ outputs in order to use them together and switch from one to the other in case of malfunctions. The receiver and antenna position is also crucial for UTC accuracy because a good data reception would allow for a reduction of the data post-processing and to reach a greater precision. The number of “seen” satellites has a great impact in terms of UTC definition reliability and precision. While it is true that even one satellite can give a precise UTC reference (once the antenna position is known with enough precision) in this configuration the system would completely depend on that specific satellite and changing it would bring jumps in the UTC reference. Moreover, correcting the received data would be more difficult and less precise. The minimum number of satellites that we are envisioning to see is 5 at any given time. They could belong to different constellations like the American GPS (Global Positioning System), the European Galileo, and the Japanese QZSS (Quasi-Zenith Satellite System). The basic idea to combine them is to have a time reference from each constellation, get the UTC reference, and, from it calculate the time distance between them.

GNSS-atomic clock interconnection topology To minimize the local time base uncertainty, the atomic clocks will be placed close to the far detector’s electronics in a cavern where the satellite’s signal doesn’t arrive. The GNSS equipment, on the other hand, will be placed outside, several kilometers away from the cavern entrance, in a position that maximizes its reception quality. To combine the cadences generated by two sets of instruments without losing synchronicity, the CERN White Rabbit technology will be used.

White Rabbit (WR) is the name of a collaborative project including CERN, GSI Helmholtz Centre for Heavy Ion Research and other partners from universities and industry to develop a fully deterministic Ethernet-based network for general-purpose data transfer and sub-nanosecond accuracy time transfer. The hardware designs and the source code are publicly available [8] but this technology can be considered a sort of an off-the-shelf solution since the hardware can be bought from companies that produce and sell WR-compliant devices.

This solution is very convenient because, over a single fiber, it is possible to transport the signals needed to the GNSS receivers (PPS and 10 MHz clock) and use the data link to transport the time information received from the satellites via Ethernet protocol. The planned topology consists of a White Rabbit switch configured as Grand Master placed close to the atomic clock inside the cavern that receives the PPS and 10 MHz clock from the fan-out reference board. It embeds the two frequencies into the data stream and sends them over a mono-mode fiber laid down in the entrance tunnel up to the building where the GNSS receivers are located. There, a second White Rabbit switch configured as a slave outputs a PPS and 10 MHz clock replica phase aligned to the Grand Master. The ethernet cable connected from the WR switches to the DAQ network and to the GNSS receivers will transport the data needed to convert the local time tags to UTC. This last part is possible due to the White Rabbit protocol compatibility with the standard Ethernet.

The events generated by the J-PARC accelerator’s particles’ packets must be identified and separated from the noise and astrophysical events. For this purpose, a specific acquisition window must be opened for each beam spill at the far detector’s site however a direct “trigger” signal can’t be sent due to the distance between them. The most effective solution to solve this problem is to guarantee that the two sites’ time bases differ from a known quantity then the accelerator’s site can “inform” the far detector about the time at which a particle’s packet has been sent trusting that the far detector data acquisition system can correlate that time to its own time base.

The best way to measure the time distance between the two sites is the so-called “common view” technique possible when the two sites are both equipped with a GNSS receiver locked on the same satellites. This method allows a direct comparison between the two timebases following the time transfer method reported here [9].

An alternative solution consists in adopting the same common view method separately between each station and the Japanese UTC consortium lab: NICT. This method can be considered as “indirect” since it implies that both the far detector and the J-PARC time bases are measured against the so-

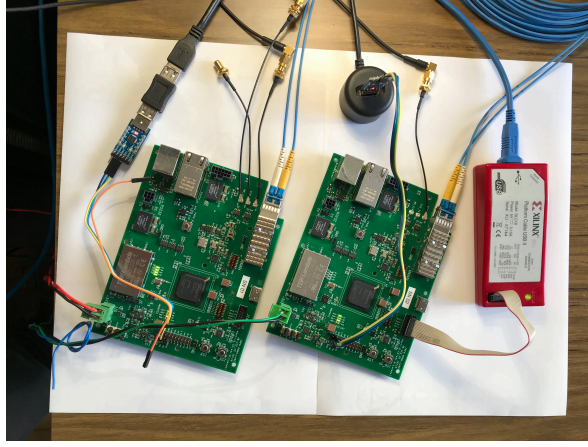


Figure 7: The White Rabbit test bench composed by two custom boards developed in the INFN test bench of Rome 1.

called UTC(NICT). By knowing the time difference of each site with respect to UTC(NICT), the time distance between the two experimental sites time bases could be computed. This method would result in a slightly larger error but would bring the advantage that both sites are related to a UTC implementation. In principle, both methods could be implemented at the same time and could be used as a crosscheck.

A data collection campaign will be performed, with a portable GNSS receiver, at the far detector site well ahead of the system deployment. This test will be useful to establish the best final antenna position and to check the number of common satellites available. The collected data will determine also the entity of the post-processing needed to achieve the experiment’s requirements. The portable equipment, composed of the same elements installed at the far detector site, will then be used as a “traveling station” to check the calibration parameter of the resident receivers during the regular data acquisition period.

White Rabbit experimental tests A test campaign has been carried out to validate the White Rabbit as a viable solution to bring the base cadences from the atomic clock to the GNSS receivers. The concept has been tested using a couple of custom boards realized by the INFN branch of Rome 1 and presented in Figure 7. The connection scheme consists of two boards, equipped with Xilinx Spartan VI FPGA, connected with an optical fiber (the blue cable), and the transmitted and received clocks are extracted by means of black coaxial cables. The data bandwidth has been measured as compliant with the Gigabit Ethernet standard, moreover, connecting one board to a computer, it has been verified that the data packets are correctly exchanged while the time information is dropped.

The clock characterization has been carried out in two steps. First, the PPS provided by the two WR nodes has been verified to be stable over different resets and its total jitter on the RX side has been measured at 17.9 ps. Then the jitter on the reconstructed clock has been measured in the frequency domain and is reported in the plot of Figure 8. The phase noise analysis starting from 10 Hz shows a jitter as low as 8 ps RMS while at frequencies below that threshold, there is a great quantity of noise. If the same measurement is performed starting from 1 Hz the total jitter rises to 67 ps and there are some hints that this additional noise is generated by the local oscillator on the transmission side.

2.4 Time corrections

As described in the previous paragraphs and visible in Figure 5, the atomic clocks have a very small jitter but they drift from an ideal time reference after a certain time. This is almost the opposite behavior of GNSS receivers which have a not-so-good jitter but are very stable in the long term. It is then clear that to have a stable system at any time scale, we need to use the atomic clock to produce the base cadence and correct its drift with data coming from the GNSS receivers. To define the best correction strategy, effective on the various sources of noise that cause the drift, we have

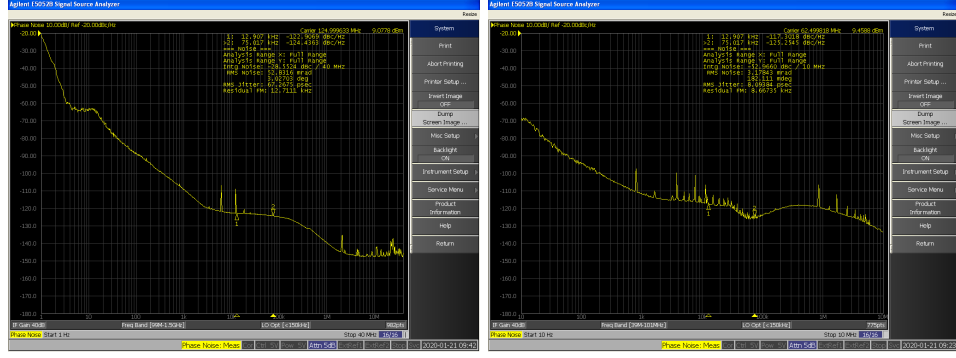


Figure 8: Frequency domain jitter measurements performed on the reconstructed clock using the White Rabbit scheme. On the left the phase noise analysis including frequencies as low as 1 Hz. On the right the same measurement starting at 10 Hz.

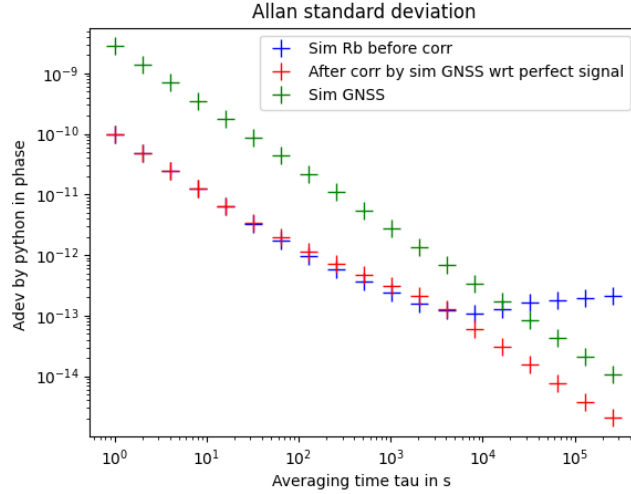


Figure 9: Allan standard deviation of the simulated Rb clock data before correction (blue, simulated GNSS data (green), and Rb clock data obtained applying the quadratic function correction (red).

studied simulated data. First, we built an ideal time scale free of any jitter or drift, then we added different sources of noise to simulate our clock sources' behavior, and, finally, we tested the correction algorithms evaluating their effect. It has been observed that the Rubidium clock drifts with a quadratic trend. So, the best method to correct it should be based on data generated with a quadratic fit. To implement this correction we have divided a given time interval affected by this drift in sections of length L and data of each section has been independently fitted with a quadratic function (a 2nd-order polynomial). In the real world, the atomic clock performances will be evaluated against the GNSS data via CGGTTS files following the method described in paragraph 2.2. Thus, to keep our simulation as close as possible to reality, we have compared the simulated 1PPS Rb data with the simulated GNSS's 1PPS once every 30 seconds for 13 minutes and skipped the next 3 minutes of data as done in the CGGTTS algorithm. The obtained coefficients have been applied to the given interval and the residual drift has been measured using the overlapping Allan standard deviation. An optimization parameter is the interval's length L , so some tests have been performed varying it. The optimum value has been found at 10^4 seconds which is coherent with the drift time scale visible on the plot in Figure 5.

The results are reported in the Allan standard deviation charts of Figure 9. The blue curve calculated is the simulated rubidium clock data affected by drift, the green curve is the simulated GNSS data and the red one is the ASD of the Rb clock after the correction described above. The

effectiveness of the defined algorithm is evident from the plot since the Rb corrected data follows very close the GNSS one.

The correction method described here works very well but can be applied only offline since it requires accumulating 10^4 seconds of data to compute the coefficients. The HK far detector time distribution system needs a method to compare the local time scale to the J-PARC and UTC in real-time so a similar method that works online has been defined.

We apply the offline correction algorithm on a “sliding” time window, that starts from the last available measurement in the CGGTTS file and goes back over $L = 10^4$ seconds; using the comparison within this window, we compute the correction coefficients that will be applied until the next measurement from the receiver will be available. This method can produce online correction values so it fulfills the experimental requirement and can be used as a real-time correction method. Testing this algorithm it has been found that a linear fit gives better results with respect to the quadratic so this formula has been retained.

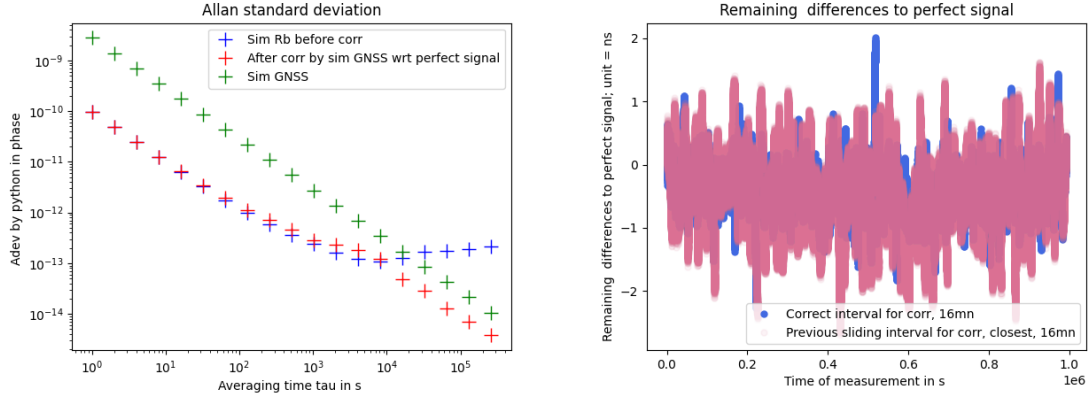


Figure 10: Left plot: Allan standard deviation implemented to evaluate the online correction. The blue line is the simulated Rb clock data before correction, the green curve is the simulated GNSS data, and the red one is the Rb clock data obtained applying the linear fit correction. Right plot: Time series plot of Rb clock data corrected with the offline algorithm (blue curve) and the online one (red curve).

The same evaluation method based on ASD plot has been used and the results are described in the left plot of Figure 10. Here the residual drift is slightly more pronounced but the accord to the GNSS data is still very good. To evaluate even better how the online correction method is effective on the drift and to compare it with the offline one a more visual graph is reported in the right plot of Figure 10. It shows a time series plot of the Rb data corrected using the “sliding window” method (red curve) superimposed to the same data set corrected using the offline algorithm (blue curve). As visible, the obtained results are very similar and the accord with the simulated GNSS data is within ± 2 ns for both methods. To further validate these corrections methods the same algorithms will be applied to real data collected at LPNHE-Paris in the near future.

If the results will be confirmed, the correction adopted in the HK far detector will be the following: a set of correction coefficients will be generated and provided to the DAQ system as soon as a CGGTTS file will be available (every 16 minutes). Afterward, the time stamps of data selected and stored on non-volatile memory will be corrected with the coefficients calculated with the offline algorithm.

2.5 Reliability, Redundancy and Risk Mitigation

To achieve the best performance and enhance reliability, 2 GNSS receivers connected to the same antenna and sharing the same PPS input, will be installed and data from both instruments will be sent to the data acquisition system via Ethernet. This information will be used to constantly monitor the equipment and guarantee that at least 1 receiver will be operational at any time in accordance with requirement 10. To be more specific the DAQ will receive the CGGTTS files of both devices and will analyze them. In the case of normal behavior, they will provide the same time distance between

the local PPS and the GNSS time while, in case of malfunctions, one of them will have a different offset.

To avoid a single point of failure, the entire chain of the atomic clock, the GNSS receivers, the time distribution reference point, and the first distribution stage will be duplicated in a hot spare configuration. This means that the second chain will be always active and its 5 MHz time base will be constantly compared with the main one. This constant time comparison is assured using the Keysight 53230A universal time/frequency counter [10] which measures the time distance between two signals with a resolution of 20 ps and sends it over Ethernet to the data acquisition system. This scheme provides a constant check of the HK time reference accuracy and an alternative, ready-to-use, reference in case of malfunction of the main one. Tracking the time distance between the main and spare time references will give enough information to merge the data tagged with the two different time bases. To further enhance the system's reliability, a third atomic clock will be acquired and used as a cold spare. It will be safely stored at the far detector site, according to the vendor recommendations, operated and checked regularly, and thus ready to be used in case the main or the hot-cold one needs a long period of maintenance.

To further enhance the whole system's robustness and create another level of redundancy, the PPS signal generated by each GNSS receiver will be transported in the cavern by means of an electro-optical converter, and the time distance to the locally generated one will be directly measured by means of an ad-hoc TDC at 8 ns resolution. The result will be constantly compared with the CGGTTS data and, although it is expected to be less precise than the one implemented inside the receivers, it will give a quick indication of any equipment malfunction.

The system maintenance will be addressed with a scheduled plan of interventions designed to change the parts before they arrive at the end of life. The plan will be realized using the information coming from the instrument producers and envisions changing the "physical package" of the atomic clocks or the entire instrument within ten years from the start of operation. We are also considering replacing the GNSS receivers approximately on the same time scale or before the end of the producer's support. The switch to new devices will be staged to avoid any possible perturbation to the HK time base.

2.6 Time Generation system at J-PARC

Recently the Hyper-Kamiokande collaboration has shown interest in having the same design proposed for the far detector also at the J-PARC accelerator site. Installing the same setup to generate the reference clock and the time base at both sides of the experiment produces clear benefits since the particle packets sent from the accelerator and received at the far detector must be precisely time-tagged. On the other hand, our proposal for the time generation system is very flexible and can be adapted to the accelerator's needs without major modifications. This aspect represents a clear benefit also in terms of IN2P3 visibility since, with a very limited design and commissioning effort, it would gain clear leadership on a critical part of the experiment. Also in terms of funds, the involvement will be contained since the needed equipment doesn't seem very expensive.

The design requirements and the needs are still under discussion and will be clarified in the next months but, the basic idea is to provide a system capable of time-tagging the particles bunches produced by the accelerator with respect to the local time base and then comparing this local time base with the one established at the far detector and used to time-tag the events "seen" by the PMTs. This comparison would allow separating the events related to those bunches from the one produced by other sources or from the background noise. Implementing this concept would require a network of atomic clocks and GNSS receivers exactly identical to the one envisioned for the far detector. The main difference would consist of the absence of the White Rabbit network since, at J-PARC, the clocks and the receivers can be installed in the same rack. The common view time base comparison described above would be easier in this scenario since it would be performed using data produced from the same kind of receivers avoiding any possible inconsistency. Moreover, the system will be installed and maintained by the same research group guaranteeing the same calibration accuracy and the same redundancy and maintenance plan.

A possible block scheme to be installed at J-PARC is reported in the picture ...

3 First Distribution Stage

3.1 Function and principles

The main function of the First Distribution Stage (FDS) is to distribute with minimal skew and jitter a reference clock at the desired selected frequency to the Second Distribution Stage (SDS) which then fans out the reference clock to all front-ends, underwater. The variations of clock skew at any end-point must be less than 100 ps during operation and after system restart. The master reference clock is provided to the FDS by an atomic clock at 5 MHz. It is scaled up in frequency to the desired value, 125 MHz in the current plan, by an appropriate clock synthesizer. In addition to the reference clock, the FDS must generate the required synchronization information for the front ends: a periodic TDC reset signal with an associated coarse timestamp counter and a 1PPS signal accompanied by a date code. The latency of synchronous signal distribution is required to be accurate to one period of the reference clock (i.e. 8 ns at 125 MHz). The FDS also has to provide a 10 MHz reference clock and a 1PPS signal for use on the GNSS receiver side. The FDS requires a certain number of user inputs for the fanout of external synchronous and asynchronous signals: a veto signal for the data acquisition, an emergency stop for high voltage sources, and possibly other ancillary signals. If this does not add too much complexity, the FDS may monitor the slow variations of delay of all, or a subset, of its transmission links, but it is not required to compensate for these variations. The FDS is housed in an electronic hut, outside of the water tank. Although reliability is a concern, this equipment remains accessible for replacement in case of failure.

The basic principle of operation of the FDS is to perform the distribution of clock and synchronization messages from their respective sources using a pair of commercial fanout chips driving the transmitter side of an array of optical transceivers and accomplish the final expansion to the required number of end-points using passive optical splitters. The baseline scheme relies on separate physical media for clock and data: a first set of optical fibers distributes the pure clock, and a second set is used to broadcast serially encoded synchronization messages. Alternatively, other schemes based on a common media may be supported: clock embedded in serial data (using a CDR technique at the receiver end), and serial data carried over a modulated clock [11]. The FDS uses entirely commercial components, including an off-the-shelf System-on-Module (SoM) based on an FPGA with embedded processor cores.

Since this part is under the responsibility of the CEA-IRFU group this document will provide just a general description of the item omitting most of the technical details since are considered not relevant for this review.

3.2 Proposed hardware architecture

The block diagram of the proposed hardware architecture for the FDS is depicted in Fig. 11. The central part is a commercial SoM. The currently selected family of products is the TE-80x from Trenz [12] equipped with a System-on-Chip (SoC), Xilinx ZynqUltraScale+ (ZU2 to ZU4). This device features two multi-core ARM processors, a large array of programmable logic resources, over 250 user defined I/O pins, and 4 high-speed GTR serial transceivers. The SoC handles all the logic functions of the FDS with the assistance of external hardware. Reference clock frequency multiplication is accomplished by a dedicated PLL. The selected part is the AD9545 from Analog Devices [13]. This state-of-the-art clock synchronizer and jitter cleaner provides leading edge performance and features several characteristics that are not always found on competitor parts, e.g. zero-delay mode, sophisticated temperature compensation based on a digital filter, and more. The 5 MHz reference clock from the atomic clock is fed to one of the inputs of the AD9545. Outputs generate the 125 MHz reference clock to be distributed, a 10 MHz reference clock for the GNSS receiver and two jitter filtered copies of the 5 MHz input clock.

The broadcast of the reference clock and messages to the SDS takes places in two steps: a first expansion of signals, by a factor 8, is accomplished in the electrical domain by a pair of commercial PECL fanout chips, e.g. Texas Instruments CDCLVP1208. After the electrical to optical conversion performed by two groups of up to eight Small Form factor Pluggable (SFP) optical transceivers, the second, and final, step of clock and serial data signals expansion is done in the optical domain by passive optical splitters. The fanout ratio of the selected optical splitters is 1:24, although 1:16 or 1:32 devices may also be considered. In total, the FDS provides a combined electrical and optical clock and synchronization data expansion factor of up 1:256 in its largest configuration of eight TX SFPs

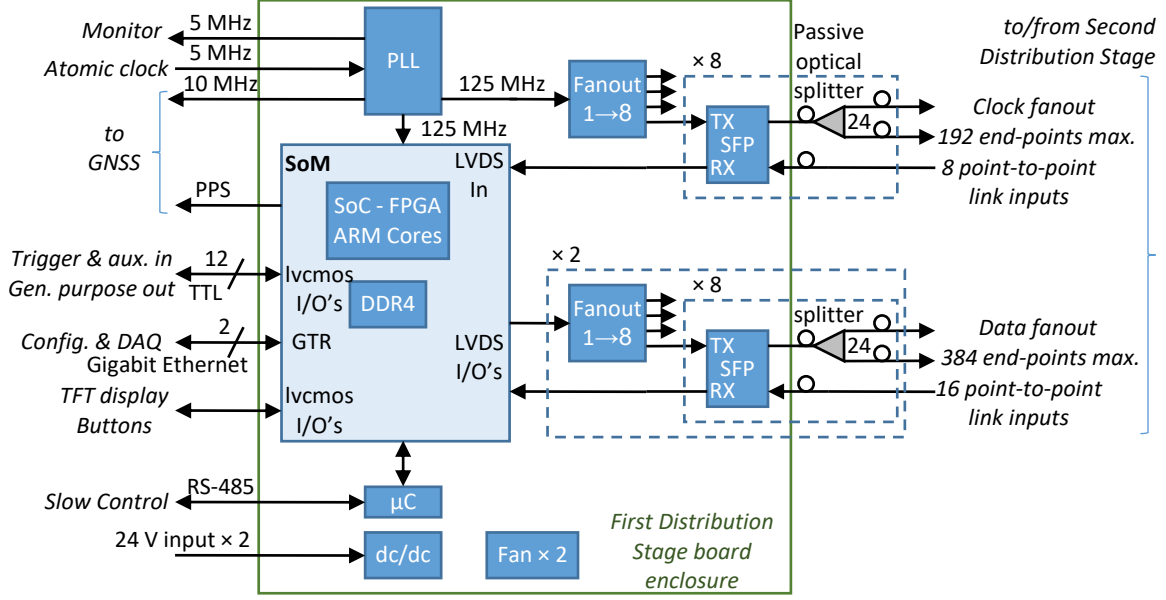


Figure 11: Block diagram of the first stage clock distributor. The central part is an electronic board based on a commercial System-on-Module, a PLL, fanout chips and SFP transceivers. The PLL receives the 5 MHz reference from the atomic clock and generates the 125 MHz clock to be distributed to the second distribution stage. The programmable logic of the SoM generates the required serial data. Fanout chips connected to SFP transceivers followed by passive optical splitters perform the expansion of the root clock and serial data signals by the desired factor.

for clock, eight TX SFPs for serial data, and two groups of eight 1:32 optical splitters. Transceivers in the 1310 nm wavelength window and 80 km reach seem adequate devices on the FDS side, while more cost-effective 20 km reach counterparts shall be sufficient on the SDS side. According to the datasheet of a typical 80 km reach transceiver, the minimum output optical power of the device is 0 dBm. The quoted attenuation of a 1:32 passive optical splitter is 17.2 dB. The minimum receiver sensitivity of a common 20 km reach SFP transceiver is -23 dBm. The safety margin on the optical budget is therefore around 5.8 dB. This is expected to remain sufficient after taking into account the loss in fiber couplers (0.1 dB per junction) and the attenuation over the length of the fibers themselves which will be very small given the short distance to cover (few tens of meters). Long reach transceivers and passive optical splitters are only usable with single mode optical fibers. Using single mode optical fibers between the FDS and SDS is not an issue because all the connections between these sub-systems are outside of the water and inexpensive fiber couplers can be used.

The path for synchronous message distribution originates from the FPGA logic of the SoC and the serializer primitive of an ordinary differential output pin pair is planned to be used. The maximum supported rate is expected to be 500 Mbps (i.e. 250 Mbps of user data before encoding), which is well within the 1250 Mbps capability of the I/O pins of the target device. The FDS is an asymmetric unit that provides clock and data broadcast capability from one source to a large number of end-points, but it has only a limited number of point-to-point communication links in the opposite direction: 16 in a minimal implementation, and up to 48 pushing the design to the limits of the number of I/O pins available on the selected SoM. No information is expected to flow from the SDS to the FDS and only a subset of the units that make the SDS have a return path to the FDS (at least one among the units served by the same passive optical splitter in the forward direction). The return path may be used to loop back the received clocks, or possibly transmit serial data from a subset of SDS units to the FDS. The planned rate is 500 Mbps or some sub-multiple of it. On the FDS, each return link uses the RX side of an SFP transceiver and connects to a pair of regular FPGA input pins. For monitoring the stability of the corresponding part of the clock distribution system, the FDS may measure the phase

shift between its local reference clock and the clocks that are looped back by the fraction of SDS units that have a return link to the FDS. One of the possible methods for the precise measurement of the phase offset between a reference clock and a synchronous delayed copy is the Digital Dual Mixer Time Difference (DDMDT) technique [14]. This proven method is notably used by White Rabbit.

The FDS logic generates a local 1PPS signal by counting the fixed appropriate number of clock cycles of the generated reference clock (i.e. 125,000,000 for a 125 MHz reference clock). This 1PPS signal is sent to all front-end (accompanied by a time code), and it is also sent to the GNSS receiver along with a 10 MHz clock, synchronous to the reference clock provided by the atomic clock. This information is used on the GNSS side to measure, and periodically record, the delay between the generated 1PPS and the 1PPS synchronous to the UTC obtained from the GNSS receiver. A 5 MHz output is provided to compare the reference clock of the main atomic clock to that of the spare atomic clock. An additional 5 MHz output is available for delay calibration or some other purpose.

The FDS has about 10 TTL level user I/O's for receiving external synchronous signals, one, and possibly two, Gigabit Ethernet ports for control and configuration, a local microcontroller with a RS485 interface for remote supervision, redundant power supply inputs (24 V), two fans, and optionally a small TFT screen and navigation buttons. The FDS is expected to fit in a single 1U 19" rack mountable enclosure. For increased flexibility, part of the functions (e.g. clock multiplication) are housed on a mezzanine card while core components are placed on a motherboard that also receives the SoM. An external, commercial, redundant, power supply unit is used to power the FDS. For system redundancy, the complete FDS is duplicated. If the main FDS fails, the secondary unit takes over. Switching between the two units is however not glitch free and system reconfiguration is expected to take up to few tens of seconds.

3.3 Prototyping

3.3.1 First Distributor Stage demonstrator

The RDHK clock distributor demonstrator is a unit designed to evaluate several principles and technical options for clock distribution. It is composed of three main elements: a custom made motherboard, a commercial SoM, and a custom made mezzanine card called "CLK_MEZZ". All these elements, two fans, a small display and a navigation panel fit in a standard 1U 19" enclosure. The RDHK motherboard houses the required DC/DC converters and voltage regulators to derive all the power voltages used on-board from a 24 V input. For redundancy, a second 24 V input is provided. The motherboard has connectors to plug the SoC module and mezzanine card, a dual SFP cage connected to GTR transceiver pins of the SoC to provide two Gigabit Ethernet ports, a QSFP cage for connectivity up to 40 Gbps (using an appropriate SoM), a RS232-USB interface for console I/O, an 8-bit microcontroller and RS-485 port (RJ45 connector) for remote monitoring, a local 125 MHz oscillator, and various ancillary circuits. The RDHK motherboard provides 6 groups of 8 SFP cages for communicating with downstream devices, i.e. up to 48-port in total. The CLK_MEZZ mezzanine card comprises the required PLL to generate the 125 MHz clock from the 5 MHz clock provided by the atomic clock. It provides also two SFP cages for additional optical I/O capability, and an RJ45 connector for cascading two RDHK units in a master-slave configuration. The RDHK is compatible with SoM model TE803 from Trenz in its different options of equipped SoC and SDRAM.

A picture of the RDHK board is shown in Fig. 12. The board has been delivered at the end of March 2022 and is still under debugging at the time of writing this document although the results are very positive for the moment and no major roadblock has been identified. Its companion card, the CLK_MEZZ, has been produced and tested. The experience gained is expected to help significantly the design of the FDS for Hyper Kamiokande which is planned to re-use the main concepts and tested components.

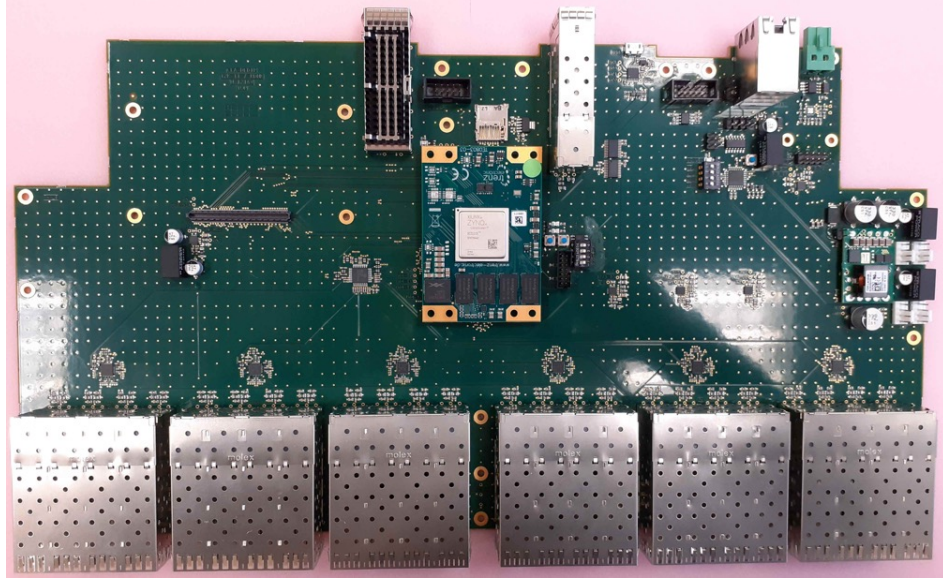


Figure 12: Picture of the RDHK motherboard and the installed SoM.

4 Second Distribution Stage

4.1 Introduction

The second distribution stage, whose block diagram is reported in Figure 13, receives the reference clock, the TDC reset, the global coarse counter, the PPS and the synchronous commands from the first stage (purple box and related blue lines in the scheme) and pass them to the front-ends. To accomplish this task (and fulfill requirement number 2 and 3) it establishes a bi-directional, synchronous, and phase deterministic link to each node over an optical fiber pair used also to exchange critical slow control information between the data acquisition system and the front-ends (yellow boxes). This module, hence, has also Ethernet connections to the DAQ network via optical fibers (gray box). All the links are handled by the FPGA's Multi-Gigabit Transceivers (MGT). The synchronous link's characteristics enumerated above represent the most critical aspect of the second distribution layer and an extensive R&D campaign has been carried out in the last two years to select the most suited technology for the Hyper-Kamiokande experiment.

4.2 Clock and Data Recovery

Many solutions have been evaluated and the selected one is based on the Clock and Data Recovery (CDR) scheme: the process of extracting time information (clock) and data from a single serial stream. The CDR is implemented by means of a specific serializer-deserializer (ser-des) couple to be used on both sides of the link. The simplicity, reliability, and the convenience of this technique have fueled its use in many different fields so that all the modern FPGAs have CDR-compliant ser-des already embedded in the silicon. This represents a further advantage for the experiment because it allows sending slow control data and distributing the system clock using one single fiber. It doesn't require any dedicated chipset besides the FPGA already used to perform all the digital operations needed for the data collection and communication with the DAQ. Reducing the components on the electronics boards has advantages on many critical aspects of the HK's design like the in-water electronics footprint, its power dissipation and the number of links and connectors between the design entities.

A time distribution scheme based on the CDR requires that one entity, called the master, receives the precise clock, the master clock, along with data and distributes it to the different nodes, called slaves. This implies that the master establishes a CDR-compliant serial link to each slave where the data and clock are merged and serialized. Each receiver separates back data and the clock from the serial stream using a deserializer. In order to guarantee the performance required by the experiment,

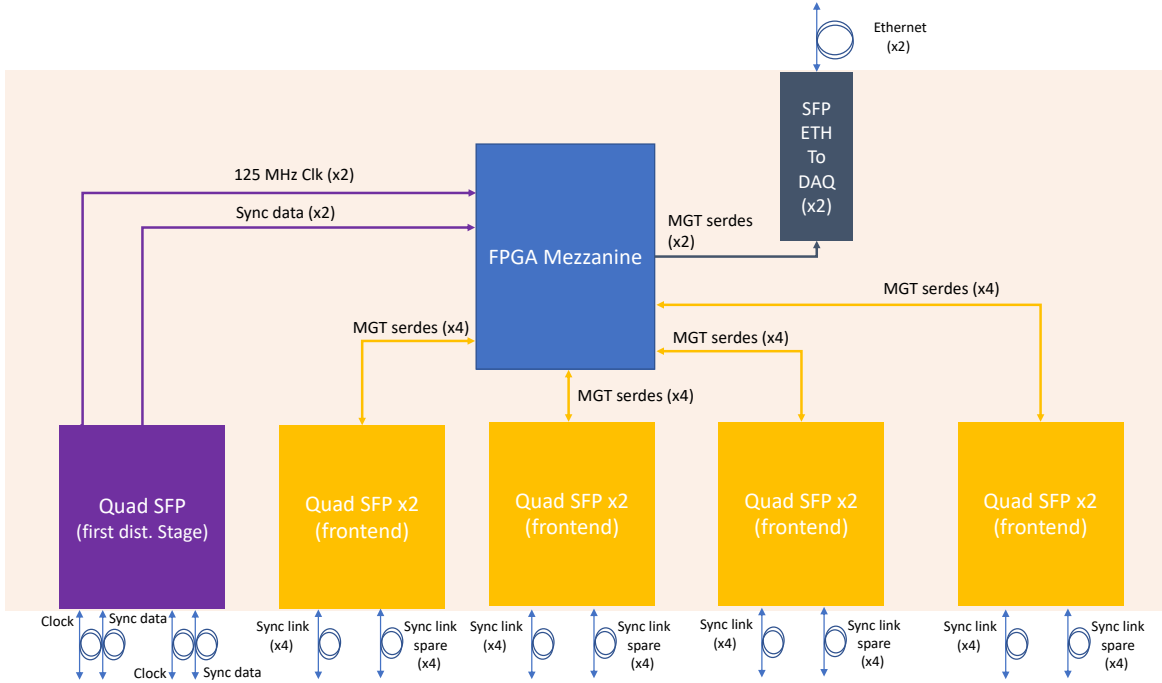


Figure 13: A block scheme of the second distribution stage. The module is controlled by an FPGA mezzanine (blue box) which has links with other time distribution’s entities via optical fibers (blue lines with circles) in turn connected via SFP (small form factor pluggable) electro-optical transceivers to the FPGA high-speed serial lines (MGT). Each quad SFP block contains 4 bidirectional fiber connections to front-ends (yellow boxes) and the first distribution stage (purple box).

extreme care must be devoted to the ser-des configuration to achieve low jitter and a fixed phase relationship between the transmitter’s and receiver’s clock. This last aspect is particularly critical since, in the standard configuration, the FPGA’s ser-des locks on a random phase after each reboot or reset. Details of the CDR concepts are reported in the block scheme of Figure 14.

A minimum number of data transitions per second needs to happen on the line to properly extract time information, therefore, data must be encoded in a specific way that guarantees the clock reconstruction on the receiving side. One of the most common encoding techniques is the so-called “8b/10b”. The phase deterministic locking mechanism selected for Hyper-Kamiokande is described on the Xilinx FPGA documentation relative to the ser-des [15, 16] in the receivers section when the PMA manual alignment mode is discussed. This technique has been widely used in many physics experiments for more than a decade and it is recognized as practical and reliable hence there are many references in the literature, the first published in 2011 [17].

The proposed locking system idea is quite simple: during the link locking phase, the master sends a conventional word to the slave, usually a so-called “8b10b” comma, over the serial line. The slave receives the serial data stream, parallelizes it and looks for this conventional word. If it is not found, the firmware performs a so-called “slide” which consists in shifting the parallel word alignment by 1 serial stream unit interval. This procedure goes on until the conventional word has been recognized. Since the clock is extracted from the data stream, the shift mechanism just described produces also a phase shift of the reference clock and, when the data alignment is reached, the reference clock replica on the slave has the same phase as the master’s.

The fixed phase clock and data recovery scheme is considered simpler and more robust than a “direct” scheme in which the clock and data are sent on two separate fibers in a network scheme such as the one between the second distribution stage and the front-ends. This aspect becomes critical in conditions like the Hyper-Kamiokande’s where the fibers’ length between the clock distribution and the different FEs varies depending on the vessel’s position in the far detector barrel and the in-water equipment has tight constraints in terms of power dissipation, heat dissipation and reliability with no maintenance foreseen for very long periods of time.

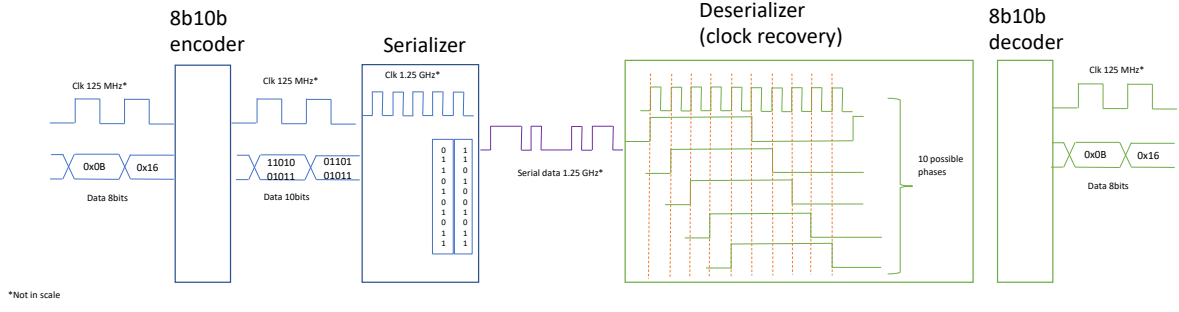


Figure 14: A schematic view of the clock and data recovery concept.

4.2.1 Experimental tests

A test campaign has been conducted to evaluate the proposed clock and data recovery concept. The experimental tests are based on evaluation boards and prototypes used as platforms to develop the firmware and the methods that will be used in the final release.

The study has been conducted using a Xilinx evaluation board KC705 equipped with the Xilinx Kintex 7 FPGA [18] as master and a custom board with a Xilinx Zynq 7000 FPGA as slave. A specific firmware has been written to establish a 1 Gigabit Ethernet communication link over an optical fiber with a special ser-des configuration that implements the fixed phase CDR method. The firmware has been installed on the board set. On each board, SMA connectors were used to output the transmitted and reconstructed clock signals so that their quality could be measured. The described setup is presented in Figure 16.

The first phase has been devoted to the data bandwidth compliance verification with the 1 Gbps Ethernet protocol; then, the attention has been focused on the jitter performance measurement for the embedded clock which represents the most important element at this stage of the R&D. An extensive measurement campaign has been carried out and the cadence characteristics have been evaluated in time and frequency domains. In the time domain, the jitter has been measured by means of an oscilloscope (Lecroy Wavepro 760Zi 6 GHz 40Gsps) and the results are reported in Figure 17.

The jitter that affects the transmitted clock is equal to 32 ps which gives a measure of the cadence quality before the distribution. As can be seen from the Figure, the reported histogram doesn't have a perfect gaussian shape, sign of a deterministic component.

The same clock signals have been evaluated also in the frequency domain using a phase noise analyzer. The principle of this kind of measurement can be explained in a simplified way as follows. The clock under study is sent to an instrument capable to recognise its frequency and generate a cadence of equal characteristics but with very low jitter. The two clocks, the input one and the one generated internally are combined using the heterodyne function (the same used in the demodulation operation) which results in the difference between the two. This waveform is then plotted and represents the frequency deconvolution of the clock jitter while the area under the curve is equal to the total jitter.

For this test, a Keysight E5052B has been used and the phase analysis plots of the transmitted and received clocks are reported in Figure 18. From the plot, the total jitter values can be obtained: 29.5 ps for the TX, very similar to the measurement in the time domain. Moreover, the spikes (spurious frequencies) are the source of the deterministic jitter. Further studies have demonstrated that the "modulation" frequency is generated by the onboard DC-to-DC power supply converters that feed the FPGA.

The jitter on the received clock this time is lower (40.6 ps total) and the "modulation spikes" are less pronounced (Fig. 19 left). The custom board is equipped also with a so-called jitter cleaner component, a Phase-Locked Loop (PLL) SI5345 capable to filter the jitter and produce a cleaner clock. A measurement of the jitter has been performed also on the clock treated by this filter and the results are shown in the right plot of Figure 19. The excellent filtering capability of the PLL is evident since the measured jitter is now 2.4 ps and the modulation components are almost gone.

The phase stability has been also tested using an oscilloscope in infinite persistence mode triggered on the transmitted clock. The receiver board has then been reset multiple times and the RX clock has been reconstructed always with the same phase distance to the TX clock every time the link has been

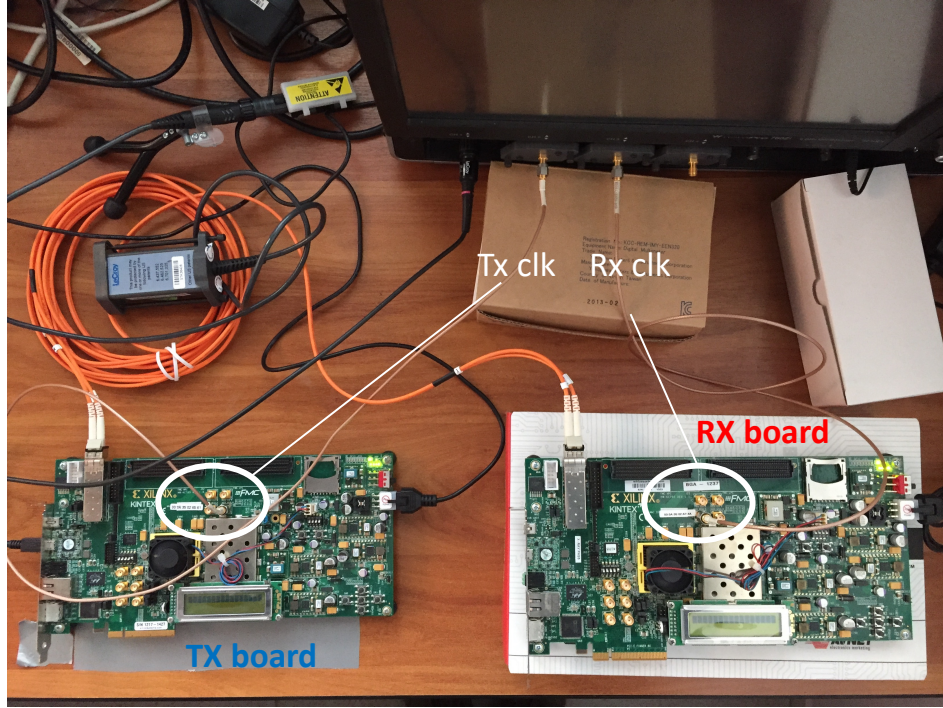


Figure 15: The custom solution test-bench based on the KC705 evaluation boards. On the left the first board is configured as transmitter (TX) and on the right, the second is configured as receiver (RX). In the photo, the orange optical fiber and the 2 cables that bring the transmitted and reconstructed clock to an oscilloscope are visible.

re-established.

The results of this extensive test campaign are very encouraging because all the Hyper-Kamiokande specifications are largely met and this clock distribution scheme is mature enough to be used in the experiment. The R&D described here shows different important aspects of the proposed solution. The method used and the selected components, including the jitter cleaner to be hosted on the FE side, are very effective and can mitigate eventual noise issues that will be discovered in the later integration stage. The group has enough skills in time distribution to analyze, identify problems and solve them.

4.3 Time Distribution Module (TDM)

The number of slaves to be served, i.e. the front-ends, in the HK case, doesn't allow the implementation of all the master's functionalities on a single electronics board hence they have to be divided upon different cards, called Time Distribution Module (TDM), as depicted in the block scheme of Fig. 1.

Each TDM is also connected to the data acquisition system using a standard Ethernet link to exchange slow control information, like the upload firmware for the FE's FPGAs or the acquisition-related commands, and pass them to all the front-end modules connected to it. A non-deterministic channel from the in-water electronics to the TDM is also established and is used to send housekeeping information and slow control data to the DAQ.

Each time distribution module is designed to perform the following tasks:

- Receive the master clock and distribute it embedded into time-related data with a jitter at the endpoint smaller than the experiment's requirement.
- Guarantee a constant channel-to-channel phase difference over each reset and power-up compensating the differences introduced by different cable lengths.
- Guarantee a bidirectional data bandwidth of at least 100 Mbps (at net of the data encoding).
- Communicate to the data acquisition system to exchange slow control data.

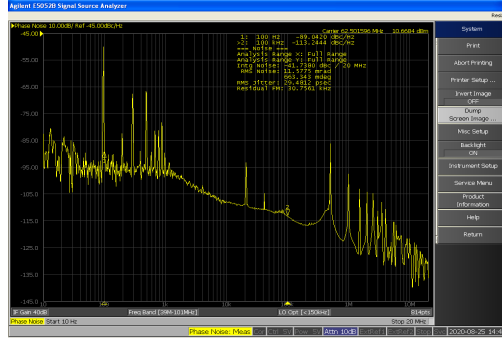


Figure 18: Frequency domain jitter measurements for the CDR solution implemented on the KC705 evaluation used as the master. In the frequency domain, the total jitter has been measured at 29.5 ps with evident components at 500 kHz.

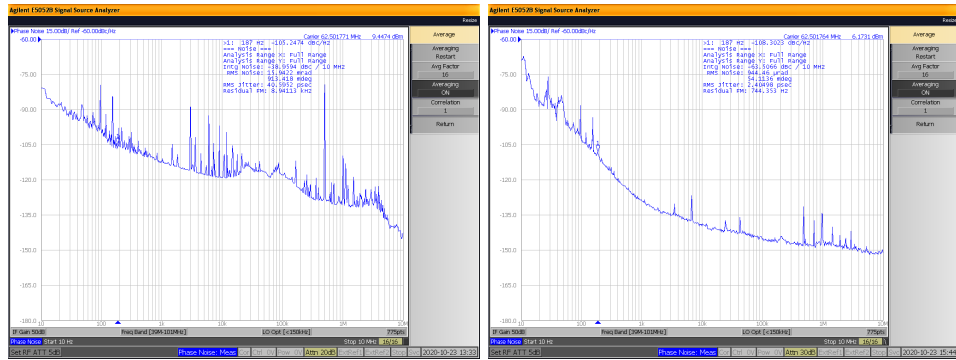


Figure 19: Frequency domain jitter measurements performed on the clock reconstructed by the custom board. On the left is the clock before the jitter cleaner PLL and on the right as measured after the filter.

group, two fibers are used to receive the reference clock and two the synchronous data from the main and spare first distribution layer. The last main section is devoted to DAQ communication where 2 1Gbps Ethernet links are implemented. The board design is completed by all the circuitry needed to power and control the optical transceivers and to monitor the system's environmental and operation parameters.

The first prototype of the time distribution module has been designed in December 2021 and the fabrication started in March 2022. A picture of the board layout is reported in Figure 20.

Reliability To guarantee the same front-end's operative level for more than 10 years reducing the maintenance at a minimum level, specific care must be devoted especially to the electro-optical transceivers used to connect the TDMs and the FEs, them being the most critical component in terms of lifetime. To mitigate any possible failure related to the loss of transmission, each second distribution layer board will be equipped with 2 separate fibers connection to each front end driven by the same ser-des. Only one of them will be active at any given time. The switching mechanism will be supervised by software and will be activated by an explicit configuration command sent by the DAQ. This “manual” procedure is preferred to an automatic one that could detect the link status autonomously as an extra security level to avoid any possible mistake that could prevent the link lock. Technically, the switching mechanism is implemented using a 1 to 2 high-speed multiplexer designed specifically for high-speed data lines. The activation of one output or the other is done via some control pins connected to the FPGA. On the prototype board, 2 slightly different multiplexers have been used on different data channels with the goal of testing them and selecting the most suited for this specific application.

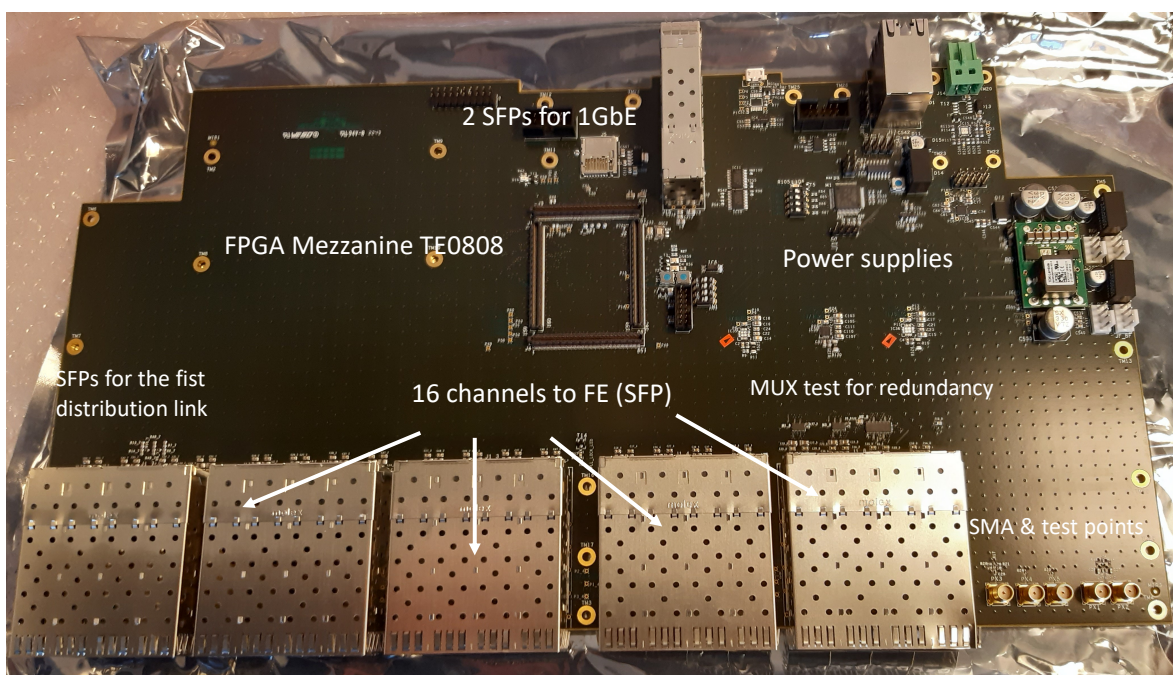


Figure 20: Second stage time distribution module prototype board layout.

Another very important aspect to enhance the electro-optical transceiver reliability is the selection of the component itself. To find the device that meets all the experiment's requirements, a market survey has been carried out and specific reliability characterization documents have been received from different producers. The study has brought to the selection of the Avago AFB5718APZ. This transceiver, compatible with the Small Form-Factor Pluggable (SFP) standard, is designed for data rate up to 1Gbps, it is capable to drive multimode fibers and is a great compromise in terms of mean time to failure (MTTF), power dissipation, performance, and price. The failure in time (FIT, defined as $1/\text{MTTF}$) is about 47 at 35°C and about 59 at 45°C . As evident for these two values and in line with the standard behavior of the electronic components, the operative temperature plays a crucial role in terms of reliability.

During the lifetime of the experiment, the boards' parameters will be constantly monitored to identify any early sign of malfunctions. Thanks to the modular design of this board, different levels of intervention can be planned to meet the required reliability goal. The first envisions changing the SFP modules when they stop working or when the critical parameters (e.g. optical budget, power consumption or temperature) are measured out of a safe range. This operation is expected to be performed without extra detector dead time thanks to the redundant links and hot-plug SFP's feature. The second level of intervention envisions the change of the FPGA's mezzanine card which is the most critical and complex element of the board. If a problem will be identified on the TDM motherboard then it will be changed with another unit. The last two levels, obviously, require a data acquisition stop but it should be relatively easy and fast. To accomplish this plan a series of spare parts will be kept at the far detector's site and the stock will be constantly re-populated by the time distribution group.

Power Consumption Estimation and Physical Dimensions The TDM is powered with a single 24 volts line and, on the board, the needed circuitry to produce all the required voltages is implemented. A first estimation based on previous experiences and tools available for the FPGA produces predicts a total power dissipation of about 5W for the FPGA part which would bring the total board consumption at 50W considering about 40 W for the optical transceivers and 5W for all the other components. A more precise assessment will be done once the prototype will be tested. All the board characteristics are summarised in the table below.

Table 5: Time distribution module board expected power and physical characteristics

Board Dimension (WHL) in mm	Power	Operating Conditions (temperature °C and humidity)	Position	Quantity Needed
214x45x400 1 kg	50W@24V	+10/+40 5%/95% (non condensing) RH	Electronic Huts	67

5 Time Distribution Endpoint

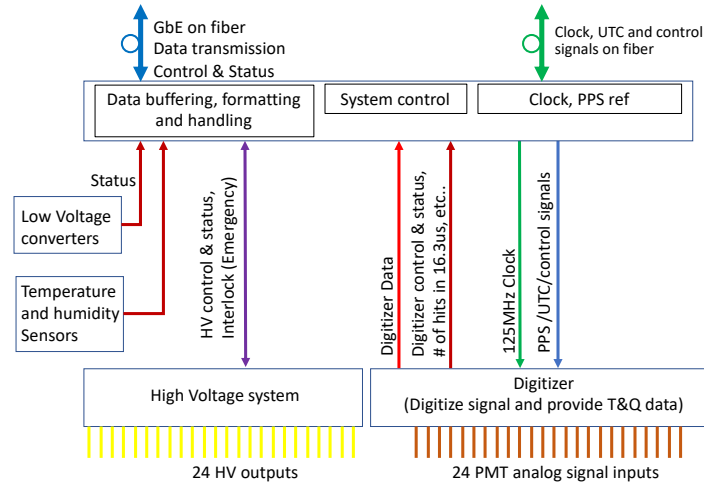


Figure 21: A front-end electronics scheme with all the functional blocks reported. The shown grouping doesn't necessarily reflect the final hardware arrangement.

The Time Distribution Endpoint (TDE) is the entity integrated into the front-end electronics that receives the data stream from the Time Distribution Module, reconstructs the embedded clock, and cleans it by means of a PLL. A FE general block scheme that reports all the logic elements is depicted in Figure 21. The TDE will be integrated into the data concentration board and it will consist of two optical transceivers (to serve the link redundancy explained before), the PLL, and a firmware IP to handle the time data stream and extract the clock from data. All these elements will be provided as part of the time distribution package.

Since the established channel will be also used to exchange slow control data between the front end and the DAQ, the firmware IP will have an interface to share this information. This proposed piece of firmware has been already tested as presented in the previous section.

6 Contributions to the timing monitoring and slow control system

6.1 Slow control needs for the time generation and distribution system

The time generation and distribution systems will be functioning for more than one decade after its installation. Since each beam or astrophysical event needs to be time-tagged, it is essential to detect any malfunctioning as early as possible and repair them in order to avoid event rejection because of poor timing. Therefore the monitoring and slow control of the timing system must be designed with high-reliability requirements. During the R&D phase described in Section 2, basic slow control was developed; this should be expanded into a more stable long-term system that is expected by the HK collaboration.

Figure 22 shows a simplified version of the overall diagram shown on Figure 1, but including the expected connections with the timing system instruments and the interfaces with the DAQ and Calibration PCs. The timing Slow Control system would be responsible of the health monitoring of

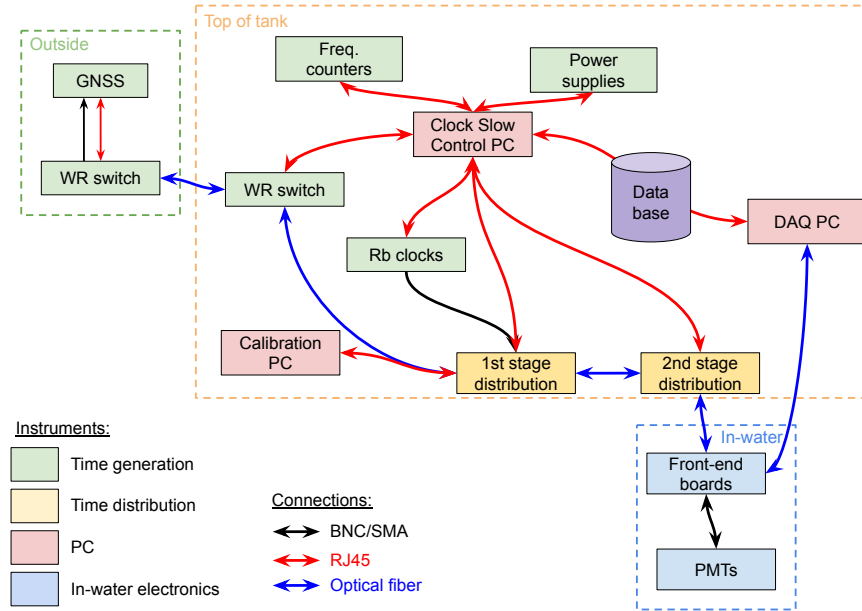


Figure 22: Simplified scheme of the Slow Control system for the timing system (time generation and distribution), and its interface with other groups, such as DAQ and Calibration.

the instruments used for the clock generation (Rb clocks and frequency counters), comparison with the GNSS receivers (including the WR link), and first and second stage distribution boards (including the health of the link to the front-end boards and the power-supplies powering the boards). In particular, several critical items needs to be properly defined and implemented:

1. The corrections to the local time base obtained by using the CGGTTS files generated by the GNSS receivers and produced by the Slow Control PC via algorithms presented in Section 2.4 need to be provided to the DAQ to be applied during the event online reconstruction.
2. The Calibration PC will send periodic calibration signals that needs to be time-tagged via the first stage distribution board and then distributed to the front-end boards and DAQ.
3. As shown by Figure 1, the timing system has a redundant chain that needs to be monitored; in particular, if a significant time drift is observed on the main timing chain by comparison with the redundant chain and backup Rb clock, it would be necessary to be alerted and possibly take actions remotely (re-tuning of the Rb clock frequency, switching to backup timing chain etc).

6.2 Deliverables from IN2P3

As mentioned above, the development of the timing system slow control was initiated during the R&D phase. Python scripts were created to control the Rubidium and PHM clocks, and frequency counters and will be used as a starting point for the slow-control and data acquisition system. We plan to develop a more reliable infrastructure using these and to-be-developed scripts. One of the first tasks is to coordinate with the other HK working groups to better define the common infrastructure to be shared among all the collaborators. In particular, a possibility would be to use the software developed by the DAQ group, the advantage being that this would help unifying the interfaces: the main issue with this is that the amount of work to develop something suitable for online monitoring and slow control (definition of the communication model and the exchanged data model, development of a web interface, development of an interface with a database...) would be rather large. Another option would be to use the MIDAS framework which is currently used for the ND280 DAQ and slow-control system: the advantage is that this software is very well known to collaborators (LPNHE and IRFU) and would allow to have all the required features out-of-the-box, but could limit the inter-connectiveness between the timing system and the DAQ one. Therefore the first task of defining timing slow-control framework is a rather important one, as it will have impacts on the overall amount of work.

The planned timeline and the main milestones are given in the following list:

- Until Summer 2023: Survey of the available software framework and definition of a common structure (discussion within the HK Collaboration)
- Until end of 2023: Definition of the interfaces with other groups and computing system e.g. DAQ and Calibration.
- Until end of 2023: Implementation of the base interfaces with each instrument (GNSS, White Rabbit switch, powersupplies control...)
- Until end of 2024: Implementation of the control of first and second stage distribution boards
- From mid 2023 until end of 2025: First implementation into a common software framework and long-run validation on test setup at LPNHE
- From end of 2025 until mid-2026: Installation and integration at HK Far Detector and J-PARC
- During HK Far detector filling: System commissioning at HK Far Detector and J-PARC by LPNHE collaborators

7 Estimation of Cost, Human Resources, Project Schedule and Technology Readiness Level (TRL)

7.1 Cost Estimation

As described above, during the ongoing R&D phase, most of the instruments' samples to be used in the final Hyper-Kamiokande time distribution system have already been purchased and the prototypes for the custom boards have been designed providing a fairly accurate idea of the proposed system's total cost. However, the global conjuncture and the ongoing electronics components' procurement crisis, could produce a relevant cost increase so the reader should evaluate the presented numbers in light of these two relevant considerations.

This estimation follows the same scheme used for the rest of the document subdividing the total cost into 3 parts related to the different subsystems of the proposed architecture. The price will be shared between the three proponent institutes in parts that will be decided at a later stage.

Time base generation and UTC The cost of the time base generation and UTC section is largely dominated by the prices of the needed instruments i.e. the atomic clock and the 2 GNSS receivers connected to 1 antenna. Considering a price of about 5.000 euros per atomic clock, 13.000 euros per GNSS receiver, and 4.000 euros for the antenna, the total cost of each chain would sum up to 35.000 euros. To enhance the system's reliability, 2 full chains will be deployed and a frequency/time comparator, quoted at 5.000 euros, will be needed to correlate them. The needed White Rabbit network to link the instruments costs about 16.000 euros, the UPS (uninterruptible power supply) system is quoted at 2.000 euros, and a small computer system to monitor the different instruments is about 2.000 euros. Summing up all the items, the total cost for the time base generation and UTC part would be about 100.000 euros.

Clock distribution network The clock distribution network cost heavily depends on the number of nodes to be served which varies on the different architectures presently studied. Another important element is the number of multiPMTs that will be installed on the far detector. At this time the final numbers are not definitively set then, for sake of clarity, this cost estimation is done considering the best guess of 1.000 FEs. Knowing that each second distribution layer board serves 16 FEs, then the total number of boards would be 63 plus 4 spares. Assuming a cost per unit of 4.000 euros the total amount would be about 268.000 euros. Two first distribution layer elements will be enough to complete the network and two others will be built bringing this part cost to about 20.000 euros. The system is completed with the needed power supplies for about 15.000 euros. The time distribution components in each FE would cost about 60 euros then a total of 60.000 euros needs to be budgeted.

The final cost estimate, including 20% contingency, is reported in the summary Table 8. It amounts to about 550 kEuros.

Annual maintenance cost After the installation and commissioning phase, the group will provide the time distribution system maintenance budget following the strategy highlighted in the previous sections. A total estimated cost of 10.000 euros per year is envisioned to cover both travel and equipment.

Time base generation and UTC at J-PARC As mentioned above, this group is proposing to implement at J-PARC a very similar system to the one for the far detector. The needs and, consequently, the proposal is not yet finalized but the basic idea is to install a system with very similar specs as the one envisioned for the time generation part of the far detector. The table 7 reflects this plan but it should be considered very preliminary. A more precise cost estimation will be done when the technical details will be sorted out.

7.2 Estimated human resources

To realize the entire project, including fabrication, testing, commissioning, and maintenance, the estimated total needed human resources is 6 full-time equivalent persons per year starting from the second half of 2022 to the end of commissioning. The required resources will come from the three

Time distribution network for the far detector			
Item	Cost per unit (euros)	Needed units	Total (euros)
Time base generation and UTC			
Atomic clock	5.000	3	15.000
GNSS receivers	13.000	4	52.000
GNSS antennas	4.000	2	8.000
Freq/time comparator	5.000	1	5.000
White Rabbit network	16.000	1	16.000
UPS	2.000	1	2.000
Computer infrastructure	2.000	1	2.000
Subtotal: Time base generation and UTC: 100.000			
Time distribution network			
First distribution boards	5.000	4	20.000
Second distribution boards	4.000	67	268.000
Power supplies	15.000	1	15.000
Time distribution endpoint	60	1.000	60.000
Subtotal: Time distribution network: 363.000			
Total including 20% contingency: 556.000			
Yearly maintenance cost: 10.000			

Table 6: Time distribution cost estimation considering the HK configuration with 1.000 FEs.

collaborating laboratories and will cover competencies in digital design, PCB design, cabling, board rework, software, and data analysis.

The LPNHE laboratory, part of IN2P3 and CNRS, is involved in many experiments in the area of high-energy particle physics and astrophysics. Its engineering group has very strong expertise in detectors and electronics design that include high-speed digital links, time distribution, low-noise analog frontends, and board design. The people involved in this proposal have already designed similar systems for other large-scale experiments, e.g. the LSST telescope and KM3NeT. The LPNHE group has also established a strong collaboration with SYRTE, the French laboratory part of the UTC consortium. In 2021 the LPNHE group has been funded by ANR, a French public national agency, for developing the time distribution for HK.

INFN Roma is involved in many experiments in the area of high-energy physics and astrophysics and its engineering lab and electronic workshop have very strong expertise in detector and electronics design, including data acquisition, low-noise analog frontends, high-speed sampling, high-speed digital links, time distribution, slow control, board design, and production. People involved in this proposal have already designed similar systems for large-scale experiments, like KM3NeT, BELLE2, BDX, and various smaller R&D projects.

The engineers from LPNHE and INFN Roma have a long history of collaboration that started in the year 2000. They have worked together on the time distribution systems in previous experiments implementing the same technologies as proposed here.

The IRFU/CEA institute is a laboratory that includes a dedicated engineering department for electronics and detector development (DEDIP). The institute has strong expertise and a very wide knowledge of related items with many previous contributions to similar systems. In particular, DEDIP has recently developed the time distribution system for the TPCs of the ND280 upgrade (the near detector of T2K which will be ported to Hyper-Kamiokande).

The IRFU and LPNHE groups have a long history of collaboration on electronics developments, a recent example is the development of the electronics readout for the TPCs of the ND280 upgrade where the two laboratories were in charge of developing respectively the two cards (FrontEnd Cards and FrontEnd Mezzanine) with an interface between them.

Table 8 summarises the human resources estimated for the LPNHE group expressed in FTE. These human resources include the Sorbonne Université PhD student Lucile Mellet who lead the instruments characterization efforts at LPNHE and developed the tools and corrections algorithms for the time transfer technique. Some seed funding money from Sorbonne Université via the AAP "Emergences

Time distribution network for J-PARC			
Item	Cost per unit (euros)	Needed units	Total (euros)
Time base generation and UTC at J-PARC			
Atomic clock	5.000	3	15.000
GNSS receivers	13.000	4	52.000
GNSS antennas	4.000	2	8.000
Freq/time comparator	5.000	1	5.000
UPS	2.000	1	2.000
Computer infrastructure	2.000	1	2.000
Subtotal: Time base generation and UTC: 100.000			
Time distribution network			
First distribution boards	5.000	4	20.000
Subtotal: Time distribution network: 20.000			
Total including 20% contingency: xxx.000			
Yearly maintenance cost: 5.000			

Table 7: Preliminary time generation cost estimation for the J-PARC system based on the idea of installing the same system envisioned for the far detector.

2019” program allowed the LPNHE group to initiate this project on the time generation for HK far detector. The ANR Bertha is now supporting the hiring of two ”CDD Chercheurs” who will devote part of their time on the implementation of the timing system instrumentation (monitoring, slow control, online timing corrections...) described in Section 6.2. These two financial supports turned out to be essential for the successful early start of the R&D of this project and the initial purchase of some of the critical items, such as the atomic clocks and frequency counters. Given the nature of such funding and the fact that the R&D work is finally complete, it is important IN2P3 fully supports this item, both in equipment, funding and person-power. In particular, the development of a reliable time generation system at HK far detector (and with a similar fraction at J-PARC) that works 24/7 requires dedicated efforts and therefore person-power: part of the needs for the initial developments will be covered as part of the BERTHA ANR and the LPNHE technical teams. However, such support will end before the installation of the systems at HK Far Detector and J-PARC. In addition, since it is necessary to maintain the time distribution and generation system for more than one decade, it seems essential that permanent staff scientists (and not just non-permanent physicists) get involved in this from the very start of such development with the expectation to maintain it afterward. Therefore the hiring of a new ”Chargé de Recherche” next year would be the perfect action to make sure this contribution is sufficiently staffed during the construction phase and the start of the data taking period.

2023	2024	2025	2026
2.8	2.5	2.6	2.1

Table 8: Human resources (FTE) allocated for the Hyper-Kamiokande time distribution system at LPNHE for the next 4 years.

7.3 Schedule

After the final design approval, the group is planning to work on the clock generation and UTC synchronization part operating the entire chain continuously for long periods in order to monitor the performance. It will be compared to the UTC(OP) time reference to discover possible weak points in the design. The two distribution layers’ first prototypes, already designed, will be tested until January 2023 then a second round of prototypes will be fabricated and tested until September 2023. The production candidates boards will follow in the period between September 2023 to the end of March 2024. The components procurement phase will take almost one year and the following production will start in November 2024 for about 6 months. The final product will be tested at the production site. The full schedule is presented in the chart of Fig. 23.

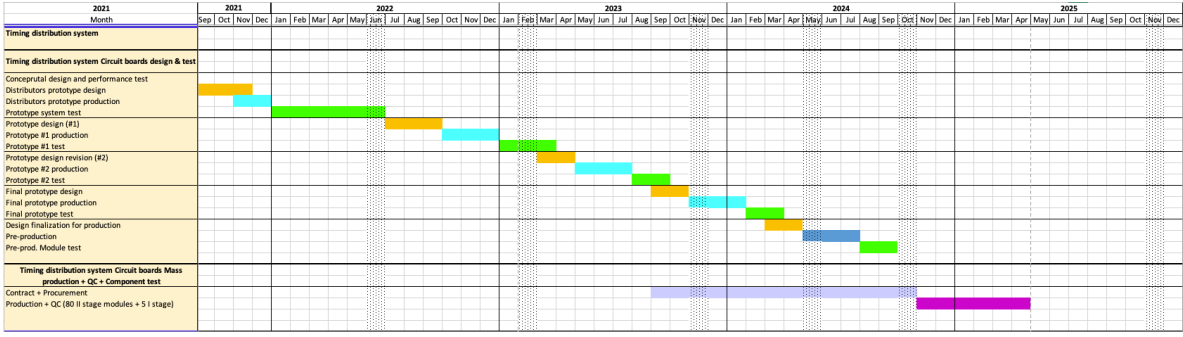


Figure 23: Proposed prototypes and production schedule for the time distribution boards.

7.4 Risk Analysis

In this section, a risk analysis for the time generation and distribution system is presented. The summary is given on the table 9 in which, a brief risk description, its level (moderate, high, or severe), the implemented mitigation strategy, and the level reached after mitigation are reported.

Table 9: Risk table of the Hyper-Kamiokande timing system

Risk Description	Risk level	Mitigation strategy	Risk level after mitigation
Electronic board production delay due to components' shortage	severe	Some of the most critical components e.g. FPGA mezzanine and SFP modules have been already purchased	high
Delay on calibration interface definition	high	The board are designed considering standard electrical interfaces in a number that would most likely exceed the calibration requests	moderate
Delay on other subsystems development that could have an impact on the time distribution development	high	A set of evaluation boards that can mimic the behavior of the different subsystem that communicate with the timing system has been purchased	moderate
Use of the Rubidium clock instead of Passive Hydrogen Maser	high	The errors in the time definition due to the use of a medium-level atomic clock can be compensated with more frequent correction but the long-term effects are difficult to evaluate for the time being	high

7.5 Technology Readiness Level

To establish the technology readiness level (TRL), the whole system has been divided into different parts and the level of each part has been described and evaluated separately. The result is reported in the table 10.

Table 10: Technology readiness level for the elements of the Hyper-Kamiokande timing system

Sub-component	Status Description	Readiness level
Time generation hardware selection and configuration	Most of the hardware components have been selected, the connection topology has been defined and long-term tests are ongoing at LPNHE with prototypes acquired in the past years. Only the final selection of the atomic clock has to be made.	8
First stage distribution board	The first prototype has been designed and fabricated. Tests are ongoing.	7
Second stage distribution firmware	The communication channel firmware (the core of the second stage distribution element) between the second distribution stage and the front end has been designed and validated on the selected FPGA. Integration tests with multiple channels are ongoing	7
Time distribution endpoint	The time distribution endpoint firmware is closely related to the second distribution stage firmware since they represent the two sides of the same communication link hence, they have the same level of maturity. The hardware components to be installed on the data processing board needed to implement the endpoint functionalities have been selected and validated	7

Appendix A UTC vs GNSS time

In this document, the terms “GNSS time”, the “UTC prediction” associated with it, and “UTC” itself are used interchangeably even though the first and second terms are less precise and could differ from the third one by an a-posteriori applied correction. It is worth highlighting here the difference between the various time scales and their dissemination to build the context in which the time measurements in Hyper-Kamiokande will be made. UTC is an International time scale computed monthly by the BIPM (Bureau International des Poids et Mesures) [21] following three steps. First, an ensemble of commercial atomic clocks spread in different countries produce their definition of the atomic time scale which average is called Echelle Atomique Libre (EAL)). The EAL steered in frequency on a group of Primary and Secondary Frequency Standards, and realizes the definition of the SI second (which is called Temps Atomique International (TAI)). Finally, the TAI becomes UTC by adding Leap Seconds to match the rotation of the Earth. The UTC is a “conventional” time scale calculated a-posteriori and made available by BIPM in its monthly Circular T [22]. National Metrology Institutes (MI) or Designated Laboratories (DL) produce physical realizations of UTC, namely UTC(k), where “k” is an acronym or a label for each given country/organization. In Circular T, the offsets between UTC and each UTC(k) are published.

On the other hand, each GNSS constellation has its own time scale, which is generically called “GNSS Time” (GPS Time, Galileo System Time (GST), and so on). In addition, the GNSS operators generate a UTC prediction, either internally or based on some existing UTC(k), to relate their internal time scale to the rest of the world. Some parameters included in the GNSS navigation messages allow making this correlation hence associating any ground user clock to this prediction of UTC. Circular T section 4 contains “Relations of UTC and TAI with the prediction of UTC(k) disseminated by GNSS” but this is currently only referred to GPS and GLONASS. This Section is about to be transformed to include similar information from other GNSS together with some uncertainty estimation (under discussions inside formal Working Groups). At present time there is not yet a formal wording for such prediction of UTC broadcast by GNSS.

Appendix B Time Distribution Data Format

The proposed communication protocol between the time distribution module and the endpoint in the front end is designed considering the need of sending a periodic TDC reset and the associated global coarse counter in a so-called synchronization packet without adding any extra delay as described in requirements 4 to 7. Along with it, a PPS and the relative time information, the PPS packet, must be sent, following the same scheme, whenever they are received from the clock generation and UTC section via the first distribution stage (requirement 8).

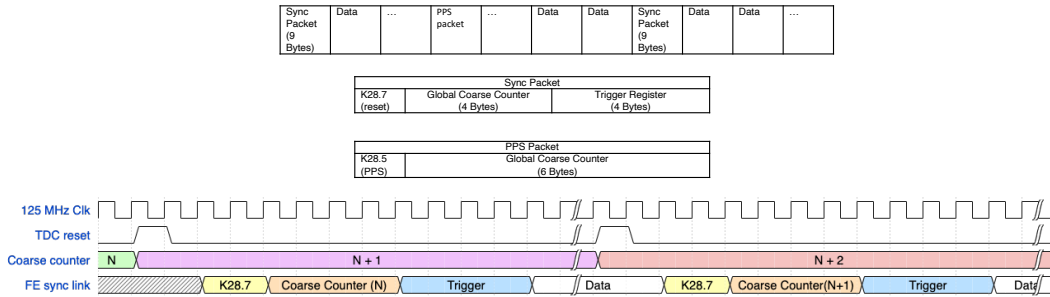


Figure 24: The sync and PPS packets. The top part contains an example of the data stream where a sync packet and a PPS packet are sent along with the non-synchronous data and the detail of the two packets. The timing diagram of the bottom part highlight the time relation between the TDC reset and the synchronous packet.

As highlighted in Figure 24, the synchronization packet starts with a “special” 8 bits character followed by the 4 bytes long TDC reset and a trigger message of the same length for a total of 9 bytes.

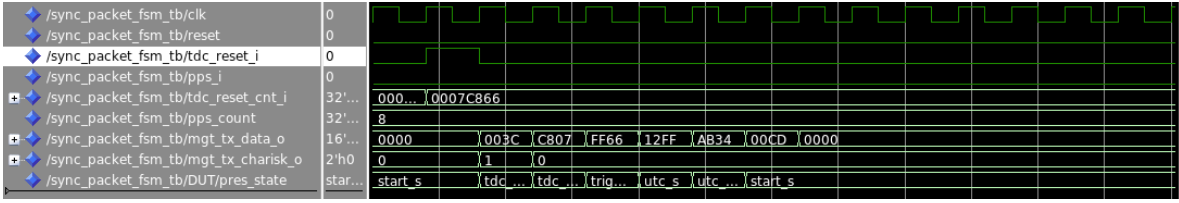


Figure 25: Simulation screenshot of a data stream associated with a TDC reset event.

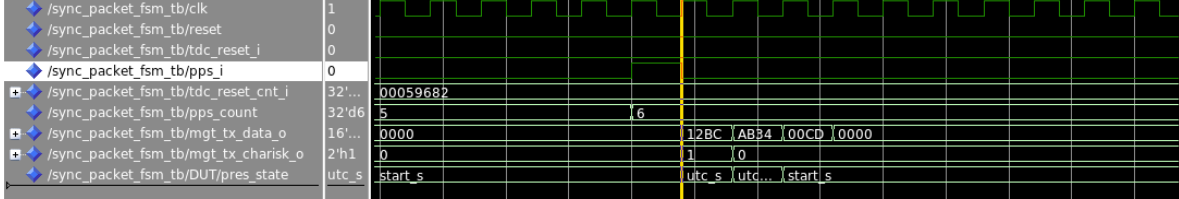


Figure 26: Simulation screenshot of a data stream associated to a PPS event.

The PPS packet is composed of another “special” 8 bits character plus the six bytes long UTC time. A third “special” 8 bits character is sent when the two signals are coincident followed by the PPS and sync packets. The actual selected TDC reset frequency is not a multiple integer of the 1 PPS then care must be taken in the design of a protocol to avoid any overlap between the two pieces of information that could bring loss of data and synchronicity. The minimum distance between the two packets has been calculated at 512 ns for a TDC reset sent at a frequency of 61.03 kHz and 64 ns for a TDC reset at 8.13 kHz which should guarantee no overlaps. Moreover, different simulations have been performed to confirm the feasibility of this idea. Some results are reported below.

Figure 25 shows the TDC reset packet as received from the time distribution endpoint while in Figure 26 a PPS packet is represented. Figure 27 shows the minimum distance in time between the two packets and Fig. 28 describes the case when the TDC reset signal and PPS overlap. All the reported plots are done simulating a firmware code compatible with the proposed ser-des hence it is ready to be implemented in the FPGA. This explains the reason for the 16-bit data bus (mgt_tx_data_o) and a clock at 62.5 MHz instead of the 125 MHz system frequency that would be associated with an 8-bit bus. To mark the start of each packet three 8b10b K-characters have been selected: K28.1, K28.5, and K28.7. The line mgt_tx_charisk_o is active when these words are received.

The actual data line will then be periodically occupied by these packets otherwise it will be available to send other information to the front end. To avoid any possible interference a bus arbitration system will be implemented on the TDM FPGA to give priority to the periodic packets over the non-synchronous data.

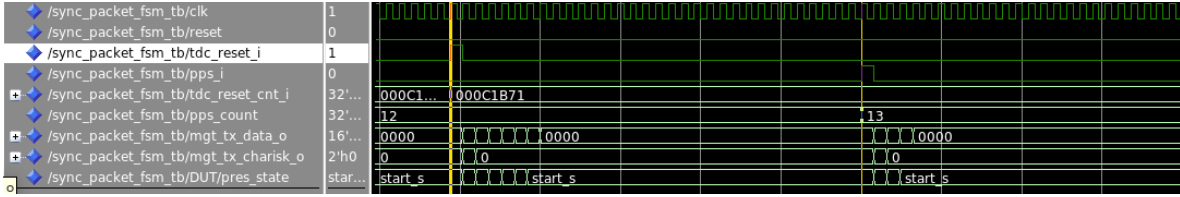


Figure 27: Simulation screenshot of the minimum distance between the TDC reset and PPS.

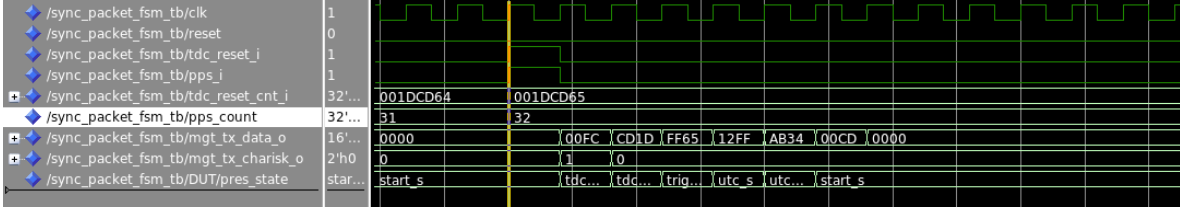


Figure 28: Simulation screenshot of a data stream associated to a PPS event and TDC reset in phase.

Appendix C CGGTTS file example

An example of the CGGTTS generated by the Septentrio GNSS receiver containing the time distances between the local time and GNSS time is given below. The explanation of different fields is given in [5]. Specifically, the field that reports the time difference measure between the local PPS and the GNSS system time is marked as “REFSYS”.

```
CGGTTS  GENERIC DATA FORMAT VERSION = 2E
REV DATE = 00-00-000
RCVR = PolaRx5TR (5.3.2)      SN3222543
CH = 80
IMS = PolaRx5TR
LAB = LPNHE
X = 4201670.132 m
Y = 172825.507 m
Z = 4779558.436 m
FRAME = ITRF
COMMENTS = LS=18; ElMask=0deg;
INT DLY = 25.8 ns (GPS P1), 22.9 ns (GPS P2)    CAL_ID = Calibration at OP vs OP73
CAB DLY = 505.0 ns
REF DLY = 0.0 ns
REF = SRS
CKSUM = 0b
```

SAT	CL	MJD	STTIME	TRKL	ELV	AZTH	REFSV	SRSV	REFSYS	SRSYS	DSG	IOE	MDTR	SMDT	MDIO	SMDI	MSIO	SMSI	ISG	FR	HC	FRC	CK
			hhmmss	s	.ldg	.ldg	.ins	.lps/s	.ins	.lps/s	.ins	.ins.lps/s.lns.lps/s.lns.lps/s.lns											
G02	FF	59693	001800	780	452	2678	6018322	-271	-513936	-272	13	61	114	3	102	13	102	13	10	0	0	L3P	6E
G04	FF	59693	001800	780	166	700	1219828	-282	-513956	-249	39	13	281	99	134	6	134	6	30	0	0	L3P	7C
G05	FF	59693	001800	780	183	3026	279947	-180	-513955	-194	43	80	257	-89	139	-78	139	-78	31	0	0	L3P	E7
G06	FF	59693	001800	780	351	2017	-3291323	-407	-513924	-267	25	35	141	27	125	25	125	25	19	0	0	L3P	A6
G07	FF	59693	001800	780	625	1419	-3723689	-282	-513929	-272	15	17	91	-5	82	6	82	6	12	0	0	L3P	68
G09	FF	59693	001800	780	505	677	2902993	-274	-513932	-248	13	73	105	11	76	-5	76	-5	9	0	0	L3P	69
G16	FF	59693	001800	780	118	411	4432147	-121	-513927	-158	42	51	387	16	78	-82	78	-82	27	0	0	L3P	98
G20	FF	59693	001800	780	460	3001	-5670792	-232	-513930	-234	22	25	113	-13	89	-22	89	-22	18	0	0	L3P	A5
G29	FF	59693	001800	780	76	3256	4549643	-265	-513933	-306	45	31	577	14	122	28	122	28	32	0	0	L3P	A2
G30	FF	59693	001800	780	430	1808	4737062	-227	-513927	-243	11	69	119	-17	108	-25	108	-25	9	0	0	L3P	BC
G02	FF	59693	003400	780	429	2582	6018078	-290	-514181	-291	16	61	119	7	97	25	97	25	15	0	0	L3P	7E
G04	FF	59693	003400	780	108	734	1219556	-206	-514197	-173	47	13	426	221	131	-57	131	-57	33	0	0	L3P	B7
G05	FF	59693	003400	780	247	3041	279725	-234	-514191	-247	23	80	193	-50	108	-35	108	-35	16	0	0	L3P	B3
G06	FF	59693	003400	780	278	1990	-3291736	-427	-514203	-287	19	35	173	43	160	37	160	37	15	0	0	L3P	BE
G07	FF	59693	003400	780	668	1273	-3723954	-243	-514184	-234	9	17	88	-2	76	-31	76	-31	8	0	0	L3P	82
G09	FF	59693	003400	780	438	715	2902707	-311	-514193	-285	15	73	117	15	86	18	86	18	14	0	0	L3P	7C
G13	FF	59693	003400	780	93	2527	-3509066	-385	-514229	-318	60	62	489	-295	219	-5	219	-5	37	0	0	L3P	D2
G16	FF	59693	003400	780	107	346	4431922	-143	-514187	-179	41	51	422	60	80	-90	80	-90	28	0	0	L3P	86
G20	FF	59693	003400	780	528	2978	-5671045	-279	-514184	-281	20	25	102	-9	84	3	84	3	17	0	0	L3P	6F
G29	FF	59693	003400	780	69	3192	4549421	-195	-514195	-236	40	31	630	101	120	-3	120	-3	27	0	0	L3P	8A
G30	FF	59693	003400	780	506	1790	4736816	-227	-514189	-243	16	69	105	-12	106	-32	106	-32	13	0	0	L3P	C3
G02	FF	59693	005000	780	393	2496	6017819	-247	-514441	-248	20	61	128	12	106	1	106	1	15	0	0	L3P	6E
G04	FF	59693	005000	780	51	770	1219233	-296	-514489	-263	69	13	850	802	157	-54	157	-54	47	0	0	L3P	C0
G05	FF	59693	005000	780	314	3047	279480	-228	-514449	-241	22	80	155	-31	102	-23	102	-23	15	0	0	L3P	9C

G06	FF	59693	005000	780	206	1968	-3292092	-447	-514425	-307	32	35	229	77	156	58	156	58	23	0	0	L3P	C8
G07	FF	59693	005000	780	686	1080	-3724228	-272	-514450	-263	8	17	87	0	80	-7	80	-7	6	0	0	L3P	40
G09	FF	59693	005000	780	373	754	2902425	-320	-514450	-294	24	73	133	20	93	33	93	33	20	0	0	L3P	61
G13	FF	59693	005000	780	151	2569	-3509374	-275	-514472	-208	40	62	308	-118	183	-52	183	-52	30	0	0	L3P	EA
G16	FF	59693	005000	780	87	285	4431668	-329	-514476	-365	50	51	517	146	101	104	101	104	37	0	0	L3P	B4
G20	FF	59693	005000	780	593	2926	-5671300	-236	-514442	-238	17	25	94	-6	75	-28	75	-28	12	0	0	L3P	9A
G29	FF	59693	005000	780	53	3130	4549211	-266	-514445	-306	80	31	802	282	114	22	114	22	49	0	0	L3P	92
G30	FF	59693	005000	780	582	1758	4736573	-253	-514447	-268	17	69	95	-8	98	-6	98	-6	13	0	0	L3P	90
G02	FF	59693	010600	780	346	2424	6017566	-253	-514695	-255	24	61	142	19	120	-7	120	-7	20	0	0	L3P	8B
G05	FF	59693	010600	780	382	3044	279240	-271	-514702	-285	26	80	131	-21	92	-5	92	-5	19	0	0	L3P	69
G06	FF	59693	010600	780	137	1948	-3292524	-419	-514722	-280	37	35	339	167	204	33	204	33	25	0	0	L3P	C9
G07	FF	59693	010600	780	672	888	-3724479	-253	-514692	-244	8	17	88	2	68	-25	68	-25	6	0	0	L3P	79
G09	FF	59693	010600	780	310	794	2902160	-302	-514690	-275	32	73	157	29	95	12	95	12	24	0	0	L3P	6F
G13	FF	59693	010600	780	210	2612	-3509656	-270	-514690	-203	34	62	225	-62	132	-67	132	-67	25	0	0	L3P	CB
G16	FF	59693	010600	780	57	231	4431471	-159	-514708	-195	69	51	759	407	76	-56	76	-56	45	0	0	L3P	AF
G20	FF	59693	010600	780	651	2829	-5671555	-261	-514699	-263	12	25	89	-4	76	-8	76	-8	10	0	0	L3P	88
G30	FF	59693	010600	780	655	1696	4736350	-218	-514685	-234	9	69	89	-5	80	-40	80	-40	7	0	0	L3P	79

Appendix D Interfaces

Origin	Destination	bidirectional	# of lines	Protocol	Kind of data
2 nd distribution stage	FE (DPB)	NO	1 (fiber)	custom 1Gbps serial	Time, clock, sync commands and slow control
FE (DPB)	2 nd distribution stage	NO	1 (fiber)	custom 1Gbps serial	Slow control
DAQ	2 nd distribution stage	YES	2 (fiber)	Gigabit TCP/IP	Slow control and house keeping
1 st distribution stage	2 nd distribution stage	NO	1 (fiber)	Custom	Clock
1 st distribution stage	2 nd distribution stage	NO	1 (fiber)	Custom	Sync commands and counter
DAQ	1 st distribution stage	YES	2 (fiber)	Gigabit TCP/IP	Counters time tags, slow control and house keeping
Calibration System	1 st distribution stage	NO	Up to 16 (NIM, copper)	Custom	Calibration data and commands
Atomic clock	1 st distribution stage	NO	1 (2.5V pp, copper)	Custom	5 MHz clock
1 st distribution stage	GNSS receiver (x4)	NO	2 (fiber)	Encapsulated in WR gigabit ethernet	10 MHz clock and 1 PPS
GNSS septentrio (x4)	DAQ	YES	2 (fiber)	Gigabit TCP/IP (via WR)	CGGTTS files to measure the phase, NTP distance to UTC and control data
Time Freq comparator	DAQ	YES	4 (copper)	Gigabit TCP/IP	Phase distance between the 2 local time references (main and spare)

Time distribution system interface table. The listed optical standards are defined by the specific SFP used and are not bound to the board. At the moment 850 nm is used. The electrical standards are self-defined for protocols like Ethernet.

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