



T2K-ND280-022

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T2K ND280 Upgrade Document
-
HA-TPC
FRONT END CARD (FEC)
FUNCTIONAL TESTS MANUAL

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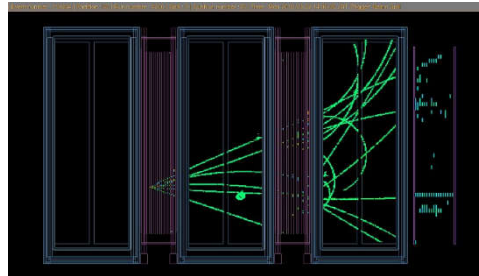
Abstract

This document describes the tests to be realized and the relevant test bench dedicated to perform functional tests on FEC boards.

Date: 21.03.2023

Version: 1.0

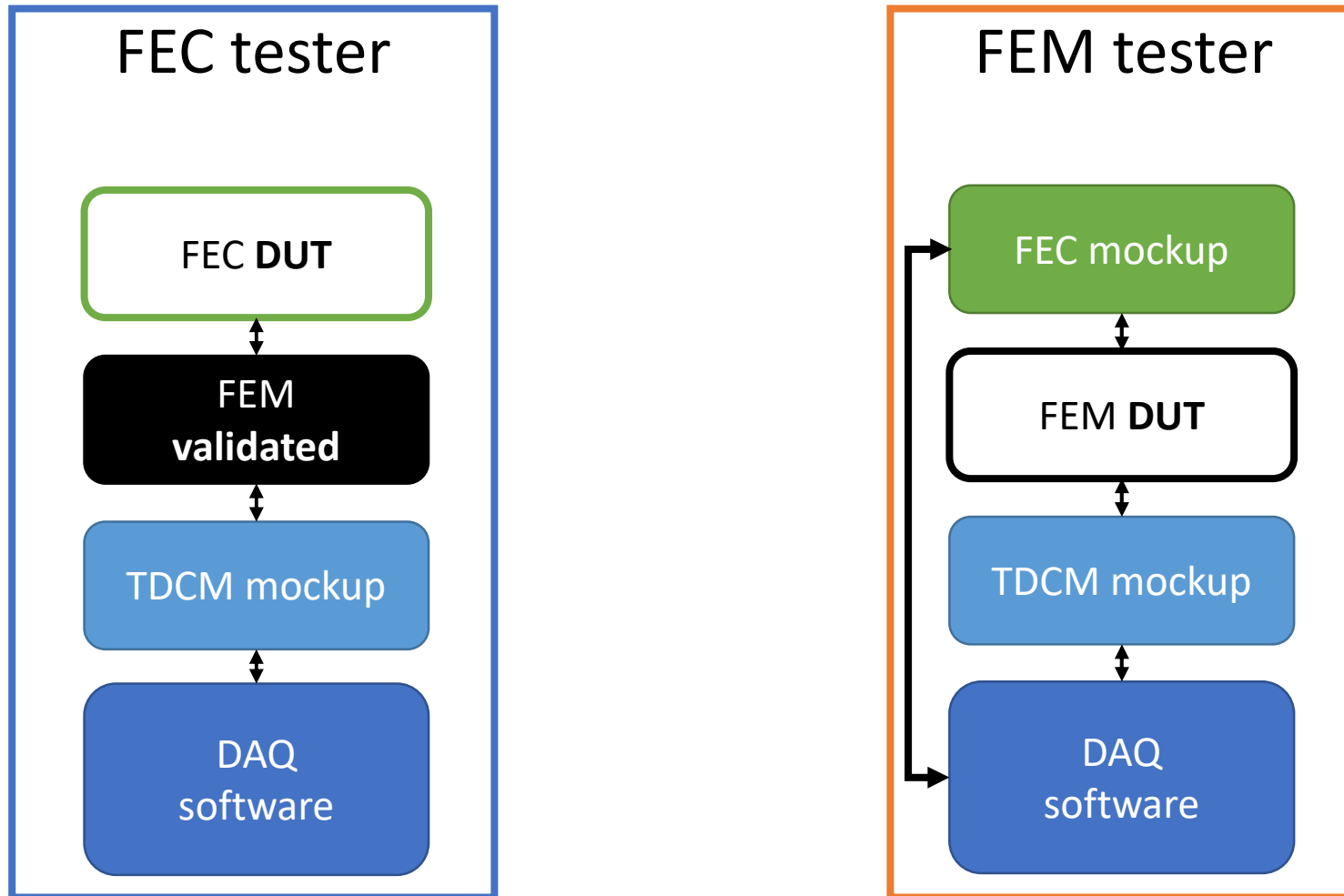
**Warsaw University
of Technology**



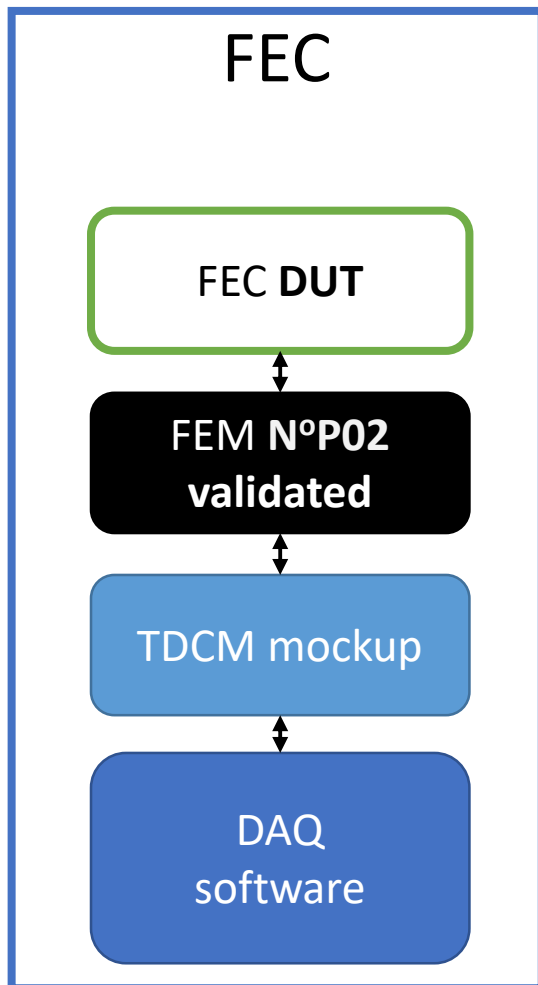
FEC/FEM Test Bench for electronics 10.2020

Andrzej Rychter
Warsaw University of Technology

Testing electronics



FEC production testbench



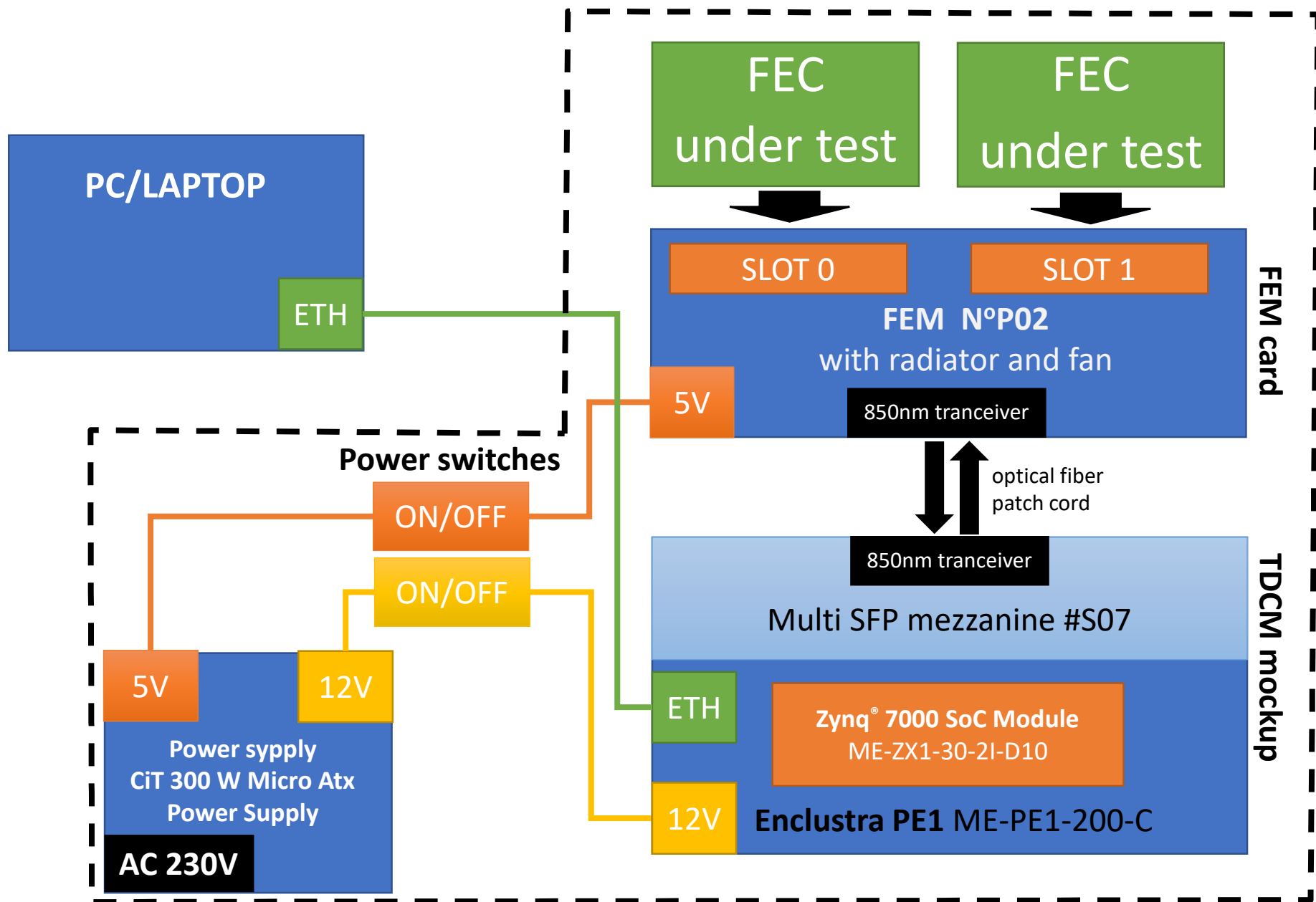
Tdcm mockup:

- Enclustra ME-PE1-200-C
- Enclustra Xilinx® Zynq® 7000 SoC Module ME-ZX1-30-2I-D10
- Multi SPF mezzanine #S07
- Firmware:
BOOT_tdcm_pe1_7z030_xemacps_02sep20.bin

What should be tested?

1. write and read-back in at least one slow control register of every AFTER chip
2. read-back the serial ID; voltage, current and temperature of the DS2438 chip of the FEC
3. Make a pedestal run and check the rms of every channel against an acceptance window
4. Try to control the ADC, configure a test pattern, get data and check them
5. Set the on-board pulser to a given amplitude and record at least one event with one channel pulsed in every AFTER chip.

FEC tester –basic system schematic



FEC tester

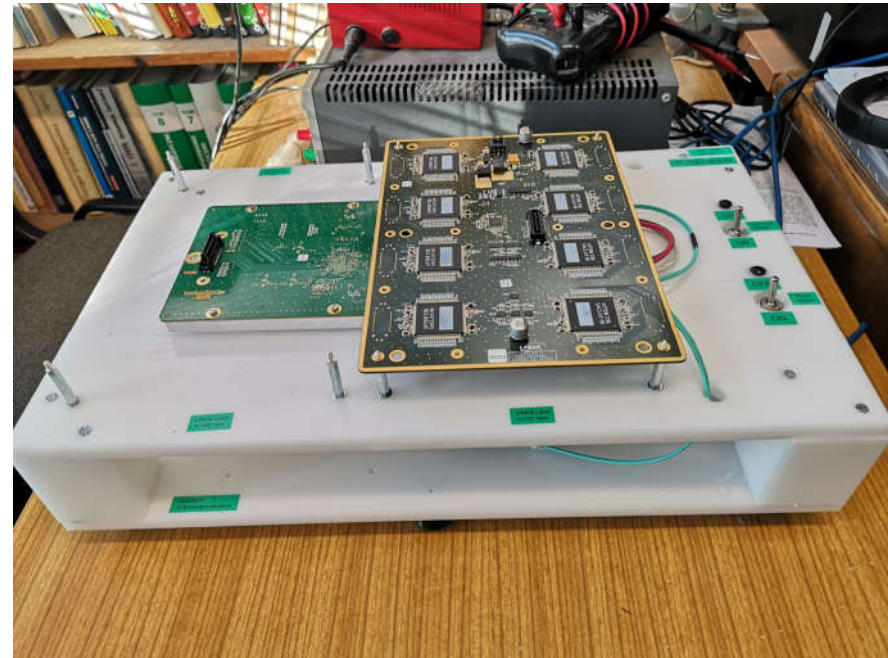
Bottom side:

1. AC 230 power supply: CiT
300 W Micro Atx Power Supply
 - 5V 16A
 - 12V 14A
2. TDCM mockup



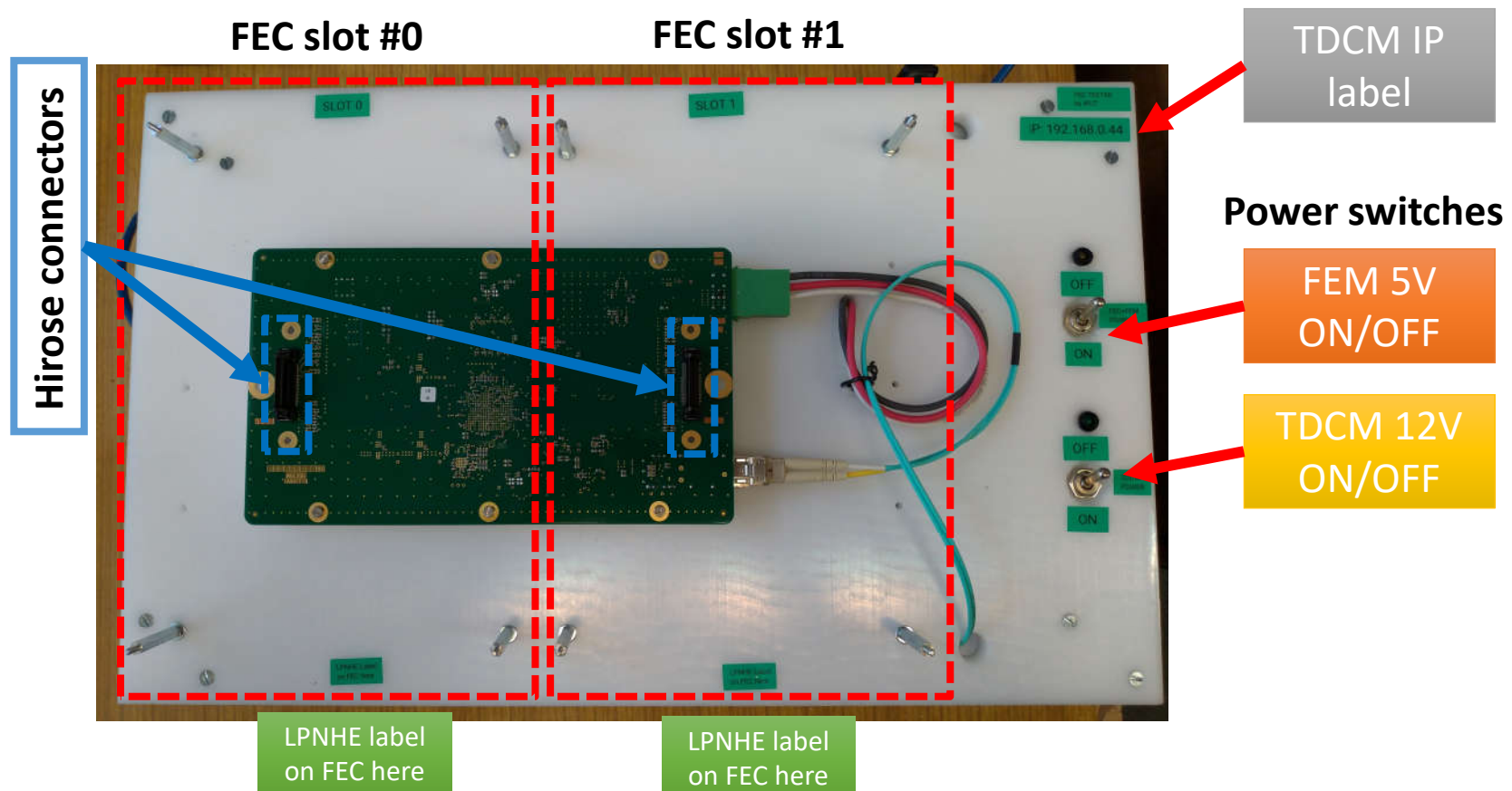
TOP side:

1. Power switches:
 - 5V FEM power
 - 12V TDCM power
2. FEM N°P02 with radiator and fan



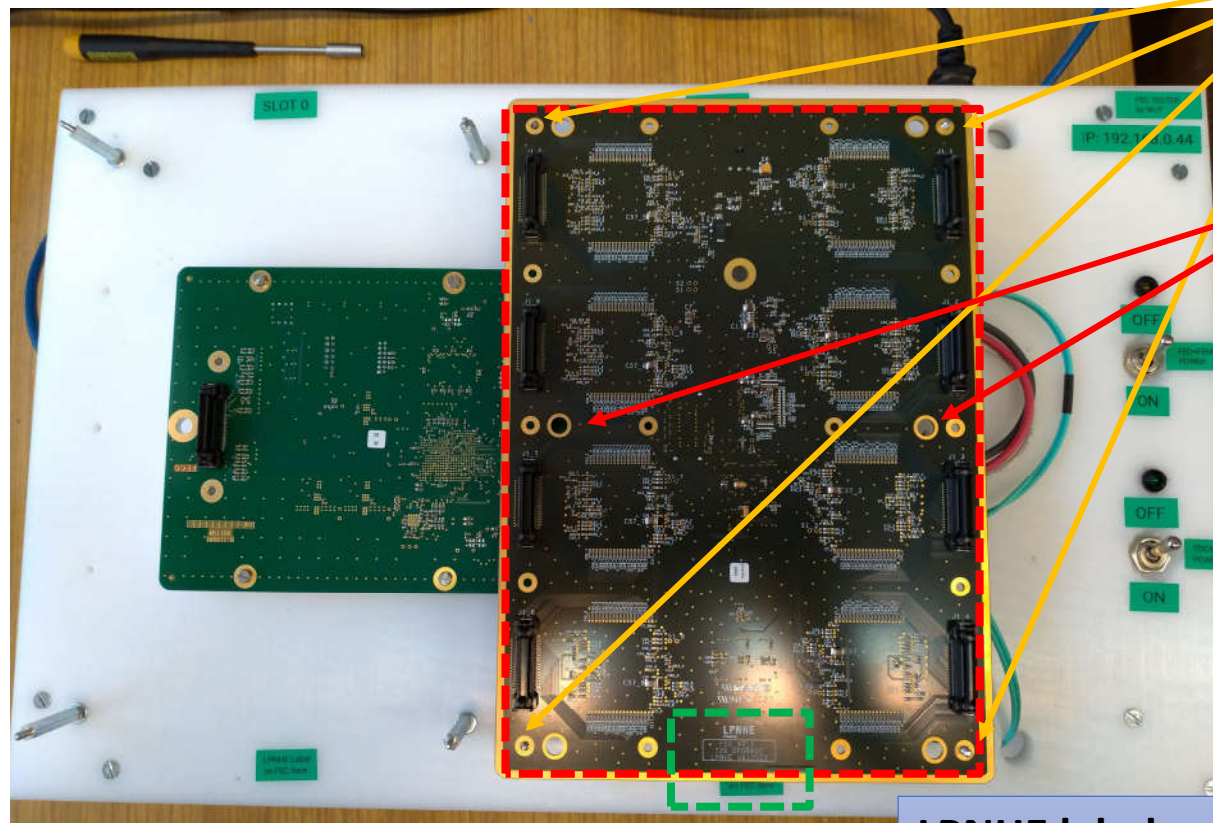
FEC tester – top view

- both FEM slots can be used for testing
- TDCM + FEC must be power cycled prior any test
- each slot is equipped with 4 metal spacers for FEC alignment
- FEC orientation -> check LPNHL label on FEC card



FEC tester – FEC plugging in

1. **Turn OFF** power supply
2. FEC card facing up with 8 Hirose connectors
3. 4 corner holes aligned with 4 metal distances
4. LPNHE label at bottom
5. Press gently in the middle of FEC card to ensure proper connection



4 metal distances aligned with 4 corner holes on FEC

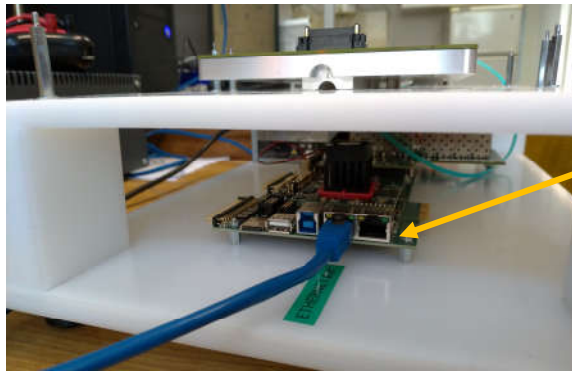
Press gently with antistatic gloves on

LPNHE label on FEC here

LPNHE label on FEC must align with bottom sticker

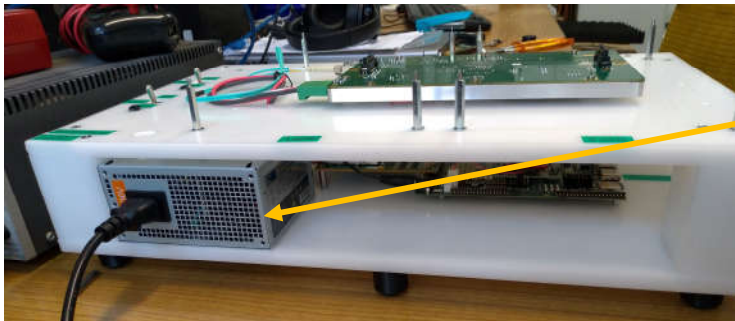
FEC tester – connecting to PC

1. IP of PC should be in network 192.168.0.XXX
2. TDCM IP number is 192.168.0.44
3. Connect TDCM with computer using Ethernet cable



TDCM Ethernet connector is next to USB – check Ethernet sticker

4. Ensure that both power switches are in **OFF** position
5. Plug in AC 230V power cable


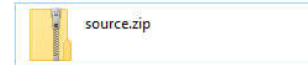


**Side view of FEM tester
CiT power supply**


6. Turn on TDCM power supply
7. Check Ethernet connection -> ping 192.168.0.44

FEC tester – setting-up environment

1. Create a folder for tests
 - address should be rather short i.e.
D:\tmp\test2
2. Download 3 files:
 - bootstrap.cmd
 - source.zip
 - startenv.cmd
3. Run **bootstrap.cmd**
4. Script will
 - unpack zip archive
 - Download python and all dependencies
 - Create virtual environment
5. When finished – press any key
6. Software is ready!
7. Click **startenv.cmd** to open python venv
8. Run **python fem_connection.py** to check tester
9. Windows may ask for permissions... click yes
10. Run **python fec_test.py** to perform FEC test



```
Installing collected packages: numpy, fpdf, pyparsing, six, python-dateutil, kiwisolver, certifi, pillow, cycler, matplotlib, asteval, scipy, future, uncertainties, lmfit
Successfully installed asteval-0.9.19 certifi-2020.6.20 cycler-0.10.0 fpdf-1.7.2 future-0.18.2 kiwisolver-1.2.0 lmfit-1.0.1 matplotlib-3.3.2 numpy-1.19.2 pillow-8.0.0 pyparsing-2.4.7 python-dateutil-2.8.1 scipy-1.5.3 six-1.15.0 uncertainties-3.1.4
Press any key to continue . . .
```



```
(venv) D:\tmp\test2\source>python fem_connection.py
Reset TDCM/FEM power and press Enter to start...
Waiting 10 seconds to start...
Connected succesfully!
Sending command: be 0 dcbal_enc 1
Response: 0 Tdcm(1) Reg(3) <- 0x80000
Sending command: be 0 inv_tdc_mosi 0
Response: 0 Tdcm(1) Reg(3) <- 0x0
```


FEC tester – check FEM connection

1. Turn ON TDCM and FEM power supply



**Both switches should be in ON position
Check if LEDs are ON**


2. Run startenv.cmd
3. Run python script **fem_connection.py**

4. If succeed, following output should occur: 

```
Sending command: be 0 moni S
Response: 0 Tdcm(1) Serial: 0000000000000000
Sending command: fe 0 moni T 2
Response: 0 Tdcm(1) Fem(00) FEM_T: 26.219 degC
Sending command: fe 0 moni V 2
Response: 0 Tdcm(1) Fem(00) FEM_Vdd: 2.490 V
Sending command: fe 0 moni A 2
Response: 0 Tdcm(1) Fem(00) FEM_Vad: 4.766 V
Sending command: fe 0 moni I 2
Response: 0 Tdcm(1) Fem(00) FEM_I: 1.714 A
Sending command: fe 0 moni S 2
Response: 0 Tdcm(1) Fem(00) FEM_Serial: 580000024d742a26
Connection closed.
*****
FEM coldstart succeed!
```

5. If there is no Ethernet connection (i.e. tdcM is not powered up ...)

```
No ethernet connection...
*****
TDCM connection failed! No ethernet connection?
```

6. If FEM is not powered up or there is communication problem 

```
Sending command: fe 0 moni T 2
Response: -1 Tdcm(1) Fem(00): FeI2C_SelectTargetBus failed: -1
Sending command: fe 0 moni V 2
Response: -1 Tdcm(1) Fem(00): FeI2C_SelectTargetBus failed: -1
Sending command: fe 0 moni A 2
Response: -1 Tdcm(1) Fem(00): FeI2C_SelectTargetBus failed: -1
Sending command: fe 0 moni I 2
Response: -1 Tdcm(1) Fem(00): FeI2C_SelectTargetBus failed: -1
Sending command: fe 0 moni S 2
Response: -1 Tdcm(1) Fem(00): FeI2C_SelectTargetBus failed: -1
Connection closed.
*****
FEM coldstart failed! FEM problem... Please power cycle and start again...
```

FEC tester – running FEC test

1. **Turn OFF** TDCM and FEM power supply
2. Click on startenv.cmd script
3. Python venv in source folder will start
4. Type: `python fec_test.py`
5. Enter following information:
 - FEM slot
 - Tester name
 - FEC label ID

**Both switches should be in OFF position
Check if LEDs are OFF**

```
(venv) D:\tmp\test2\source>python fec_test.py
Loaded settings from settings\json_fectest_settings.txt
Enter fem slot (0 or 1): 0
Enter tester name: Andrzej
Enter fec label: 003
Reset TDCM/FEM power and press Enter to start...
```

6. **Turn ON** TDCM and FEM power supply
7. Test will take approx. 3-4 minutes and will output multiple lines...
8. When test is finished following output should occur:

**Both switches should be in OFF position
Check if LEDs are OFF**

```
Generating FECTEST pdf report...
Generating summary...
Generating table...
Generating pedestal tables
Report saved to ..\out\fectest_report_fec_003_2020_10_21_15_08_16.pdf
Test finished in 2.7 minutes
Test result: Success
```

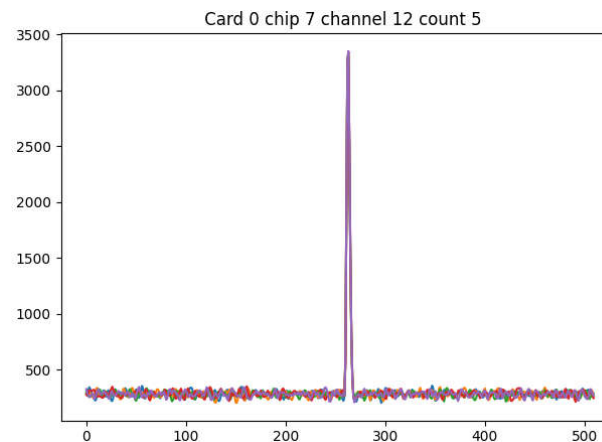
9. **Turn OFF** TDCM and FEM power supply
10. Check out folder for report

FEC tester – test list

1. **Monitoring values** script verifies basic FEM-FEC communication with DS2438 chip: electronic serial ID, voltage, current, temperature and analogue voltage
2. Slow control registers - the script to check read and write operations to the configuration registers of the AFTER chips
3. Pedestal run – script writes After settings and reads pedestals before and after equalization
4. ADC (AD9637) test patterns: the script to write operations to the configuration registers of the ADC of each FEC, different test patterns are set to 8 ADC channels. Data run is performed, waveforms are collected to verify pattern of each channel.
5. Pulser test
 - the script to set the amplitude of the pulser to given value (DAC 483),
 - test is performer for one channel of each ASIC chip (daq channel 12),
 - 5 waveforms are collected for each AFTER chip
 - script verifies if amplitude of recorded signal is correct

```
# Program created: 2020_10_21-15-08-47
Commands sent: 9
0      cmd: fe fec_enable 1          Reg(1) <- 0x40000
1      cmd: fe 0 moni T 0           FEC_T: 28.344 degC
2      cmd: fe 0 moni V 0           FEC_Vdd: 3.270 V
3      cmd: fe 0 pulser 0 model T2K2 pulser_DAC <- 3 (T2K2)
4      cmd: fe 0 pulser 0 base 0x3FFF Pulser_Base <- 0x3fff
5      cmd: fe 0 pulser 0 load      Reg(1) <- 0x0 GEN_GO pulsed
6      cmd: fe 0 moni A 0           FEC_Vad: 1.940 V
7      cmd: fe 0 moni I 0           FEC_I: 1.418 A
8      cmd: fe 0 moni S 0           FEC_Serial: 3c0000024da1b926
```

ADC channel #0	P#1 (Midscale short 2048)
ADC channel #1	P#2 (+Full-scale short 4095)
ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)
ADC channel #3	P#7 (One/zero-word toggle)
ADC channel #4	P#1 (Midscale short 2048)
ADC channel #5	P#2 (+Full-scale short 4095)
ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)
ADC channel #7	P#7 (One/zero-word toggle)



FEC tester – script output

1. All result are saved in out folder

Nazwa	Data modyfikacji	Typ	Rozmiar
fectest_report_fec_003_2020_10_21_15_08_16.pdf	21.10.2020 15:11	Foxit Reader PDF ...	457 KB
fectest_report_fec_003_2020_10_21_15_02_53.pdf	21.10.2020 15:05	Foxit Reader PDF ...	414 KB
fectest_report_fec_003_2020_10_21_15_08_16	21.10.2020 15:11	Folder plików	
fectest_report_fec_003_2020_10_21_15_02_53	21.10.2020 15:08	Folder plików	

2. PDF report with following name

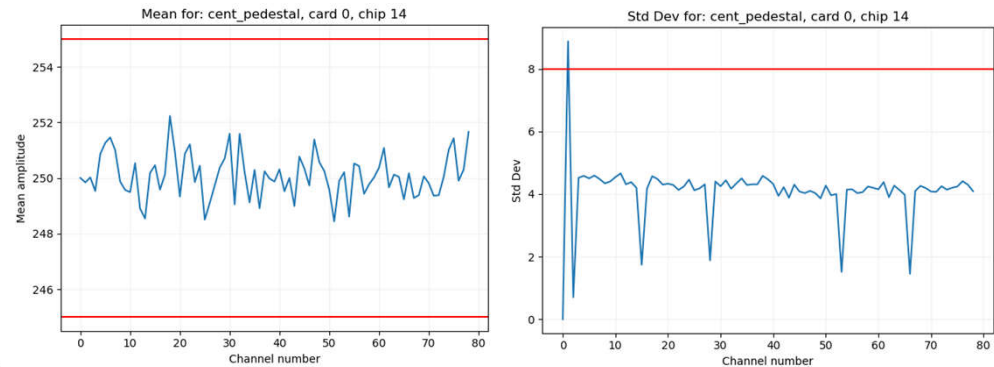
fectest_report_fec_XXX_YYY where:

- XXX is a fec label ID
- YYY is date+time of test

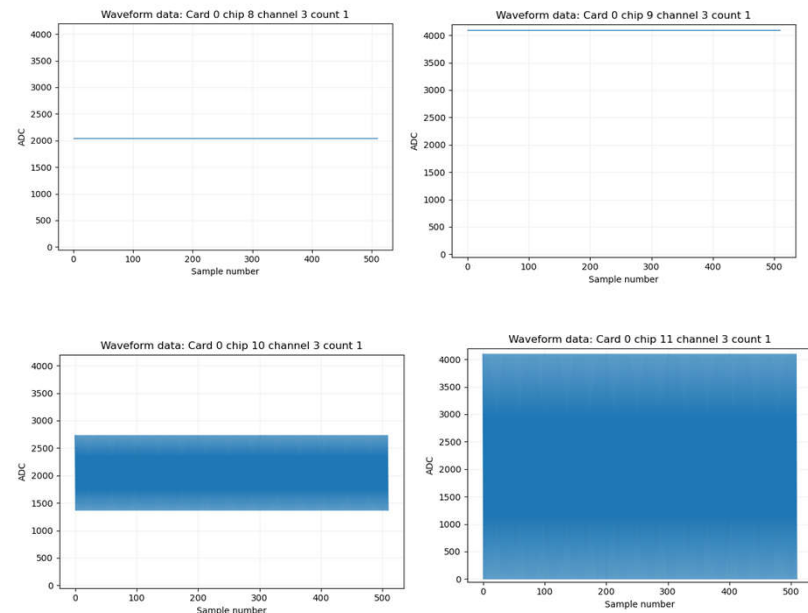
3. Folder with the same name containing

- Txt files with commands sent and received for 5 test runs
- Png files in data subfolder
 - Pedestal run files for each AFTER (mean + rms)
 - ADC pattern test figures
 - Calibration pulser test figures

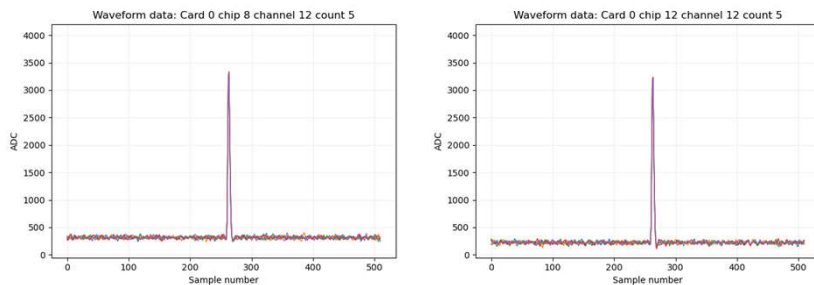
Pedestal data figures



Pattern test data figures



Pulser test data figures



FEC tester – pdf report

PDF report consists of following pages

1. Summary page with results of 5 tests
 1. Monitoring values
 2. Slow control registers
 3. Pedestal run
 4. ADC test patterns
 5. Pulser test
2. Pages 2-5: tables with commends sent and received for every test:

Monitoring test			
NO	Command	Error	Response
0	fe fec_enable 1	0	0 Tdcm(1) Fem(00) Reg(1) <- 0x40000
1	fe 0 moni T 0	0	0 Tdcm(1) Fem(00) FEC_T: 24.312 degC
2	fe 0 moni V 0	0	0 Tdcm(1) Fem(00) FEC_Vdd: 3.270 V
3	fe 0 pulser 0 model T2K2	0	0 Tdcm(1) Fem(00) pulser_DAC <- 3 (T2K2)
4	fe 0 pulser 0 base 0x3FFF	0	0 Tdcm(1) Fem(00) Pulser_Base <- 0x3fff
5	fe 0 pulser 0 load	0	0 Tdcm(1) Fem(00) Reg(1) <- 0x0 GEN_GO pulsed
6	fe 0 moni A 0	0	0 Tdcm(1) Fem(00) FEC_Vad: 1.950 V
7	fe 0 moni I 0	0	0 Tdcm(1) Fem(00) FEC_I: 1.426 A
8	fe 0 moni S 0	0	0 Tdcm(1) Fem(00) FEC_Serial: 3c0000024da1b926

3. Page 6 Pedestal table before pedestal run
4. Page 7 Pedestal table after pedestal run

Fec test report:

Date: 2020_10_21-15-08-16

Tester name: Andrzej

Test#1 Monitoring values				Passed
0	FEC label	003		OK
1	FEC DC2438 ID	3c0000024da1b926		OK
2	FEC_T (to 35°C)	28.344		OK
3	FEC_Vdd (3.2V to 3.4V)	3.270		OK
4	FEC_I (1.1A to 1.5A)	1.418		OK
5	FEC_Vad (1.9V to 2.0V)	1.940		OK

Test#2 Slow control registers:				Passed
Test#3 Pedestal run:				Passed
0	After chip #0	Mean OK	STDDEV OK	OK
1	After chip #1	Mean OK	STDDEV OK	OK
2	After chip #2	Mean OK	STDDEV OK	OK
3	After chip #3	Mean OK	STDDEV OK	OK
4	After chip #4	Mean OK	STDDEV OK	OK
5	After chip #5	Mean OK	STDDEV OK	OK
6	After chip #6	Mean OK	STDDEV OK	OK
7	After chip #7	Mean OK	STDDEV OK	OK

Test#4 AD9637 test patterns				Passed
0	ADC channel #0	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
1	ADC channel #1	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
2	ADC channel #2	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
3	ADC channel #3	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK
4	ADC channel #4	P#1 (Midscale short 2048)	MAX 2048 MIN 2048	OK
5	ADC channel #5	P#2 (+Full-scale short 4095)	MAX 4095 MIN 4095	OK
6	ADC channel #6	P#4 (Checkerboard 1365 to 2730 toggle)	MAX 2730 MIN 1365	OK
7	ADC channel #7	P#7 (One/zero-word toggle)	MAX 4095 MIN 0	OK

Test#5 Pulser run				Passed
0	After chip #0	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3043	OK
1	After chip #1	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3040	OK
2	After chip #2	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3064	OK
3	After chip #3	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3091	OK
4	After chip #4	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3114	OK
5	After chip #5	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 2964	OK
6	After chip #6	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3080	OK
7	After chip #7	DAC: 483 G(120) ADC(2850 to 3200)	ADC AMPL: 3044	OK

FEC test final result: **Passed**

FEC tester – settings json file

At start Fec_test.py settings from json file
`json_fectest_settings.txt` localized in path:
`<test_folder>\source\settings`

```
(venv) D:\tmp\test2\source>python fec_test.py
Loaded settings from settings\json_fectest_settings.txt
Enter fem slot (0 or 1): 1
Enter tester name: Andrzej
Enter fec label: 002
```

JSON file consists of multiple fields that are used
by testing programs, i.e.:

- Gain = 120
- Shaping time = 100ns
- Trigger rate
- Trig range
- Pulser settings: pulser_ampl, pulser_delay...

Filed `c_vals` sets values boundaries that are
checked whne report is generated:

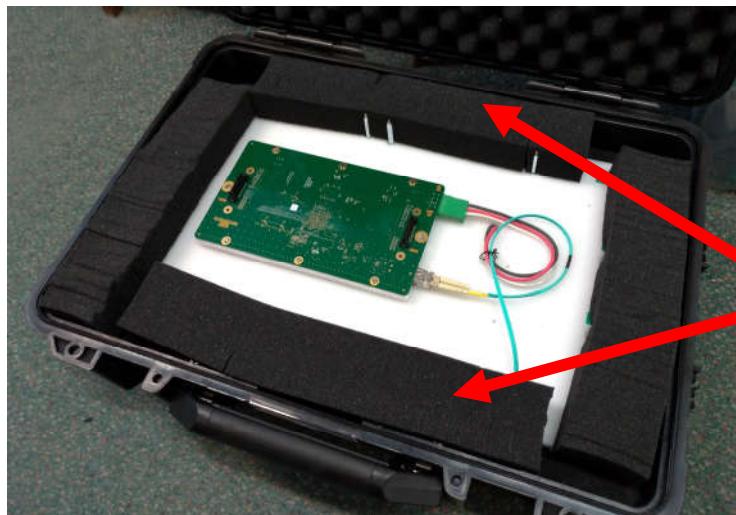
```
"c_vals": {
    "temperature": 35,
    "FEC_Vdd_low": 3.2,
    "FEC_Vdd_high": 3.4,
    "FEC_I_low": 1.1,
    "FEC_I_high": 1.5,
    "FEC_Vad_low": 1.9,
    "FEC_Vad_high": 2.0,
    "max_ped": 255,
    "min_ped": 245,
    "max_std": 8,
    "max_std_fpn": 4,
    "fpn_channels": [15, 28, 53, 66],
    "reset_channels": [0, 1, 2],
    "pulser_ampl_h": 3200,
    "pulser_ampl_l": 2850
}
```

Test#1 Monitoring values

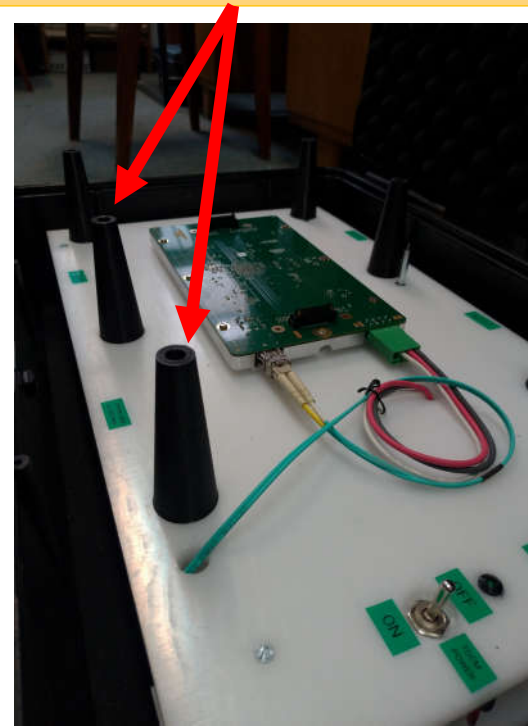
Test#1 Monitoring values			Passed
0	FEC label	003	OK
1	FEC DC2438 ID	3c0000024da1b926	OK
2	FEC_T (to 35°C)	24.312	OK
3	FEC_Vdd (3.2V to 3.4V)	3.270	OK
4	FEC_I (1.2A to 1.5A)	1.426	OK
5	FEC_Vad (1.9V to 2.0V)	1.950	OK

FEC tester – transport

FEC tester should be transported in black plastic toolbox



Black plastic distances are only for transportation – remove them for tests



Use also additional foam for transport