Clocks In the ASICs:

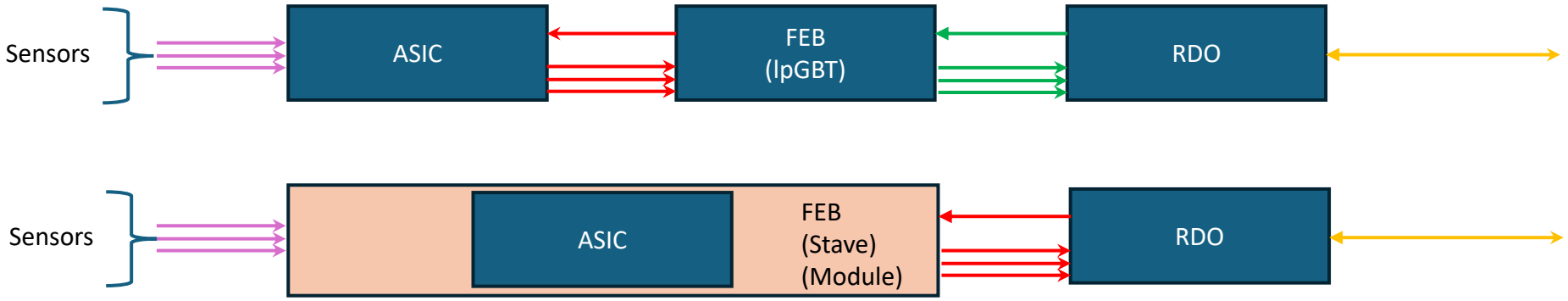
The question discussed on 10/9/24 referred to changing the clock on the CALOROC from 200 MHz to 320 MHz to support the lpGBT operation.

I think this was confusing to some of us because the we have talked about the ASIC clocks as being either the EIC/Synced CERN bunch clock (39.4 MHz) or the EIC clock (98.5 MHz). The 200 MHz, 320 MHz are the potential source clocks for the CALOROC, but in any case there are multiple internal clocks.

The reason for a 200 MHz input clock was that (pre-lpGBT) the EIC RDO was going to provide a multiple of the EIC clock and leave the clocking issues to the ASICs, so this was one of the changes the CALOROC was going to make for us. With the lpGBT based detectors, though, we will provide 39.4 MHz clocks from the RDOs. This makes the 200 MHz unneeded so it gets rid of one of the complicating changes that would need to be implemented!

The following pages describe the various clocks and how they are related:

Digitization clocks:



Sensor Digitization:

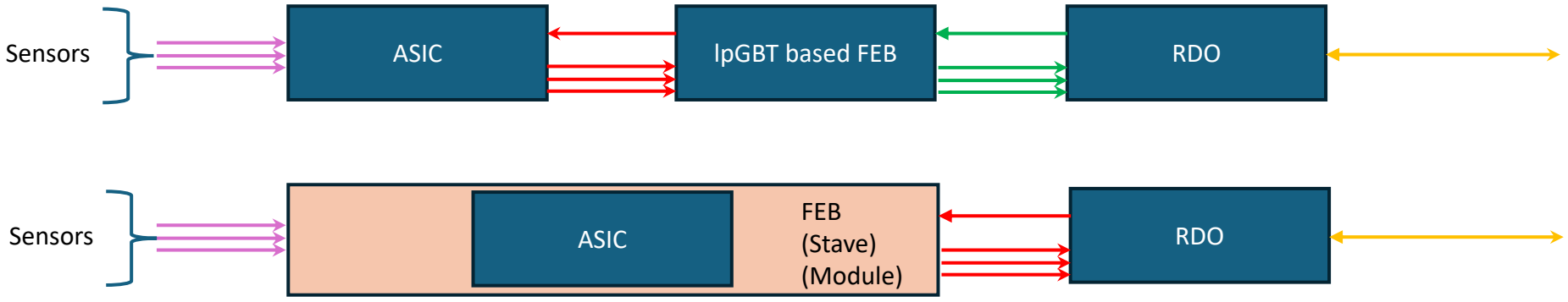
This clock is only relevant for time-binned ADC data. The digitization clock is built into sensor/ASIC. For the most part, these numbers are not under current discussion.

EICROC: 39.4 MHz, CALOROC: 39.4 MHz, ALCOR: N/A, SALSA: 49.75MHz, FCFD: ?(N/A) MHz

Ramifications:

1. For TOA/TOT the time is defined by discriminating the input voltage, not from integrated ADC values, so this clock is not directly related to time resolution for CALOROC/EICROC… but for mixed TOA/TOT + ADC modes the ADC part is relevant
2. If the shaping time is longer than the digitization clock the time resolution comes from an average(fit) of ADCs, and can be much better than the time step, so a clock slower than 98.5 Mhz can still resolve times to a bunch crossing level using ADCs
3. A clock different from the EIC Clock prevents the use of timing windows to separate collision data from backgrounds (as expected for ALCOR)
4. When the clock edges start at a different time with respect to the collision, there could be subtle effects (the shape of the pulses, slewing, etc…) So there might need to be 5 different calibrations one for each potential collision phase for sampled ADCs @ 40MHz

ASIC downlink connections:



Supplied Downlink Clock:

The supplied clock also doubles as the bit rate for the serial communication, so it is correlated to the fast commands available.

Typically, there is 1 downlink per ASIC and 1 ***or more*** uplinks per ASIC. The uplink/downlink are not necessarily at the same speed.

lpGBT supports: 80 MHz, 160 MHz, or 320 MHz downlinks

downlink supplied: EICROC: ? , CALOROC: (old 200 MHz, new 320 MHz), ALCOR: 394 MHz, SALSA: ?, FCFD: ?

Downlink frame rate: EICROC 39.4 MHz, CALOROC 39.4MHz, ALCOR 98.5MHz, SALSA: 98.5MHz, FCFD: ?

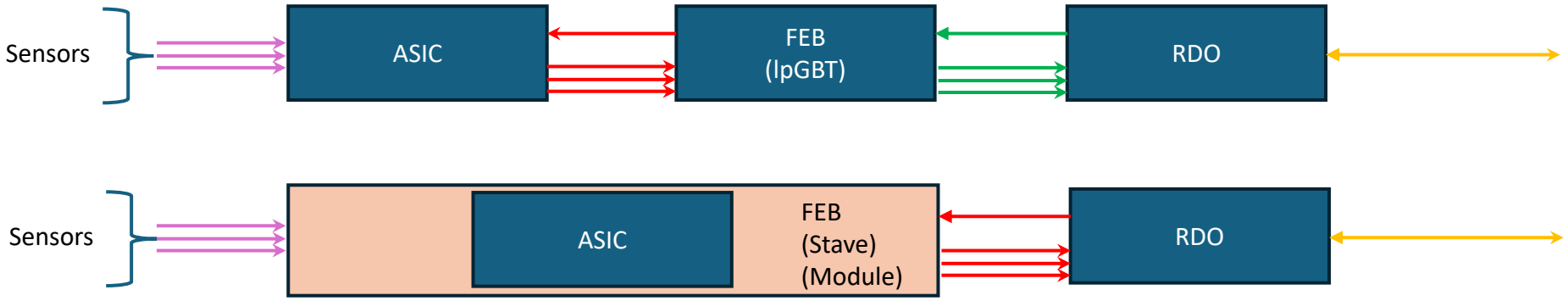
Ramifications:

1. The relationship between the internal ASIC clocks and supplied clocks is complex but not critical to the interfaces. They might affect the external specs, but the external specs are what matters, not the internal clocks.
2. The downlink serial interfaces use this clock, so it defines bandwidth of synchronous commands available
3. lpGBT only supports specific rates ***and*** the number of distinct connections allowed depends upon the rates
   - Downlinks:

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

   - The only clocks provided to the ASICs by lpGBT are the uplink/downlink clocks, so the ASIC ***must*** derive any internal/digitization clocks from the uplink or downlink clock. For ASIC based RDOs one could imagine separate clocks for the ASIC supply and the serial link rates.
4. When we are talking about the RDO clock we usually mean the frame rate for this clock. This clock/number of bits per synchronous command. This is always going to be 40 MHz for lpGBT.
5. We should consider the idea of ALL synchronous command delivery to be oriented towards 50.76 ns (5 x BX time) (Note that 1260 BX / revolution including abort gaps, divides 5)

ASIC uplink connections:



Uplink Clock : The electrical connections to/from ASICs:

Typically, there is 1 downlink per ASIC and 1 ***or more*** uplinks per ASIC. The clocks here are bit rates and define the data transfer rates. The uplink/downlink are not necessarily at the same speed.

lpGBT supports: 80MHz, 160MHz, 320 MHz, 640MHz, or 1.28GHz for uplink

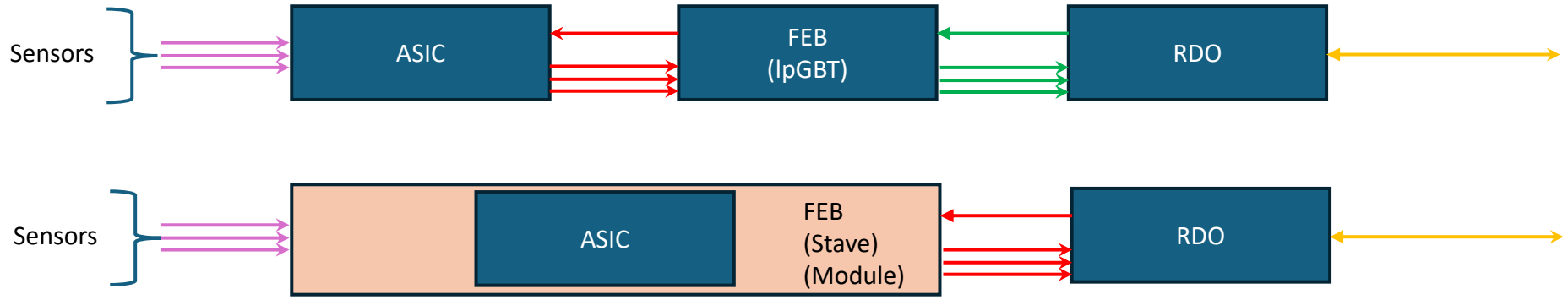
uplink: EICROC: (1.28 GHz perhaps lower), CALOROC: 1.28 GHz, ALCOR: 788 MHz, SALSA: ?, FCFD: ?

Ramifications:

1. The relationship between the internal ASIC clocks and the uplink/downlink and sensor digitization is complex but not critical to the interfaces. They might affect the external specs, but the external specs are what matters, not the internal clocks.
2. lpGBT only supports the specific rates ***and*** the number of connections allowed per lpGBT depends upon the rate used
   - Uplinks:

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

lpGBT optical protocol:

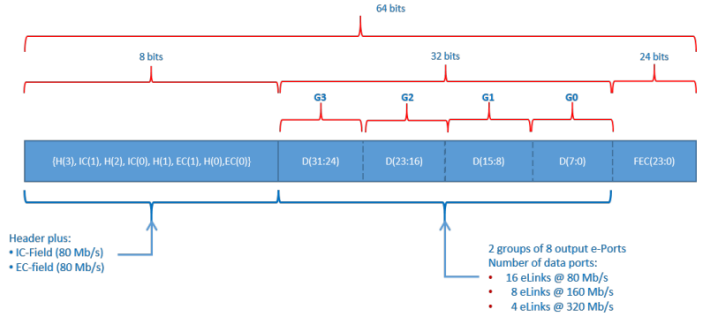


lpGBT optical links:

The optical links of the lpGBT are the serial drivers/receivers that connect the VTRX+ fibers. The optical part is a serial protocol, but this is translated automagically and presented as parallel frames with ***n*** bits transferred on a 39.4 MHz clock.

Downlink Frame Format: (Serial rate 64 x 39.4 MHz= 2.5 Gb/s)

- 40 bits are available for data
- 2 bits (80 MB/s) for controlling internal registers
- 2 bits (80 Mb/s) exported to "EC" pins
- 32 bits (1.2 Gb/s) exported to directly to ASIC downlinks



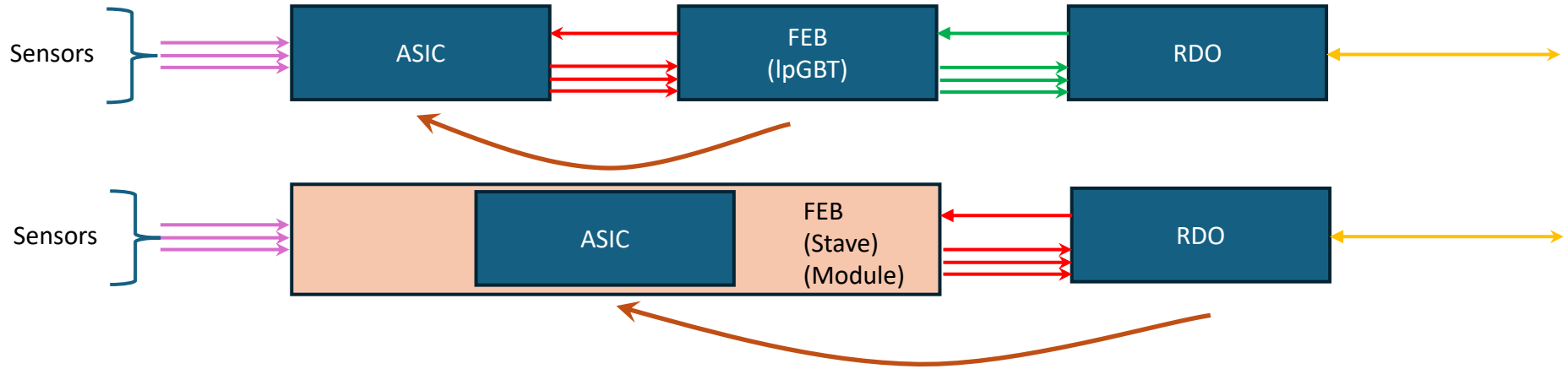
Uplink Frame Format: (Serial rate 256 x 39.4 MHz = 10 Gb/s)

- As Downlink frame but 224 bits available for data
- Bits still grouped according to their respective ASIC serial lines (8 bits per 320 Mb/s rate)

Ramifications:

- lpGBT doesn't support any mode other than direct fiber access to the ASIC serial uplinks and downlinks. Only specific clocks are supported (at multiplies of 39.4 MHz)

ASIC Slow Control connections (I2C or Programable logic port (PIO)):

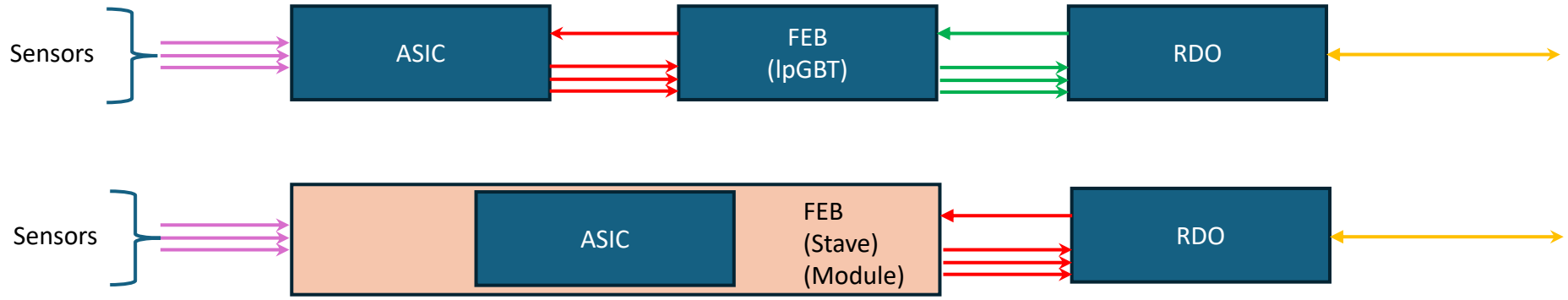


Slow control links: these are effectively unlimited (in lpGBT 16 I/O ports, 3 I2C Masters capable of addressing multiple ASICS)

lpGBT: There is an 80 MHz (39.4 MHz x 2 bits) “internal command” bit. This allows the setting of registers which control the slow I2C &/or PIO interfaces. The information is read/write. Sending/receiving data over these lines is going to be much slower. (I’m guessing 500Kb/s or so, but we’d have to gather information from experts)

FPGA based RDO: This isn’t specified yet but expected to be similar.

DAQ Optical Protocol:



DAQ Optical Protocol: Serial Clock Assumed ~10 GHz

Pre-lpGBT:

- 64 Bit frames @ 98.5 MHz
- RDO has knowledge of actual BX
- Fast commands are sent to the RDO which has the internal intelligence to distribute (by copies) to particular ASICs

Decoded Synchronous Command Structure							
[0:7]	[8:15]	[16:23]	[24:31]	[32:39]	[40:47]	[48:55]	[56:64]
Lower 40 bits of master BCO					CMD		Comma

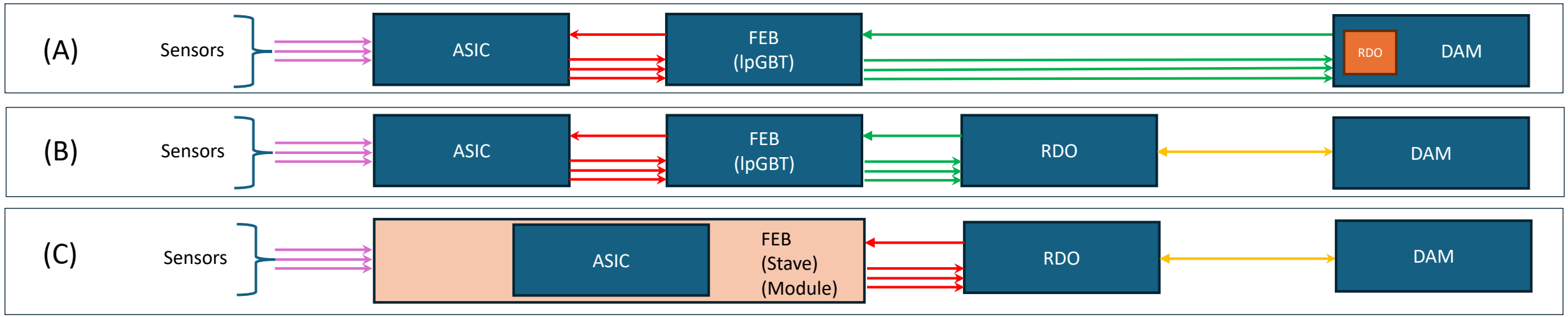
Decoded Synchronous Command Structure							
[0:7]	[8:15]	[16:23]	[24:31]	[32:39]	[40:47]	[48:55]	[56:64]
Flexible Command Data Encoding					FAST CMD		Comma
type	type specific				FAST CMD		Comma

- Unlike lpGBT aggregation protocol "zero-suppressed" rather than purely positional with all bits transferred to fiber.

Issues to resolve:

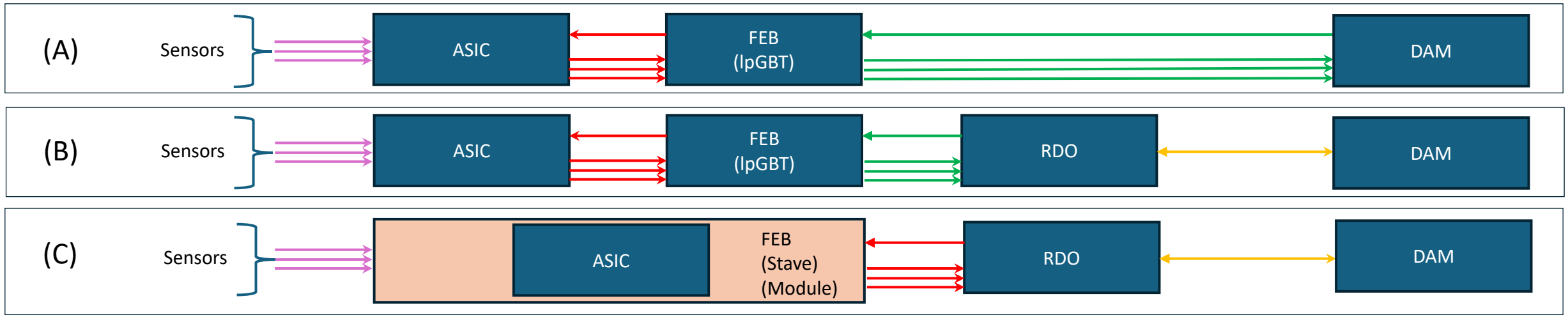
1. 3 different tech: 39.4 MHz @ 2.5Gb/s downlink, 98.4 MHz @ 2.5 Gb/s downlink, 98.5 MHz @ 10 Gb/s downlink
   - Option 1: All RDO use 100 MHz. RDO converts 39.4 MHz -> 100 MHz
   - Option 2: Some RDO at 100 MHz, some at 39.4 MHz. DAM converts 39.4 -> 100 MHz
2. Exact protocol for ASIC communications is different. How does this affect proposed command protocols?

Summary



ASIC	Downlink (baud) (Mhz)	Downlink frame frequency (MHz)	Uplink (baud) (MHz)	Uplink frame frequency (MHz)	FEB (baud) (MHz)	FEB frame freq (MHz)	RDO (baud) (MHz)	RDO Frame freq (MHz)	Digi clock (MHz)	RDO UP baud (MHz)	RDO UP Frame (MHz)	Intern clock (MHz)	Chain Type	Optics Type
EICROC	?lpBGT?	39.4	?lpGBT?	39.4?	2521	39.4	-	-	39.4	9850	39.4		A (B?)	VTRX+
CALOROC	315.2	39.4	1260x4	39.4	2500	39.4	7880	39.4	39.4	9850	39.4	315.2	B	Com
ALCOR	788	98.5	788	98.5			3152	98.5	n/a	9850	98.5	394	C	VTRX+
SALSA	?	?	1000 x 4	98.5	2462	98.5	3152	98.5	49.25	9850	98.5		B	VTRX+
FCFD	?(80)	39.4	1260	39.4	2521	39.4	-	-	n/a	9850	39.4	39.4	A (B?)	VTRX+
Discrete														
Astropix														
ITS-3														
(...)														

Summary



ASIC	Downlink (bits) (Mhz)	Downlink frame frequency (MHz)	Uplink (bits) (MHz)	Uplink frame frequency (MHz)	FEB (bits) (MHz)	FEB frame freq (MHz)	RDO (bits) (MHz)	RDO Frame freq (MHz)	Digi clock (MHz)	RDO UP bits (MHz)	RDO UP Frame (MHz)	Intern ASIC clock (MHz)	Chain Type	Optics Type
EICROC	?lpBGT?	39.4	?lpGBT?	39.4?	2521	39.4	-	-	39.4	9850	39.4		A (B?)	VTRX+
CALOROC	315.2	39.4	1260x4	39.4	2521	39.4	7880	39.4	39.4	9850	39.4	315.2	B	Com
ALCOR	788	98.5	788	98.5			3152	98.5	n/a	9850	98.5	394	C	VTRX+
SALSA	?	?	1000 x 4	98.5	3152	98.5	7880	98.5	49.25	9850	98.5		B	VTRX+
FCFD	?(80)	39.4	1260	39.4	2521	39.4	-	-	n/a	9850	39.4	39.4	A (B?)	VTRX+
Discrete														
Astropix														
ITS-3														
(…)														

2521 = 64 x 39.4 (lpGBT DL)
3152 = 32 x 98.5 (VTRX max DL)

Assume:

7880 = 80 bits x 98.5 (William Gu)
3152 = 32 x 98.5 (VTRX+ max DL)

Assume ~10 Gb/s