Scintillator Tileboards for the CMS HGCAL

Design, Integration, Performance

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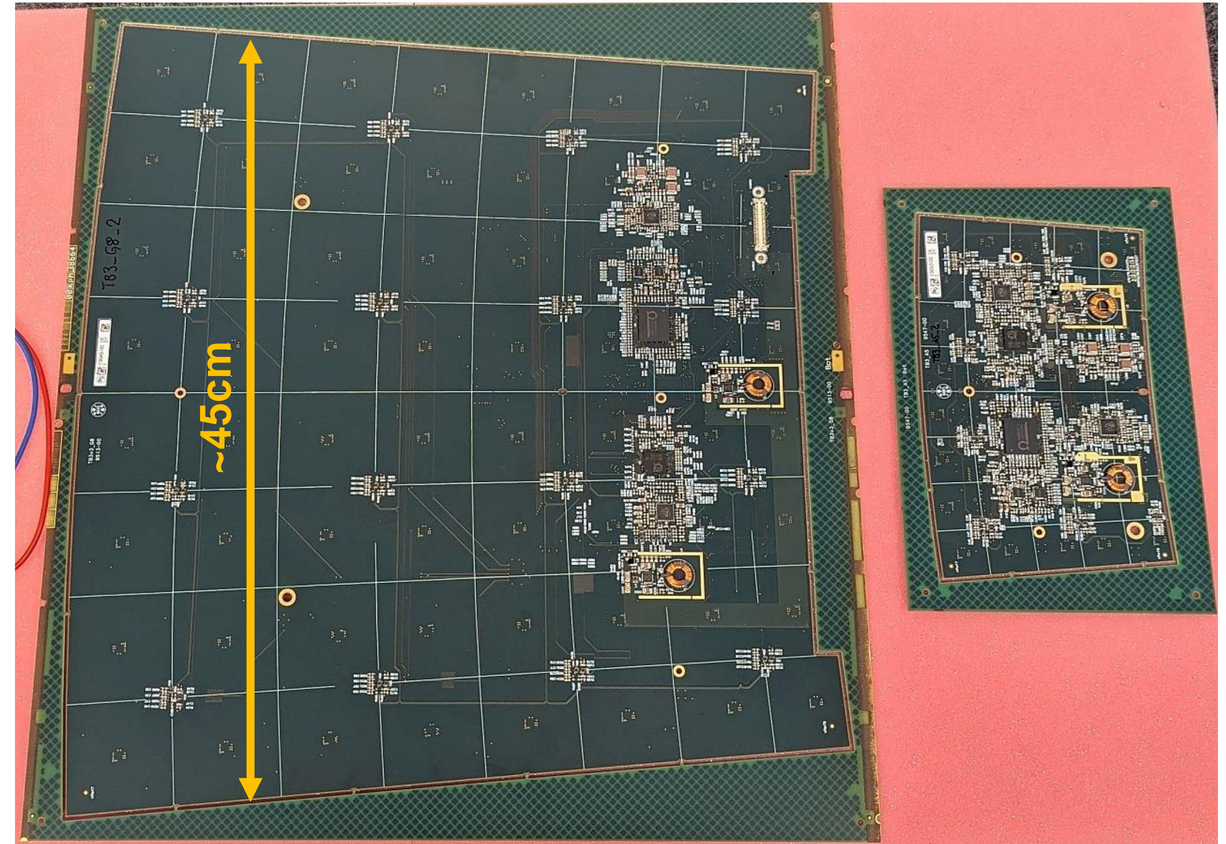
CMS HGCAL ESR day1,
Nov. 10th, 2023

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

Outline

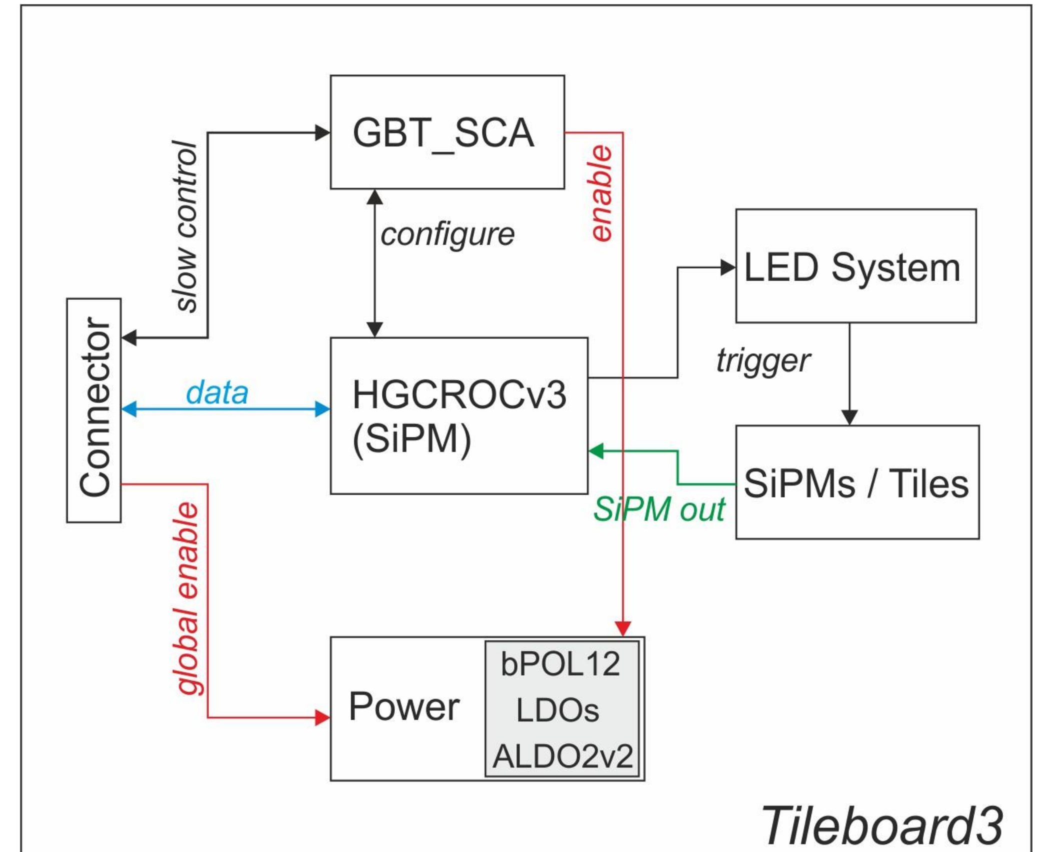
- Tileboard Introduction
- Tileboard Prototypes – History
- Pre-Series Status
- Tileboard Types and Status of Final Design
- Mechanical Integration (3D), Thermal Simulation
- Powering System
- Results from Bench Tests
- Results from Beam Tests
- Open Points



Pre-Series Tileboards TB3_G8 and TB3_A5

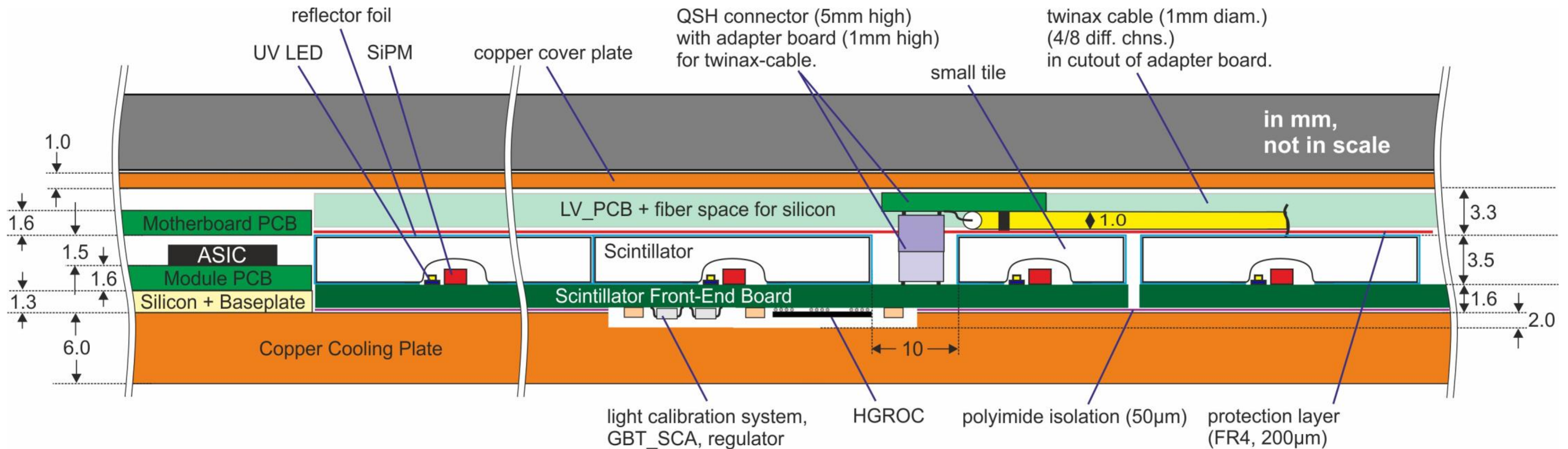
Tileboard3 - Introduction

- Basic Detector-Module for CMS HGCAL Scintillator Detector.
- Typically 64 SiPMs and plastic scintillator tiles.
- One or two HGCROCv3(b) in LD packages.
- GBT_SCA for slow-control
- Integrated LED system for gain calibration and monitoring.
- On-board integrated power setup.
- Single connector as only interface for power and signals.



TB3 Block-Diagram

Tileboard3 - Introduction



- Scintillator Tileboards with SiPMs, LEDs and Tiles on copper heatsink (-30°C).
- All other active components are on the backside in pockets of the copper heatsink.
- Polyimide isolation foil (50µm) under tileboards, FR4 protective cover (600µm) on top.

Tileboard Prototype History

- Tileboard_Prototype0 (Jan. 2019):
  - GBT_SCA,
  - 8 temperature sensors, power producers (Resistors),
  - LED test circuit.
- Tileboard Prototype 1 (TB1, Sept. 2019), TB1.2 (March 2020), TB1.3 (Sept. 2020)
  - HGCROCv1
  - CALICE based LED system
  - Commercial LDOs, FEAST DCDCs
  - SiPMs in CALICE package (TB1) and in first custom packages (TB1.2, TB1.3)
- Tileboard Prototype 2 (May 2021)
  - HGCROCv2
  - New, MOSFET-based LED system
  - Commercial LDOs, FEAST DCDCs
  - SiPMs in custom HGCAL packages ($2mm^2$ and $4mm^2$).
- Tileboard_Prototype3 (Nov. 2022):
  - HGCROCv3
  - bPOL12V and HGCAL LDOs
  - ALDO2v2
  - SiPMs in custom HGCAL packages ($2mm^2$, $4mm^2$ and $9mm^2$).
- Mini Tileboard HD (Sept. 2021), LD (May 2023)
- Pre-Series Tileboards (A5, B12, D8, E8, G8): June 2023.

- 4 years of experience with basic signal chain and board structure
- Thermal validation as 1st step 2019
  - (back-up slide)

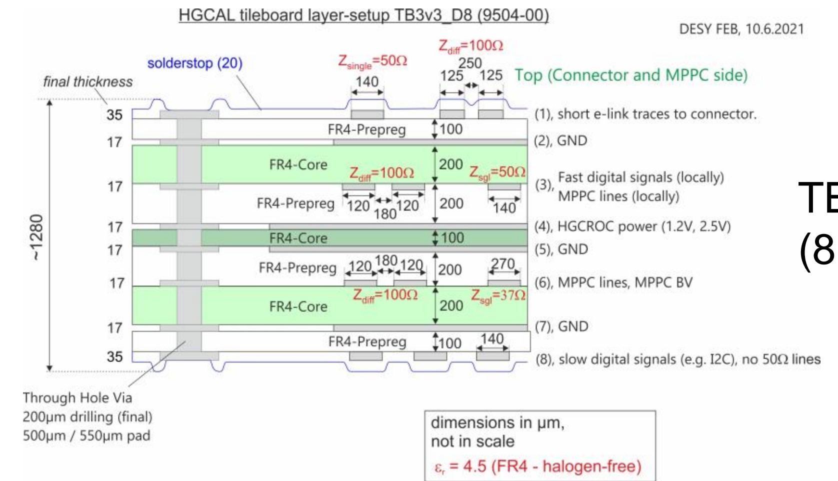
Scintillator Tileboards – Layer Structure

- Full tileboard specifications: Procurement Document. See backup for technical details.

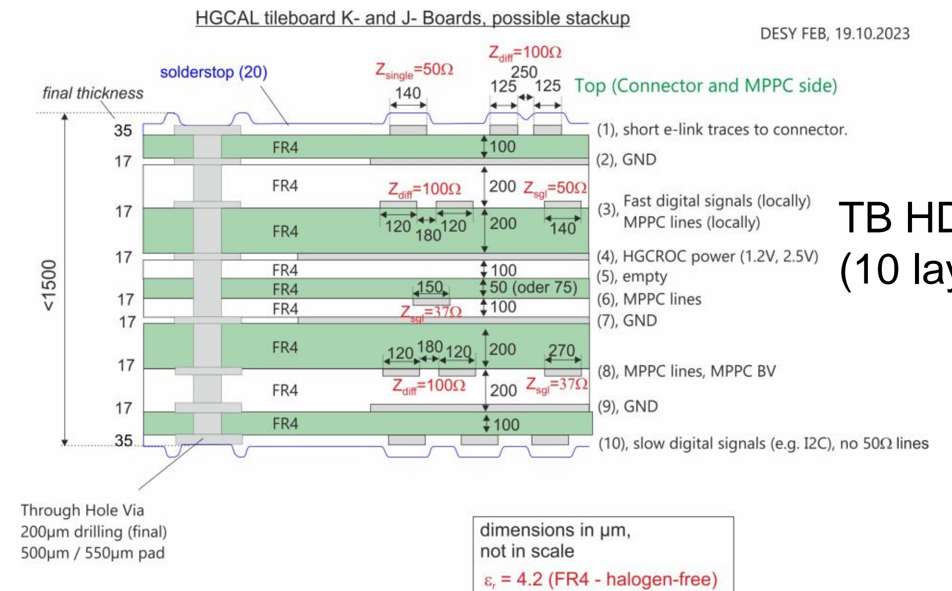
- Typically: 8 signal layers
- 100Ω differential lines, SiPM lines adapted to HGCROC input impedance (37Ω).
- Near SiPMs and power consumers: thermal vias.

- New: High-density Tileboards in front section (former FH).
  - 64chs => 144chs.
  - 10 signalling layers required.
  - Setup under discussion with vendors.

- No buried/micro-vias, no via-in-pad (costs, complexity).
- Except board size for largest tileboards (G8: 475x440mm²) no critical design features.



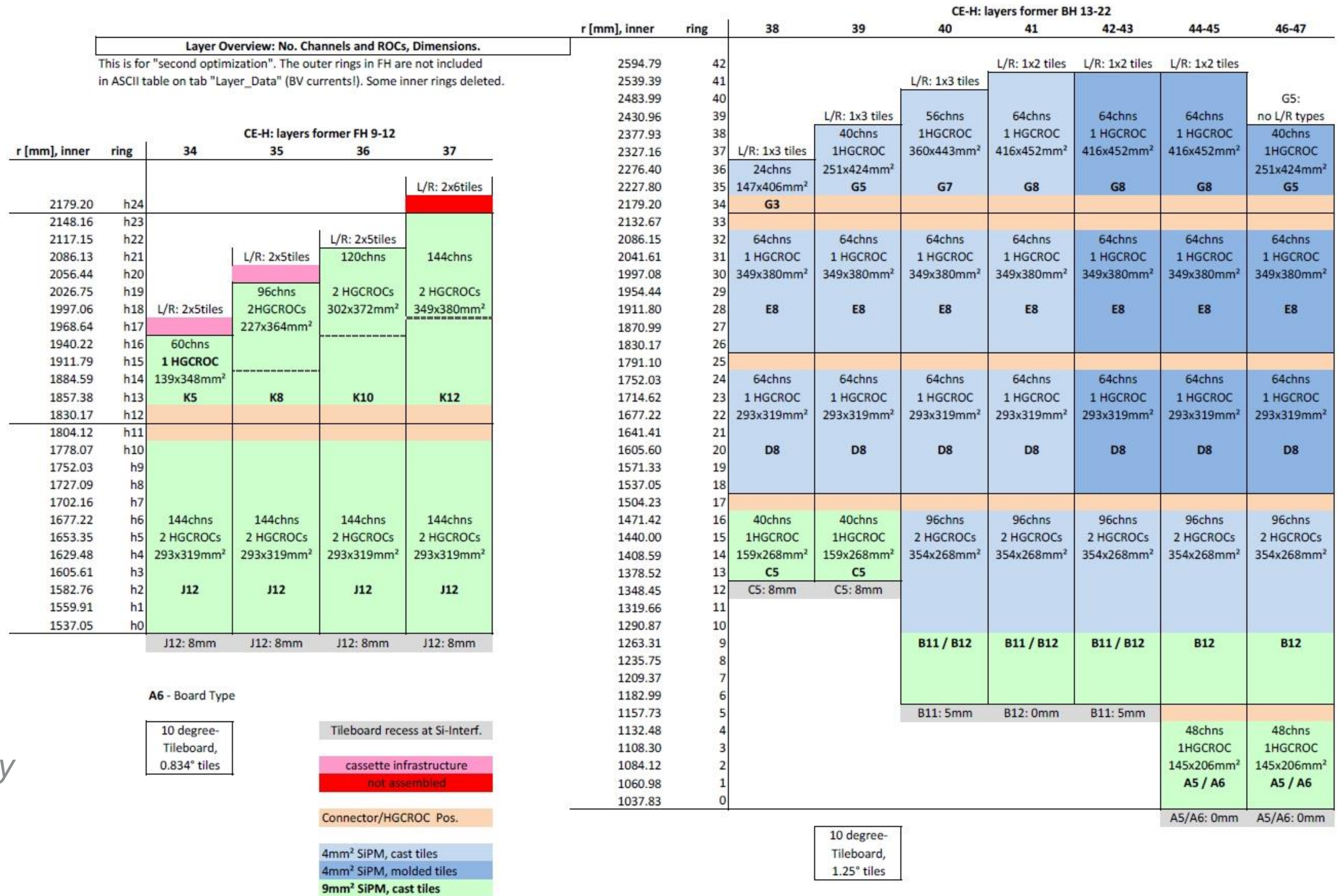
TB LD
(8 layers)



TB HD
(10 layers)

Scintillator Tileboards – Variants

- 8 basic types
  - LD: A, B, C, D, E, G
  - HD: J, K
- 35 sub-types in total
  - removing rows or corners



Cross-sectional view of CMS endcap, showing only the scintillator detector

Pre-Series Production - Status

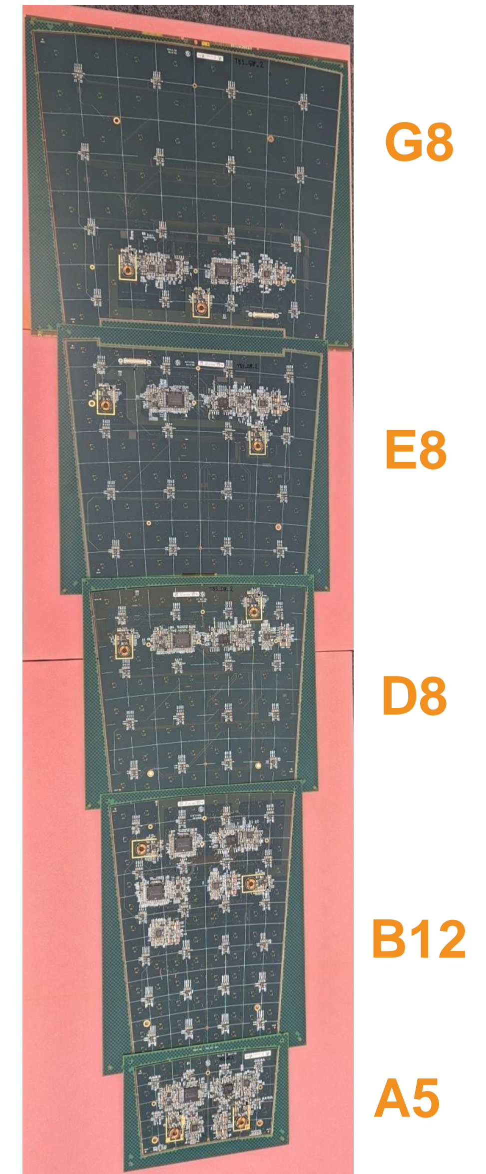
- Currently 2 Tileboards of A5, B12, D8, E8 and G8 assembled (10 in total)
- Commissioning of A5, D8, E8 and G8 completed.
  - All work fine on testbench.
  - A5 and G8 have been at DESY testbeam in August.

- Commissioning of B12 ongoing. Data taking already works.

- Remaining 31 tileboards are being assembled next week.

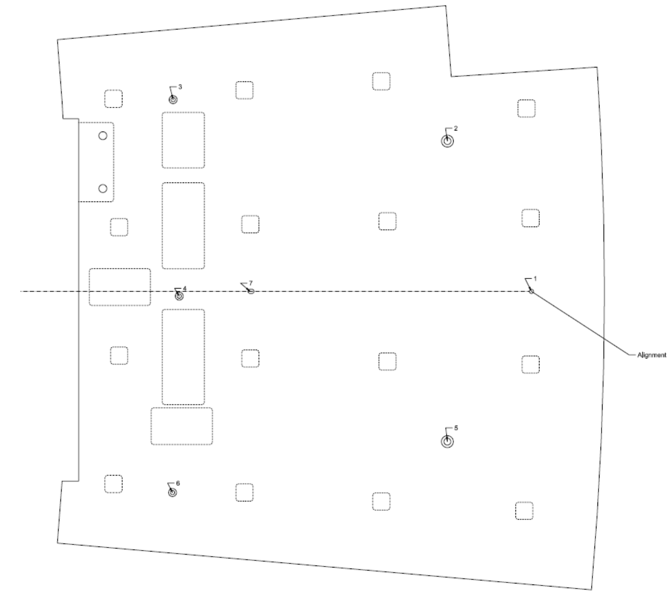
- One 10° sector reserved for HGCROCv3b.
- First pre-series Tileboards have been sent to US.
  - Motherboard tests and Tilemodule assembly optimisation

- TB3.0 has been sent to UMD (USA) earlier. Teststand in operation.
  - UMD students and postdoc have been trained in Tileboard operation at DESY



Scintillator Tileboards – Remaining Design Work

- Scintillator and Tileboard geometry in optimisation until recently.
- Status LD boards is final.
- Status HD boards:
  - Mechanical integration of Wingboard and Motherboard to be finalised
- Still minor schematics updates (from tests, ALDO2v2 peripheral components). **Mostly done.**
- Scenario with all SiPMs in 9mm² package still to be implemented for several types (few days per type).

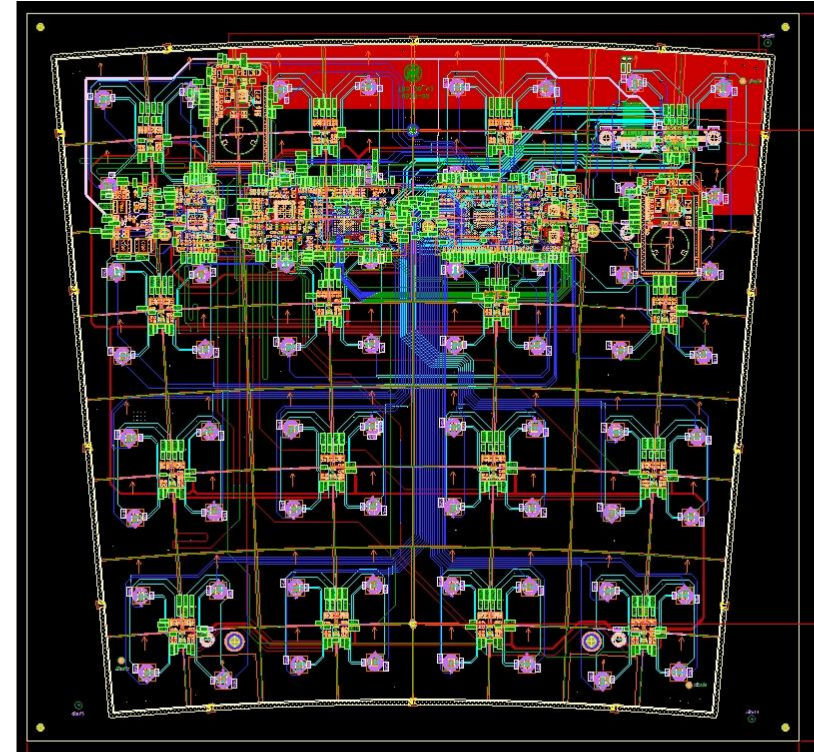


TB3_G8L envelope

Scintillator Tileboards – Status Layouts

- 3 Layouters now working on updates
  - 2 working on LD boards
  - 1 (me) working on K12 in HD granularity
- Layouts in final state: A5/A6, B12, D8, C5, B11
- Layouts done to 98%: E8, G8, G3, G8L, G8R
- Next Layouts, to be completed very soon (end Nov.): G3L, G3R
- End 2023: G5, G7 with L/R, waiting for 9mm² SiPM decision.

- K12 with essential progress expected end Nov.
  - Expected to be in time for vendor qualification
- Beginning 2024: J12, K5, K8, K10 (Ks with L/R)
  - Expected to finish in time for production contract (April 24)

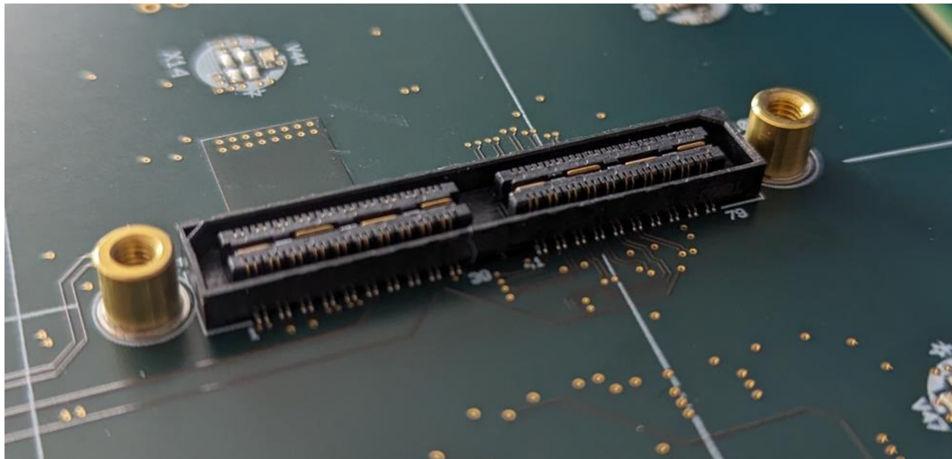


TB3_D8 layout (planes not shown)

- All basic types designed (LD section)
- LD designs validated by final prototypes
- HD prototype cycle before production starts

Tileboards – Mechanical Integration

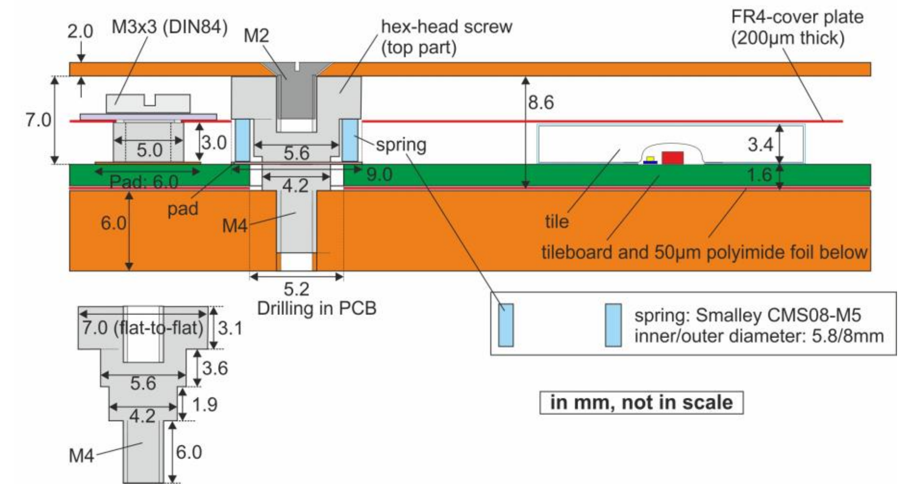
- Tileboard fixation agreed with cassette mechanical design team at FNAL.
- Use SMD nuts with inner threads (no copper cut-out) to fix:
  - Protective cover: M3x3mm.
  - Twinax Adapter: M3x5mm.
  - Flexleads (E- and G-Boards): M2.5x2.5mm.

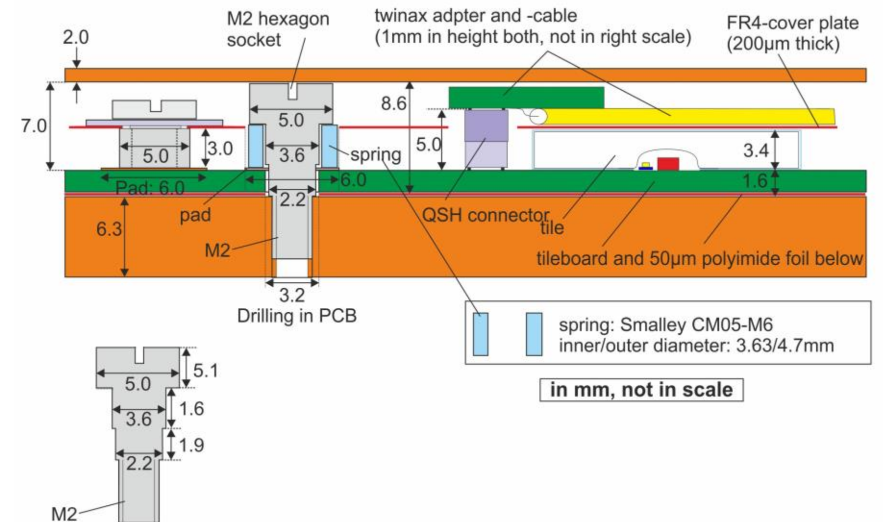


5mm-high SMD nuts next to QSH connector with inner M3 thread to fix twinax adapter

Tileboard3 - Cassette Mounting

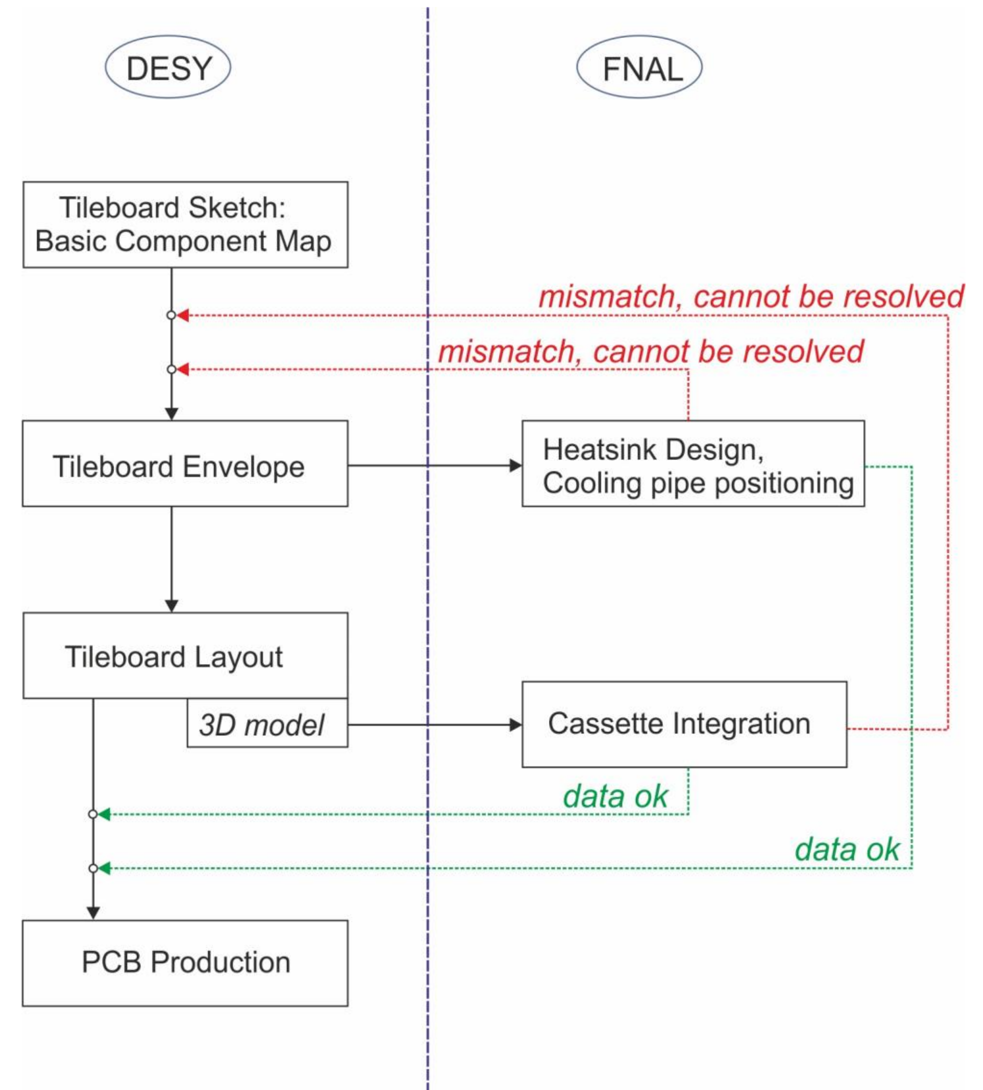
DESY, version 8.0, March2023





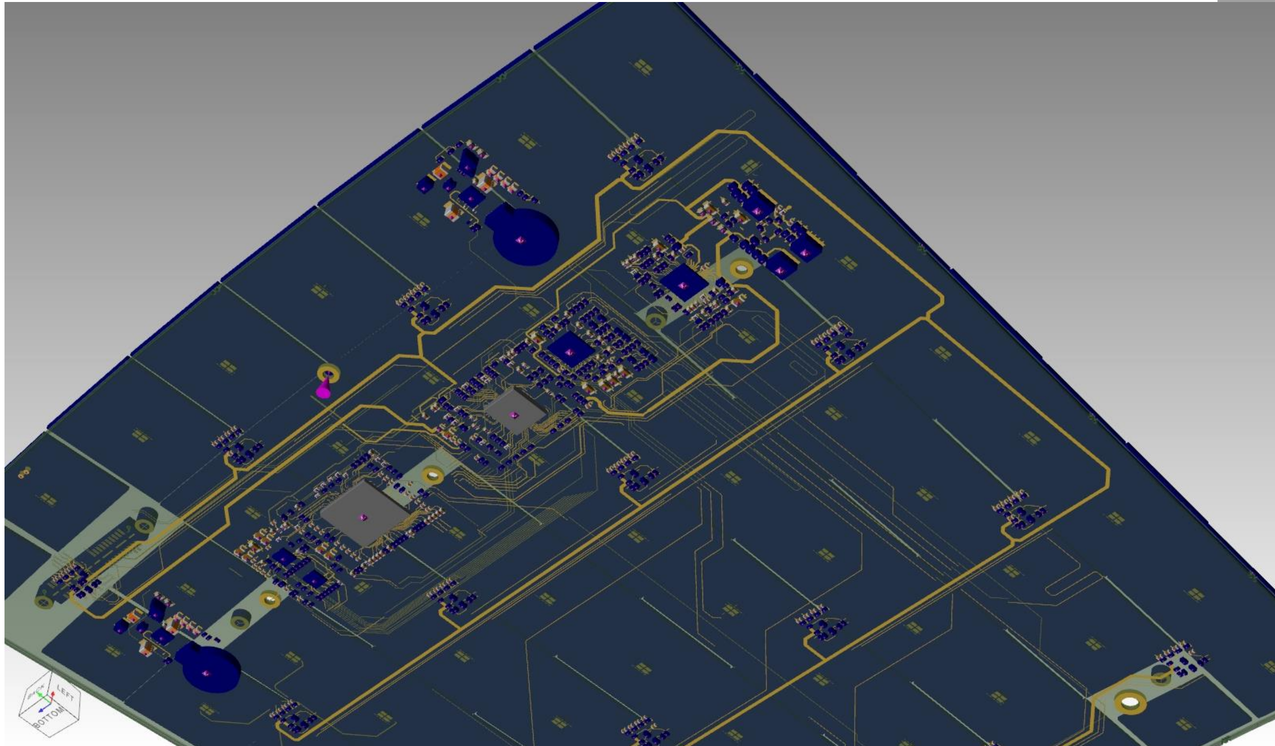
Tileboards – Mechanical Integration

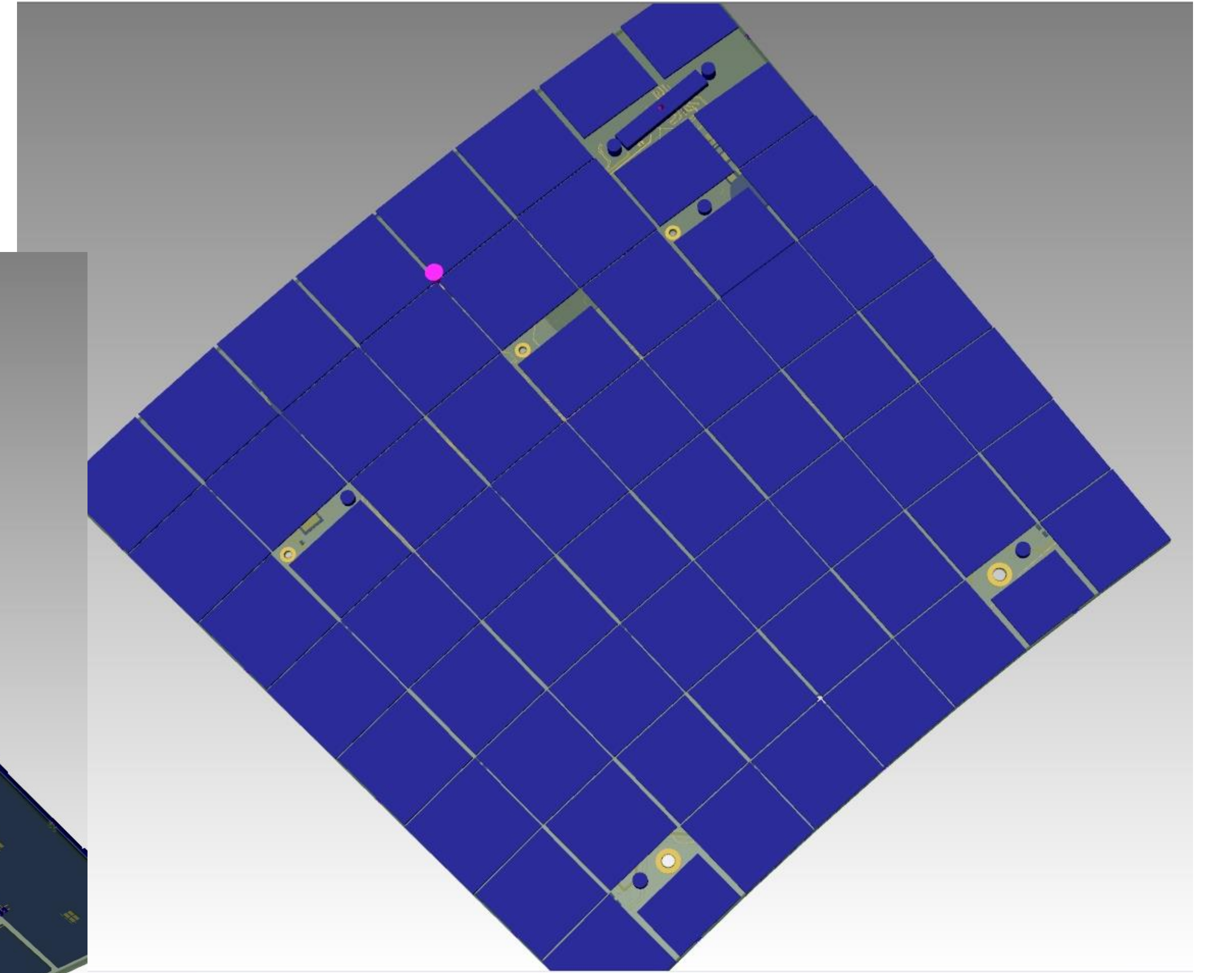
- Tileboard Designs start with basic mechanical models (3D):
  - Board Outline, SiPM positions, Drillings, Heatsink pockets, Tiles.
- Resulting Envelopes are used for:
  - heatsink/cassette design at FNAL (3D). Positioning of the cooling pipes (with possible feedback to envelopes).
  - tileboard layout preparation (2D).
  - Enables parallel development of copper heatsink and tileboard layouts without mechanical conflicts.
- From tileboard layouts detailed 3D models of tileboards are generated for cassette integration verification at FNAL.
- PCB production when passing verifications.



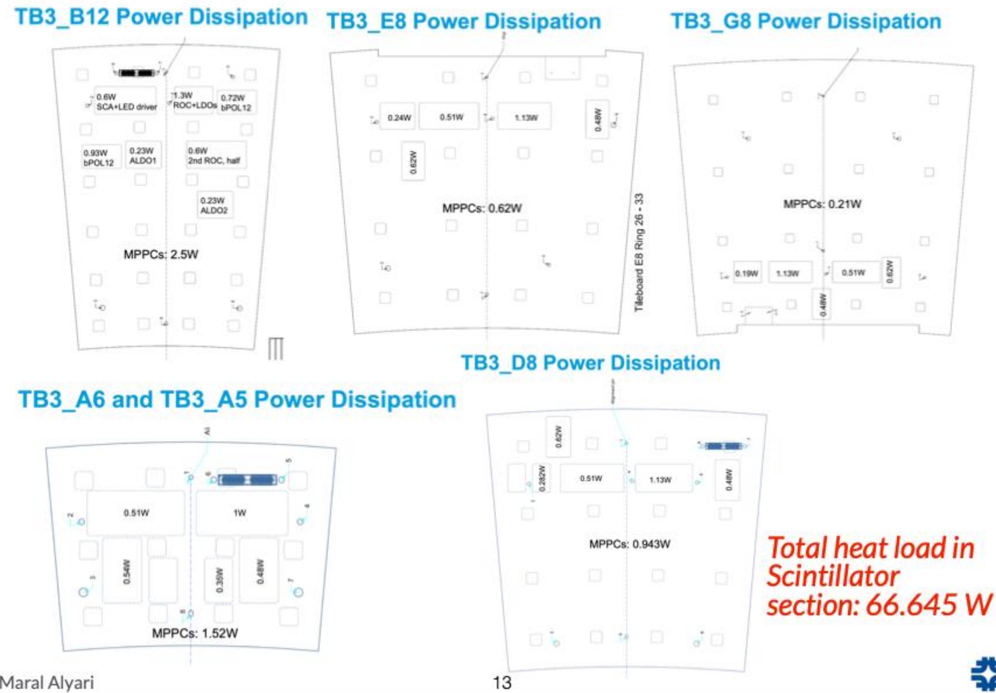
Tileboards – Mechanical Integration

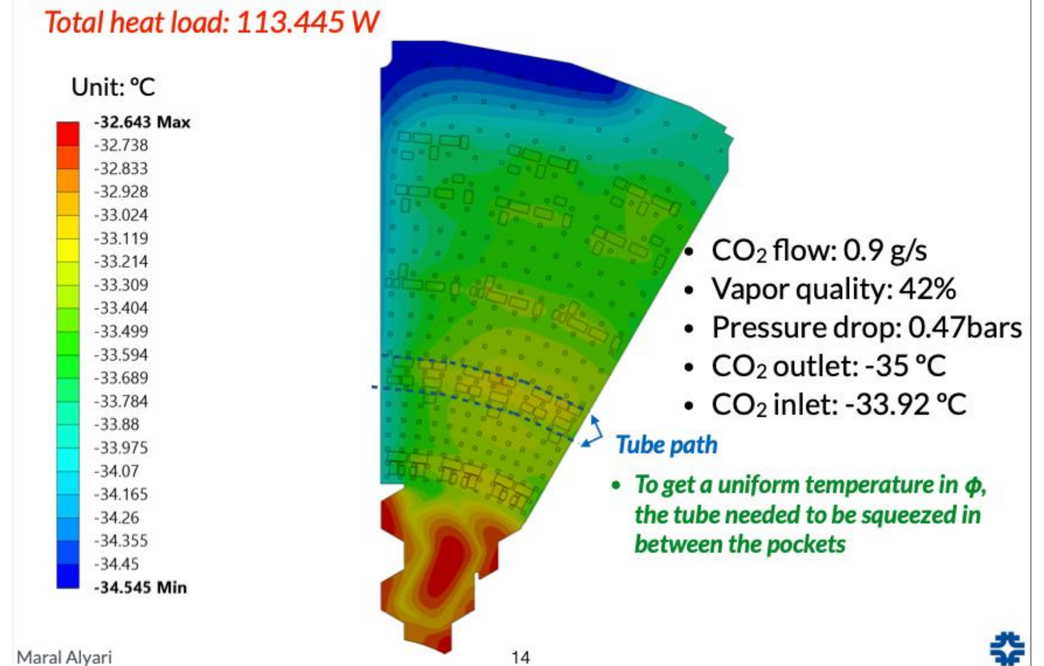
- 3D Tileboard Models for cassette integration verification.
- 3D models are generated in parallel to layout generation.
- Data compatibility checked with CERN/FNAL.





Tileboards: Thermal Integration (Simulation @FNAL)





- Power map of all tileboards provided to FNAL.
- SiPM currents at end of lifetime (see backup).
- Switch to 9mm² SiPMs: No increase of power budget: Reduction of global overvoltage to meet HGCROC input current limit of 1.2mA per channel.

- Hot spot in silicon region only.
- Temperature increase/gradient in scintillator region within 1.5°C: No problems expected.

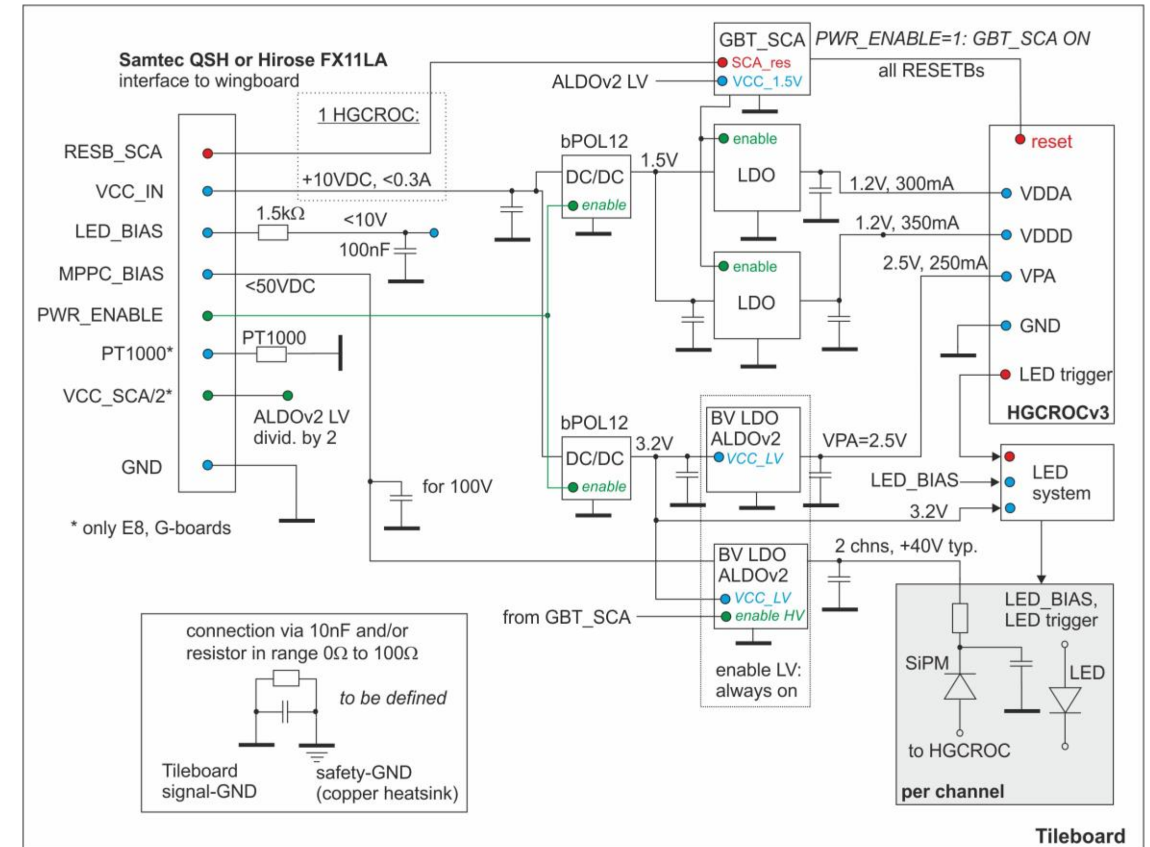
Scintillator Tileboards – Power and Ground

- Single connector as interface for power and signals.
- Integrated bPOL12Vs (no mezzanines)
- HGCAL LDOs for HGCROCv3 powering.
- ALDO2v2 from BTL group:
  - SiPM BV and HGCROCv3 analog input stage.
  - Qualification for CMS from BTL colleagues with more stringed operation limits. PRR of ALDO2v2 done.
  - Production yield (Milano): ~99%
- GBT_SCA (supply voltage 1.5V) for slow-control.

- No fuses on tileboards. In discussion: Fuses on wingboards.

- Huge HF capacitance Tileboard to Heatsink.
- Special connection of tileboard GND to heatsink (safety GND) for LF noise optimization.

- Powering Setup (LV and BV) is described in detail in edms document 2476375.



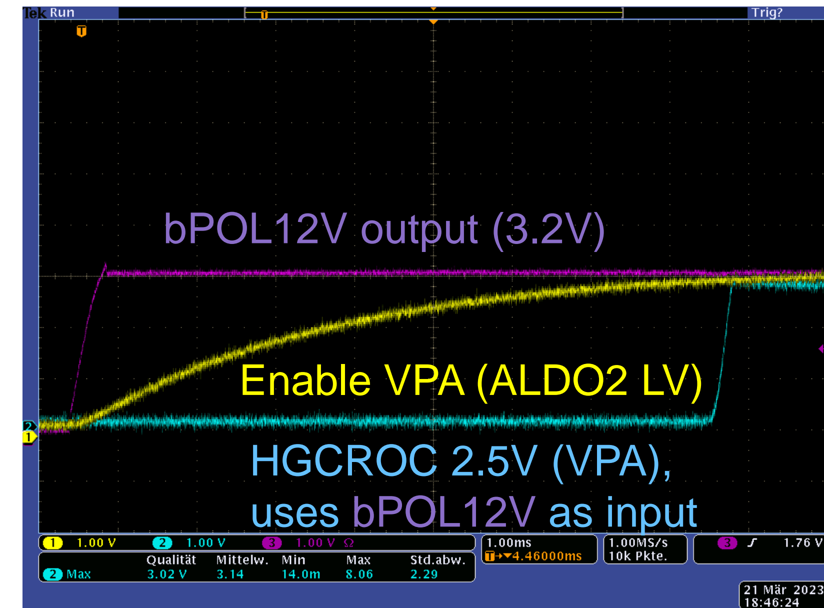
Tileboard powering setup

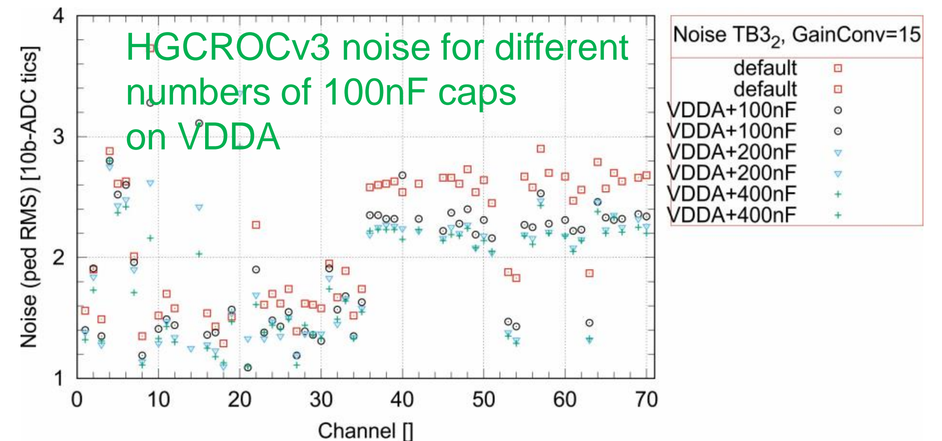
Tileboard3 – Supply Voltage Ripple, Switching and Filtering

- TB3 supply voltages tested with oscilloscope:
  - Integrated bPOL12 outputs,
  - HGCROC voltages, ALDO2v2 LV outputs
  - SiPM bias voltages (LDO: ALDO2v2)
- Ripple (below detection limit of scope), Spikes checked.
- Switch-on characteristics: No over-, undershoots.

- TB3 filtering setup has been checked by removing / adding filter capacitors at regulator in- and outputs:
  - noise performance.
  - supply voltage stability (no oscillation).
  - filtering setup has been optimized based on these results.

- Sufficient margin on the filter setup on all voltages.
- If unexpected issues (excessive noise, oscillation on supply voltages) occur, improvements still possible:
  - Removing filter capacitors, changing capacitor sizes
  - Changing connection to safety GND (via R and C).

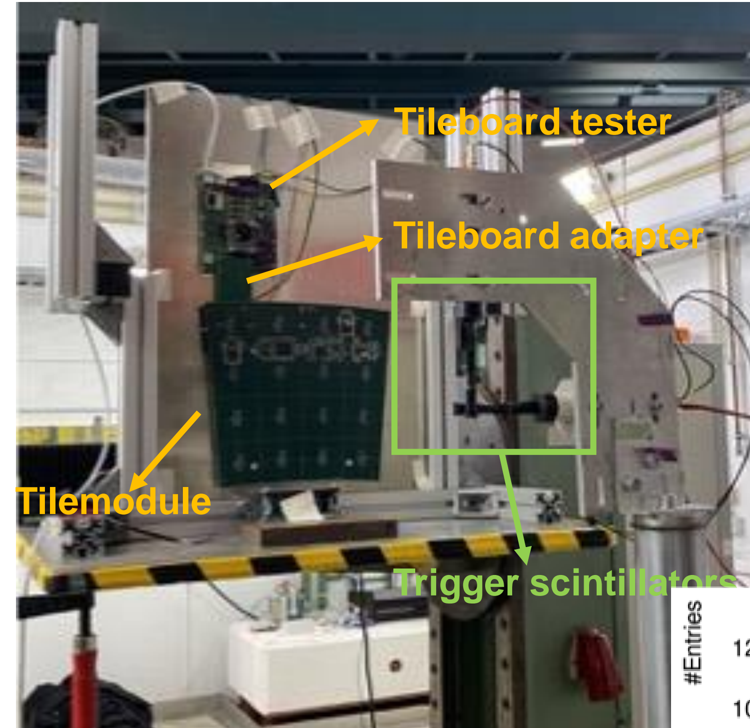


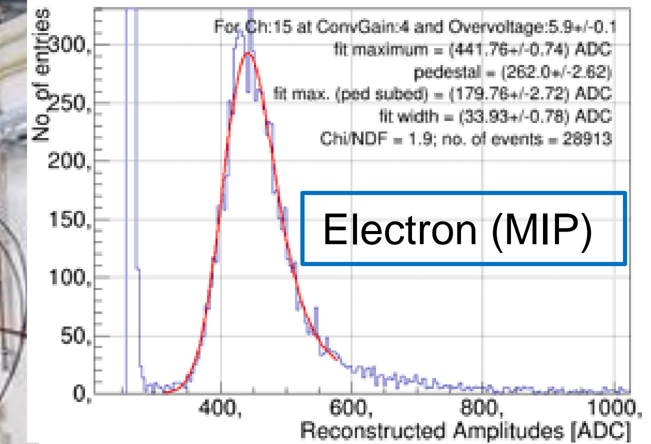


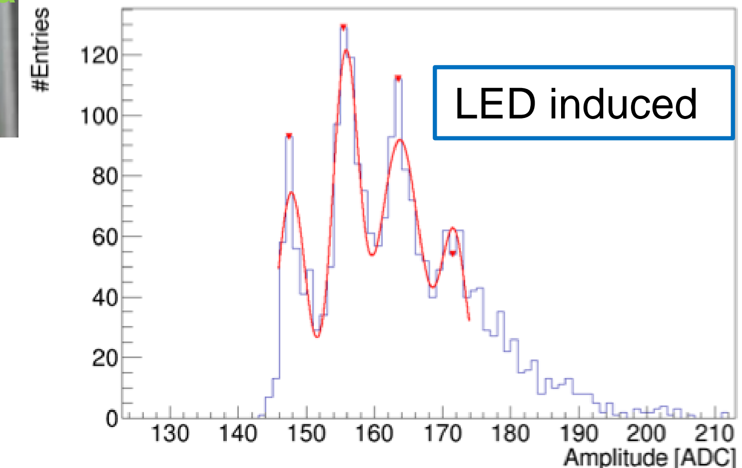
Tileboards in Testbeams

Tileboards routinely used for scintillator tile and SiPM validation in realistic environment

- Most tests done at DESY with 3 GeV electrons
  - producing MIP-like response in Tileboards without absorber
- Many different tile and SiPM types tested
  - Basic scaling laws of signal variation with tile and SiPM size verified
- Optical performance of SiPM-tile system characterised in terms of light yield
  - LY = MIP / gain (from single ph.e. peaks)
- Results entered into optimisation of detector layout in expected radiation field.
- Testbeam: Tilemodule performance verification:
  - Realistic harsh environment. No stability issues (crashes) observed (DAQ communication).
  - Realistic power supplies.
  - Smallest signals to be detected: Single ph.e. peaks could be well recorded.
- No issues with noise with unirradiated SiPMs.





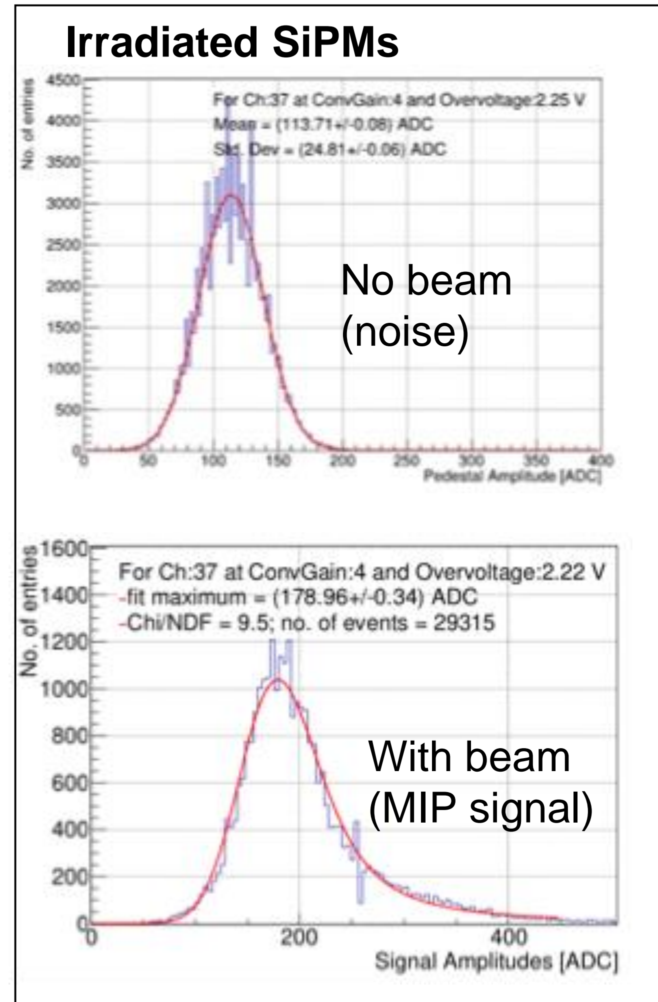


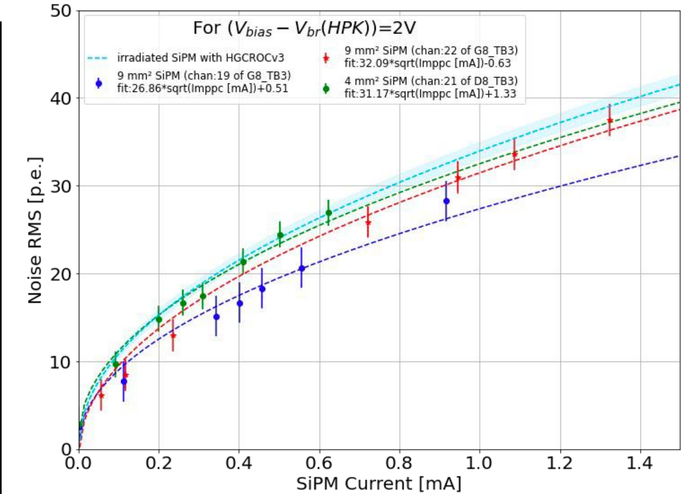
Tests with irradiated SiPMs

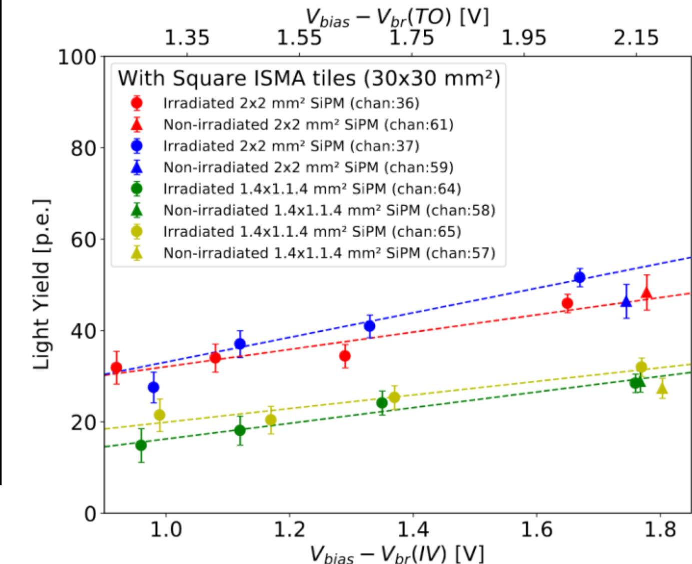
- Irradiated SiPMs on tileboards:
  - 2E12 n/cm² at RT equivalent to 5E13 n/cm² at -30°C.
- Noise behavior has been characterized by
  - Irradiated SiPMs
  - Un-irradiated SiPMs illuminated by DC light source.
- Model confirmed also on tileboards: SiPM dark current to pedestal width (noise).

- Light yield (LY) compared for un-irradiated and irradiated SiPMs in DESY testbeam for different SiPM sizes.
- No deviation from LY predictions observed for irradiated SiPMs.

- Signal (LY) and noise validated for 9mm² SiPMs in the same way as well.



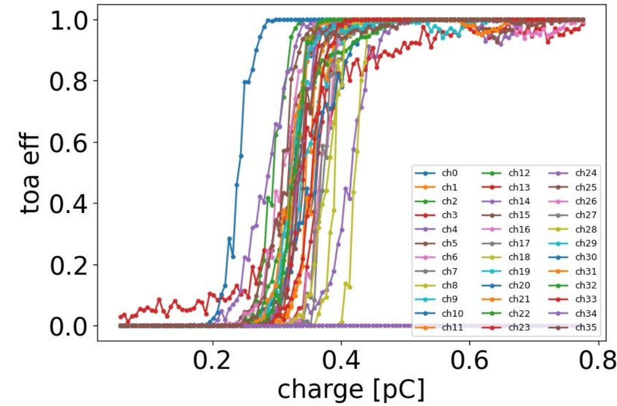


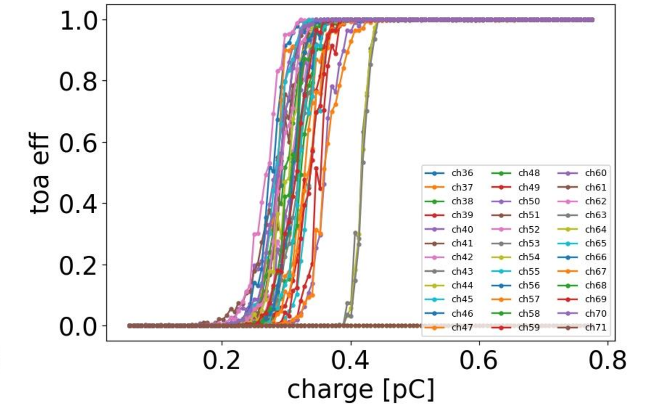


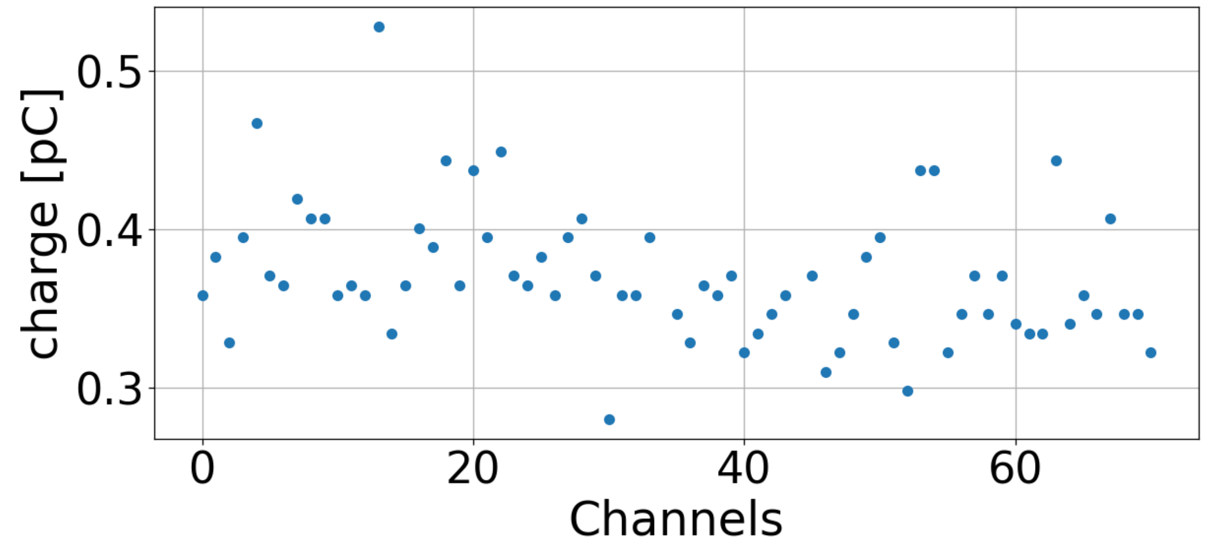
Tileboard3 – Data Taking scripts (DAQ)

- Data taking scripts for all important tasks in place, as e.g.
  - Pedestals /noise
  - Timing scans
  - Amplitude scans.
  - Testbeam data taking with external (beam) trigger.

- Further improvements of the scripts in preparation as for example ‘setting of Minimum TOA threshold’:
  - Results different for HGCROC alone and HGCROC on tileboard.
  - Isolated HGCROC results without capacitance (SiPM) at the inputs.
  - After configuration correction, good agreement of results. Minimum TOA threshold in the range of 1MIP possible for almost all channels.





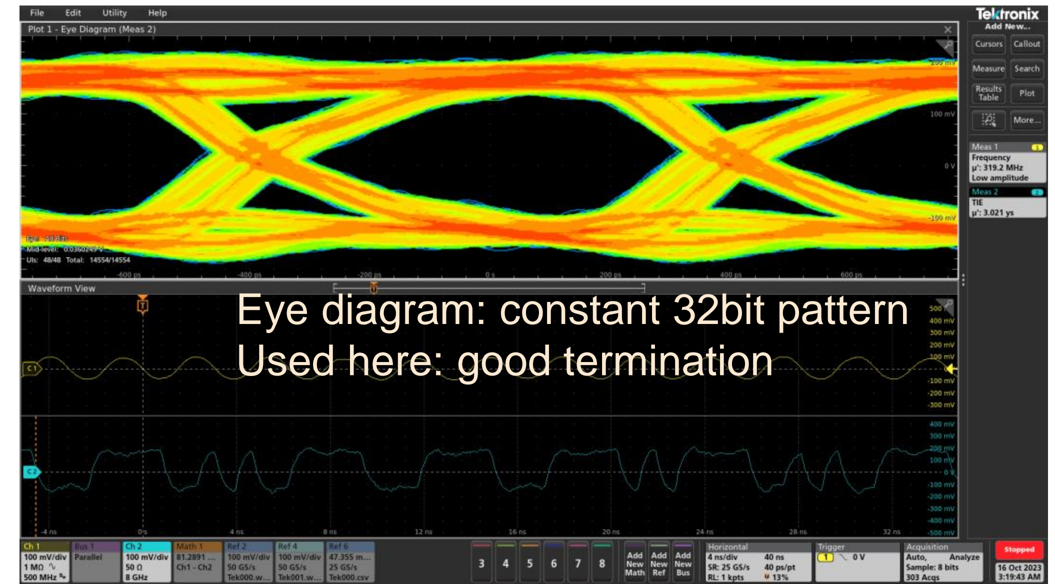


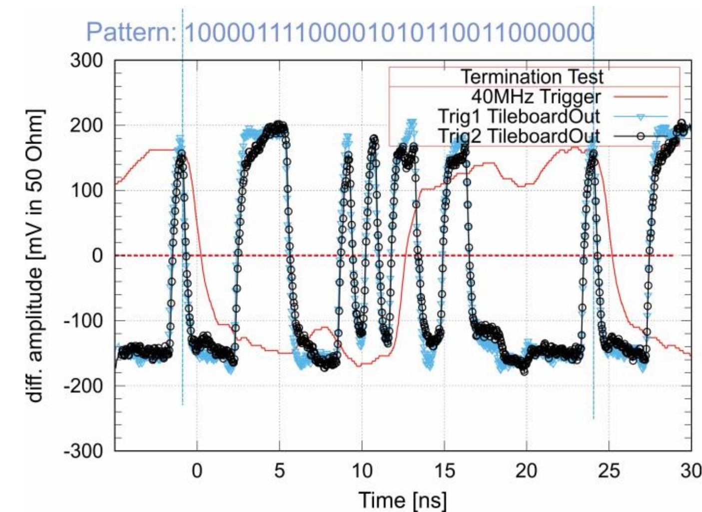
Charge Q(1px)= ~30fC (2V OV).
1MIP: 10px to 100px (tile size, material).
TOA(min) < 1MIP for most channels possible.

Tileboard3 – Fast Outputs Signal Integrity

- HGCROCv3 has 6 fast digital outputs, each operated at 1.28GBit/s.
- Signal integrity studies with TB-Testerv2 show problems:
  - Termination cannot be set correctly on TB-Testerv2.
  - Reflections cause significant eye-diagram degradation.
  - Common-mode level not correct.
- TB-Testerv2 will be replaced soon by KRIA based DAQ with correct termination.

- Termination tests with 100Ohm on adapter between tileboard and TB-Testerv2 show good eye openings and signal shapes (test setup).
- Tests need to be repeated in final setup with twinax cable and motherboard.

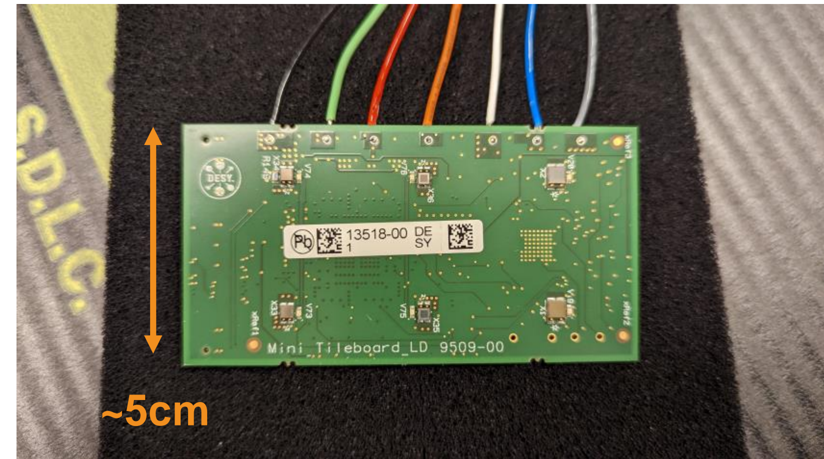


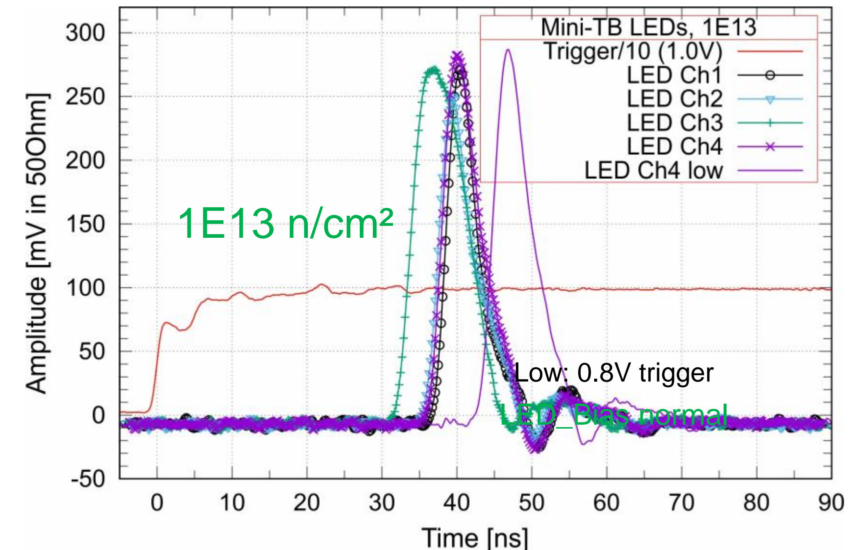


Terminated at TB-Testerv2 input,
Terminated at Tileboard output:
~10cm length difference

Mini-TB irradiation tests

- Mini-TB allows system irradiation tests: ROCv3 + GBT_SCA + SiPMs + new LED system.
- How much irradiation (neutrons, gammas) does the LED system tolerate?
- Most important: LED system must not come into critical state.
  - Considered unlikely – but prefer to test.
- Irradiation of 4 un-biased Mini-TBs at JSI Ljubljana with fluences:
  - 2E12 n/cm², 1E13 n/cm², 5E13 n/cm² (maximum expected dose), 1E14 n/cm²
- No special annealing. These tests: 6 months later.
- LED system fully functional till 1E13n/cm². No critical state till 5E13n/cm².
- Next test: TID (no critical states expected)





- Note that LED system mainly used for tests and commissioning, initial light yield calibration
- Later: not critical, but nice to have, and must be safe

Scintillator Tileboards – Open points

- Finish commissioning of B-tileboards (DAQ issues solved now, up to now no problems).
- Transition from HGCROC3 to HGCROCv3B.
- Prototype validation of HD tileboards (J- and K-).
- Irradiation (TID) tests of Mini-TB.
- Performance of tileboards in cassette with motherboard and twinax cable (full system test).
  - Signal/Noise in cassette environment
  - Signal transfer via twinax cable
  - Grounding and power stability
  - Cooling, temperature profiles
  - Options available in filtering setup and connection to safety ground to improve power / noise / grounding setup.

- No issues expected from any of the listed items.
- Expect results on these topics within the next 6 months.

Conclusion

- Tileboard design is mature, production of design variants is routine now and well advanced.
- Prototypes were tested extensively on testbench and in many testbeam campaigns, at DESY and in the US.
- Pre-series Tileboards are in operation. B12 tests not completed. Up to now no issues.
- Assembly of remaining pre-series boards ‘now’.
- Tileboard Procurement at CERN and in the US has started.
- Finishing remaining designs and tests in parallel.
- ESR2: System tests.

Backup

Tileboard Thermal Tests

Mixed Cassette Mockup Effort at Fermilab

Thermal teststand at Fermilab

Mock-up tileboard:

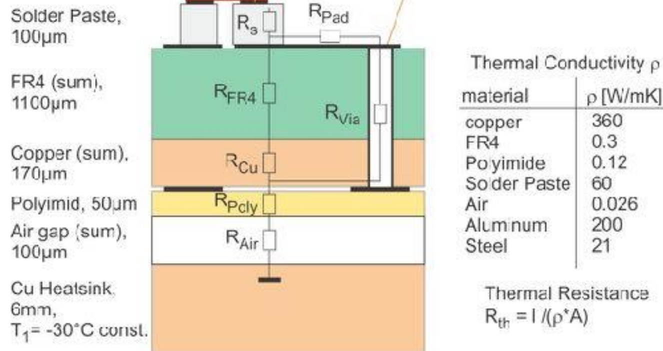
Full cycle to -30°C ✔

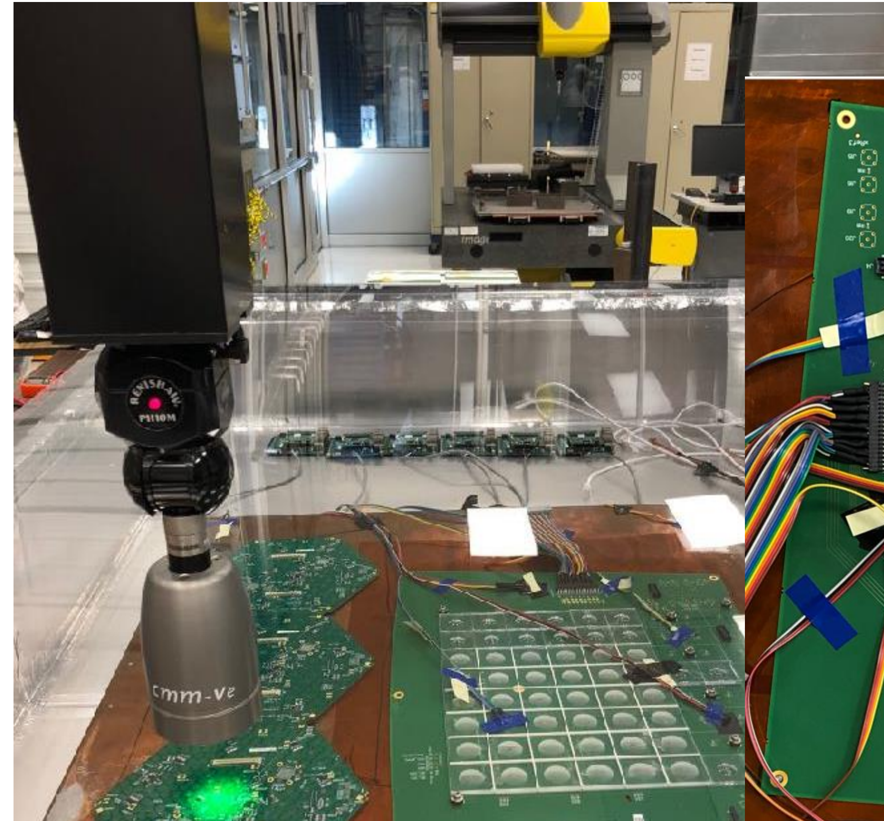
validate SiPM cooling through PCB using thermal vias

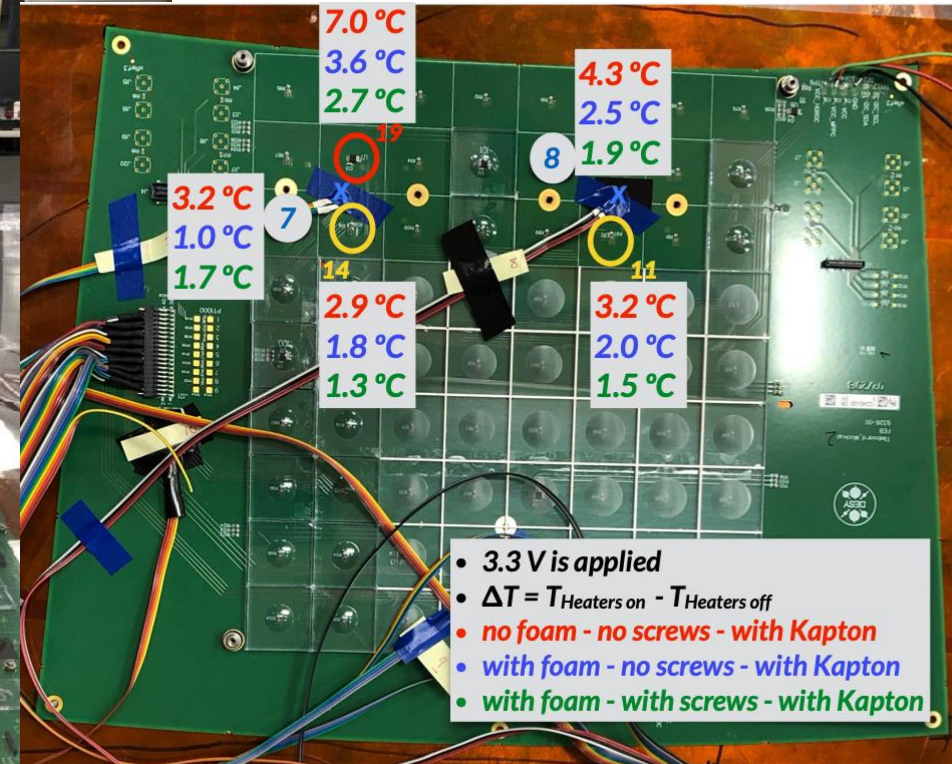
max increase with load: 2K

no strong gradients

heat conductance: contact to cooling plate (100 K/W) is largest effect







Scintillator Tileboards – Status of Designs

TB3.1 Design Status
Version 1.0 20.10.2023

Section	Tileboard	Board Number	Envelope (vers. 25)	Schematic 1)	Layout 1)	Prototype produced
LD (former BH)	TB3_D8	9533-01	done	done	done	9533-00, eWA 505496
	TB3_B12	9528-01	done	done	done	9528-00, eWA 505497
	TB3_B11	9549-00	done			
	TB3_E8	9512-01	done	in progress	in progress	9512-00, eWA 505498
	TB3_G8	9513-01	done	in progress	in progress	9513-00, eWA 505506
	TB3_G8L	9554-00	done	in progress	in progress	
	TB3_G8R	9555-00	done	in progress	in progress	
	TB3_A6	9531-00	done	done	in progress	
	TB3_A5	9547-01	done	done	done	9547-00, eWA 505499
	TB3_C5	9537-00	done	done	done	
	TB3_G3	9548-00	done	in progress	in progress	
	TB3_G3L	9561-00	done	in progress	in progress	
	TB3_G3R	9560-00	done	in progress	in progress	
	TB3_G5					
	TB3_G5L					
	TB3_G5R					
	TB3_G7					
	TB3_G7L					
	TB3_G7R					
HD (former FH)	TB3_J12		in progress			
	TB3_K12	9567-00	done	done	in progress	
	TB3_K12L			in progress		
	TB3_K12R			in progress		
	TB3_K10					
	TB3_K10L					
	TB3_K10R					
	TB3_K8					
	TB3_K8L					
	TB3_K8R					
	TB3_K5					
	TB3_K5L					
	TB3_K5R					

Done
Done to 98% (very minor changes)
Started (new main geometry)
Not started

- All basic types designed
- LD designs validated by final prototypes

Scintillator Tileboards – QC

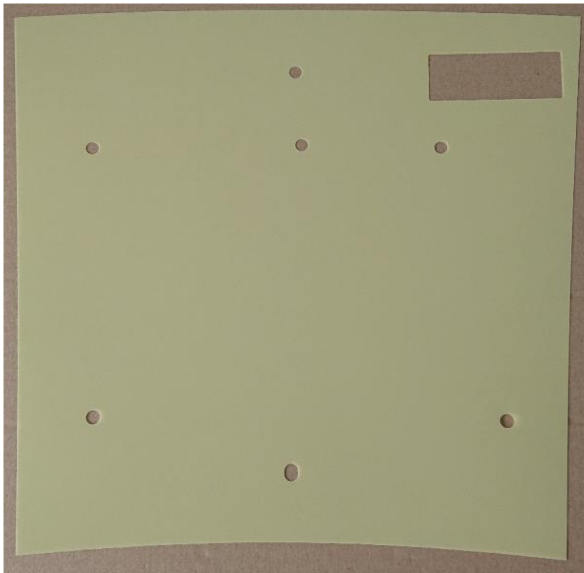
- QC for bare boards, mainly by vendor:
- Acceptance tests at TACs
- See procurement document.

- QC procedure of Tileboards (no tiles) and Tilemodules (with tiles) in TACs discussed with UMD.

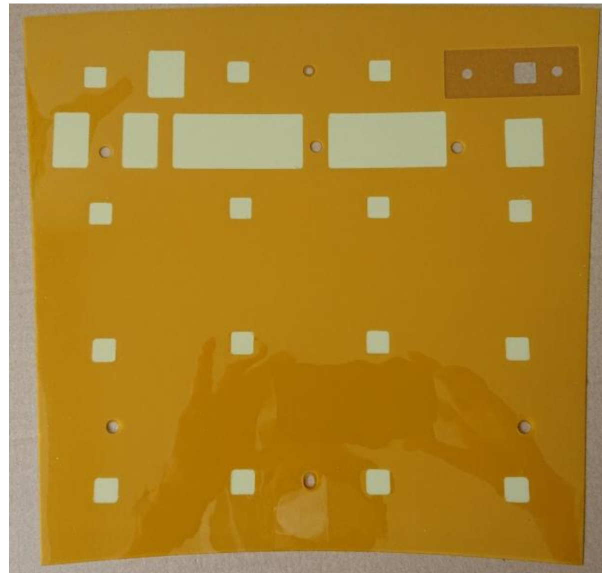
- Tileboard QC for DESY TAC to be developed together with KIT.
  - Tileboard TB3p1_D8 at KIT, but no TB-Testerv2/KRIA yet
  - Required scripts for QC exist as separate tasks in general DAQ or at DESY (tileboard specific)
- Scripts and procedures need to be optimised and automatised:
  - Not all procedures / scripts work satisfactorily yet, e.g. TOA/TOT threshold adjustment
  - Define pass/fail criteria for tests
  - Result transfer to database.
  - Hardware setup (multi-channel power supplies with remote control, setup for parallel board tests)

Pre-Series Production – Protective Foils

- Pre-series TB3.1s in cassettes will have protective covers on top and isolation foil below.
  - All designs ready for pre-series.
  - Protective covers are made from halogen-free FR4 and will be ordered as PCBs at PCB company in thicknesses 600µm (final).
  - Isolation foil (50µm polyimide) will be cut at DESY (Aristo cutter for tile reflector foils). Base material at DESY.
  - Both: Not on time-critical paths.



Protective Cover



Polyimide Isolation Foil (50µm)

Scintillator Tileboards – PCB specifications

Mechanical Description	
External size	Smallest: 14cm x 20cm Largest: 42cm x 45cm
External size tolerance	+100µm / -300µm (outer tileboard: x1+x2 AND y1+y4 in Fig. 4)
Thickness	1.3mm +/- 0.15mm
Number of layers	8

Finished copper thickness requirements	
External layers	35µm-50µm (final thickness)
Internal layers – planes	17µm plus/minus 10%
Internal layers – signals	17µm plus/minus 10%
Hole (via) wall metallization	>=25µm

Board finish requirements	
Silkscreen on top	Yes
Silkscreen on bottom	Yes
Silkscreen colour	White
Soldermask on top	Yes
Soldermask on bottom	Yes
Soldermask colour	Green
Surface finish	ENIG – electroless nickel immersion gold according to **IPC-4552**
Nickel thickness	3µm minimum – 8µm maximum
Gold thickness	0.04µm minimum – 0.125µm maximum

Tileboard specifications	
Blind/buried holes (vias)	No
Micro vias	No
Vias class 2 derogation	No
Minimum track width	0.1mm
Minimum track/pad clearance	0.1mm
Minimum hole (via) diameter	0.20mm (final diameter)

Additional specifications	
Filled and capped vias?	No
Via holes filled with resin	No
Specified stackup	Yes
Controlled impedance	Yes (plus/minus 10%)
Electrical tests	Yes
Test coupons required	Yes
Exclusively halogen-free materials	Yes
RoHS compliant	Yes

Laminate and copper-foil requirements

Base material, when used, shall be flame retardant rated **UL 94V-0** laminate glass-fibre epoxy and conform to L94 according to **IPC-4101/128, halogen-free**. Copper shall be type H with pits and dent, class B. When procuring base material, the following are required: minimum **TG 160°C**; minimum **TD (5%) 350°C**; minimum **T-288 35min**; maximum Z-axis thermal expansion coefficient above **TG 280PPM/°C** (alternatively Z-axis thermal expansion coefficient between 50-260°C of **3.5%** maximum is acceptable)

Prepreg material shall conform to P94 according to **IPC-4101/128**, halogen-free and be subjected to the same requirement set forth for the laminate base material.

All internal layer copper foils shall conform to **IPC-4562/2 CU-E3, class 2**

Additional plating requirements

Finished external layers shall be 35µm-40µm and plated through holes plating shall be >=25µm. The copper plating shall be performed with plating chemistries/processes commensurate with the maximum aspect ratio plated hole in the board.

The quality of the copper plating shall be verified according to **IPC-TM-650, 2.4.18.1** as to tensile strength and according to **IPC-TM-650, 2.4.2.1** as to ductility.

Thieving may be added outside the circuit board border to compensate for high density areas on the board. For thieving within the borders of the circuit board approval is required.

Vias/through-hole requirements

Via drillings must be inside via pad – no breakouts are allowed

Negative etchback is not allowed. Positive etchback is permissible to 5µm maximum.

All holes shall be located within a 100µm-diameter of true position. Drilling should be according to **IPC-DR-572**.

Via holes and drillings are specified as final hole size.

Additional board-finish requirements

Solder mask over bare copper according to **IPC-SM-840**, class H. All fiducials, lands, vias and holes shall be free of solder mask material.

Silkscreen shall be with permanent, organic, non-conductive and RoHS compliant ink. Silkscreen ink must be capable to withstand peak temperatures of 260-270°C for a duration of 60 seconds and at least 3-4 cycles without discoloration.

An identification marking shall be applied on the PCB. It shall contain the PCB manufacturer logo, UL marking, date-code and surface finish according to **J-STD-609**. Marking shall be applied on silkscreen at a specified position.

Additional quality-control requirements

The printed wiring board, and test coupon when used in lieu of a production board, shall be according to **IPC-2221 and IPC-2222, type 3, class2**. Date code and PCB manufacturer logo shall be present on test coupons for traceability.

Acceptance of finished printed boards shall be in accordance with **IPC-A-600, class 2**.

Fabrication and inspection shall be according to **IPC-6011 and IPC-6012, class 2**.

The maximum allowable bow and twist shall be **0.75%**.

All quality controls shall be performed per **IPC-TM-650** procedures and per **IPC-4552**.

Packing requirements

Boards shall be wrapped in sulfur-free neutral PH wrapping paper and shipped in vacuum-sealed anti-static bags. A humidity indicator and desiccant should be inserted in the bags.

Table 2: Technical specifications for tileboard PCBs

Scintillator Detector – SiPM Bias Currents

Bias currents per ring and tileboard (8 channels, 40V) in µA for fluence 5*10^13n/cm²

Preliminary! ALDOv2 (2 BV channels per ASIC), 25mA per channel max.

CE-H: layers FH 9-12

r [mm], inner	ring	34	35	36	37
2179.20	h24				(not assembled)
					1760
				2210	1810
			2630	2220	1860
			2640	2260	1940
		3140	2690	2330	2020
		3210	2780	2420	2130
		3340	2910	2540	2250
1830.17	h12	3510	3080	2700	2390
		3740	3280	2880	2560
		4020	3530	3100	2750
		4360	3820	3350	2970
		4770	4150	3640	3220
		5230	4540	3980	3500
		5770	4990	4360	3830
		6390	5500	4790	4190
1537.05	h0	7090	6080	5290	4600

	34	35	36	37
(1): BV Current Sum per Tileboard, µA, 10°	13200	16730	16680	16160
(2): BV Current Sum per Tileboard, µA, 10°	41370	35890	31390	27620
(3): Sum (10°, µA), OLD Granularity	54570	52620	48070	43780
(1) * 2.25	29700	37643	37530	36360
(2) * 2.25	93083	80753	70628	62145
(3) * 2.25, NEW Granularity	122783	118395	108158	98505
Number of ALDOv2 per Tileboard	1	1	1	1
Number of ALDOv2 per Tileboard	2	2	2	2

Shown here: Old Setup for J/K Boards
Goto tab "Layer_Overview" for actual setup

10 degree-Tileboard, 0.834° tiles

not assembled

Connector/HGCROC Pos.

A6 - Board Type

4mm² SiPM, cast tiles
4mm² SiPM, molded tiles
9mm² SiPM, cast tiles

"Number of ALDOv2s per Tileboard" defines the number of ALDOv2s with the BV section enabled (with the big capacitors). The ALDOv2 for the VPA (2.5V) has the BV outputs disabled! So each tileboard has one more ALDOv2 than in this table, here only BV is shown!!

New: Only 4mm² in design. BV currents of former 2mm² fields have been doubled

New: Higher Granularity and 9mm² SiPMs in FH section. We assume that BV current only scales with number of channels: Factor 2.25

CE-H: layers BH 13-22

r [mm], inner	ring	38	39	40	41	42-43	44-45	46-47
2594.79	42							
2539.39	41				310	220	160	
2483.99	40			460	350	240	160	
2430.96	39			510	390	260	180	140
2377.93	38		740	550	430	260	180	140
2327.16	37		810	600	470	280	200	160
	36	1160	870	640	500	280	200	160
2227.80	35	1230	930	690	530	300	220	180
2179.20	34	1300	990	730	570	320	220	200
2132.67	33	1380	1050	780	600	340	240	220
2086.15	32	1450	1120	820	640	340	260	220
2041.61	31	1530	1180	880	670	380	280	260
1997.08	30	1610	1250	930	720	400	300	280
1954.44	29	1700	1330	1000	760	420	320	300
1911.80	28	1810	1410	1060	810	460	340	340
1870.99	27	1920	1510	1140	870	480	380	360
1830.17	26	2050	1610	1230	930	540	400	400
1791.10	25	2190	1730	1320	1000	580	440	440
1752.03	24	2350	1860	1430	1080	630	480	480
1714.62	23	2530	2010	1550	1170	690	540	540
1677.22	22	2730	2170	1690	1280	760	600	600
1641.41	21	2960	2360	1840	1390	840	660	660
1605.60	20	3230	2570	2010	1530	930	740	720
1571.33	19	3520	2810	2210	1680	1040	820	800
1537.05	18	3850	3080	2430	1850	1150	920	900
1504.23	17	4220	3380	2680	2050	1290	1040	990
1471.42	16	4650	3720	2960	2270	1440	1170	1100
1440.00	15	5120	4110	3270	2520	1620	1320	1220
1408.59	14	5650	4540	3620	2800	1820	1480	1350
1378.52	13	6250	5020	4020	3130	2040	1680	1500
1348.45	12			4470	3490	2300	1890	1660
1319.66	11			4970	3900	2590	2140	1840
1290.87	10			5530	4360	2920	2420	2040
1263.31	9			6150	4890	3290	2740	2260
1235.75	8			6850	5470	3710	3110	2500
1209.37	7			7630	6130	4190	3520	2770
1182.99	6			8500	6860	4720	3980	3070
1157.73	5						4500	3400
1132.48	4						5080	3770
1108.30	3						5740	4170
1084.12	2						6480	4620
1060.98	1						7310	5110
1037.83	0						8230	5650

10 degree-Tileboard, 1.25° tiles

	38	39	40	41	42-43	44-45	46-47
BV Current Sum per Tileboard, µA, 10°	3690	4340	4180	3550	2160	1520	980
BV Current Sum per Tileboard, µA, 10°	13450	10460	7840	6000	3360	2520	2380
BV Current Sum per Tileboard, µA, 10°	23360	18590	14480	10980	6620	5200	5140
BV Current Sum per Tileboard, µA, 10°	25890	20770	60650	47870	31930	26490	22300
BV Current Sum per Tileboard, µA, 10°	0	0	0	0	0	37340	26720
Sum (10°, µA)	66390	54160	87150	68400	44070	73070	57520
Number of ALDOv2 per Tileboard	1	1	1	1	1	1	1
Number of ALDOv2 per Tileboard	1	1	1	1	1	1	1
Number of ALDOv2 per Tileboard	1	1	1	1	1	1	1
Number of ALDOv2 per Tileboard	1	1	2	2	2	2	2
Number of ALDOv2 per Tileboard	0	0	0	0	0	1*	1*

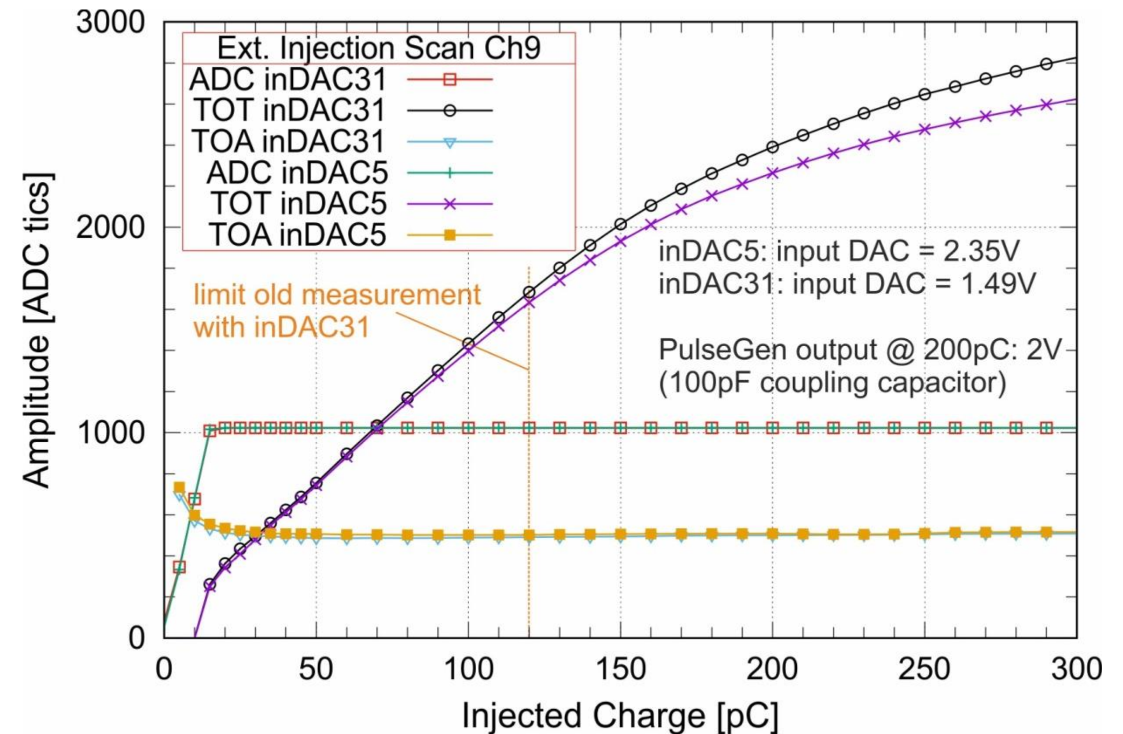
1*: ALDO current limit is 25mA per BV channel, 2 BV channels per ALDOv2 . There is no space on A6 for 2nd BV ALDOv2. 1 ALDO should be ok.

Tileboard 3 – Dynamic Range

- Test of maximum expected charge (design value: 300pC) by charge injection and HGCROCv2:
  - Sufficient dynamic range?
  - Do the HGCROC input protection diodes fire on huge input signals and cause sharp cut-off?

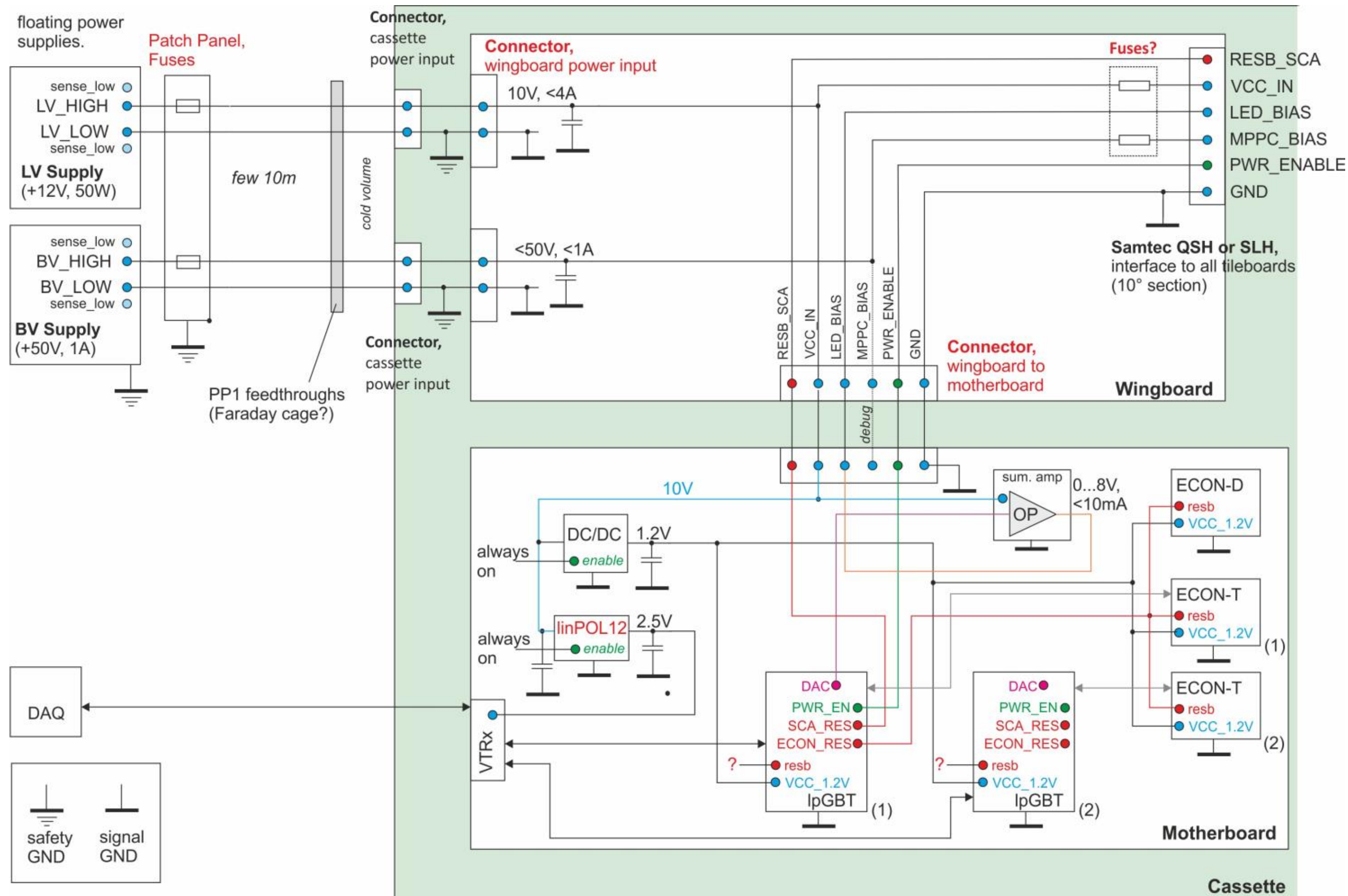
- Some saturation on TOT, but no cut-off and 300pC possible.

- Dynamic range for 9mm² SiPMs: Difference to 4mm² SiPMs can be compensated by conveyor gain (HGCROC input). To be verified.
- New in upcoming HGCROCv3b: Timing for ADC and TOT/TOA can be set separately.



Dynamic Range (Charge Injection), TOT, TOA behaviour

Tileboard 3 – Powering Environment



To tileboard