CE ESR1: SiPM-on-tile system overview, motherboards, cable assemblies

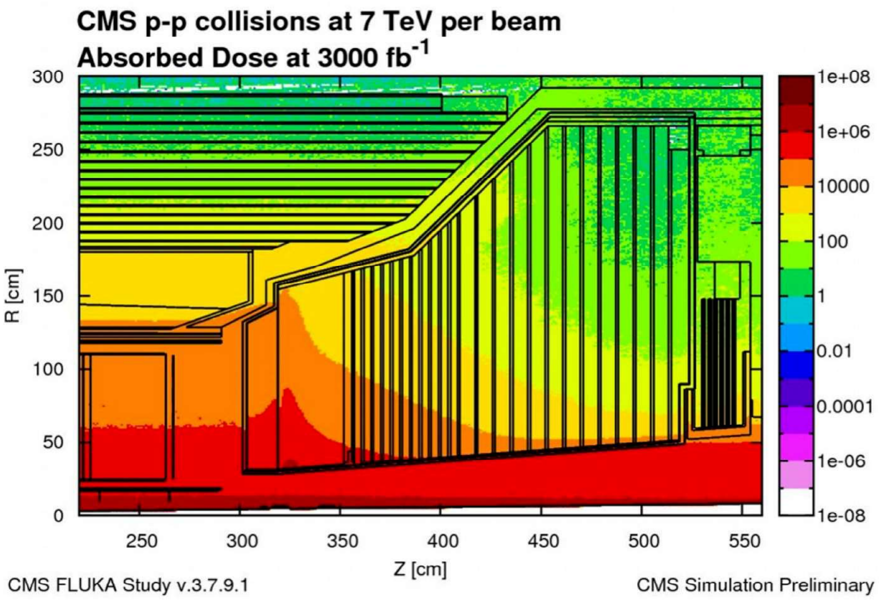
Ted Kolberg (FSU)
for HGCAL SiPM-on-tile group

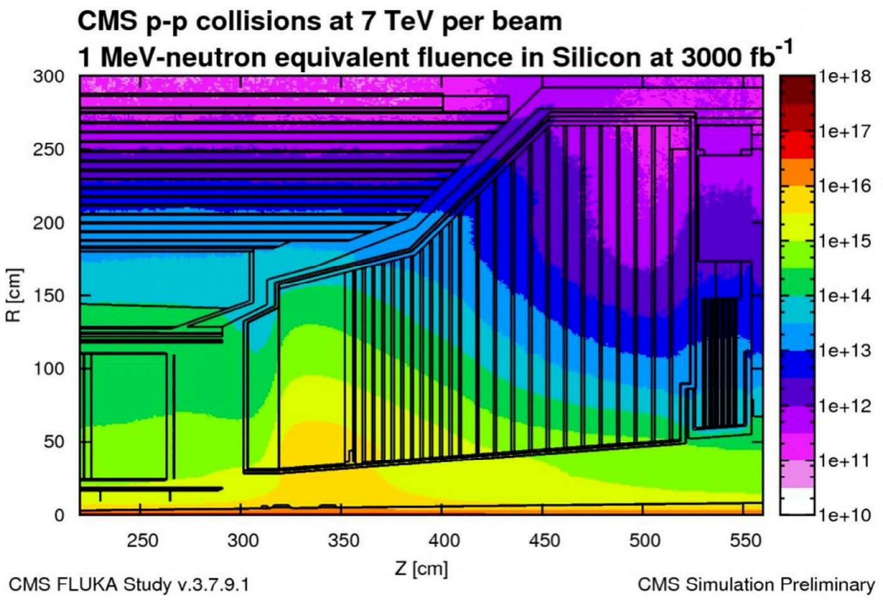
CE ESR1, Nov 10, 2023

Overview

- **Requirements & specifications**
- **Overall system design**
- **Technical progress:**
  - Cable assemblies (twinax)
  - Wingboards (BH type)
  - Next two talks: tileboard design, production readiness
- **Plans for ESR2**
  - Motherboards: status & plans
  - Wingboards (FH type), flex cable assemblies

Requirements & specs





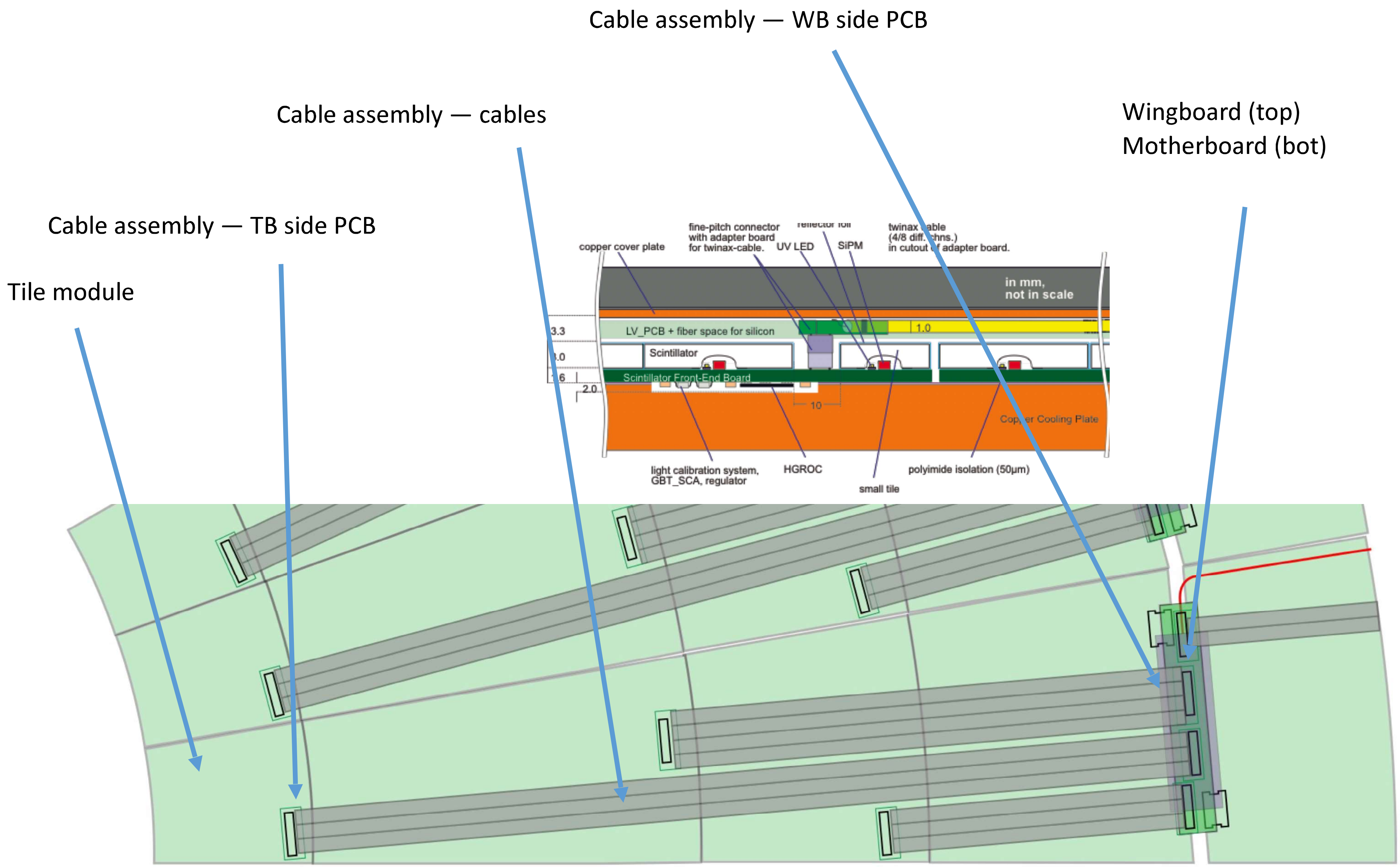
- Areas of the detector with fluence below 5×10^{13} MeV-neutron equivalent at 3000 fb^{-1} can use **plastic scintillator as the active material, with a significant cost savings** relative to silicon.

- Placing the whole detector, including the hadronic part, in the cold volume at -30 °C allows **direct SiPM-on-tile readout** to be used.

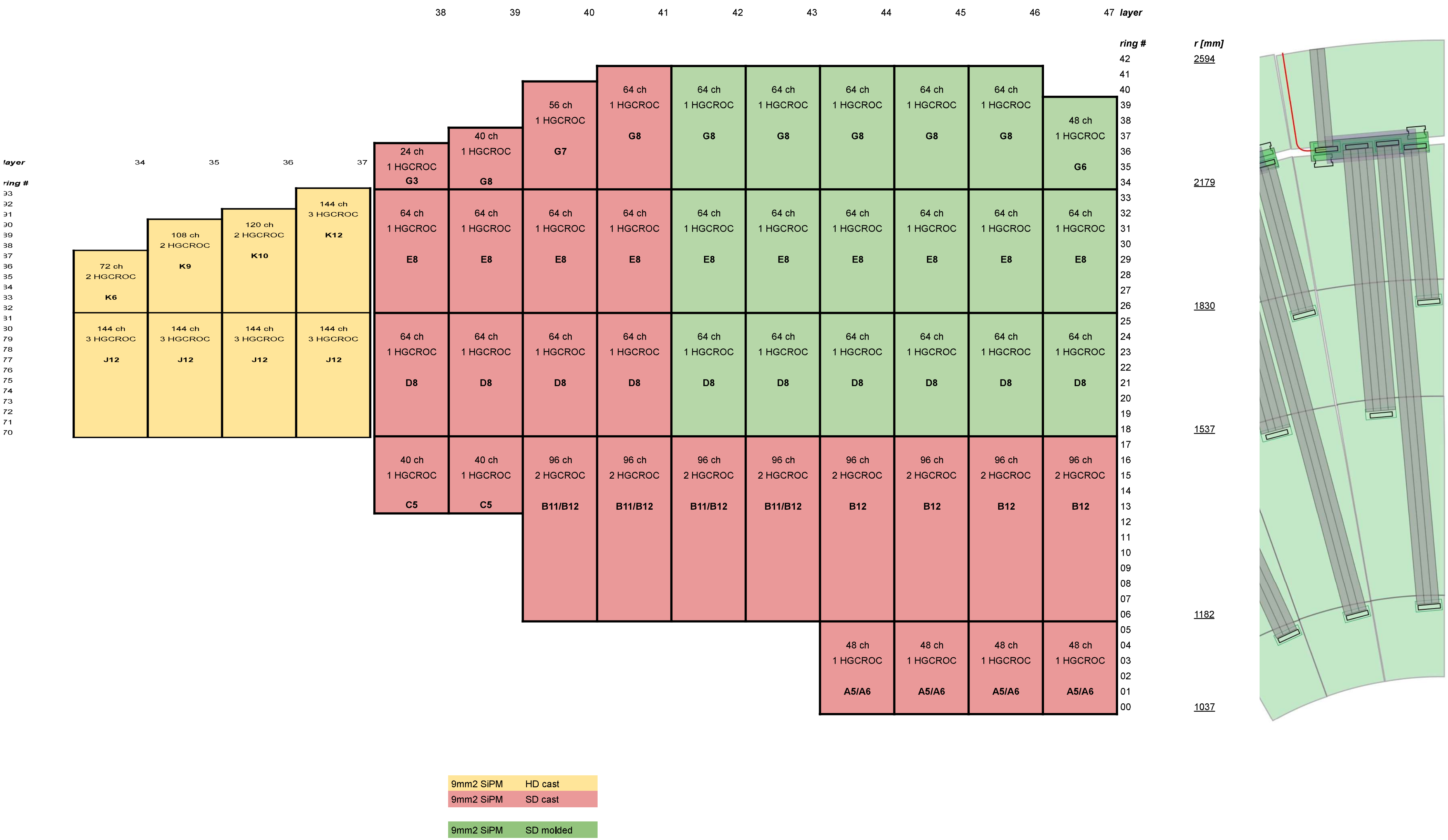
- SiPM-on-tile technology is flexible in terms of design: performance requirements can be reached by adjusting the **tile material, tile size, and SiPM size**.

    - Design goal is to instrument the whole volume while maintaining the possibility to **calibrate each channel with MIPs**.

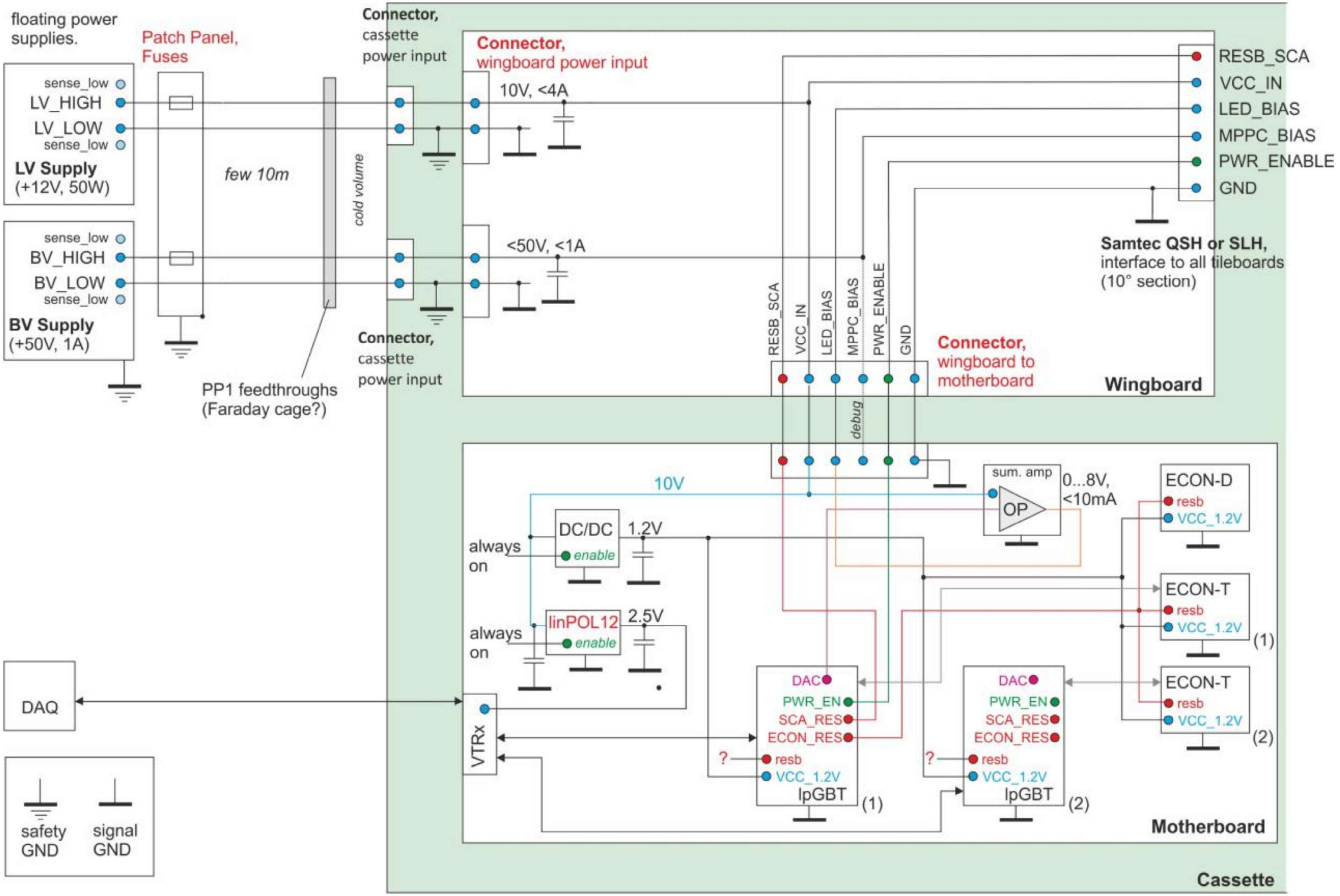
Mixed cassette — scintillator part



Configuration of tile boards

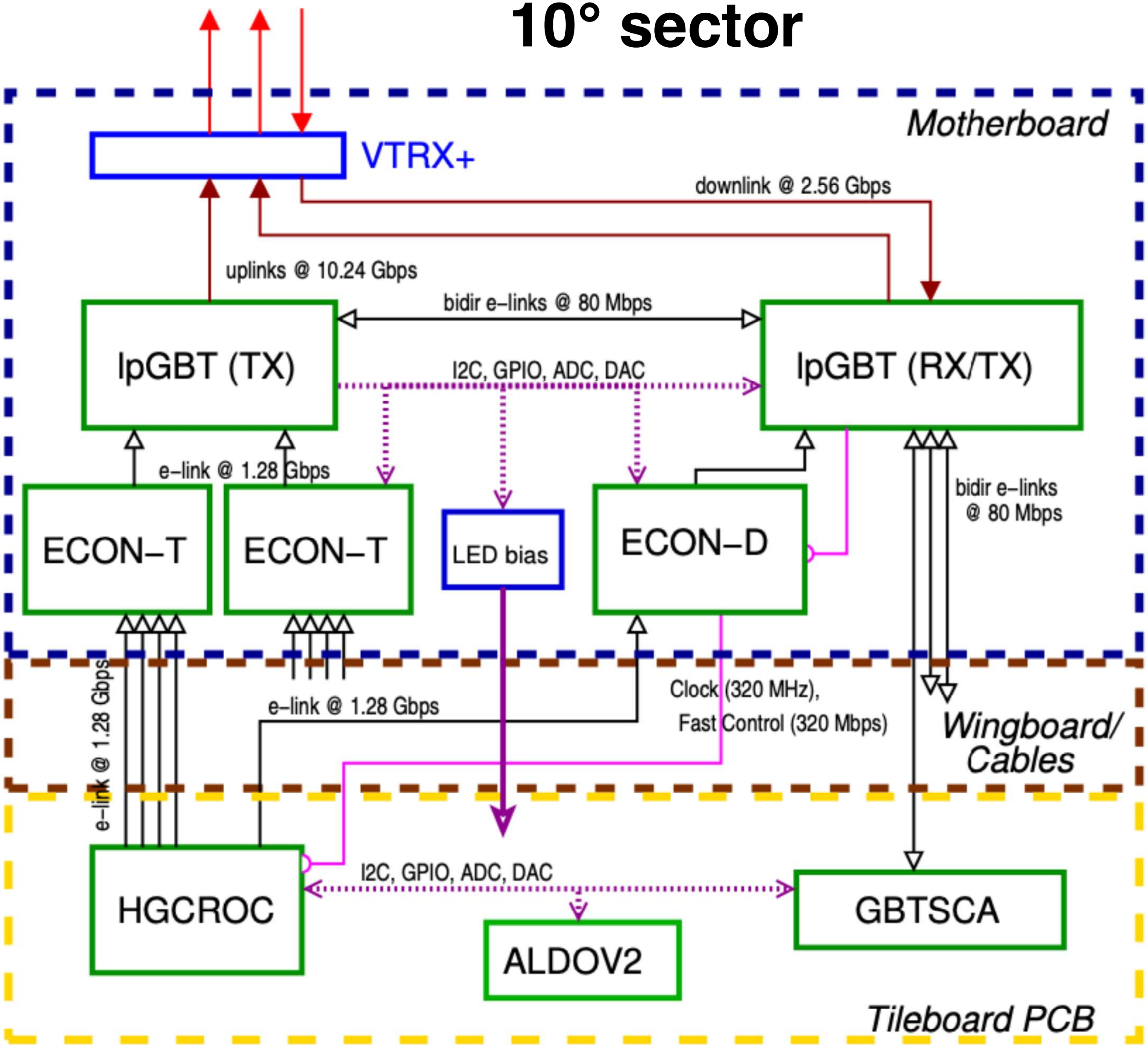


Powering scheme



Readout architecture

10° sector



up to 5 TB w/ up to 6 HGCROC

Tileboards

SiPMs are surface mounted on a **tile module PCB ('tileboard')**.

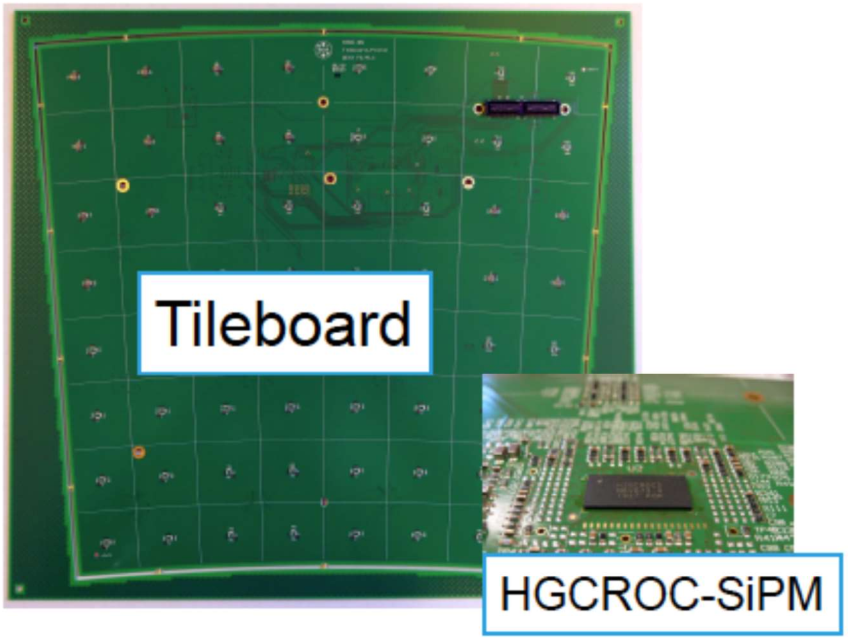
- Typical tile module hosts **64 channels read out by a single HGCROC-SiPM**, as well as associated controls.

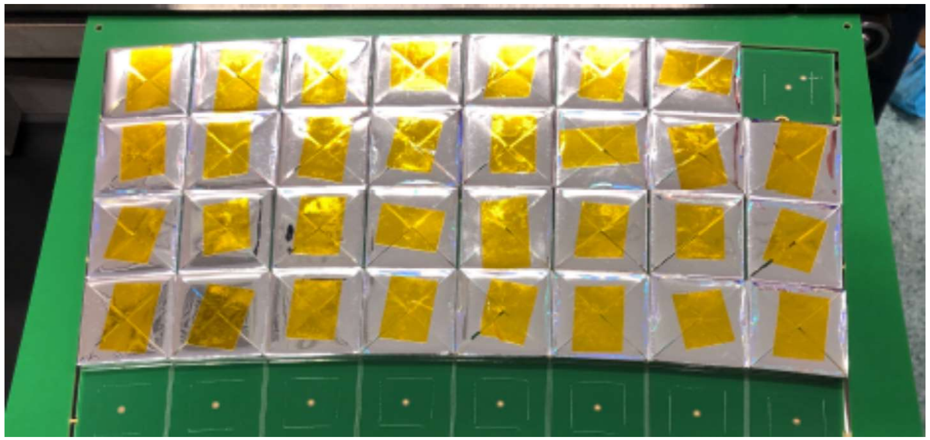
- LED system for commissioning and monitoring (one LED per channel).

Tiles are placed over the assembled tileboard by PnP and held in place by an adhesive.

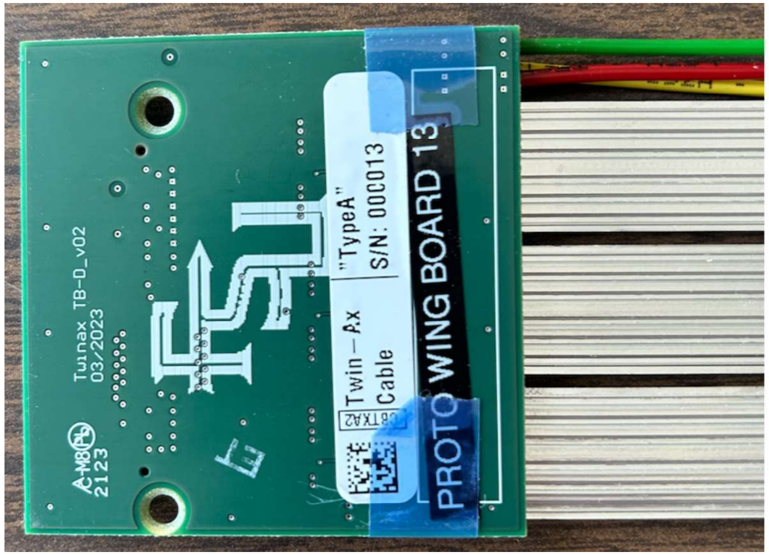
- Pre-series tile boards have been **constructed and are under test** — assembly of tiles to occur this fall.

Main topic of ESR1 for SiPM-on-tile system — next two talks will go into the detailed design.





Cable assemblies



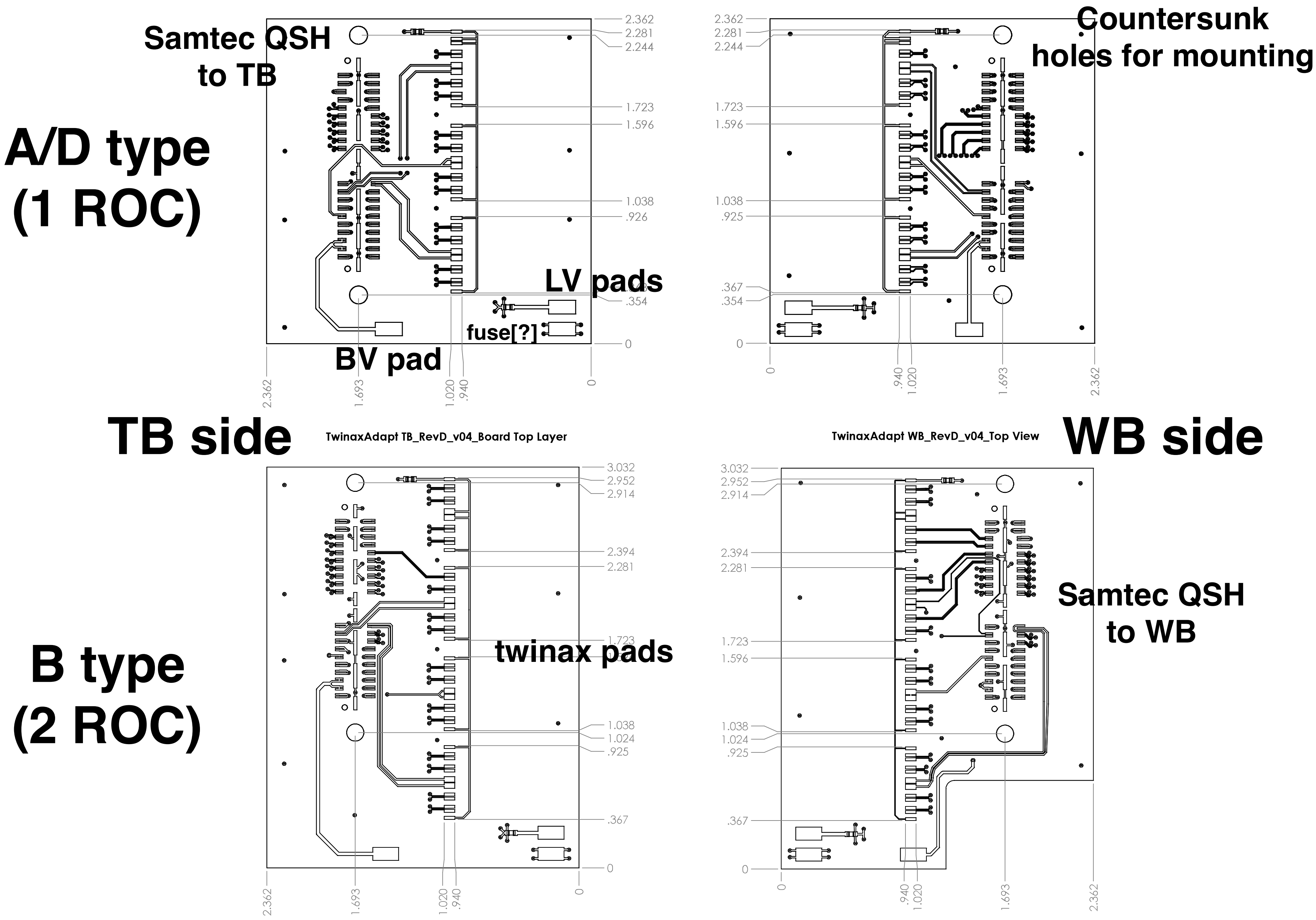
Cable assemblies are used to connect the individual tileboards to the motherboard via a passive wingboard.

For A, B, C, and D type tileboards (not adjacent to wingboard) twinax assemblies are used. PCBs to be produced and assembled commercially, with final soldering of cables and testing of assemblies in house at Notre Dame.

- 3M SL8800 series cable ribbons have capacity for multiple gigabit e-links.
- Assemblies already used to readout tileboard test stands.
- Production of pre-series assemblies under way (ND).

For tileboards next to the wingboard, small flex PCBs are used (no cable needed).

Cable assembly PCB designs



TwinaxAdapt TB_RevD_v04_Board Top Layer

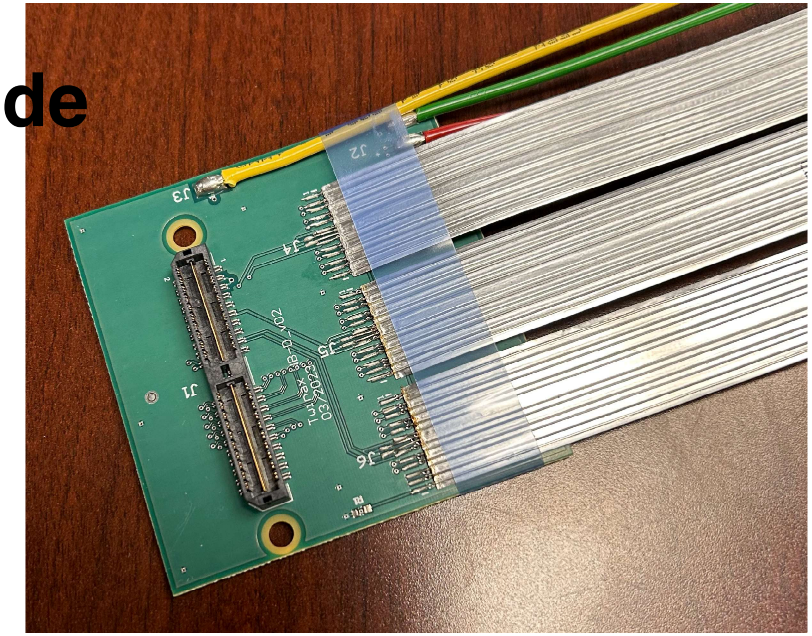
TwinaxAdapt WB_RevD_v04_Top View

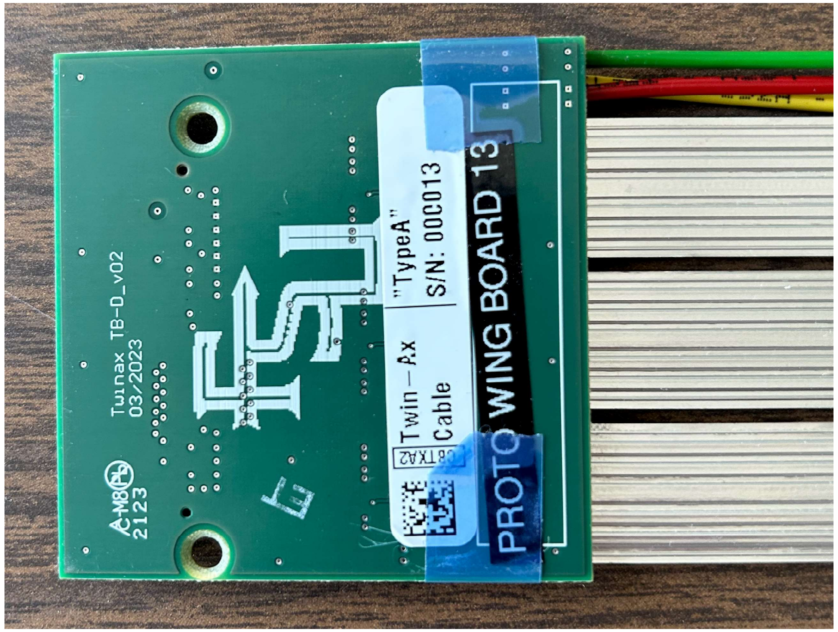
TwinaxAdapt TB_2ROC_RevA_v00_Board Top Veiw

TwinaxAdapt WB_2ROC_RevA_v00_Board Top Veiw

Pre-series cables

TB side





top side

E-link TX vs BER	Cable 1	Cable 2	Cable 3	Cable 4	Cable 5	Cable 6	Cable 7	Cable 8	Cable 9	Cable 10	Cable 11
HGCROC1_DAQ_OUT1	0	73		76	71	74	71	74	55	53	55
HGCROC2_DAQ_OUT1	0	0		0	0	0	0	0	0	0	0
HGCROC1_TRIG_OUT1	168	169		167	164	167	0	168	154	152	148
HGCROC1_TRIG_OUT3	142	142		141	141	141	141	141	124	124	124
HGCROC2_TRIG_OUT1	0	0		0	0	0	0	0	0	0	0
HGCROC2_TRIG_OUT3	0	0		0	0	0	0	0	0	0	0
ELINK_FAST_CMD	167	169		167	0	168	164	167	149	148	0
ELINK_FAST_CMD2	0	0		0	0	0	0	0	0	0	0
ELINK_SCA_IN	163	160		162	160	159	161	162	154	148	153

Power line (MΩ)	4.99	4.99	
SiPM+LED (MΩ)	4.99	4.99	
RTD+VMON (Ω)	10.6	10.6	
PWR_EN+SCARTSB (Ω)	10.5	10.5	
SCA_CLK P+N (Ω)	10.9	10.9	
	Type D	Type D	Type D
Retests starting 7/12			
E-link TX vs BER	Cable 1	Cable 2	Cable
HGCROC1_DAQ_OUT1	72		

07/25/23											
E-link TX vs BER	Cable D1	Cable D2	Cable D3	Cable D4	Cable D5	Cable D6	Cable D7	Cable D8	Cable D9	Cable D34	Cable D35
HGCROC1_DAQ_OUT1	72	75		73	72	75	74	74	75	76	74
HGCROC2_DAQ_OUT1	0	0		0	0	0	0	0	0	0	0
HGCROC1_TRIG_OUT1	170	170		167	168	168	167	169	169	166	168
HGCROC1_TRIG_OUT3	141	141		142	141	141	141	142	142	143	140
HGCROC2_TRIG_OUT1	0	0		0	0	0	0	0	0	0	0
HGCROC2_TRIG_OUT3	0	0		0	0	0	0	0	0	0	0
ELINK_FAST_CMD	169	169		169	168	169	168	[illegible]	168	170	169
ELINK_FAST_CMD2	0	0		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	0	0
ELINK_SCA_IN	163	141		164	161	161	161	139	164	162	162
Power line (Ω)	2.06	2.06		2.06	2.06	2.06	[illegible]	2.06	2.06	2.06	2.06
SiPM+LED (MΩ)	1.68	1.68		1.68	1.68	1.68	1.68	1.68	1.68	1.68	1.68
RTD+VMON (Ω)	10.5	10.6		10.6	10.6	10.5	10.5	10.5	10.5	10.5	10.6
PWR_EN+SCARTSB (Ω)	10.5	10.5		10.5	10.5	10.5	10.5	10.5	10.4	10.5	10.5
SCA_CLK P+N (Ω)	10.9	10.9		10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9

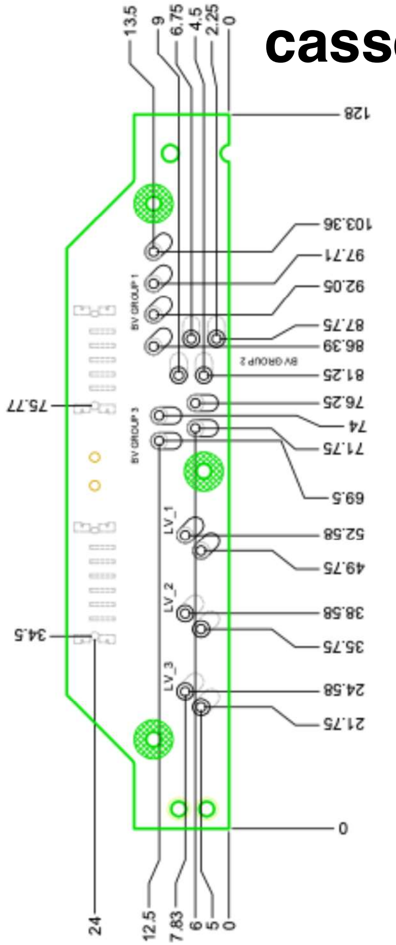
QC test results

Some features in test system but cable quality generally good

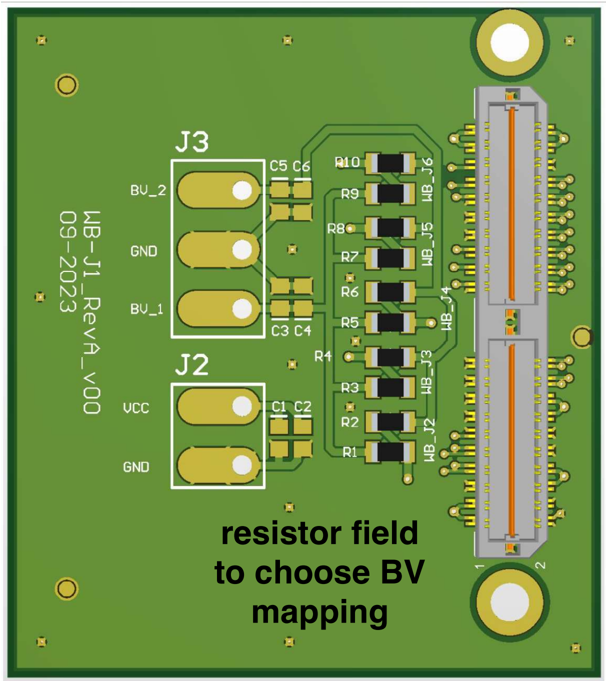
Power cable assemblies

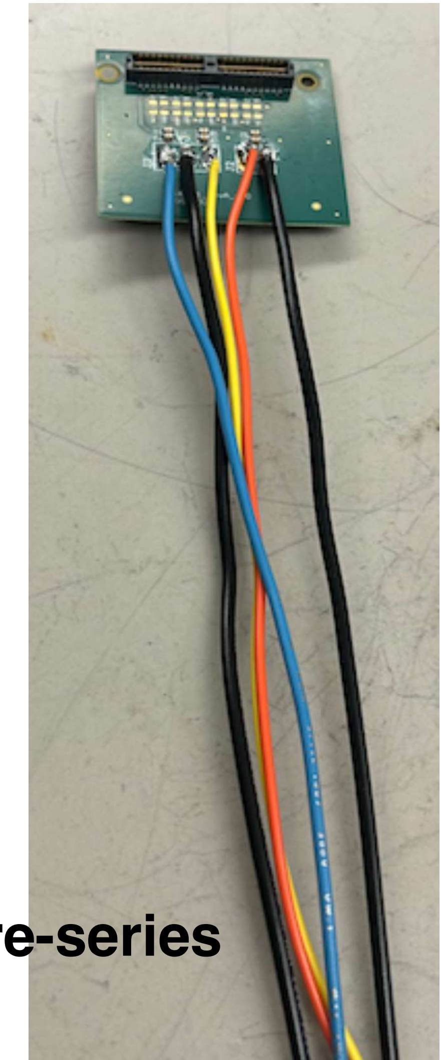
Power cables assemblies land LV and BV from cassette interface (up to 2 channels / 10°) at the wingboard, which distributes the voltages to the tileboards in that sector via cable assemblies.

cassette interface (30°)



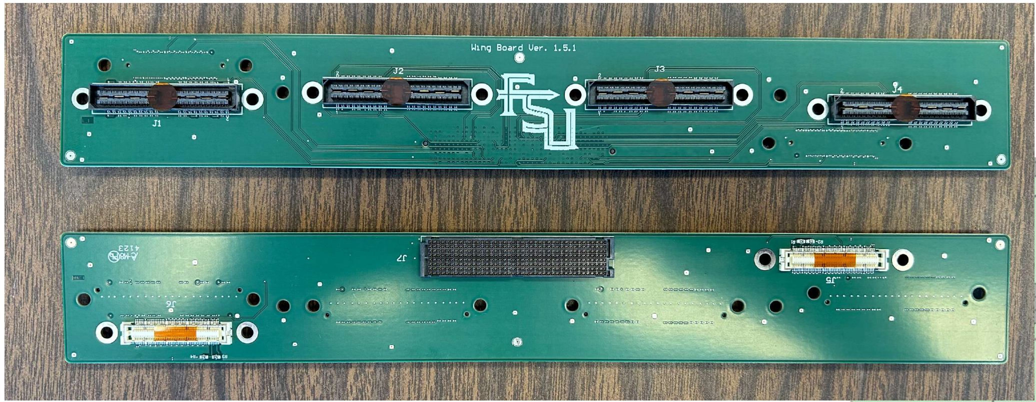
power adapter (10°)

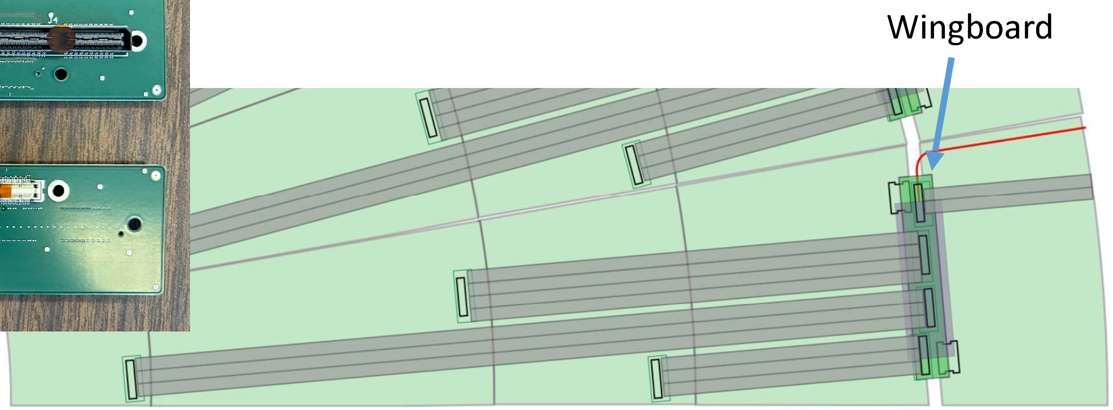




pre-series

Wingboards





Wingboard collects the signals from up to 5 TBs in a 10 degree wedge, and packs them onto a single connector to the motherboard.

- Wingboard above the cooling plate, with motherboard below, minimizes gaps in the scintillator layer.

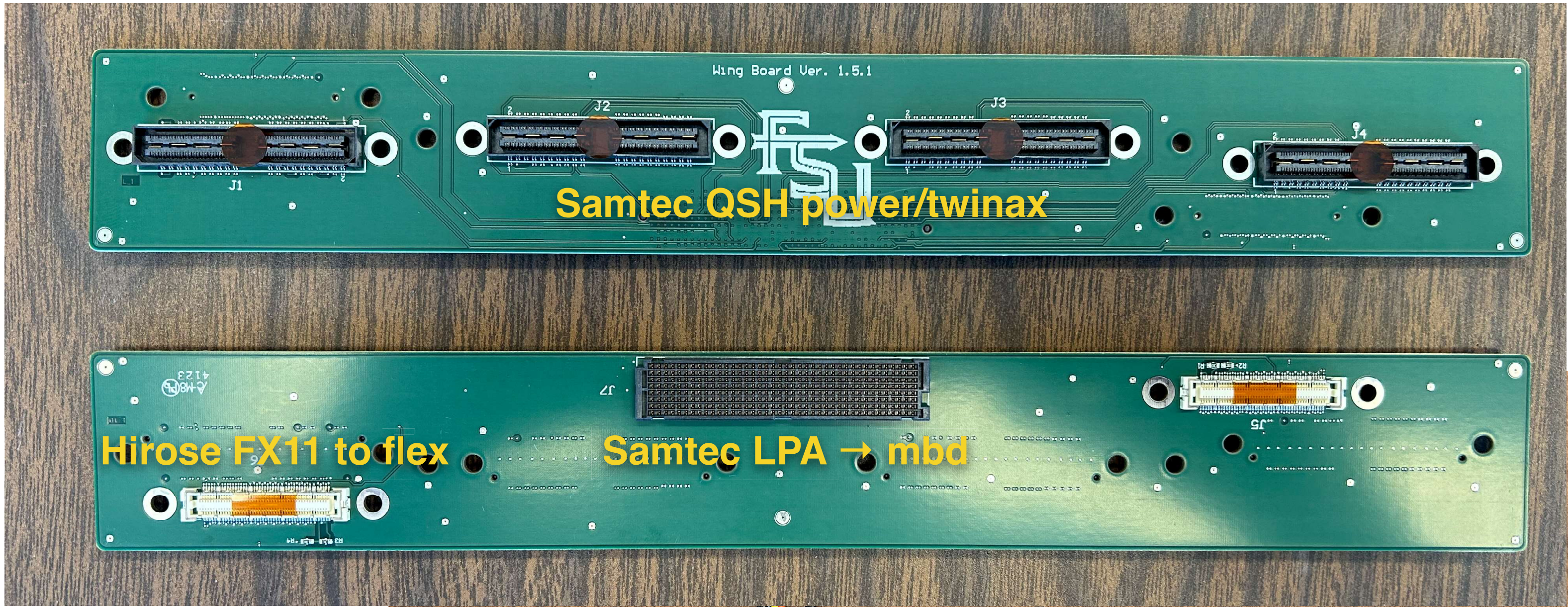
Pre-series wingboards have been produced.

- Documented in EDMS doc 2392324.

First four layers will use a smaller, simpler variant.

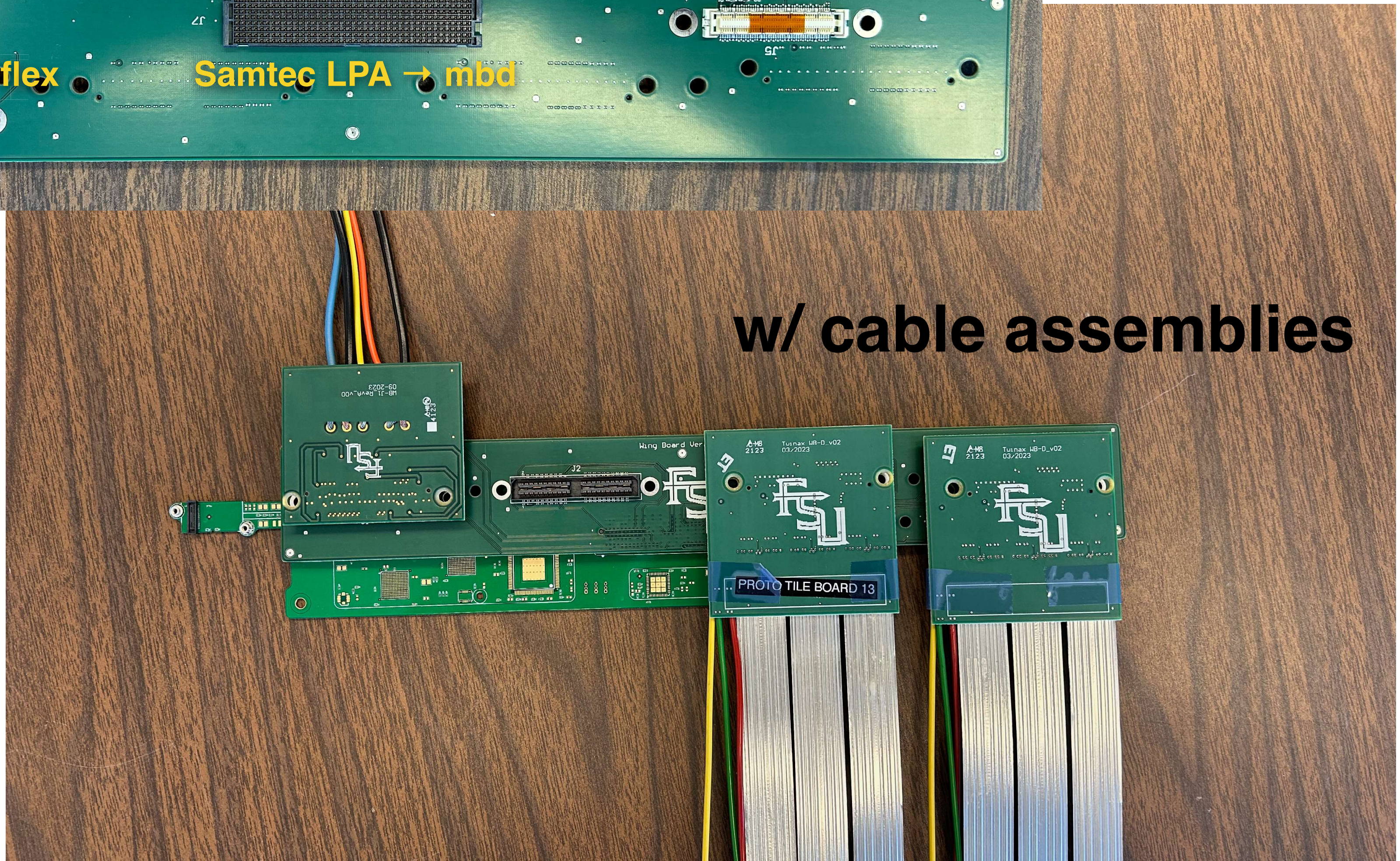
- In the mechanical design stage.

Wingboards (cont.)



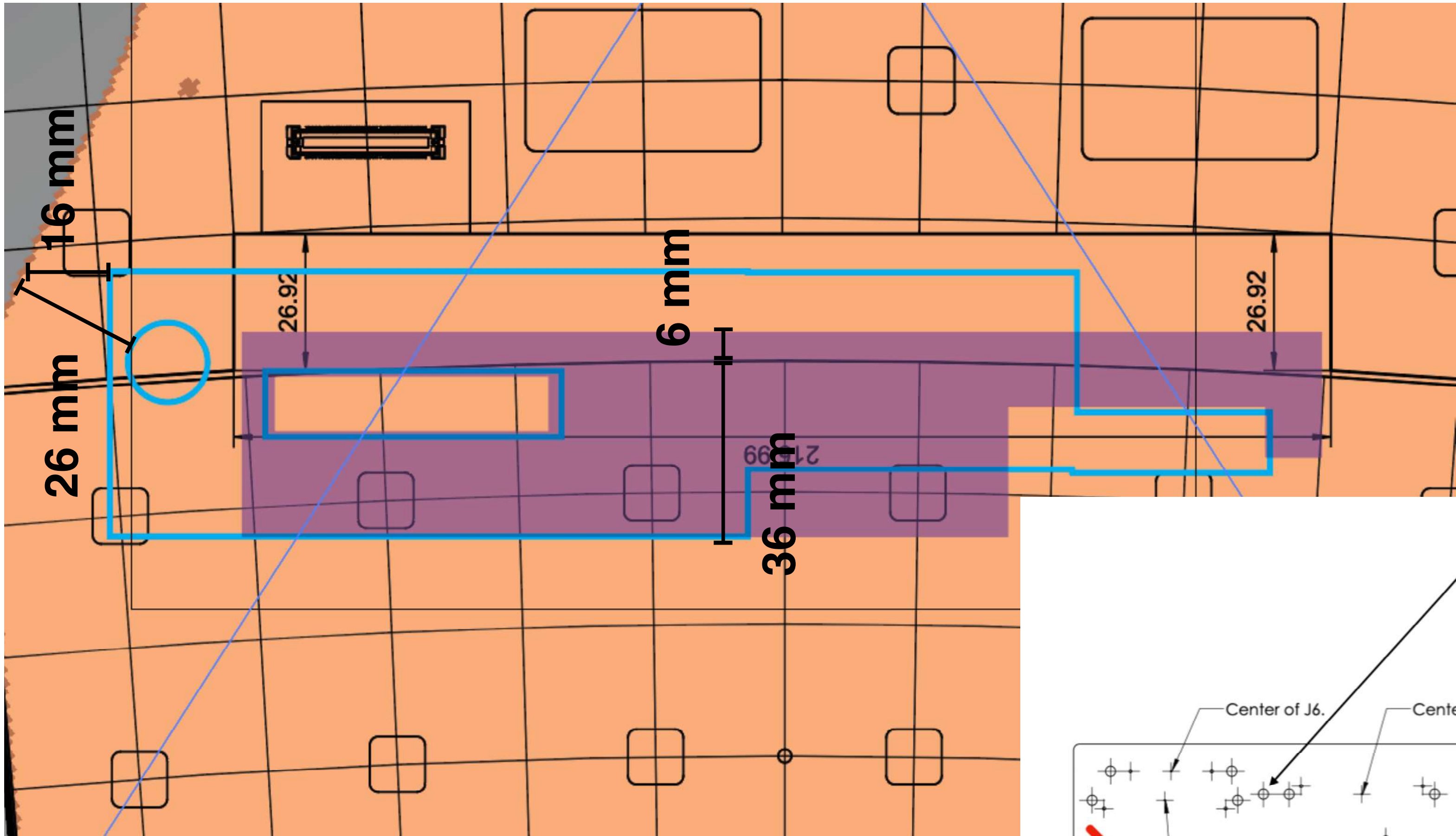
top

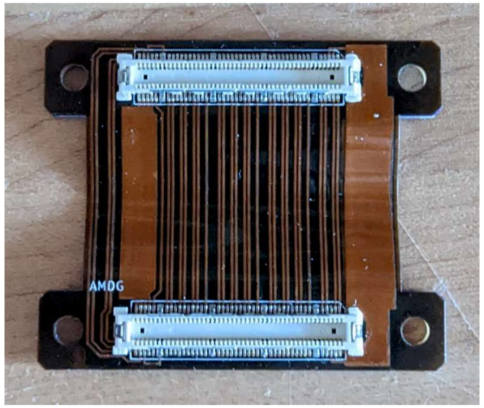
bottom



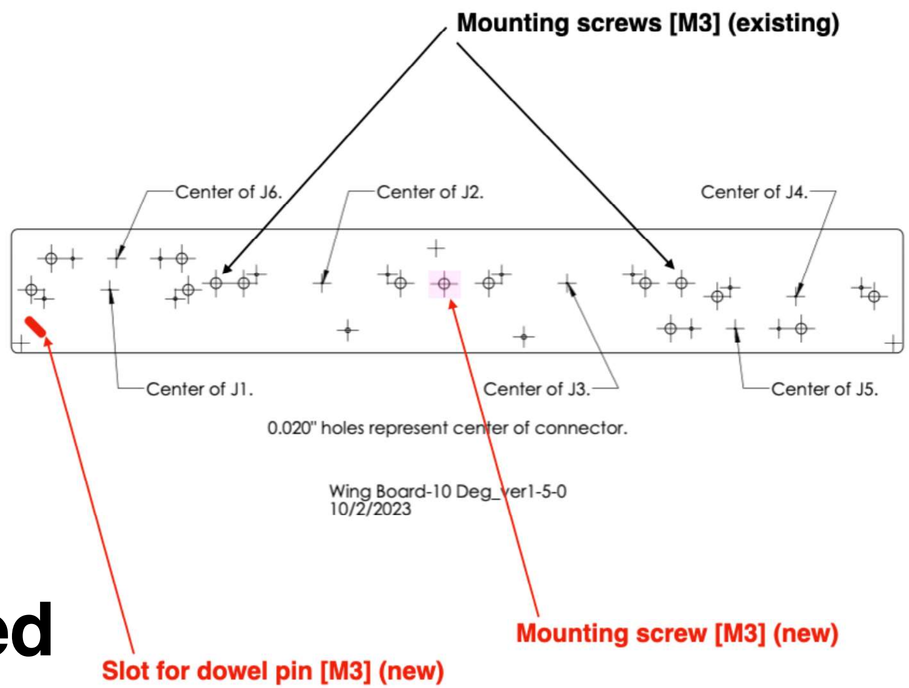
Preview: ESR2

Wingboards - mechanics



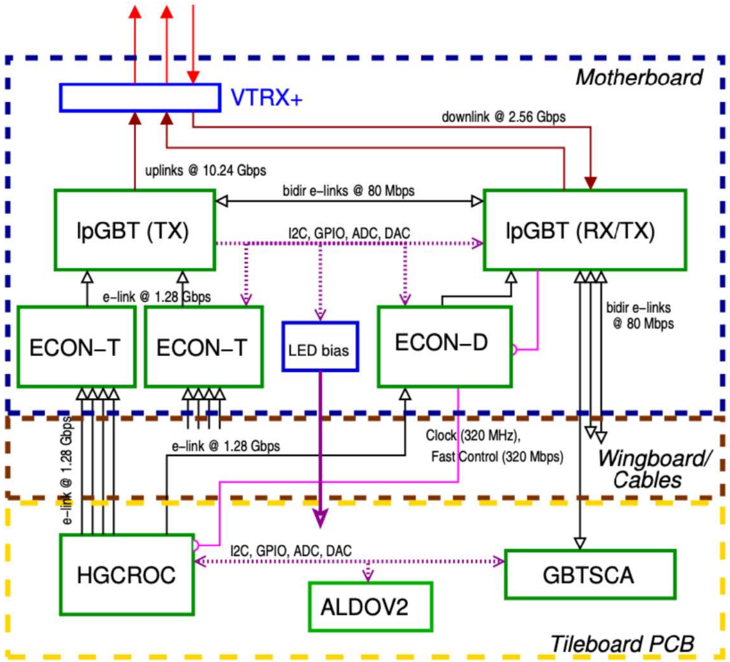


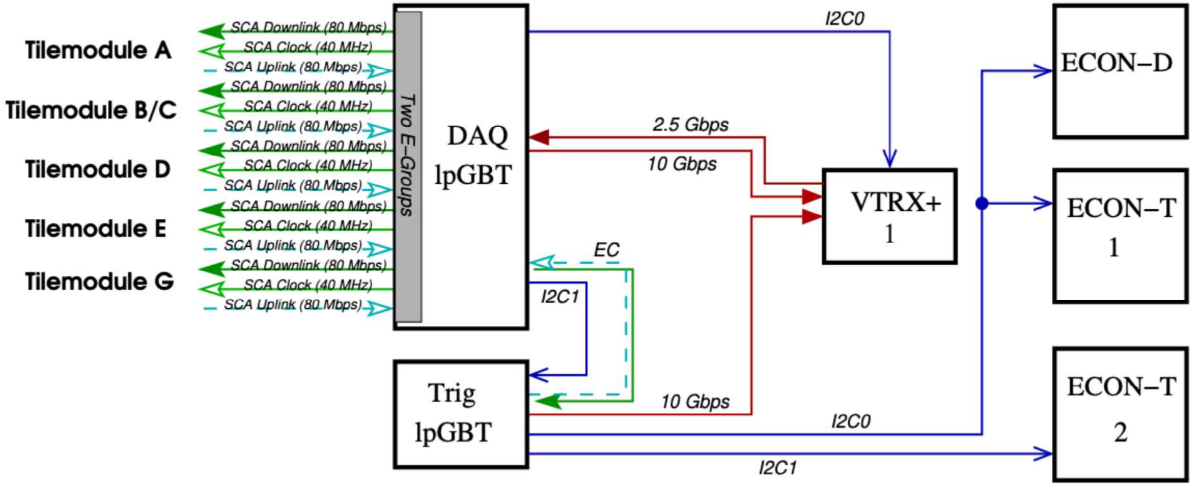
concept for
FH wingboard



proposal
for improved
mounting

Scintillator motherboards





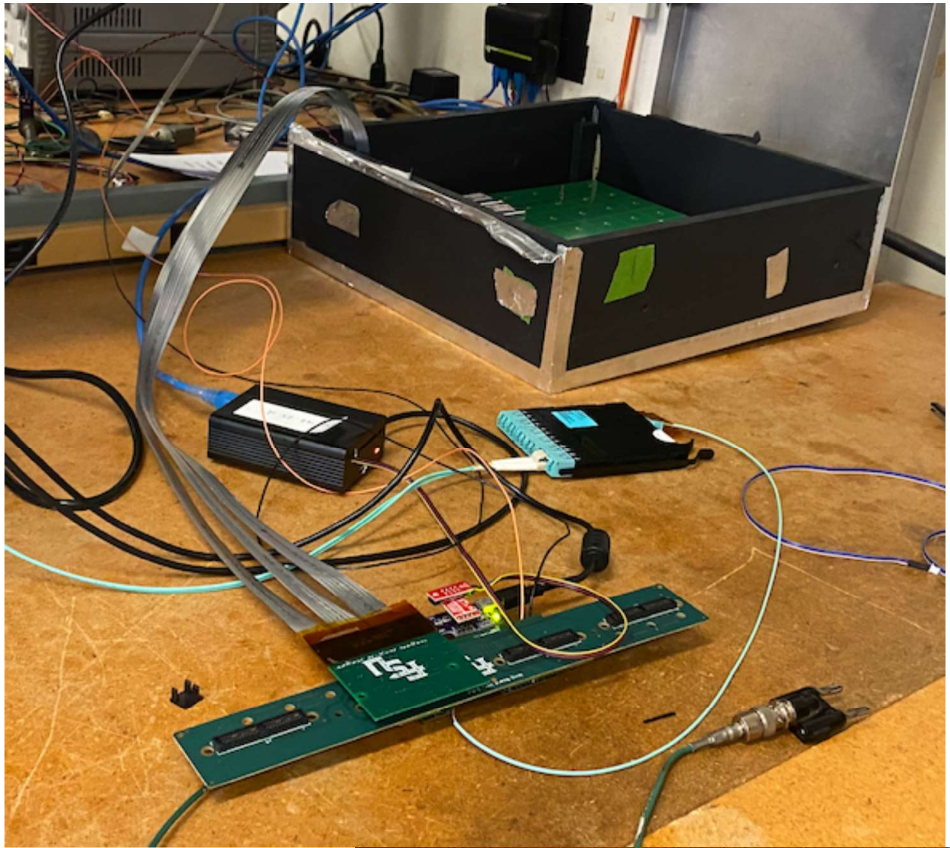
Scintillator motherboard uses ECON ASICs to manage controls and readout for a 10 degree wedge (up to 5 TBs with up to 6 HGCROCs).

- Performance of high speed elink transmission through chain of TB, cable assembly, wingboard, and motherboard studied on FNAL test stand.

First motherboard prototypes have been constructed and are under test.

- Design document at EDMS doc 2756943.

Motherboard tests

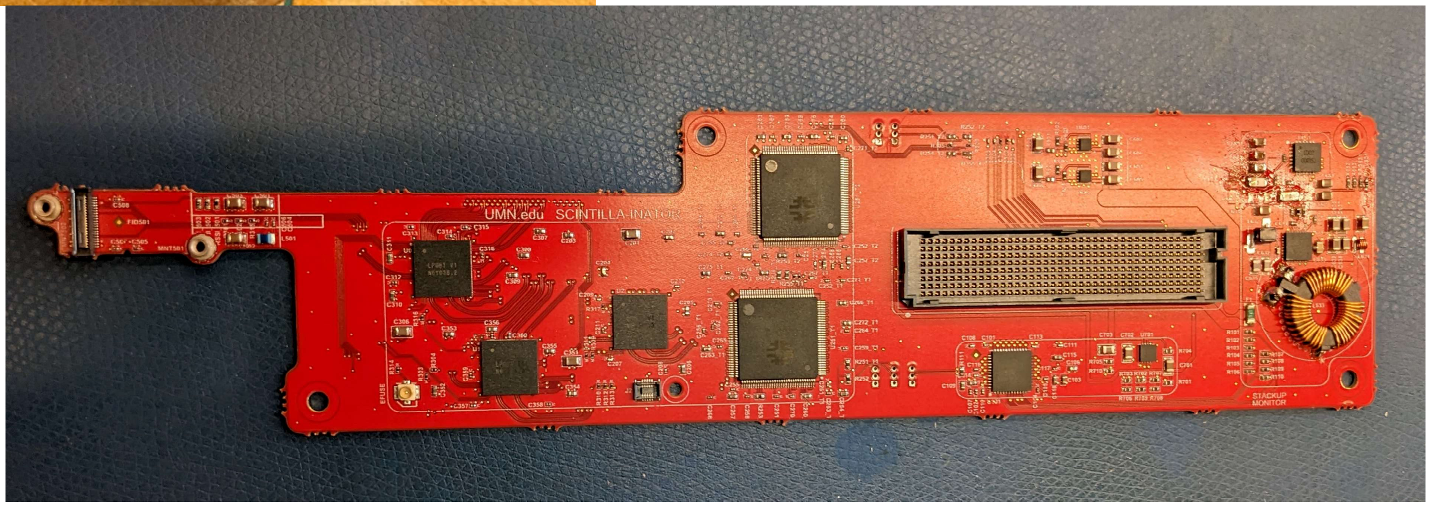


Scintillator V2 system test bench at FNAL:

- Tileboard with HGCROCv2 read out through cable assembly, wingboard, to Si engine w/ 'interposer'.
- Good signal integrity with this setup.

Now preparing components for V3 test (whole cassette).

- No ECON-D on V3 motherboards (DAQ signals pass-through with lpGBT)



Cost and schedule

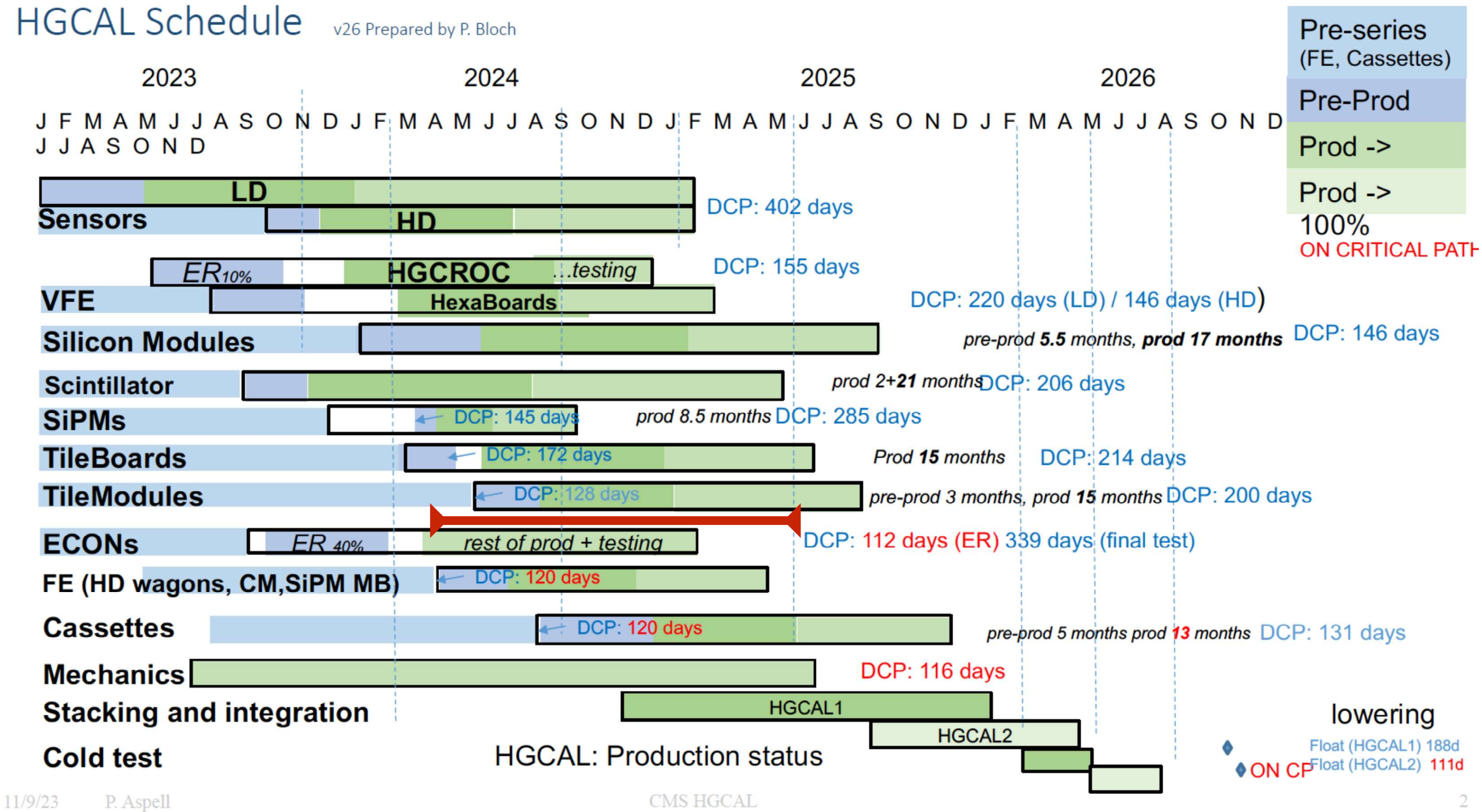
Production cost for cable assemblies and wingboards, excluding labor: estimated at $230k

- Driven mainly by large number of connectors to be bought
- Foreseen to begin Q2 2024 with testing continuing through Q2 2025

Production cost for motherboards, excluding labor: estimated at $425k

- Driven by ASICs and PCB manufacture/assembly
- Foreseen to begin procurement Q2 2024 with testing continuing through Q2 2025

Schedule



Cables, wingboards, motherboard production

Summary

Component	Prototyopes made/ tested	Ready for production?	Next steps
Twinax cable assemblies	A/D type: few dozen w/ good results B type: preparing pre-series	Yes*	Test in V3 cassette
Power cable assemblies	Pre-series produced; ready to test in cassette	Yes*	Test in V3 cassette
Flex assemblies	Handful of prototypes	Not yet	Produce pre-series
Wingboard	BH: pre-series made and under test FH: mechanical design	Not yet	BH mounting scheme FH electrical design
Motherboard	First V3 prototypes, initial tests	Not yet	Continue V3 tests incl. cassette Incorporate ECON-D

Tileboard status: next talk

Backup

Backup: documentation

Connector specification: https://edms.cern.ch/file/2311520/1/Tileboard_Proto1_Connector_11.pdf

Twinax adapter PCB designs: https://edms.cern.ch/file/2311520/1/Tileboard_Proto1_Connector_11.pdf

Scintillator cassette interface: https://edms.cern.ch/ui/file/2769568/1/CI_CE-H_scint_LVBV_RA_RH_v0.pdf

Pre-series wingboard: https://edms.cern.ch/document/2392324

V3 motherboard architecture: https://edms.cern.ch/document/2756943

V3 motherboard design: https://edms.cern.ch/ui/#!master/navigator/document?P:101053777:101212404:subDocs

Physics requirements

The SiPM-on-tile part should enable CMS to fully exploit physics channels with high-rapidity jets on the full HL-LHC dataset. To **maintain the energy resolution under irradiation**, the individual channels need to be calibrated accurately until the end of HL-LHC.

The large number of channels render **in-situ calibration with MIPs** as the most feasible strategy. This requires that all detector channels remain MIP-sensitive until end-of-life. NB that the calorimetric performance (JER) **does not depend critically on the exact MIP S/N** in the range we are discussing.

Studies on MIP calibration [DN-2022/010] indicate that this can be achieved with a **MIP S/N $\gtrsim$ 3**. There is no hard cutoff below which calibration becomes impossible, but it becomes **increasingly difficult** and requires a longer integration time as the S/N drops. At this level, the calibration can be repeated ~daily as conditions change.

The goal of S/N $\gtrsim$ 3 represents a **compromise** between the desire for **safety margin** in case of unexpected effects or longer running (4500/fb?) on one hand, and considerations of **cost and technical feasibility** on the other.