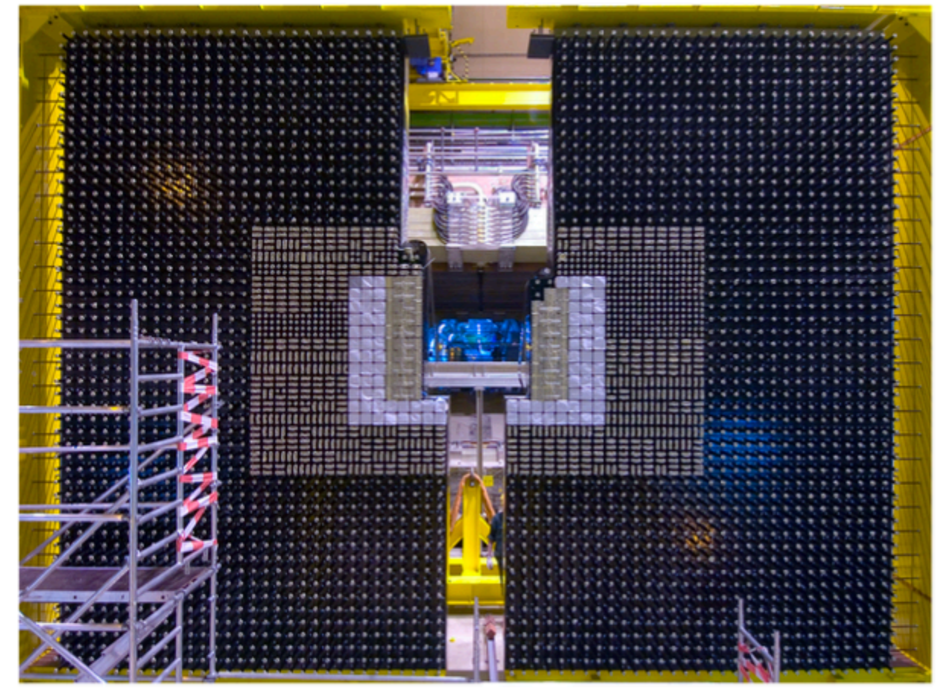
LHCb Upgrade II: PicoCal

Christina Agapopoulou - IJCLab

Conseil Scientifique in2p3

Paris, 13 / 02 / 2025

The LHCb ECAL today

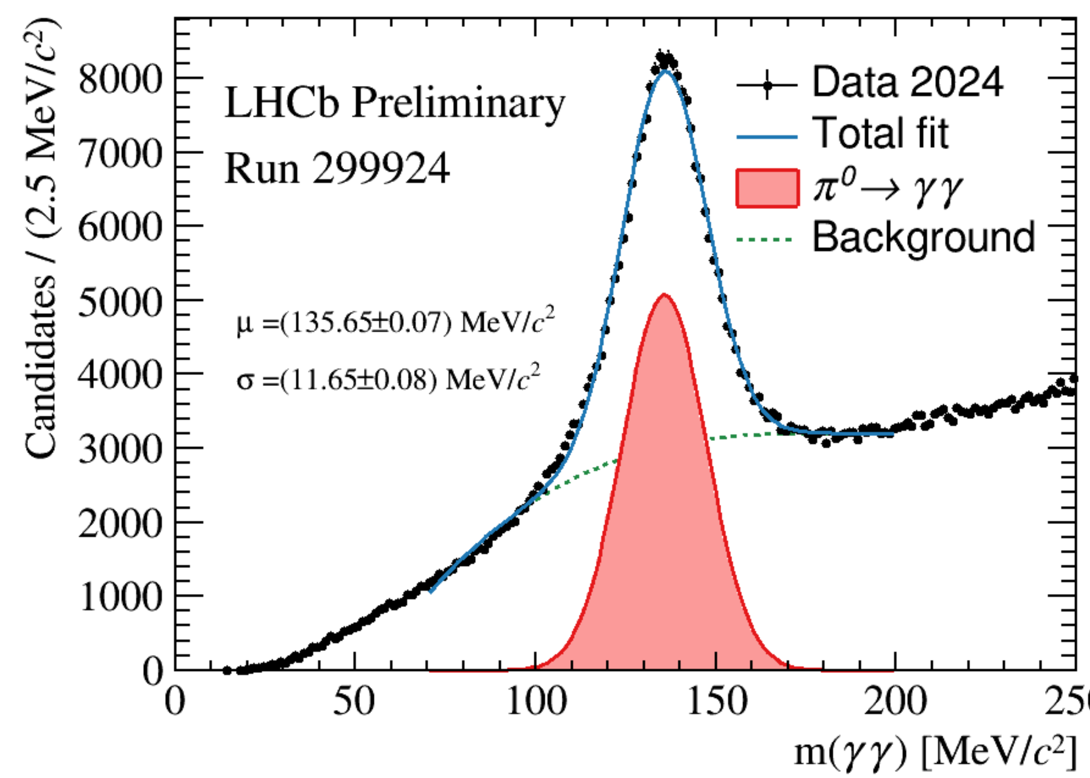


Detector design

- Shashlik technology coupled with PMTs
- 4x4, 6x6 and 12x12 cm² cell size - occupancy <10%
- ~6k channels
- Energy resolution: $\sigma(E)/E \sim 10\,\%/\sqrt{E} \oplus 1\,\%$
- Radiation hard up to 40 kGy
- Energy range: few GeV to 100 GeV

Status today

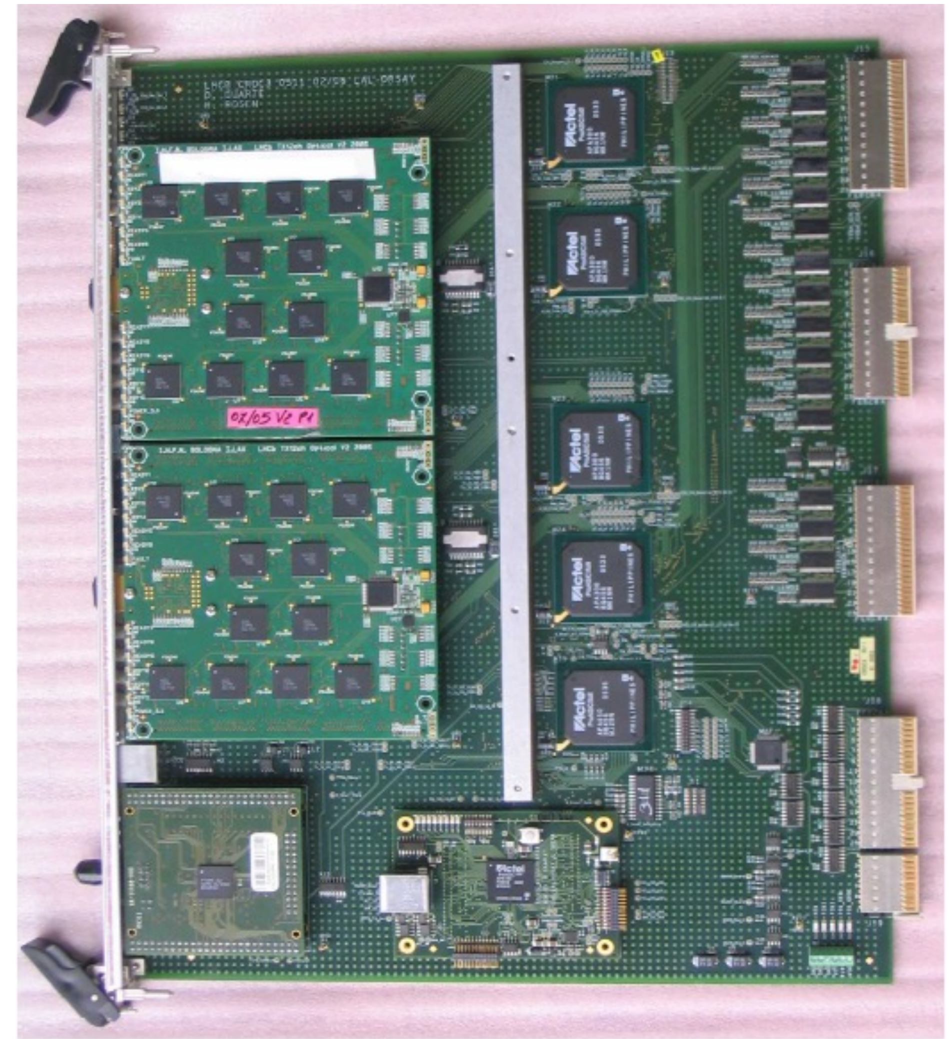
- Operating smoothly since Run 1
- Electronics upgraded in Run 3 to adapt to new DAQ scheme - readout at 40 MHz without hardware trigger
- Continuous calibration to account for aging - good resolution of photons and π^0 at 2x10^{32} cm^{-2} s^{-1}
- **Expected accumulated dose at end of Run 3: 40 kGy for innermost modules**



A detector with a large historical contribution from the French community

French contributions to today's ECAL

French institutes with historical contributions to LHCb's CALO: **IJCLab, LPCA, LAPP**



- Design, testing, production, installation and maintenance of **front-end electronics** (front-end boards, controller and ECS boards) starting from Run 1 to Run 3
- Design & operation of **L0 ECAL hardware trigger**
- Qualification & tests of **PMTs**
- Participation in **infrastructure** mechanics and **installation** campaigns
- Development & maintenance of **calorimeter simulation & reconstruction algorithms**

LHCb 2001-123
CAL
26 September 2001

A clustering algorithm for the LHCb electromagnetic calorimeter using a cellular automaton

V. Breton, N. Brun, P. Perret

Clermont-Ferrand LHCb group

A significant and diverse contribution to major aspects of the LHCb calorimeter for 20+ years!

Physics with the LHCb ECAL

Electrons, photons and π^0 crucial for key LHCb analyses, both today and in the future

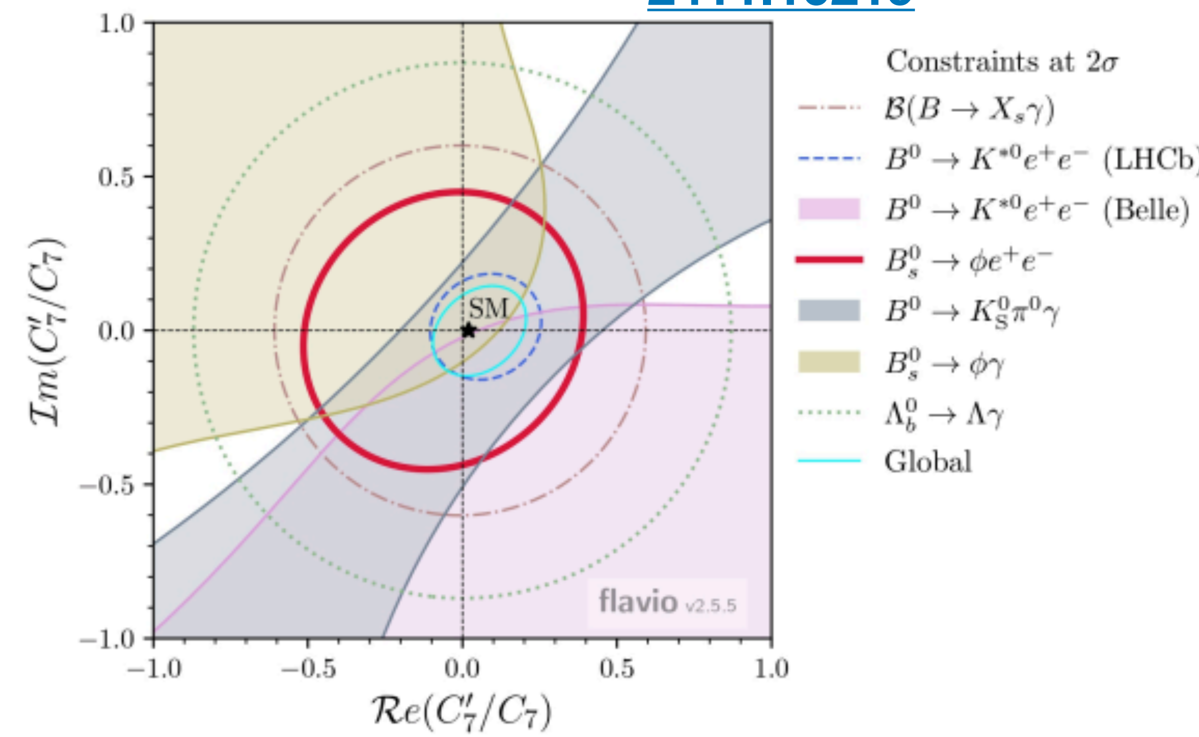
Long-standing history of IN2P3 LHCb institutes' involvement in analyses using calorimeter objects

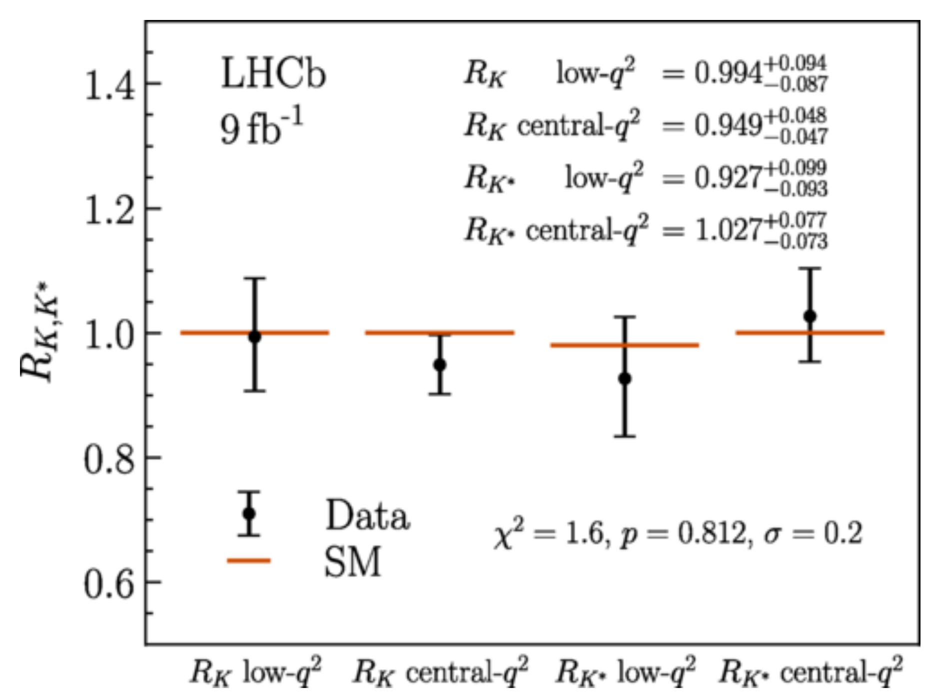
A few highlights from the recent years:

- Angular analysis of the $B_s^0 \to \phi e^+ e^-$ decay at low e+e- mass (virtual photon) constraining the photon polarisation - complementary to previous measurement of $B^0 \to K^* e^+ e^-$ that provided world's most precise measurement
- Combined lepton Flavour Universality measurement of $B^+ \to K^+ \ell^+ \ell^-$ and $B^0 \to K^{*0} \ell^+ \ell^-$ modes

Well recognised expertise of IN2P3 LHCb groups in analyses with electrons and photons

2411.10219





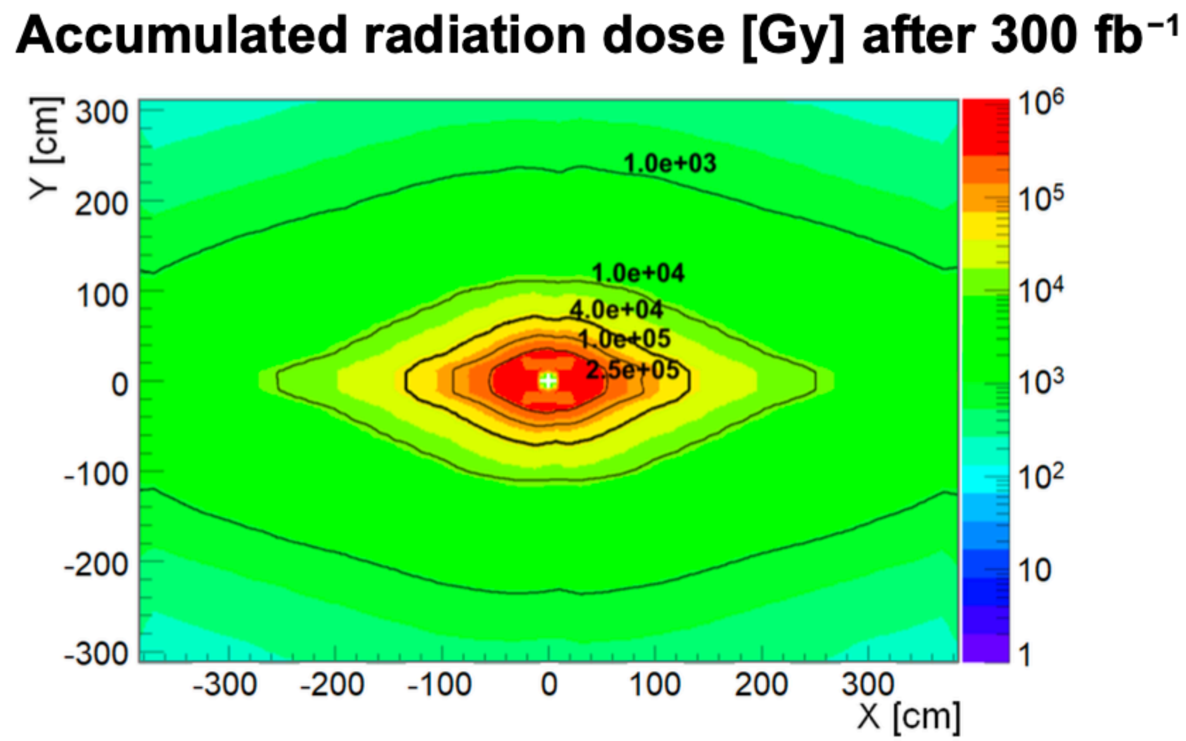
PhysRevD.108.032002

Motivation for PicoCal

Targets for U2

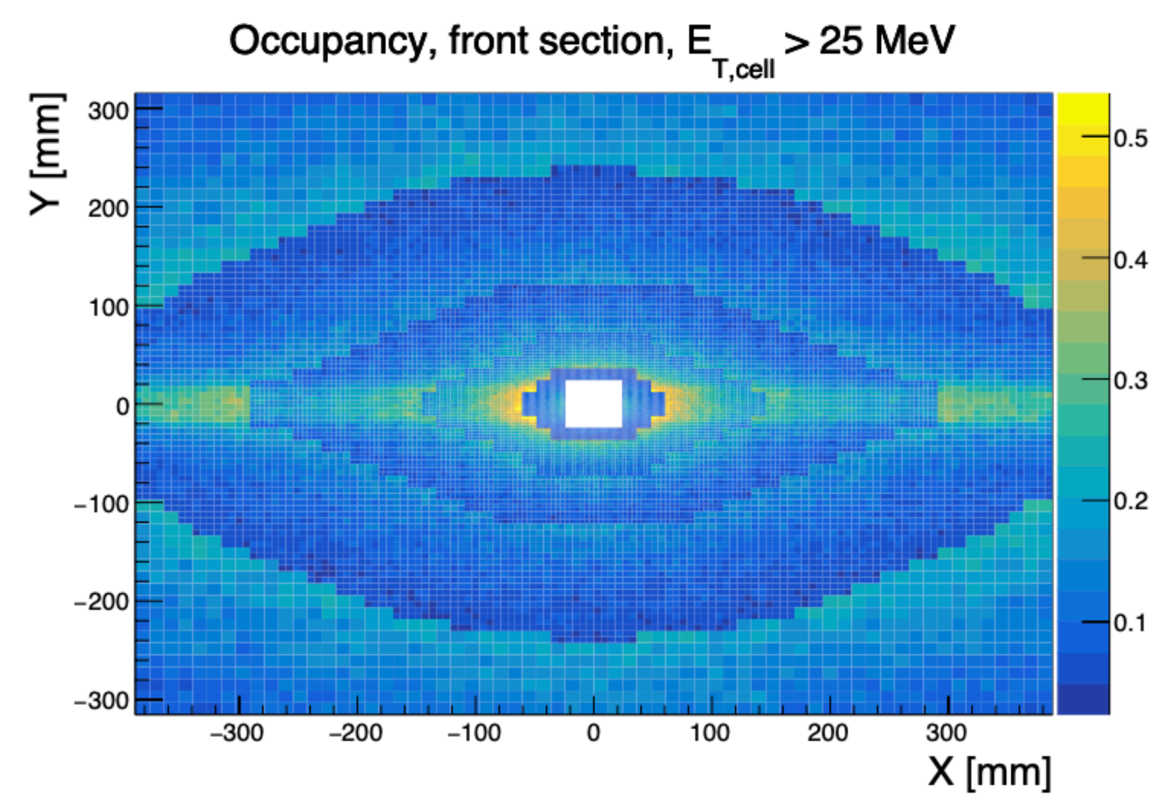
- Instantaneous luminosity increased by x5-7 - operate at 1.5 x 10^{34} $cm^{-2}s^{-1}$ to collect ~300 fb^{-1}
- Sustain radiation doses up to 1 MGy and ~6x10^{15} MeV n_{eq}/cm^2
- Maintain current energy resolution
- Keep low occupancy for performant particle separation

The current ECAL will require a major upgrade to sustain higher pile-up, occupancy and radiation doses of U2



Main design features of the upgrade

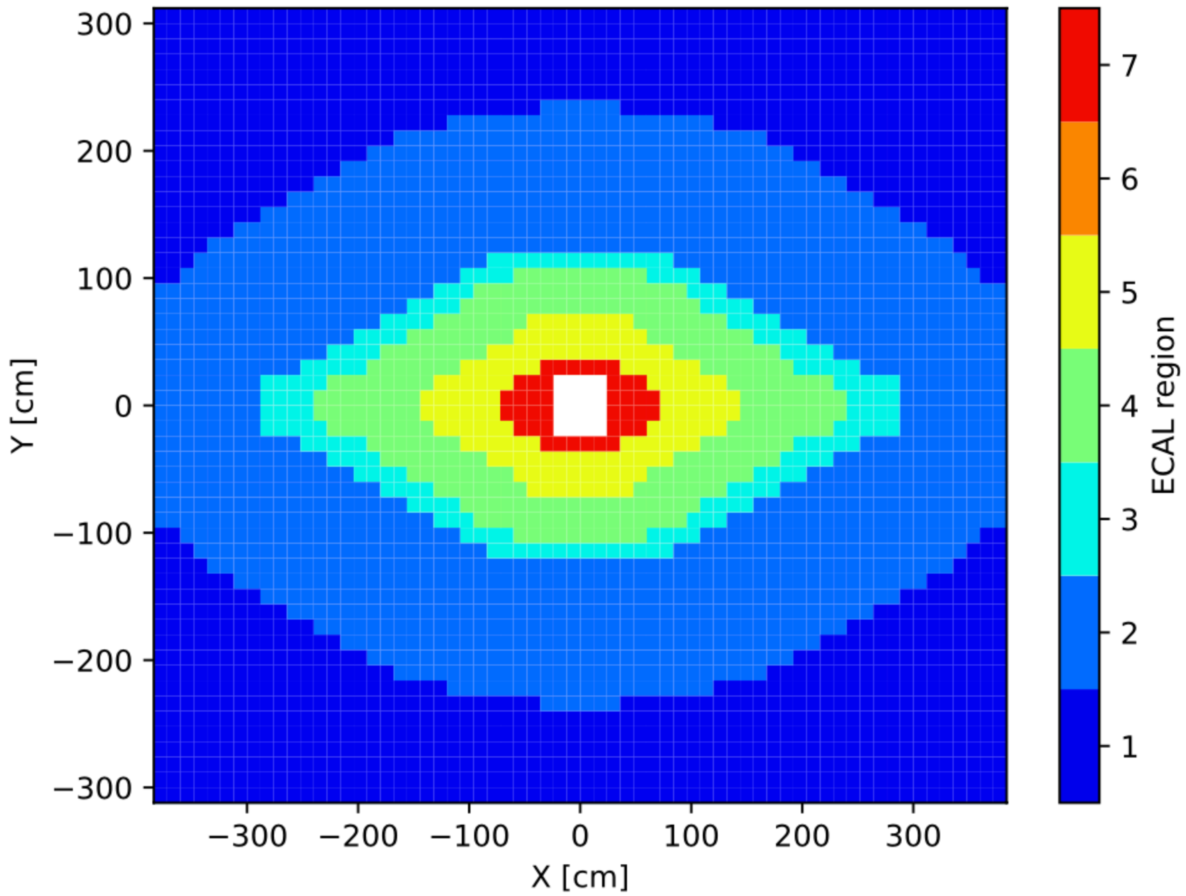
- Finer cell granularity to handle higher occupancy - SpaCal technology
- Complemented by precise (O(ps)) timing information
- More radiation-hard technologies for the innermost regions
- Longitudinal segmentation to improve clustering, reconstruction and PID



PicoCal overview

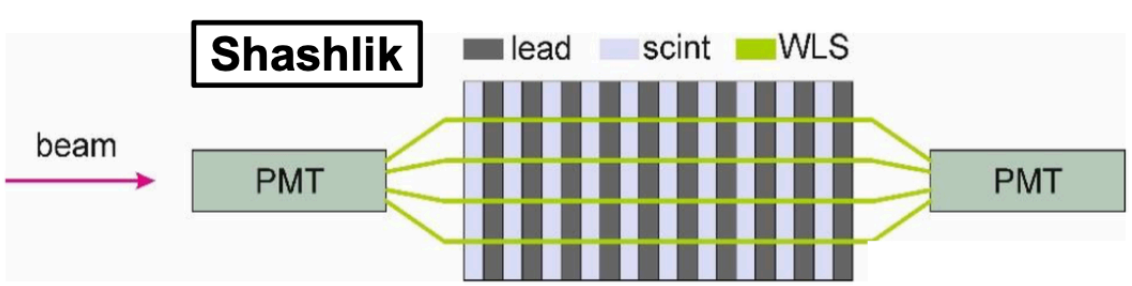
Geometry:

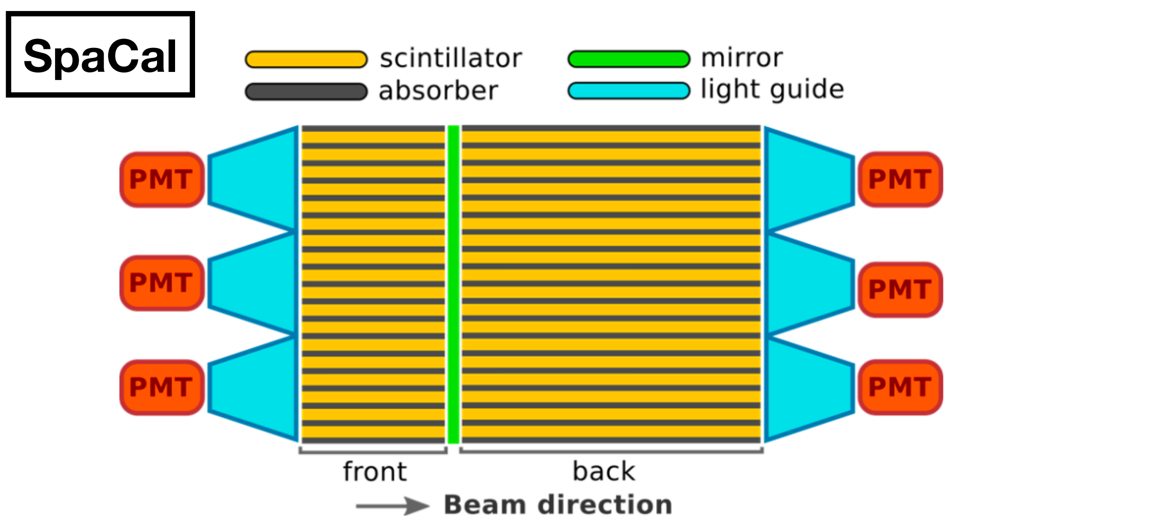
- 5 regions, arranged in rhombic shape to better follow the radiation profile
- First 3 innermost regions equipped with **SpaCal cells**
  - Crystal fibers / W absorbers for innermost region
  - Intermediate regions with plastic fibres and Pb absorber
  - Cells tilted by 3° + 3° wrt beam direction for enhanced energy resolution
- Last 3 innermost regions equipped with modified **Shashlik cells** with improved timing resolution



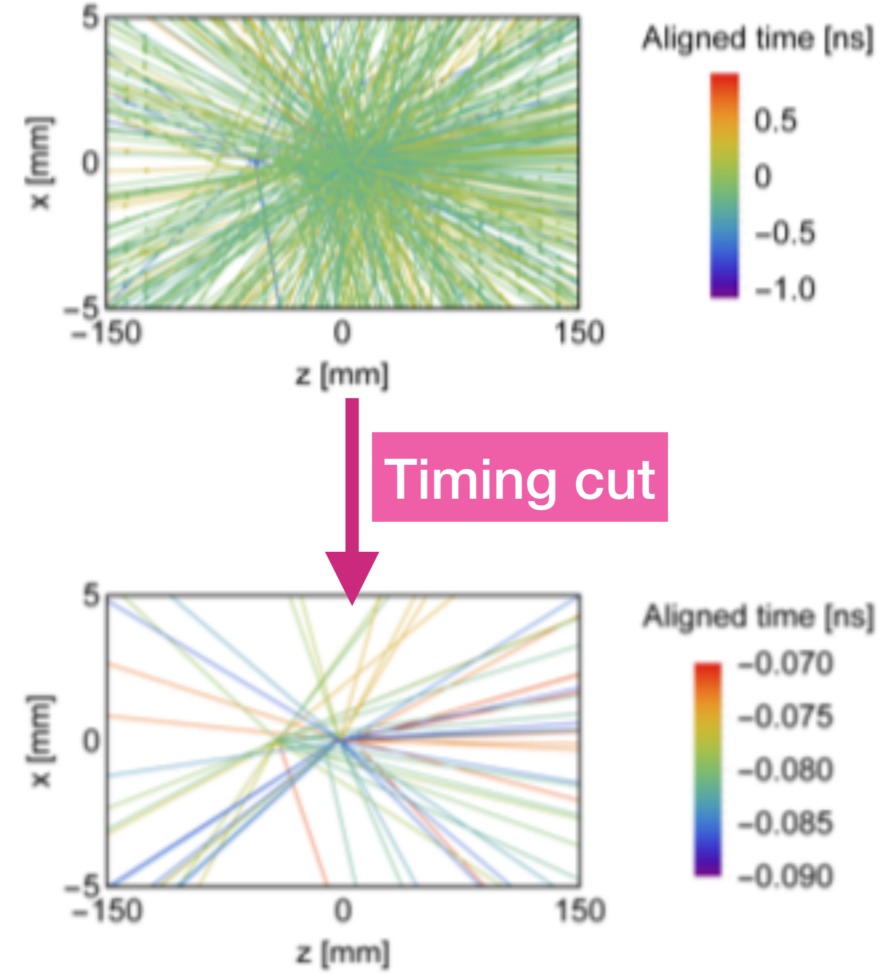
****LS3 enhancement**: innermost region equipped with intermediate sized cells made of plastic scintillating fibres + W absorber*

From Run 3 total of 6016 → 30976 cells in U2



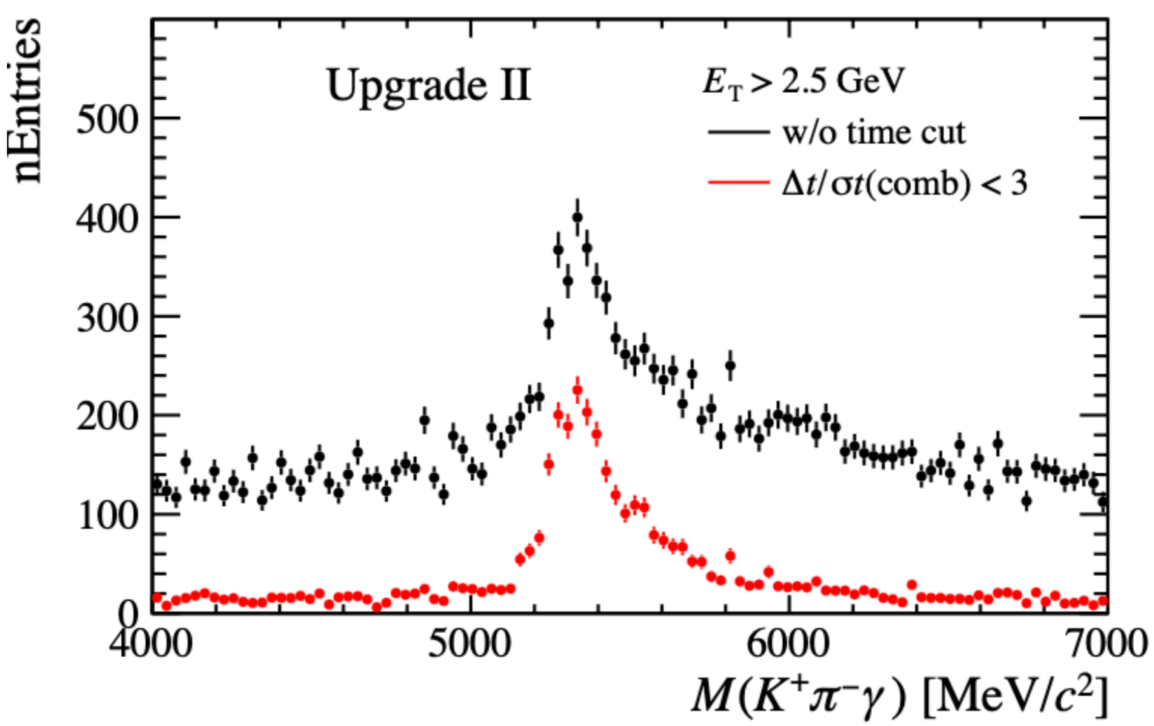


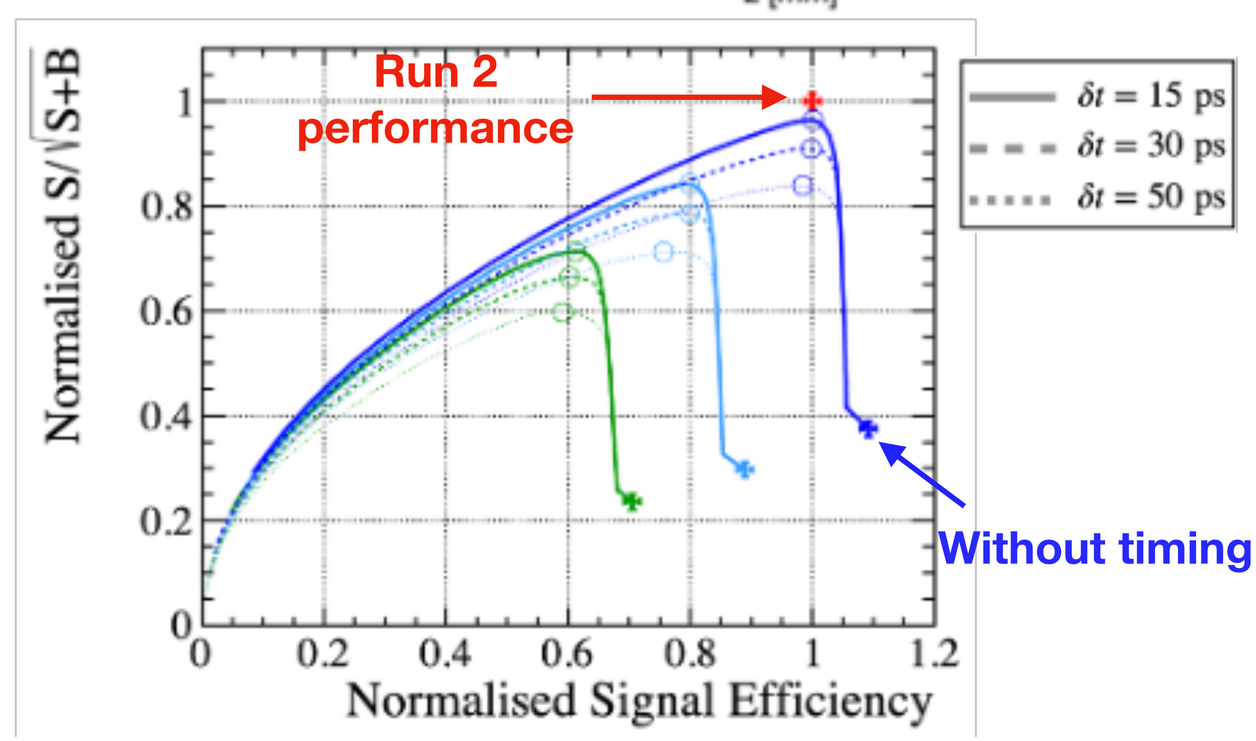
The need for timing



In U2 we will go from ~ 5 to 40 simultaneous pp interactions - **pile-up mitigation and correct cluster-to-PV association is crucial**

- Finer cell granularity not enough in all ECAL regions
- Beamspot spread of O(200) ps → **targeting timing info of 15 ps**
- PV and track timing to be provided by VELO detector with same time resolution target
- **Requires excellent intrinsic resolution of SpaCal and Shashlik technologies & specialised front-end for time measurement extraction**



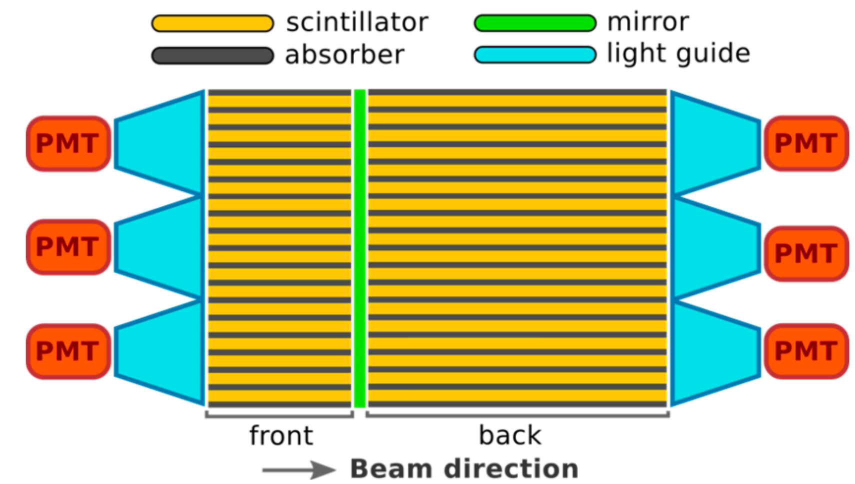


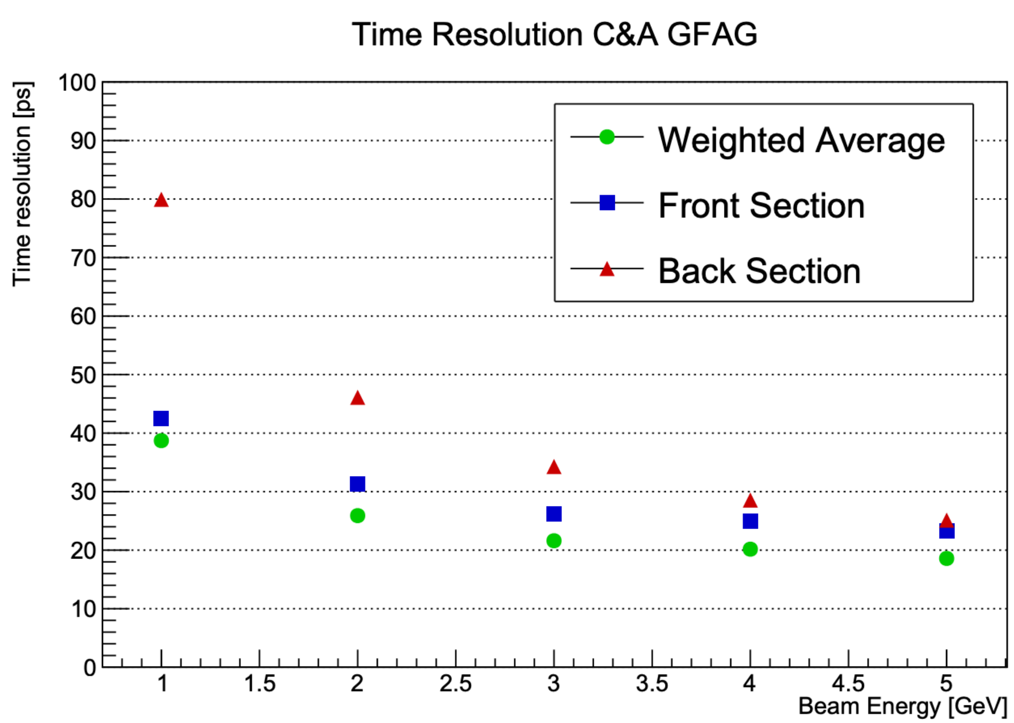
Precise timing information of the order of O(15ps) is a crucial component for the ECAL upgrade

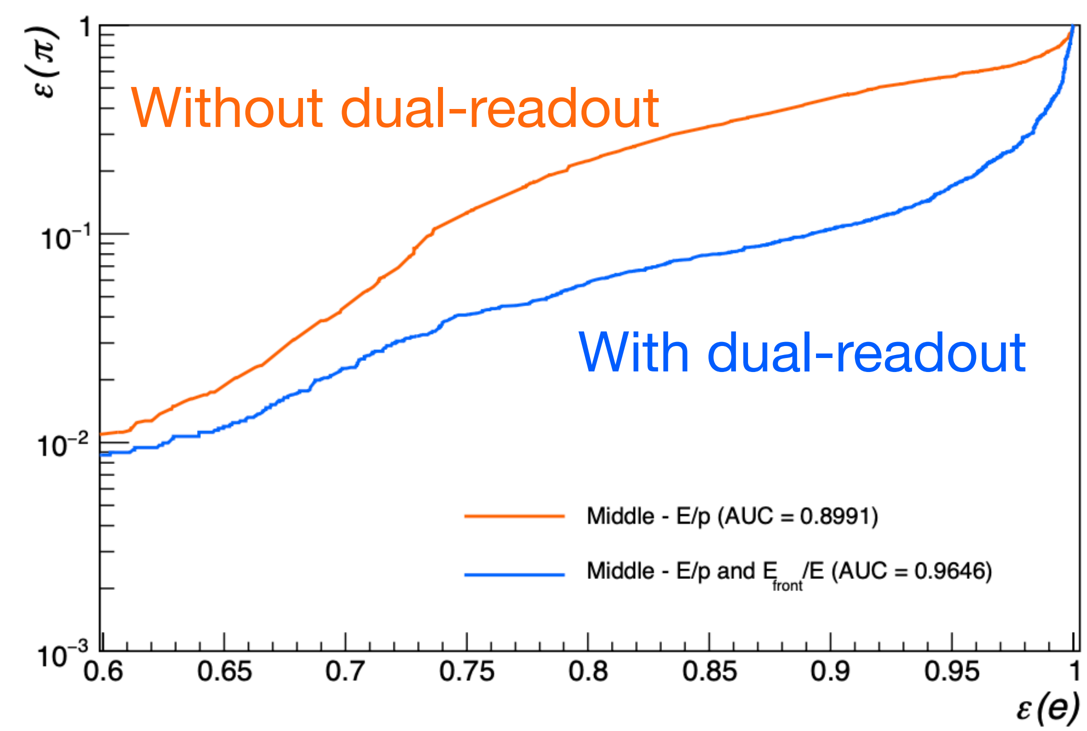
Longitudinal segmentation

PicoCal modules will be read-out from both front- and back-side (dual readout)

- Both energy & time measurements → double the amount of channels
- Effectively two measurements / particle → improved time & energy resolution
- Longitudinal shower information significantly improves PID performance





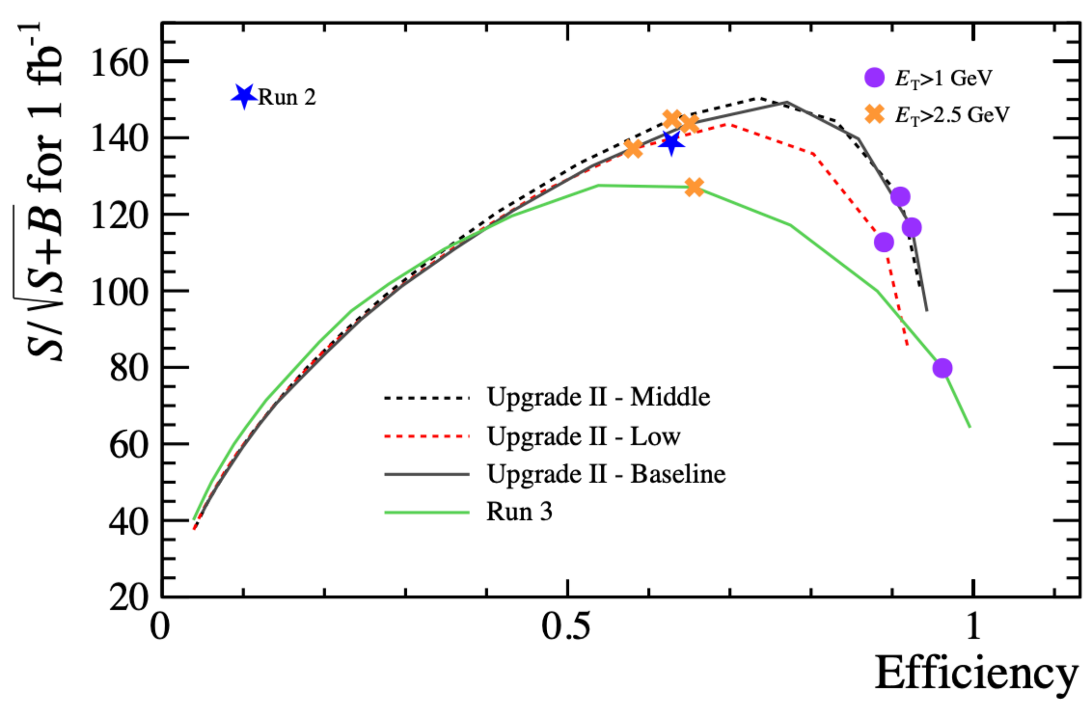


Dual readout expected to significantly improve PicoCal performance, especially PID

Descoping scenarios for PicoCal

PicoCal in the two proposed LHCb U2 descoping scenarios:

- **Middle:**
  - decrease inst. luminosity from 1.5 → 1 x 10^{34} $cm^{-2}s^{-1}$
  - PicoCal design unchanged - thanks to an improvement of the Baseline scenario cost wrt FTDR
  - slightly enhanced detector performance wrt Baseline, thanks to lower pile-up
- **Low:**
  - decrease inst. luminosity from 1.5 → 1 x 10^{34} $cm^{-2}s^{-1}$
  - single read-out for all modules except 176 innermost ones
  - degradation of detector performance



Precise timing information is an integral part of PicoCal in every scoping scenario

An upgrade split in two

Run 3						Long Shutdown 3														Run 4																Long Shutdown 4							
2025				2026				2027				2028				2029				2030				2031				2032				2033				2034				2035			
Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4

- **LS3 enhancement**
  - LS between Q3/2026 - 2029 - detector to be operated for Run 4 (2030 - 2033)
  - Instantaneous luminosity ~2 x 10^{33} c $m^{-2}s^{-1}$ (similar to Run 3)
  - Profit from long shutdown for ATLAS/CMS upgrades to anticipate LS4 needs
  - Introduce single-readout radiation tolerant SpaCal (2x2 and 3x3 cm^2 cells) in inner regions
  - Restructure ECAL in rhombic shape to improve performance
  - SpaCal-W & SpaCal-Pb modules with plastic fibres

- **LS4 Upgrade - PicoCal**
  - LS between 2034 - 2035 - detector to be operated up to end of HL-LHC (Run 5 + 6)
  - Instantaneous luminosity 1.0/1.5 x 10^{34} c $m^{-2}s^{-1}$ (factor 5 w.r.t Run 3)
  - **Dual readout and timing information**
  - Radiation hard SpaCal (1.5x1.5, 3x3 and 4.4 cm^2 cells) - innermost cells equipped with crystal fibres
  - Shashlik modules with improved timing

LS3 enhancement

Module design

Radiation-tolerant scintillating fibers:

- Baseline: 3HF - already used in various test-beams, available from several producers

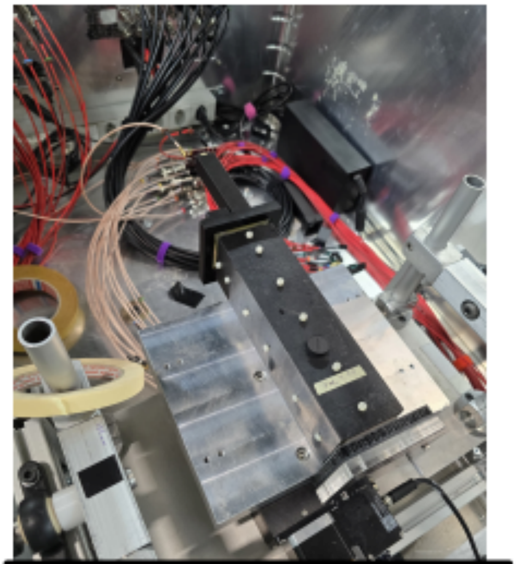
PMTs:

- Baseline: two different single-channel PMT models for the two SpaCal LS3 regions (2x2 & 3x3) to achieve optimal light collection
- SpaCal-W model available, SpaCal-Pb model expected in ~5 months
- Irradiation&ageing tests ongoing and showing promising results

PMT-module optical coupling

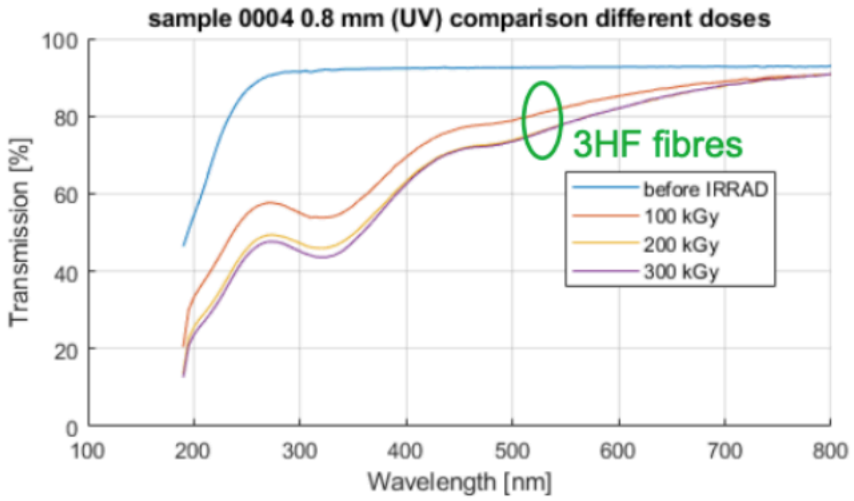
- Design in two stages (short bundler + long hollow light guide) for optimised light output and spacial homogeneity

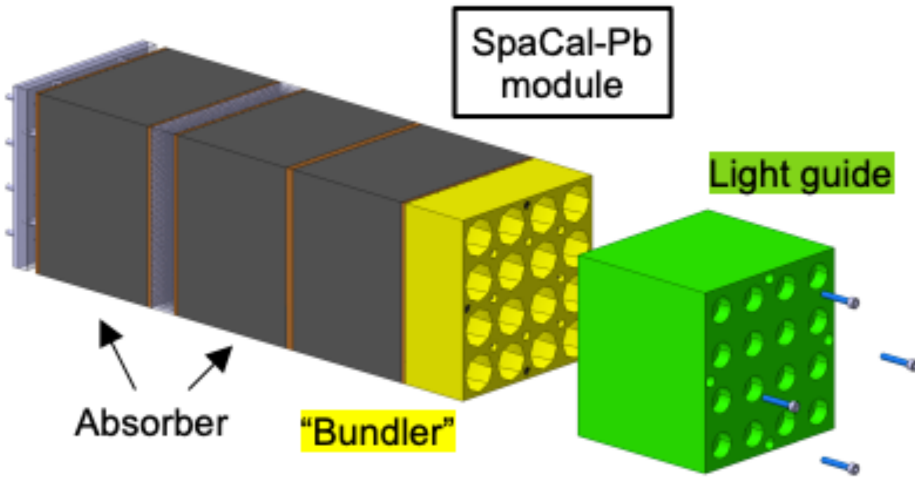
Approaching final LS3 SpaCal design



Test of different fibres in W absorber

Irradiation of PMT entrance window:



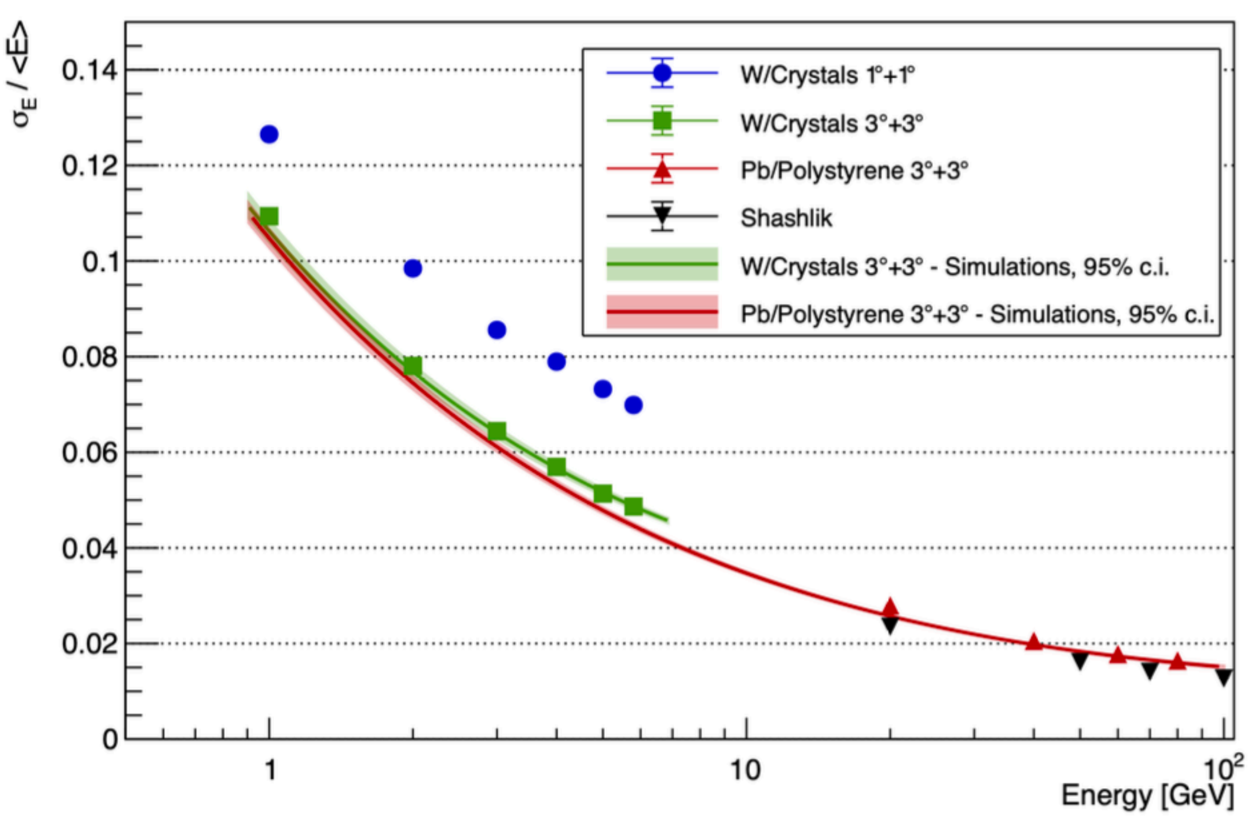


Module performance

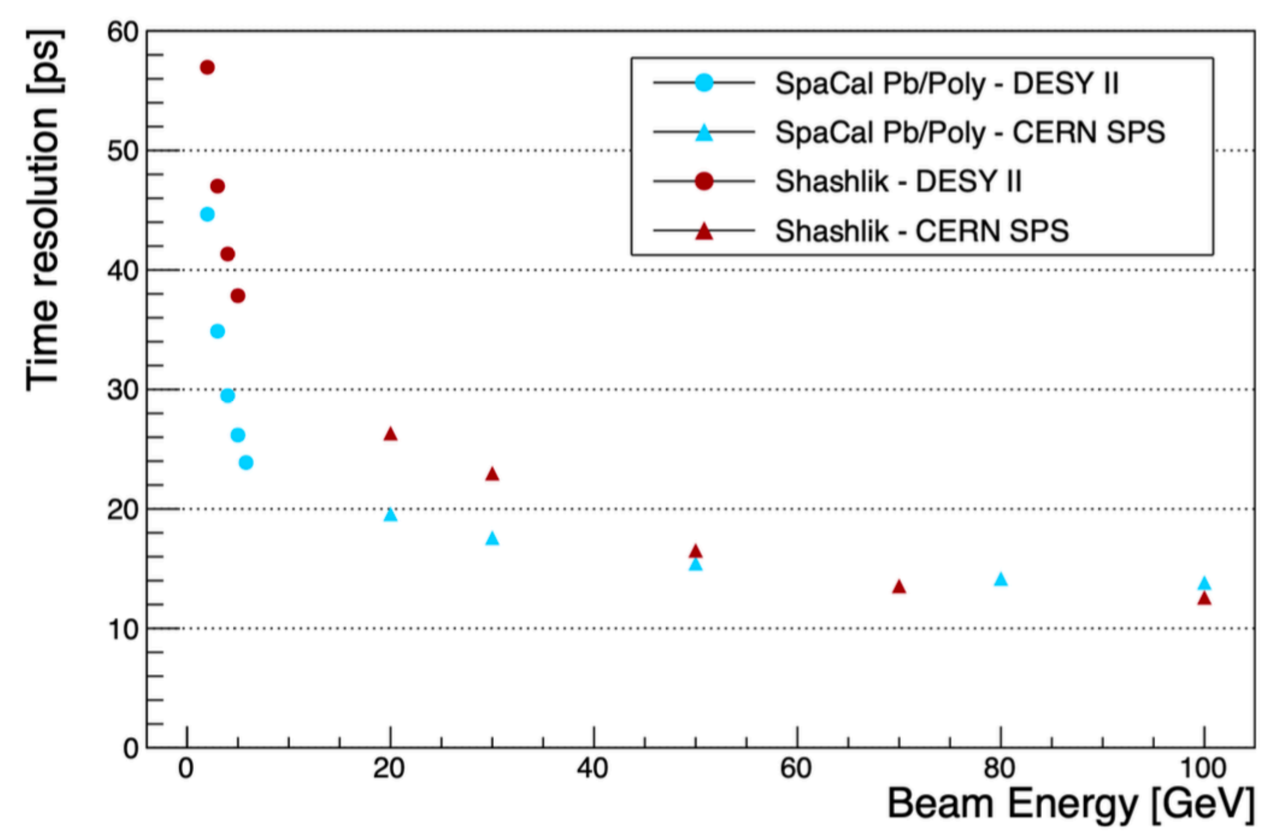
Several test-beams, both at DESY ($e^{\pm}$ 1 – 6 GeV) and at CERN SPS (e^{-} 20 – 300 GeV)

- SpaCal and Shashlik prototypes with main material candidates
- $3^{o} + 3^{o}$ orientation wrt to beam enhances energy resolution → $10\%/\sqrt{E}$ target achieved
- DAQ system based on waveform sampling in analog memories: DRS4 + WaveCatcher → time resolution below 20 ps at high energy

Energy resolution of SpaCal & Shashlik modules



Time resolution of SpaCal & Shashlik modules



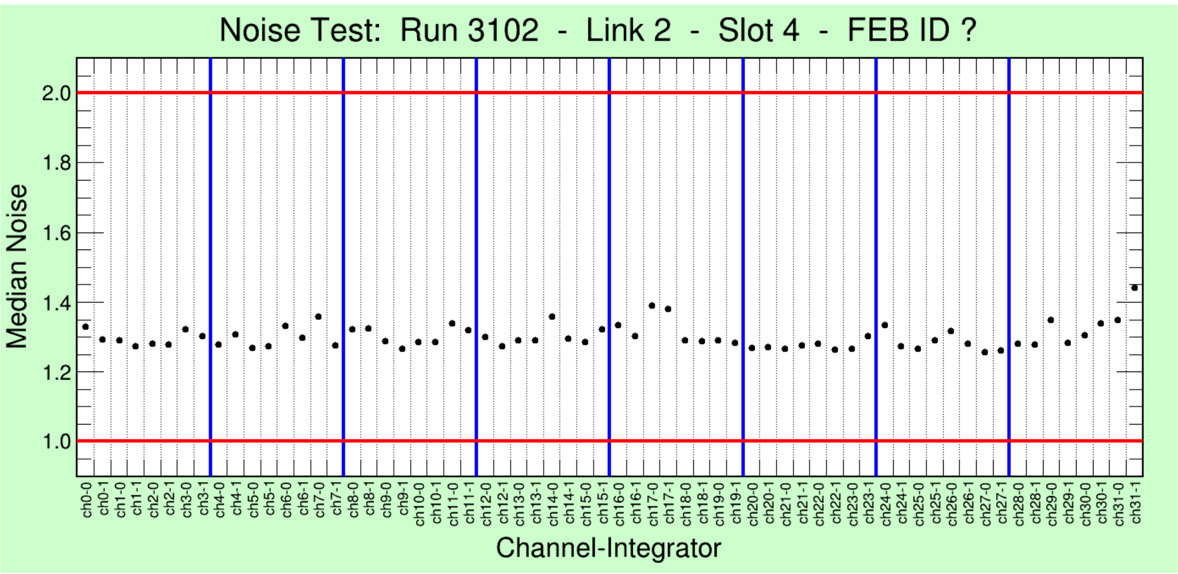
Time & energy resolution of Shashlik & SpaCal modules within requirements both for LS3 & LS4

LS3 Electronics

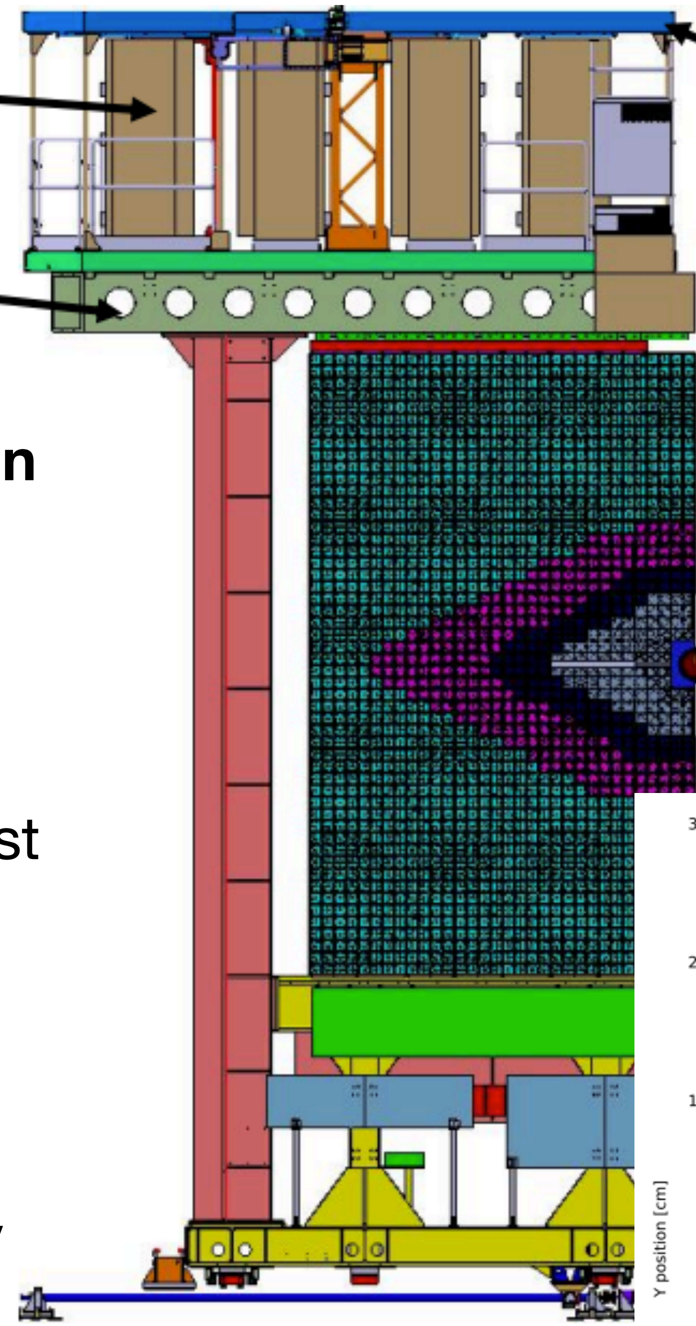
- With the LS3 enhancement we have 3072 additional read-out channels compared to today
- Each front-end board will **read-out 32 channels**
  - 120 new front-end boards (incl. spares) need to be produced
  - Similar design as the current boards but with new DC/DC component (FEAST -> bPOL12V) - **power part of the board redesigned by LPCA**
  - First prototype available - **tests started at IJCLab in Feb. 2025**
  - Market survey in 2026, production in 2027
- 8 Control Unit boards (3CU) already produced → **to be tested at IJCLab**

LS3 FE board design / testing / production fully under the responsibility of IJCLab + LPCA

First noise test of LS3 FEB prototype with modified mezzanine - 04/02/2025



Infrastructure & LS3 installation

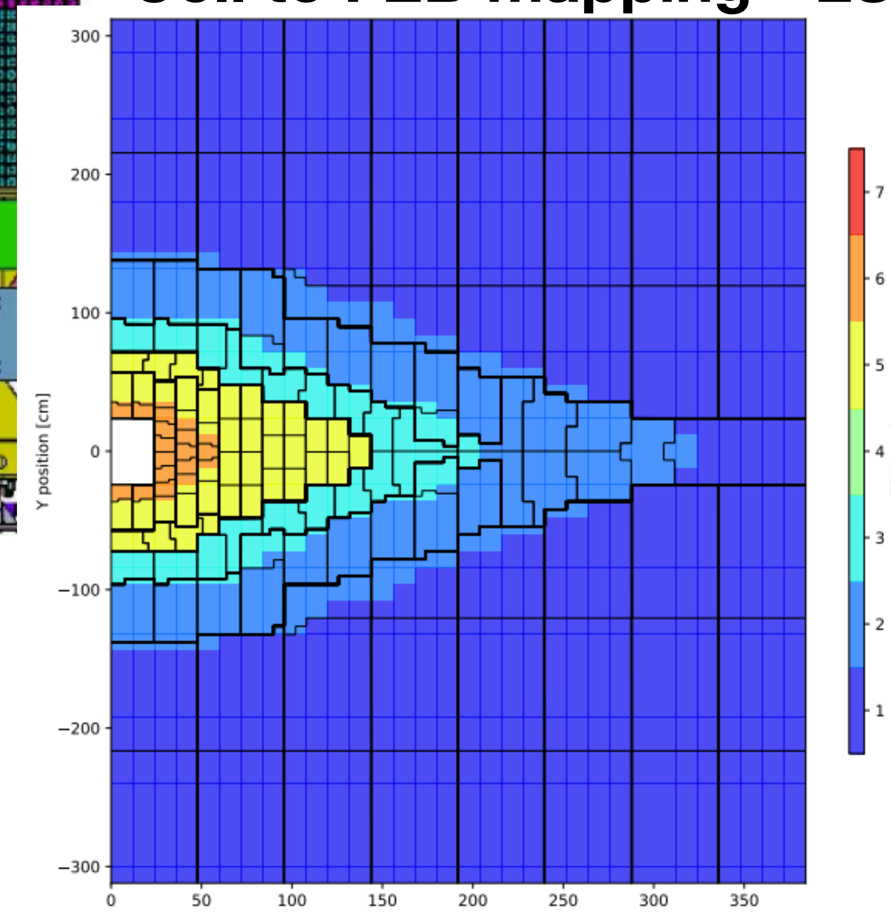


The majority of infrastructure/installation work for both LS3 enhancement and PicoCal will happen during LS3

- The ECAL will need to be disassembled and reassembled with new SpaCal modules + new rhombic geometry - most likely inside the cavern, best position under investigation
- **LAPP heavily involved in mechanics infrastructure for LS3**
- **Cable mapping for LS3 + LS4 is ready (IJCLab)**

Personpower from IN2P3 institutes will be needed at CERN for assembly & installation

Cell to FEB mapping - LS3



LS4 - PicoCal

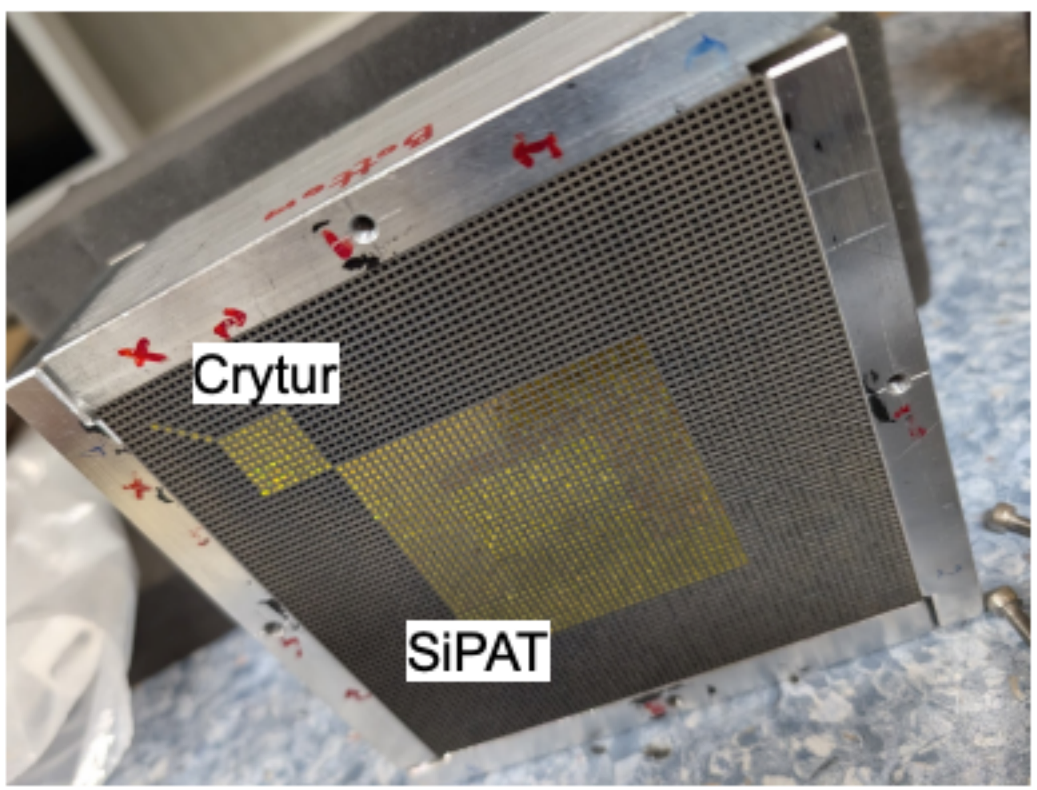
SpaCal and Shashlik R&D for U2

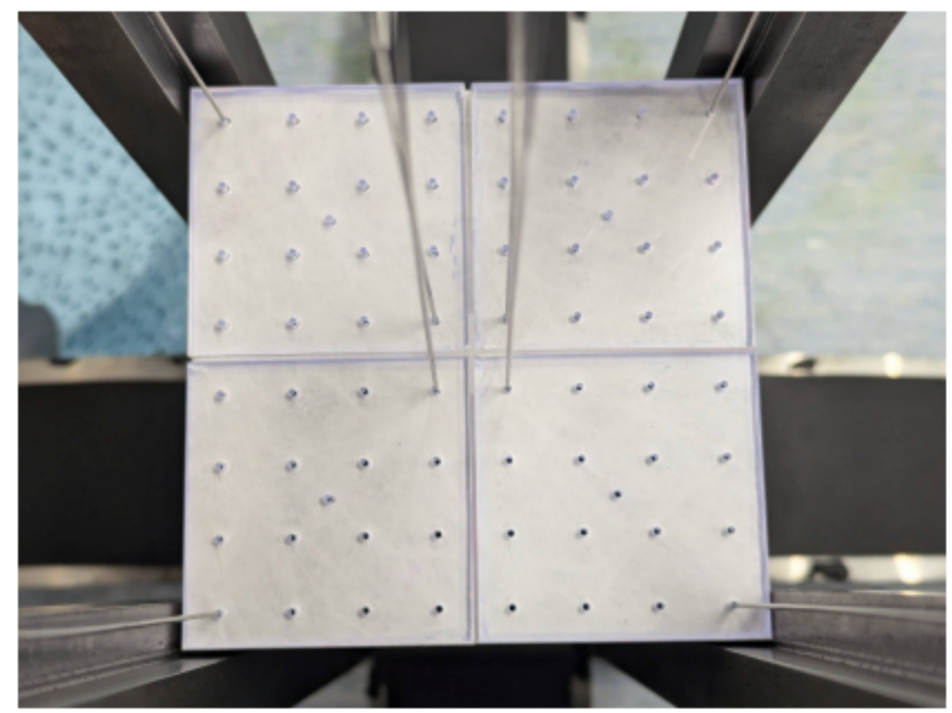
SpaCal for U2

- Crystal fibers with W absorber needed for the innermost region
- A GAGG-W prototype has been assembled in 2024 from SiPAT and Crytur
- Tested in DESY / SPS testbeams of 2024, analysis ongoing

Modification of Shashlik modules for U2

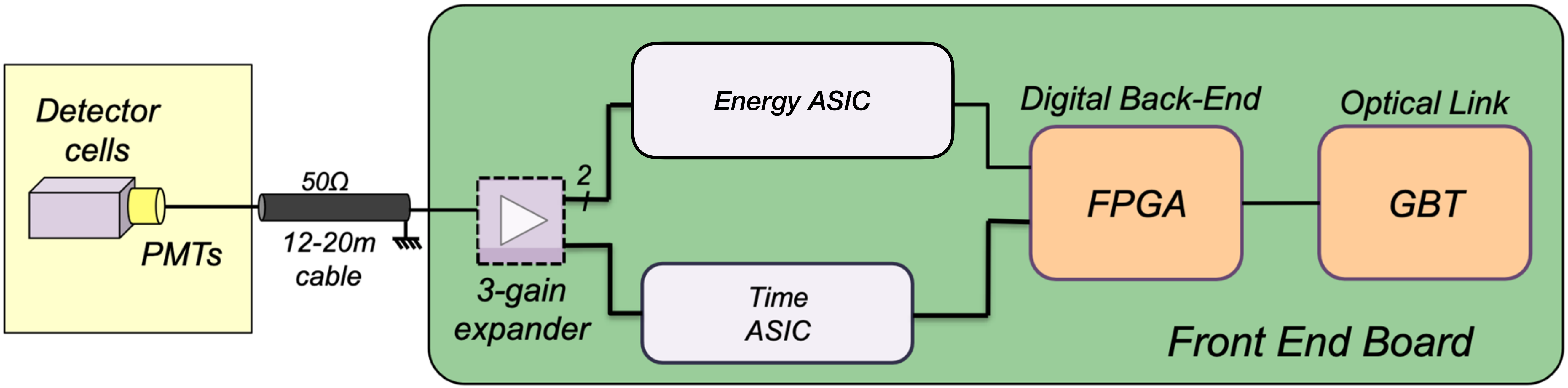
- Assembly tool for cutting tiles in Pt 8
- First tests successful , initial test-beam results of cut tiles as expected
- Current rate: 1 module / person day





Testing of modules with LS4 specifications ramping up

Front-end electronics in LS4



- Photodetectors readout solution follows the same scheme as in current ECAL - **Major modification is the addition of the timing measurement**

- ASIC/chipset in TSMC 65 nm with separate energy and timing paths
  - Energy ASIC: **ICECAL65** designed by Barcelona and Valencia LHCb institutes
  - Timing ASIC: **SPIDER** designed by **IJCLab, LPCA, LPC-Caen, IP2I and Subatech Nantes**

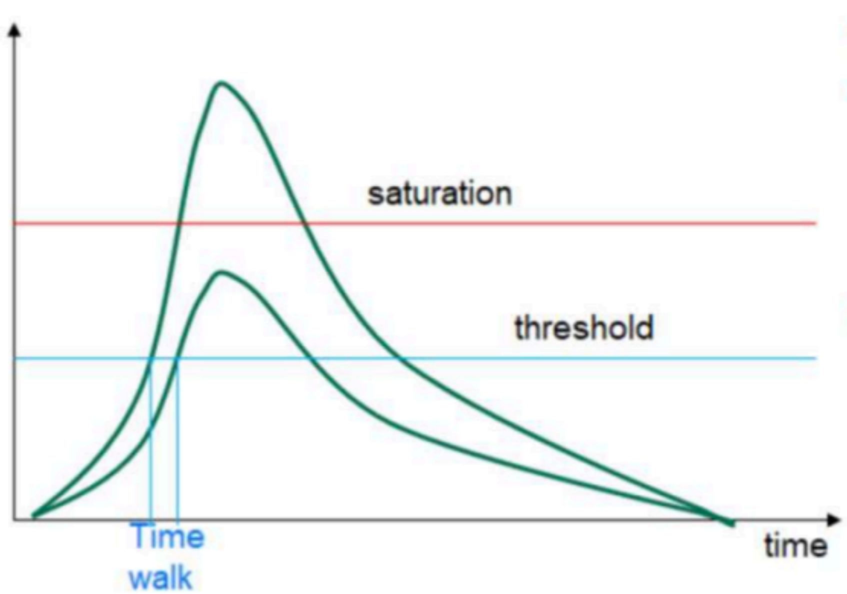
Timing measurement

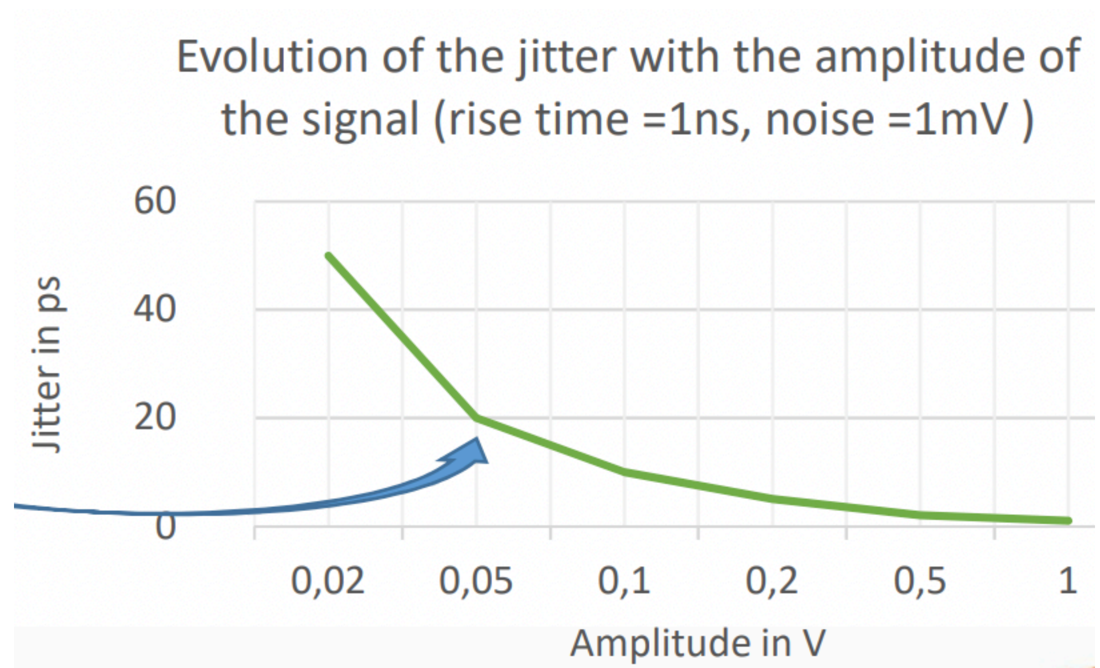
Requirements:

- Time resolution for entire chain: **15 ps** at high energy
- Dynamic range: **E_T = 50 MeV to 5 GeV**
- Up to an average cell occupancy of **50% (baseline 10%)**
- Possibility to process up to **8 consecutive events at 40 MHz**

- **Theoretical time resolution :** $\sigma_t = \frac{t_{rise}}{SNR}$
- Typical rise-times (as seen in test-beam): 1-5 ns, quite challenging to reach time resolution goal

Time measurement based on leading edge discriminator





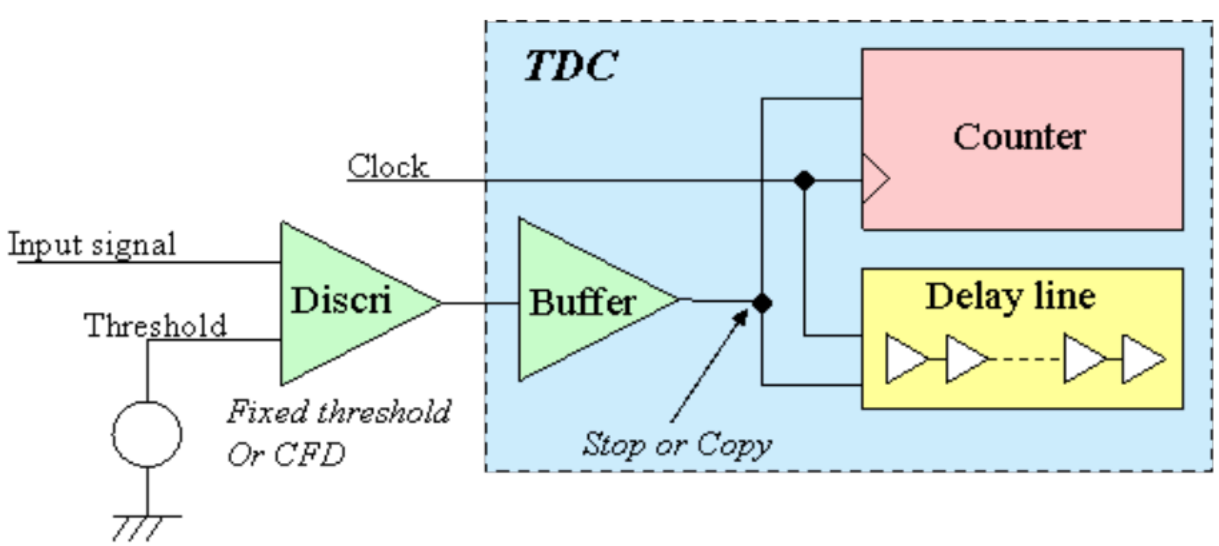
Timing extraction methods

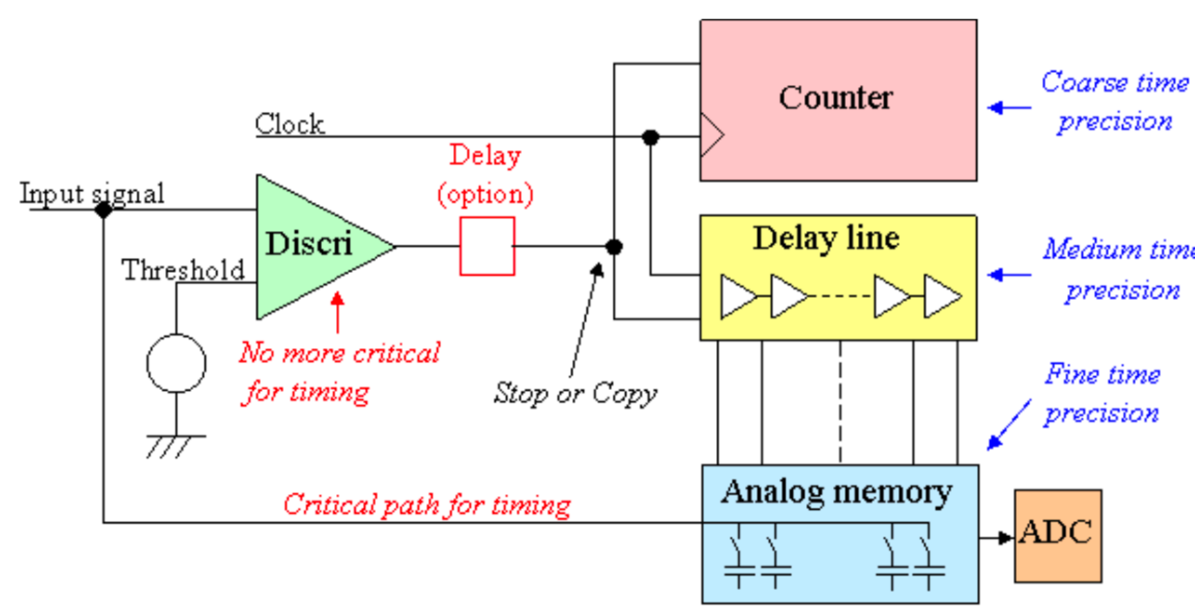
Leading-edge discriminator + Time-to-digital converter (TDC)

- High counting rate and low dead time
- Hard to achieve good resolution over large dynamic range because of the constant discriminator threshold
- Requires time walk compensation

Waveform TDC + digital Constant Fraction discriminator (CFD)

- Good resolution over large dynamic range thanks to waveform sampling (discriminator not on the critical path)
- Time walk strongly compensated by CFD
- Successful implementation in SAMPIC & WaveCatcher chips (CEA & LAL, D. Breton, E. Delagnes)
- Main limitation is rate and dead time

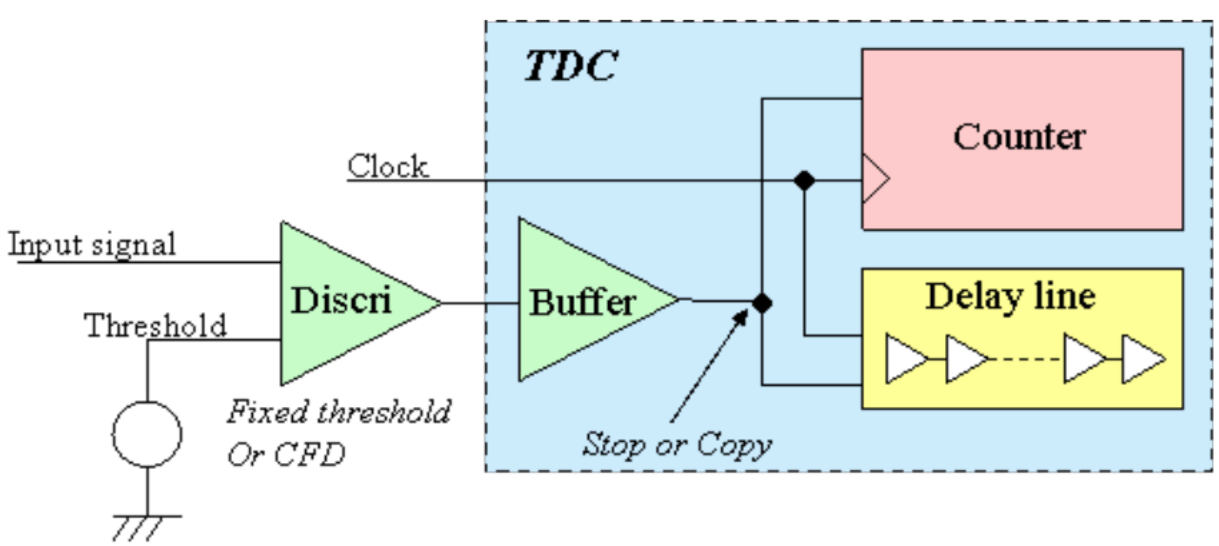




Timing extraction methods

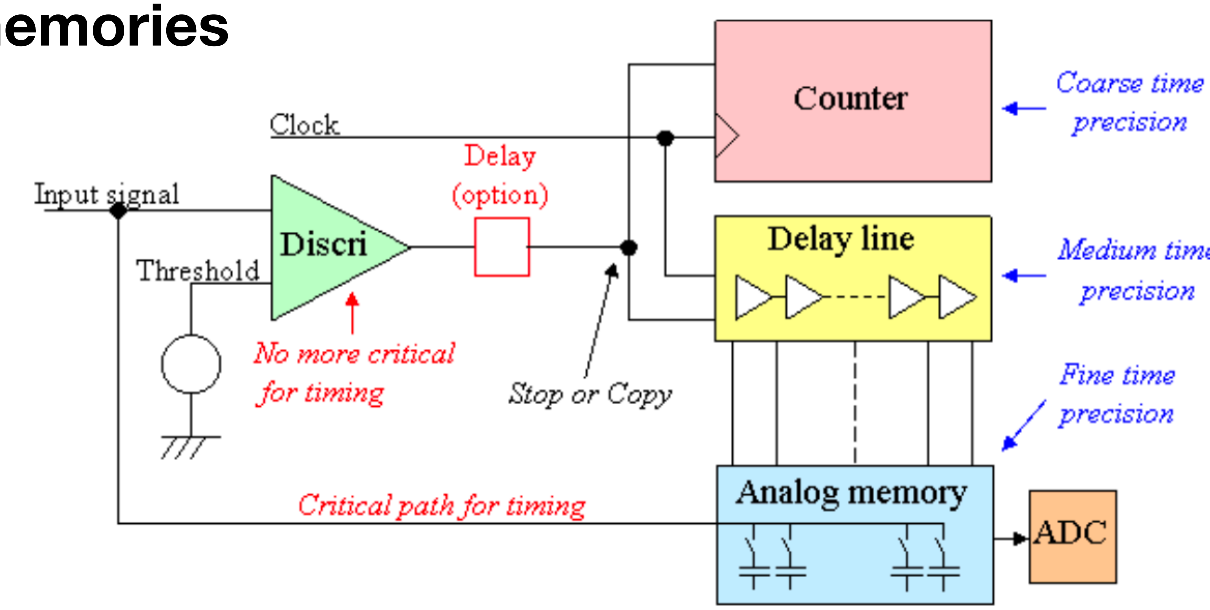
Leading-edge discriminator + Time-to-digital converter (TDC)

- High counting rate and low dead time
- Hard to achieve good resolution over large dynamic range because of the constant discriminator threshold
- Requires time walk compensation



Waveform TDC + digital Constant Fraction discriminator (CFD)

- Good resolution over large dynamic range thanks to waveform sampling (discriminator not on the critical path)
- Time walk strongly compensated by CFD
- Successful implementation in SAMPIC & WaveCatcher chips (CEA & LAL, D. Breton, E. Delagnes)
- Main limitation is rate and dead time - **can be mitigated with the use of pipelined analog memories**

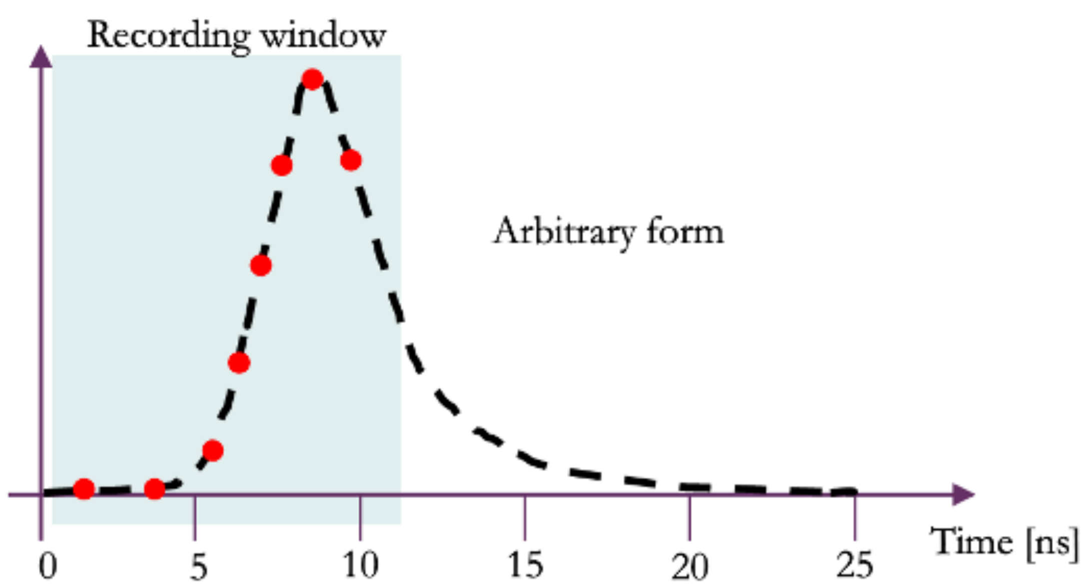


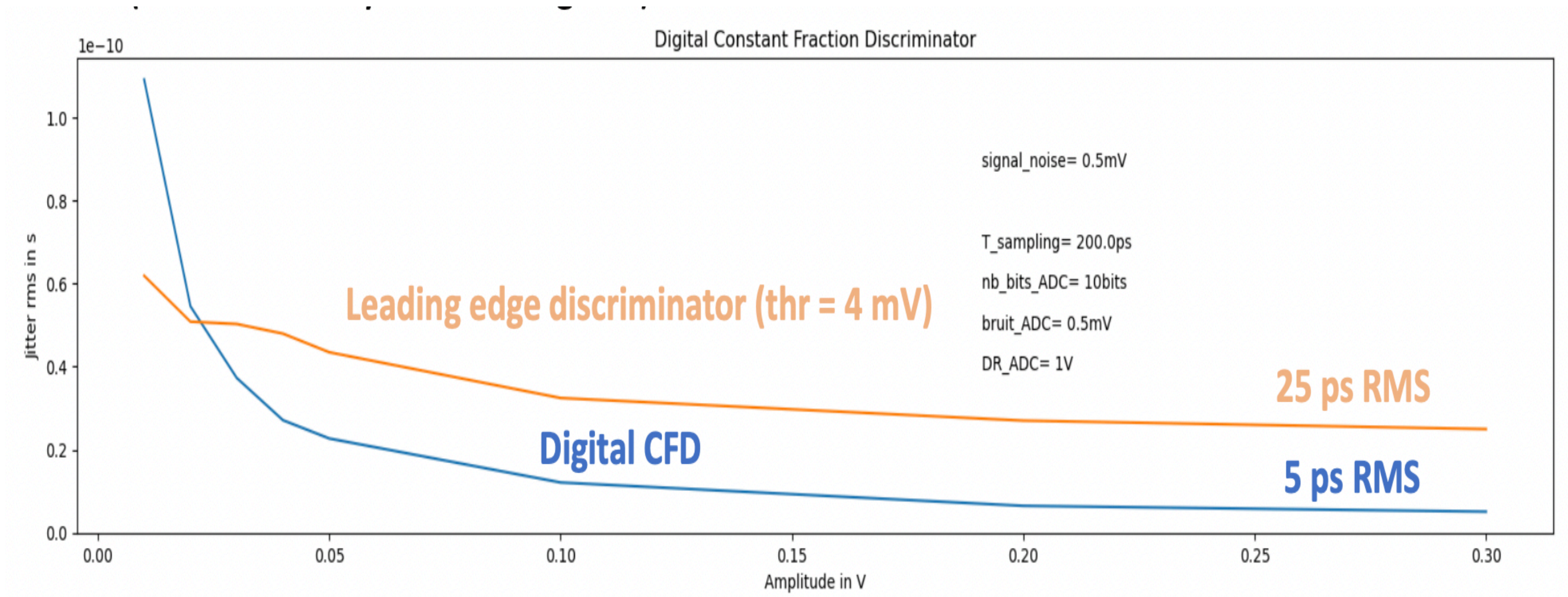
The SPIDER ASIC: a Swift Pipelined DigitizER

Waveform TDC + digital CFD

- Designed in 65nm TSMC - 8 channels / ASIC
- Counting rate limitation is mitigated by introducing a **pipeline of fast analog memories** recording discontinuous time segments linked to the LHC clock
- 8 32-cell banks per channel - adjustable sampling frequency : 2.5 to 20GS/s
- Adjustable sampling window around signal to reduce memory bank size - acquisition triggered by discriminator, so timing will only be available for particles with E_T>50 MeV
- Read-out rate minimised by sending only necessary samples - typically 8 samples
- CFD (or alternative time extraction / preprocessing methods) applied on FE FPGA

Based on years of experience with WaveCatcher and SAMPIC - IJCLab + LPCA among world leaders in this technology

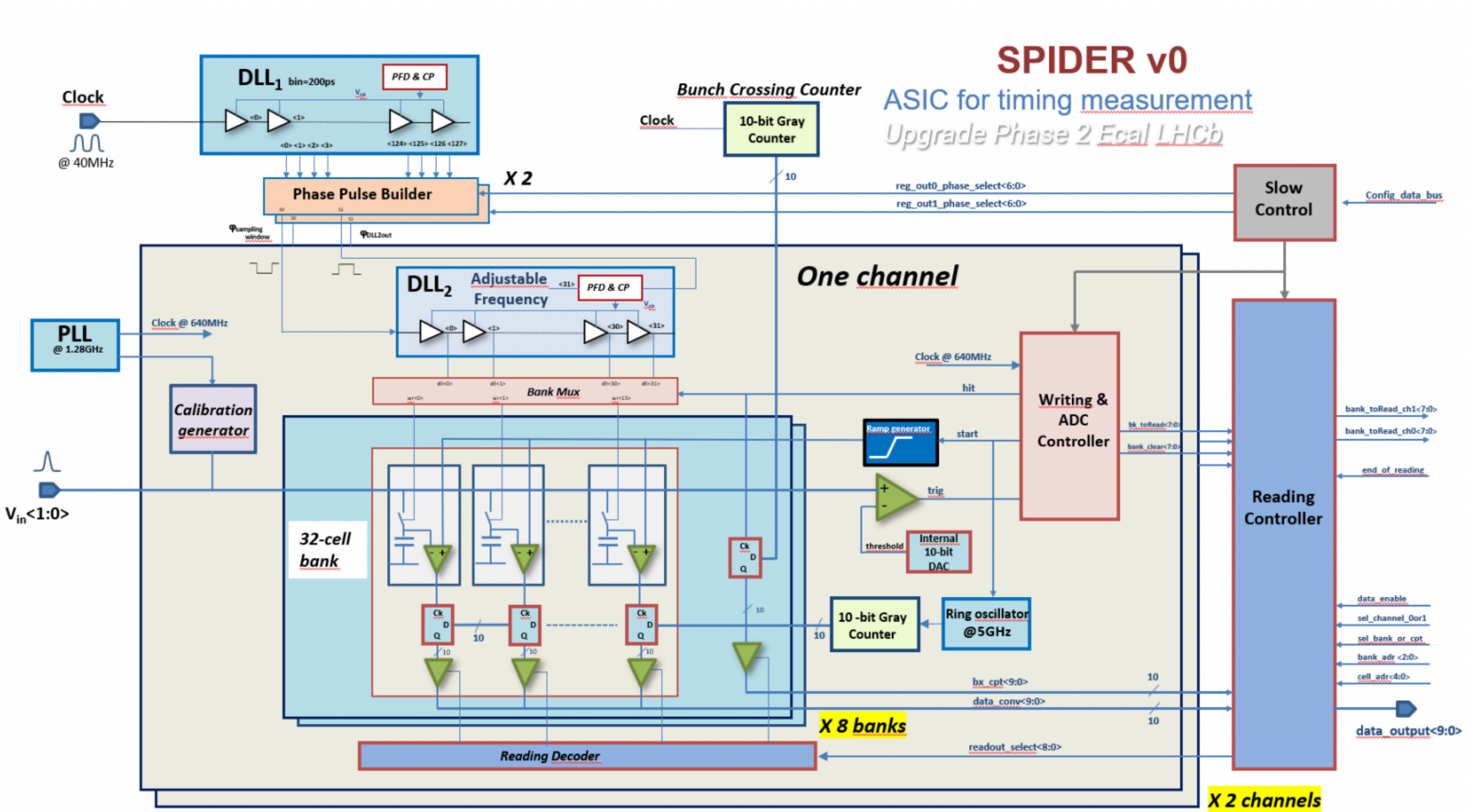




Towards SPIDER v0

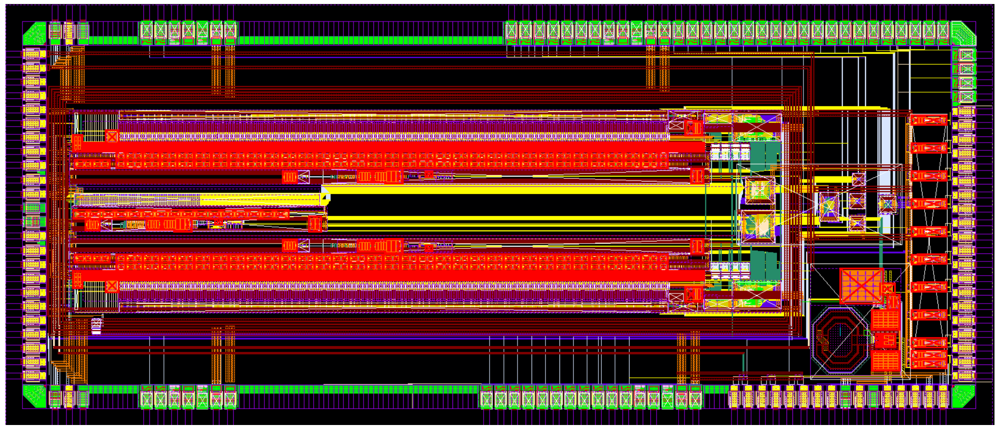
- **First prototype of SPIDER**
  - 2 self-triggering channels: channel design very similar to final specifications, simplified readout interface
  - PLL for time calibration
  - 2 test-benches foreseen @ **IJCLab + LPCA**

Submitted in Jan. 2025 - expected to be ready for testing in Q3 2025!



Next steps

- Characterisation of 1st prototype, and design of 2nd prototype in 2025-2026
- Design & characterisation of 8-channel rad. hard prototype (V2) in 2026 - 2027
- Additional prototypes planned for potential issues / margin
- Production in 2030 - 2031



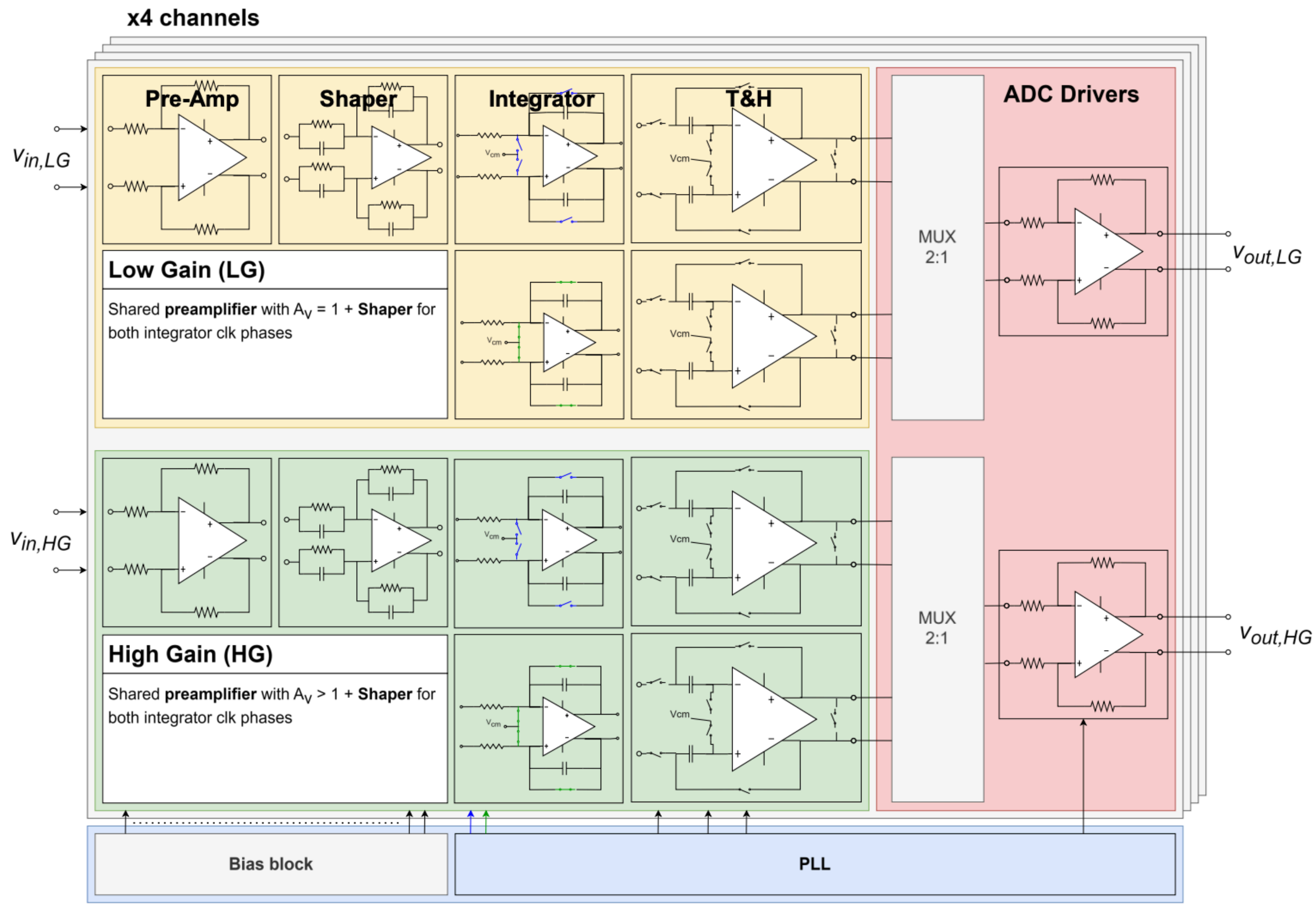
Energy ASIC: ICECAL65

- Design based in the current ASIC, adapted to TSMC 65 nm
- Moved from single to double-gain system to achieve dynamic range of ET [0, 40 GeV] on 11 bits

Planning:

- First prototype expected in beginning of 2025
- Second prototype (full channels) to be submitted in 2025 - tested in 2026

ICECAL65 planning in line (and a bit in advance) wrt to SPIDER planning



Front-end Boards for LS4

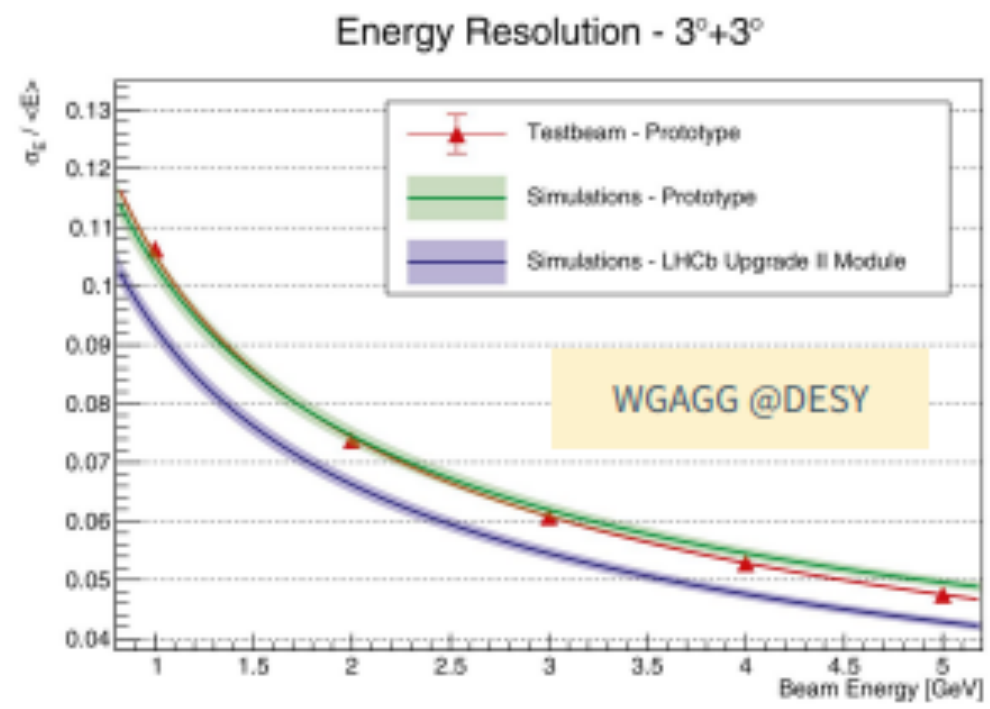
- All FE boards will need to be replaced for LS4:
  - Current ones not meeting radiation requirements of U2 (400 kRad at end of Run 5)
  - New design to host both energy and timing ASIC
  - Power supplies getting obsolete → will also need replacement
- **LS4 FEBs R&D and production under the responsibility of IN2P3 LHCb labs**
  - Number of new FEBs: 500 (including spares) to read-out ~30000 channels
  - 64 input channels / FEB, in 24 crates
  - No more Controller needed, direct connection for fast/slow control from FEB to PCie400
  - Planning to use radiation hard components from CERN, and share with ATLAS/CMS productions
- **Next steps:**
  - Preparation for 1st LS4 prototype will start mid-2025
  - 2 more prototypes foreseen: complete (ICECAL + SPIDER) + final (with final DAQ and interface components)
  - Test radiation hard component candidates (for example FPGA PolarFire)

LS4 FE board design planned responsibility of IJCLab
LS4 FE board testing / production planned to be shared between IJCLab + LPCA

Simulation & reconstruction

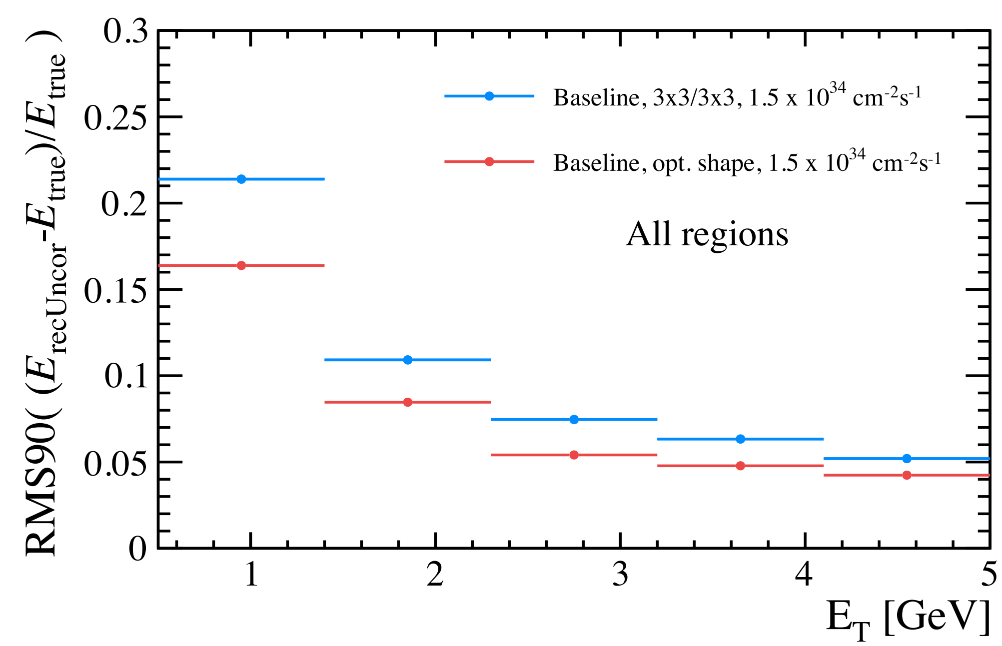
Hybrid simulation framework developed for fast turn-around of simulation production during R&D phase

- Good agreement with full simulation and testbeam results
- Migration to full LHCb Simulation Framework ongoing - should be ready for TDR studies



Reconstruction studies also done in a standalone framework for flexibility

- First version of clustering algorithm (Cellular automaton) available
- Work ongoing to include timing information and longitudinal segmentation in the clustering
- Migration to full LHCb Reconstruction Framework ongoing - targeting also TDR studies
- Performance improvements via reconstruction optimisations under study



Main target for TDR is to have a full PicoCal simulation and first reconstruction version on the LHCb framework

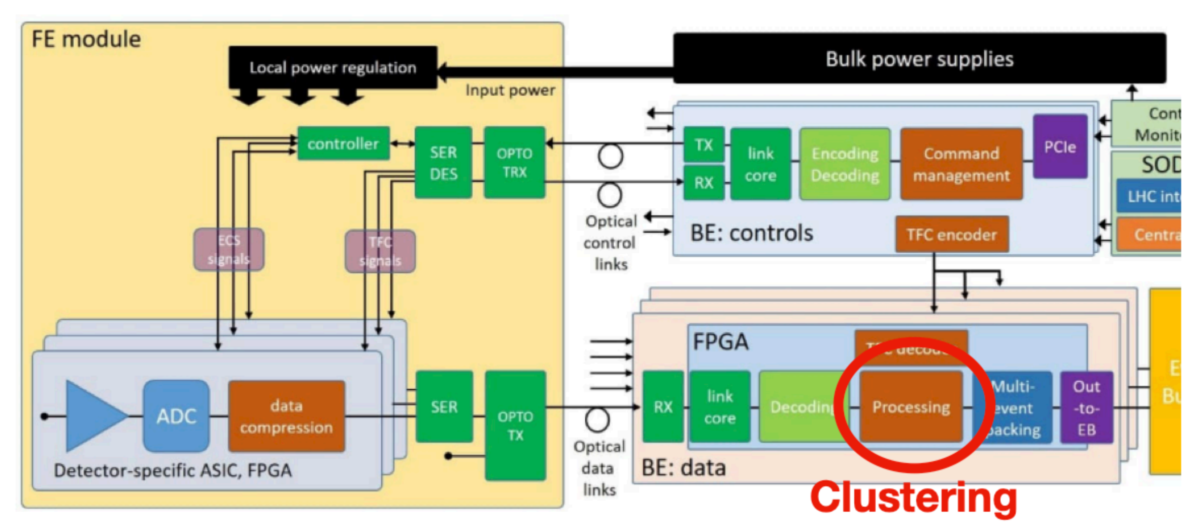
Real time reconstruction & pre-processing

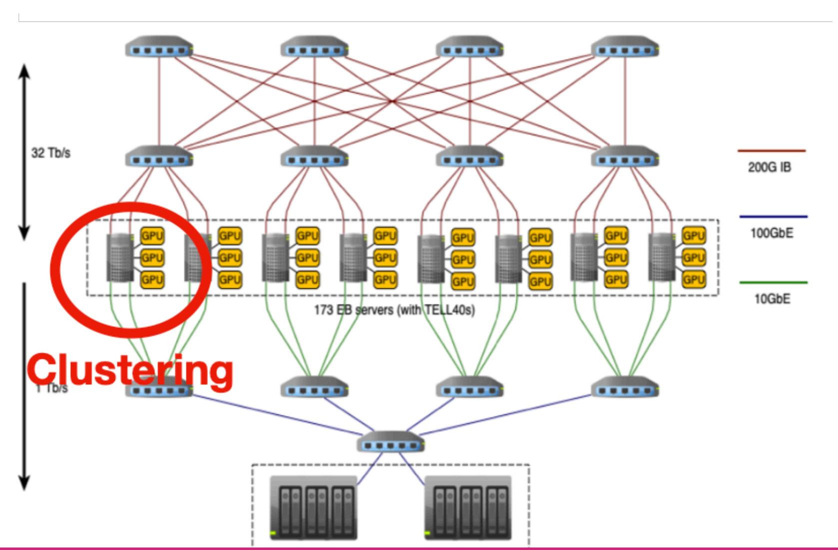
PicoCal will have x5 more channels than current ECAL, with additional information from timing-it will also need to operate at the full LHC rate → Read-out rate and real-time reconstruction **challenging**

Pre-processing solutions being explored

- Compression algorithms at front-end boards :
  - Compress waveform to extract timing info more precisely/with same/fewer bits
  - Auto-encoders currently being explored by MIT (Boston)

- Pre-clustering/clustering at back-end
  - Zero-suppression, primitives finding or full clustering at back-end FPGAs (PCIe400)
  - Reduce event-size / speed-up HLT processing
  - **IJCLab/LAPP starting to look into such solutions**
  - Benchmarking must be done together GPU-based reconstruction to explore benefits/caveats in a comprehensive way





Work requiring close collaboration with online & RTA, required expertise all within IN2P3

Project organisation

Project organisation

ECAL LS3 Enhancement Organisation
Project Leader: P. Roloff (CERN)

WP1: Absorbers
CERN, China*
H. Gerwig (CERN), S. Kholodenko (CERN), L. Zhang (Tsinghua)

WP2: Optics assembly (fibers & lightguides)
Maryland, Milano, China*
M. Salomoni (Milano), Z. Yang (Peking)

WP3: Organic & crystal fibers R&D
CERN, China*
E. Auffray (CERN), M. Zeng (Tsinghua)

WP4: PMT & HV & LED system
CERN, ICCUB, CSIC, Maryland, Cincinnati, Bologna, Milano
P. Hamilton (Maryland), Y. Guz (Peking), C. Henderson (Cincinnati)

WP5: Electronics
IJCLab, LPCA, LAPP, ICCUB, CSIC, Syracuse
P. Robbe (IJCLab), C. Beigbedder (IJCLab)

WP6: Infrastructure
CERN, LAPP, Imperial
A. Golutvin (Imperial)

WP7: Detector software
CERN, China*, IJCLab, LAPP, La Salle, Milano, Padova, MIT, Syracuse
M. Pizzichemi (Milano), L. An (Peking)

WP8: Test beam coordination & analysis
CERN, All
L. Martinazzoli (CERN), D. Manuzzi (Bologna)

*China: Peking, Tsinghua, Wuhan and SCNU

French contributions:

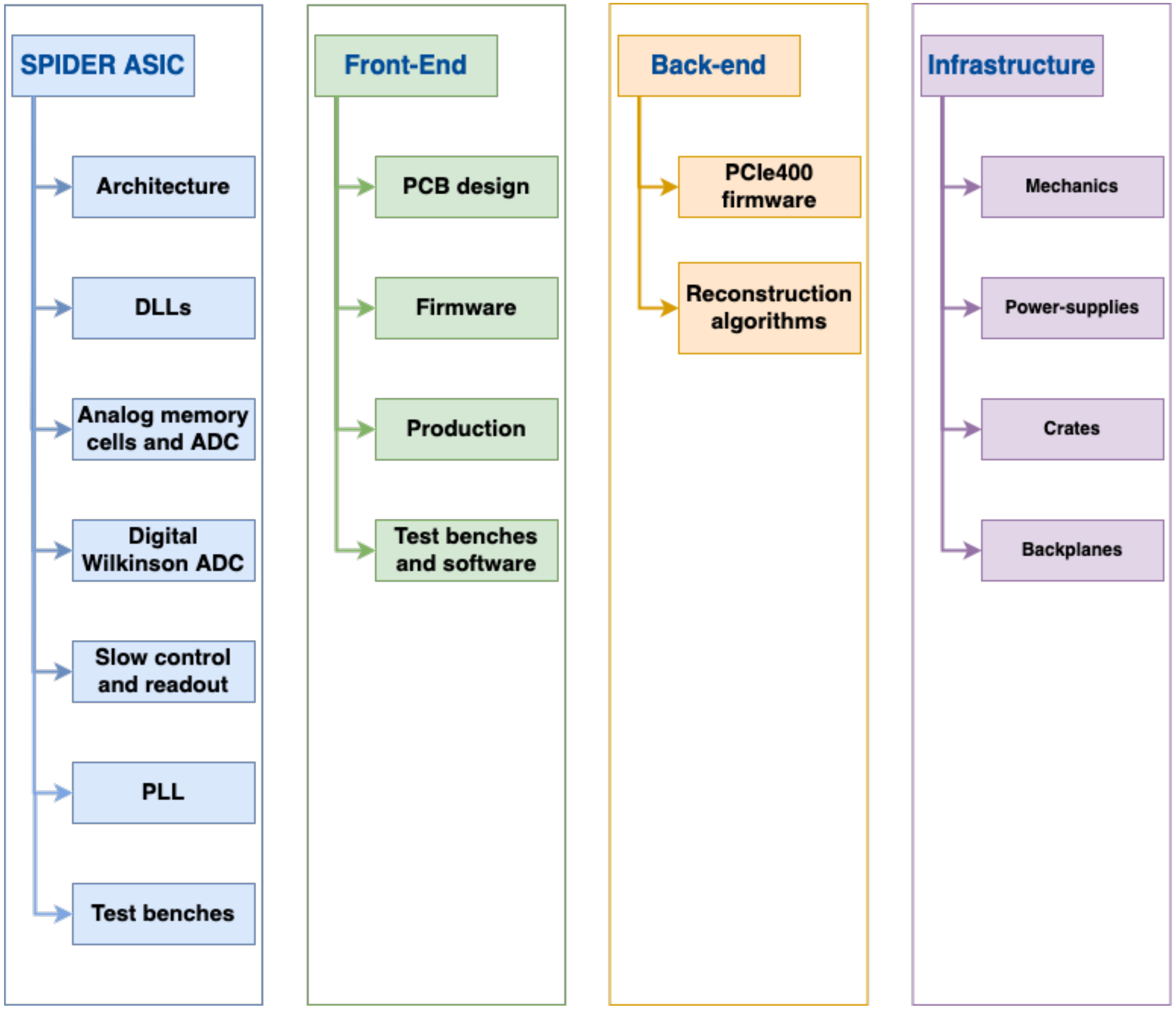
- mainly focused on WP5 -Electronics and WP6 - Infrastructure
- contributions to WP7 - Software and WP8 - Testbeam envisaged

Within France

French responsibles: P. Robbe, V. Tisserand

Electronics: C. Beigbeder

SPIDER ASIC developments: P. Vallerand, B. Joly



- **SPIDER ASIC:** IJCLab, LPCA, IP2I Lyon, LPC Caen, Subatech Nantes
- **Front-end:** IJCLab, LPCA
- **Back-end:** LAPP
- **Infrastructure:** IJCLab, LPCA, LAPP

Involved IN2P3 institutes

IJCLab

Permanents	Engineers
C. Agapopoulou	C. Beigbeder
Y. Amhis	D. Breton
S. Barsuk	Z. Kiraz
P. Robbe	J. Maalmi
M.H. Schune	P. Vallerand
	C. Sylvia

LPCA

Permanents	Engineers
S. Akar	N. Arveuf
V. Tisserand	G. Blanchard
	B. Joly
	F. Jouve
	A. Contamine
	M. L. Mercier
	R. Vandaele

LAPP

Permanents	Engineers
J. F. Marchand	N. Allemandou
S. T'Jampens	J.P. Baud
	L. Journey
	B. Lieunard
	G. Vouters

IP2I Lyon

Engineers

E. Bechetoille

H. Mathez

LPC Caen

Engineers

L. Alvado

L. Leterrier

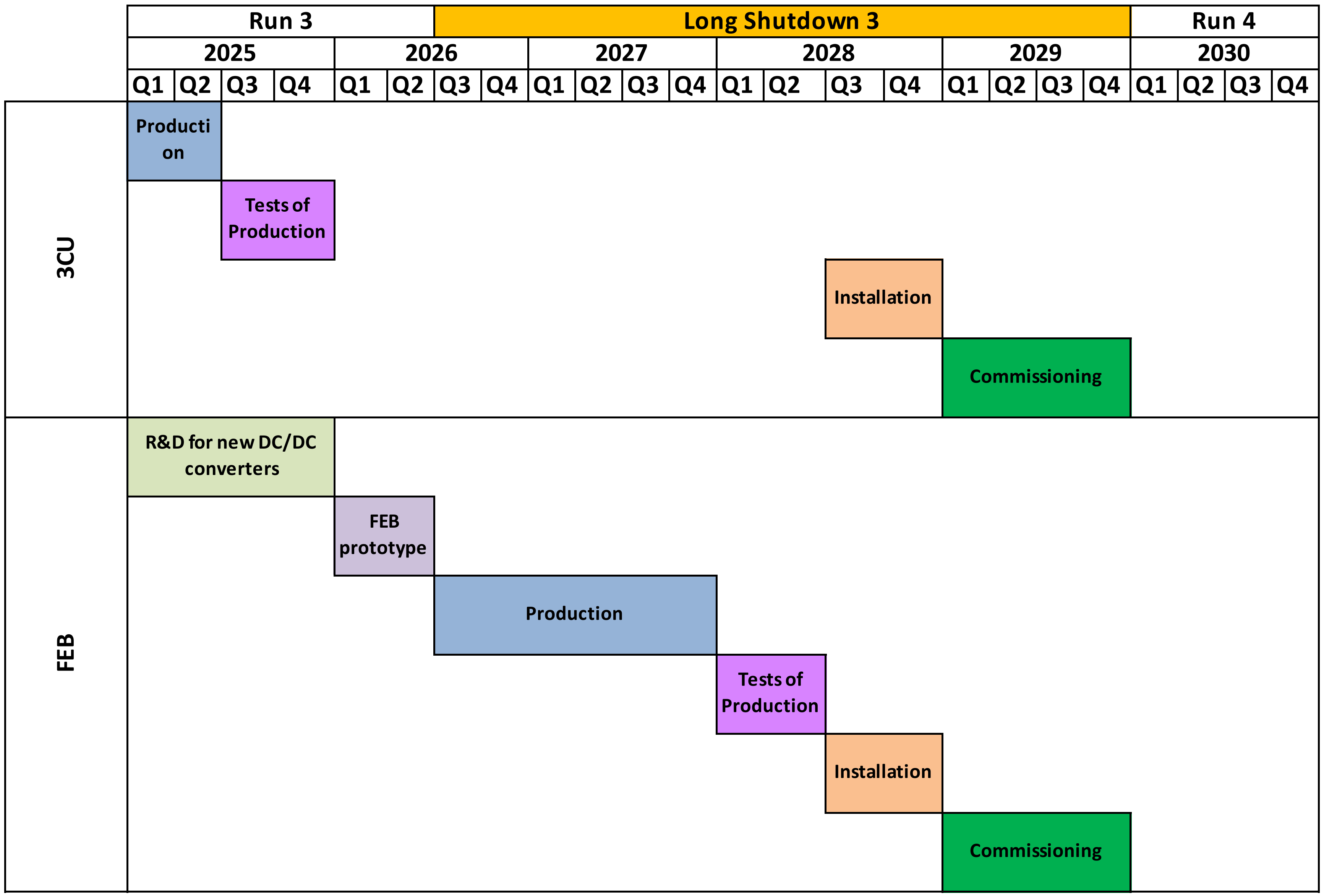
Subatech Nantes

Engineers

D. Charrier

LS3-enhancement schedule

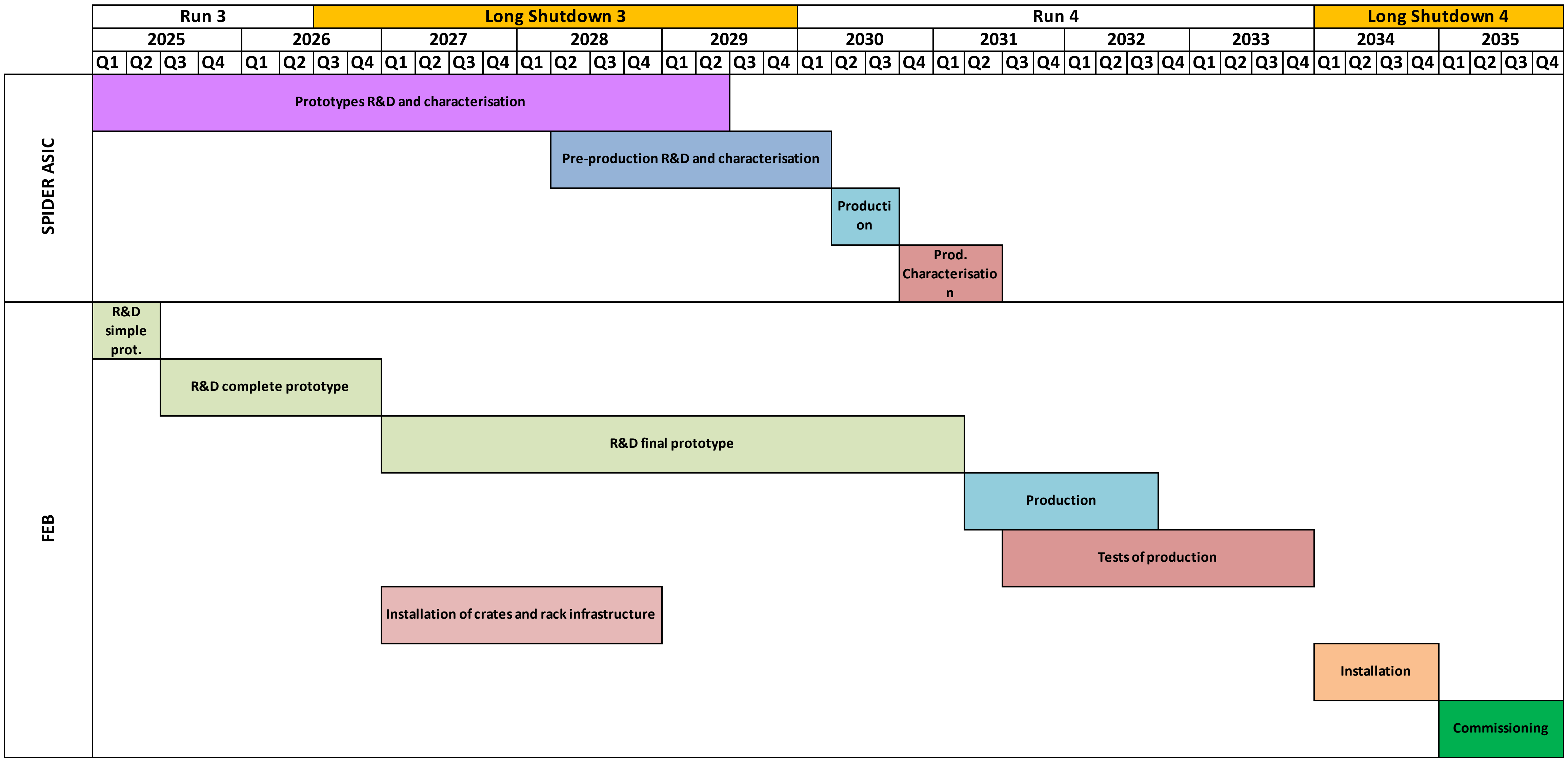
Main responsibility of IN2P3 institutes for LS3-enhancement: production & testing of FEBs and 3CU boards



- 3CU boards already produced (move some budget/personpower earlier in the schedule)
- 1st FEB prototype available in Q1 2025
- 6 months margin in production

LS4 electronics schedule

Main responsibility of IN2P3 institutes for LS4: R&D, production & testing of SPIDER ASIC and FEBs



- **SPIDER:** 5 prototypes (2 only there in case of discovered issues, otherwise can be used as margin). IJCLab, LPCA and Syracuse interested in tests of production
- **FEBs:** 6 month margin in production, 1 year margin in test of production

IN2P3 costs

LS3 & LS4 costs of IN2P3 institute activities in PicoCal, in k€

Item	Run 3	LS3				Run 4				LS4		Total
	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	
LS3 FE production		385										385
LS3 installation mission					15							15
SPIDER protytpes	39	39	39	39								156
SPIDER production						39	360					399
LS4 FE prototypes		10	10	10								30
LS4 FE production							875	875				1750
LS4 Power supplies			120	120								240
LS4 Backplane boards						5	35					40
test bench material	1	8	4	4	4							21
test beam material		2	4	4	4							14
LS4 installation mission											15	15
Total per year	40	444	177	177	23	44	1270	875	0	0	15	3065

- IN2P3 contribution: ~3 M€ over a 10 year period
  - 400 k€ for LS3 enhancement, 2.6 M€ for LS4 (in baseline / middle scenario)
  - SPIDER / ICECAL65 production shared to reduce cost
- Low scenario:
  - Timing information still provided for the full detector
  - Smaller amount of channels (no longitudinal segmentation in external part modules)
  - IN2P3 Cost: 2.5 M€

Personpower

Estimated required FTEs for PicoCal (LS3 + LS4)

	Run 3	LS3				Run 4				LS4		Total
	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	
Management	0,3	0,3	0,3	0,3	0,3	0,3	0,3	0,3	0,3	0,3	0,3	3,3
Microelectronics	5	5	4	4	4	3	2	2	1	0,3	0,3	30,6
Electronics	3	3	3	3	3	3	2	2	1	0,3	0,3	23,6
Mechanics	1,7	1,4	0,7	0,3								4,1
Computing/Software	0,85	0,7	0,5	0,5	0,5	0,5	0,5	1	1	2	2	10,05
Instrumentation	0,3	0,3			0,3	0,3	0,3					1,5
Cabling/Installation			2	2	1				1,6	5	5	16,6
Total	11,15	10,7	10,5	10,1	9,1	7,1	5,1	5,3	4,9	7,9	7,9	89,75

Available FTEs for PicoCal (LS3 + LS4)

	Run 3	LS3				Run 4				LS4	
Physicists	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
IJCLab	1.5	1.75	1.7	1.7	1.2	1.2	1.2	1.2	1.2	2.5	2.5
LAPP	0.25	0.5	0.5								
LPCA	1	0.7	0.7	0.7	0.7	1	1	1	1	1	1
Total	2.75	2.95	2.9	2.4	1.9	2.2	2.2	2.2	2.2	3.5	3.5

	Run 3	LS3				Run 4				LS4	
Engineers	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
IJCLab	3.55	2.8	2.8	2.2	2.2	2.2	1.2	1.2	1.2	2	2
LAPP	0.7	0.8	0.9	0.8							
LPCA	3.25	3.25	3.25	3.25	3.25	2.7	1.5	1.5	1.5	2	2
LPC Caen	0.2	0.2	0.05	0.05	0.05	0.05	0	0	0	0	0
SUBATECH	0.5	0.5	0	0	0	0	0	0	0	0	0
IP2I Lyon	0.2	0.2	0.05	0.05	0.05	0.05	0	0	0	0	0
Total	8.4	7.75	7.05	6.35	5.55	5	2.7	2.7	2.7	4	4

Based on real estimates until 2029, projections from 2030 onwards

- Person-power ok until 2029
- From 2030 onwards, available FTEs based on projections, will need enhancements from PhD/postdoc students + potential newcomers + recruitment of CR at LPCA

Risks

- **ASIC technology (analog memories, 65 nm) - Addressed during R&T phase:**
  - 3 year SPIDER R&T, also past R&T on DLL components (non-LHCb), financed by IN2P3
  - 65 nm sustainable for the next 10 years
  - good performance of 65 nm SPIDER ASIC in simulation
  - Test-beam results with WaveCatcher prove analog memory technology can reach the required resolution

Remaining risks

- **Availability and price of FE components (provided by CERN, common with ATLAS/CMS Phase II upgrades)**
  - **Mitigation strategy: order components as soon as design is frozen to profit from ATLAS/CMS shared orders**

- **Retirement of key personnel, in particular electronics experts**
  - **Mitigation strategy: new IR position, newcomer expected in March 2025. Will focus on knowledge transfer during the FEB prototyping phase, to eventually take over a position of expertise in the project**

- **Long term commitment of IP2I Lyon who are not LHCb members and whose participation is only ensured until end of 2026**
  - **Mitigation strategy: development plan adapted to take this into account, their blocks of responsibility expected to be ready in the early phase of the project (with SPIDER v0)**

Conclusions

- The LHCb U2 upgrade gives the opportunity to fully take advantage of the High-Luminosity LHC to enhance the full LHCb physics program

- The ECAL is a critical component of the experiment, enabling analyses involving electrons & neutral particles in the unique environment of LHCb - **its upgrade is a requirement to reach the ultimate U2 precision in these analyses**

- The ECAL upgrade for U2, PicoCal, is the natural continuation of the IN2P3 involvement in LHCb since the beginning, both for the electronics, detector operation, reconstruction and physics analyses, in which we want to maintain our leadership

We would like to thank IN2P3 for its support during the R&T phase of the LHCb-PicoCal project, thanks to which we obtained a first prototype of the SPIDER ASIC

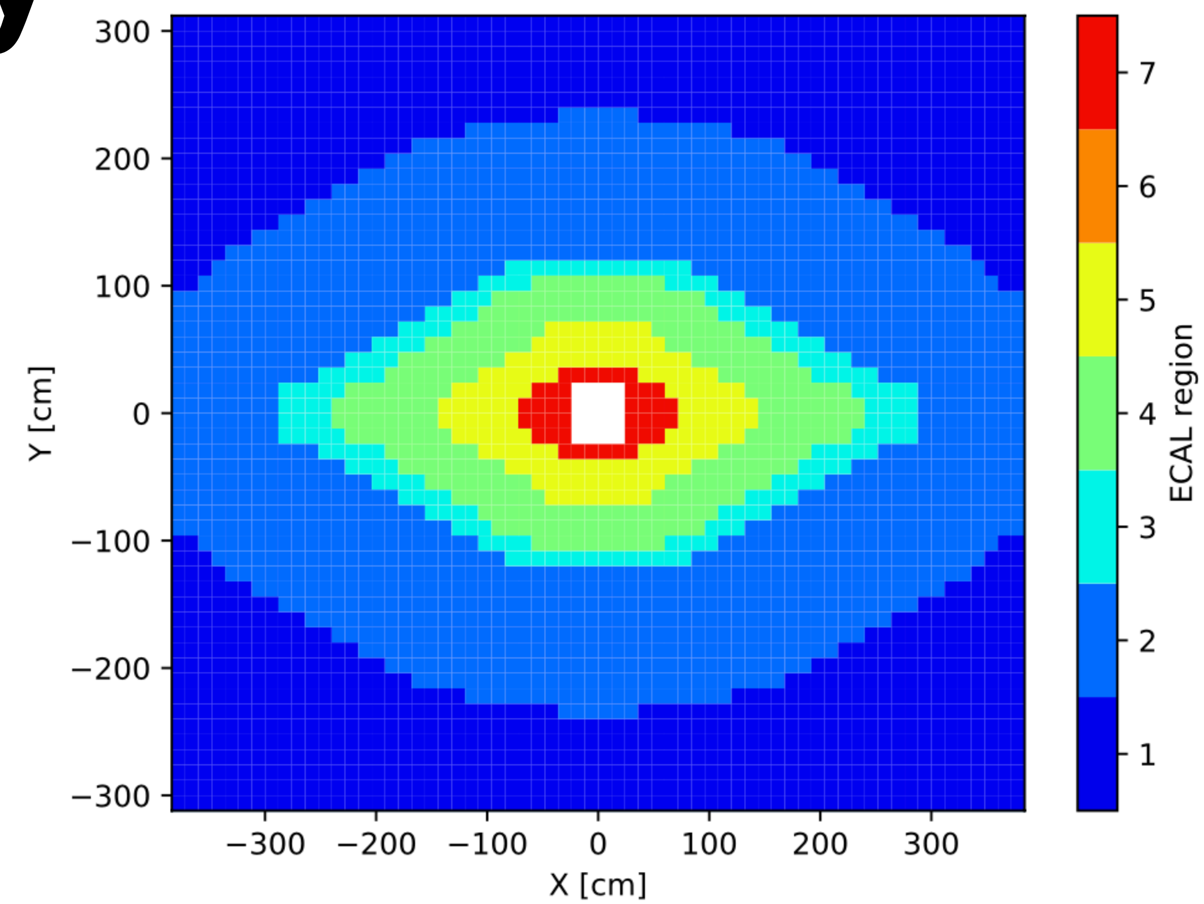
LHCb relies on the leading expertise acquired by engineers and physicists at IN2P3 in precise timing electronics and Front-End electronics for the success of the PicoCal project. For the IN2P3 laboratories, this is an unique opportunity to maintain and develop these competences for future developments, within the HEP community and beyond

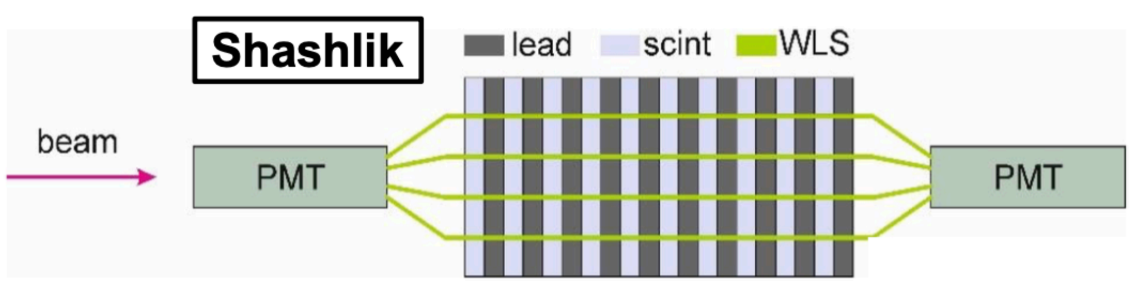
Backup

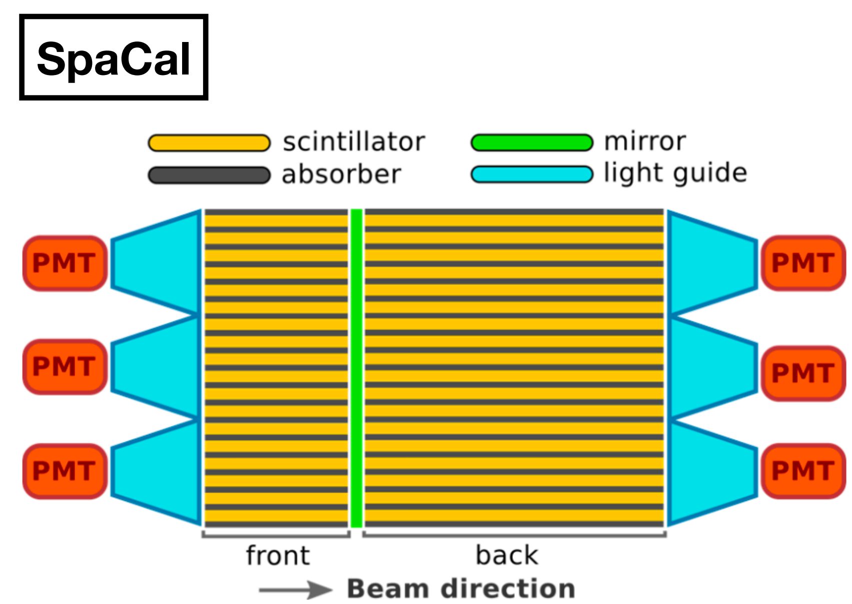
Detailed geometry

Region*	Cell size	Number of modules
1	12x12 cm^2	1344 Shashlik
2	6x6 cm^2	1344 Shashlik
3	4x4 cm^2	176 Shashlik
4	4x4 cm^2	272 SpaCal
5	3x3 cm^2	136 SpaCal
7	1.5x1.5 cm^2	40 SpaCal

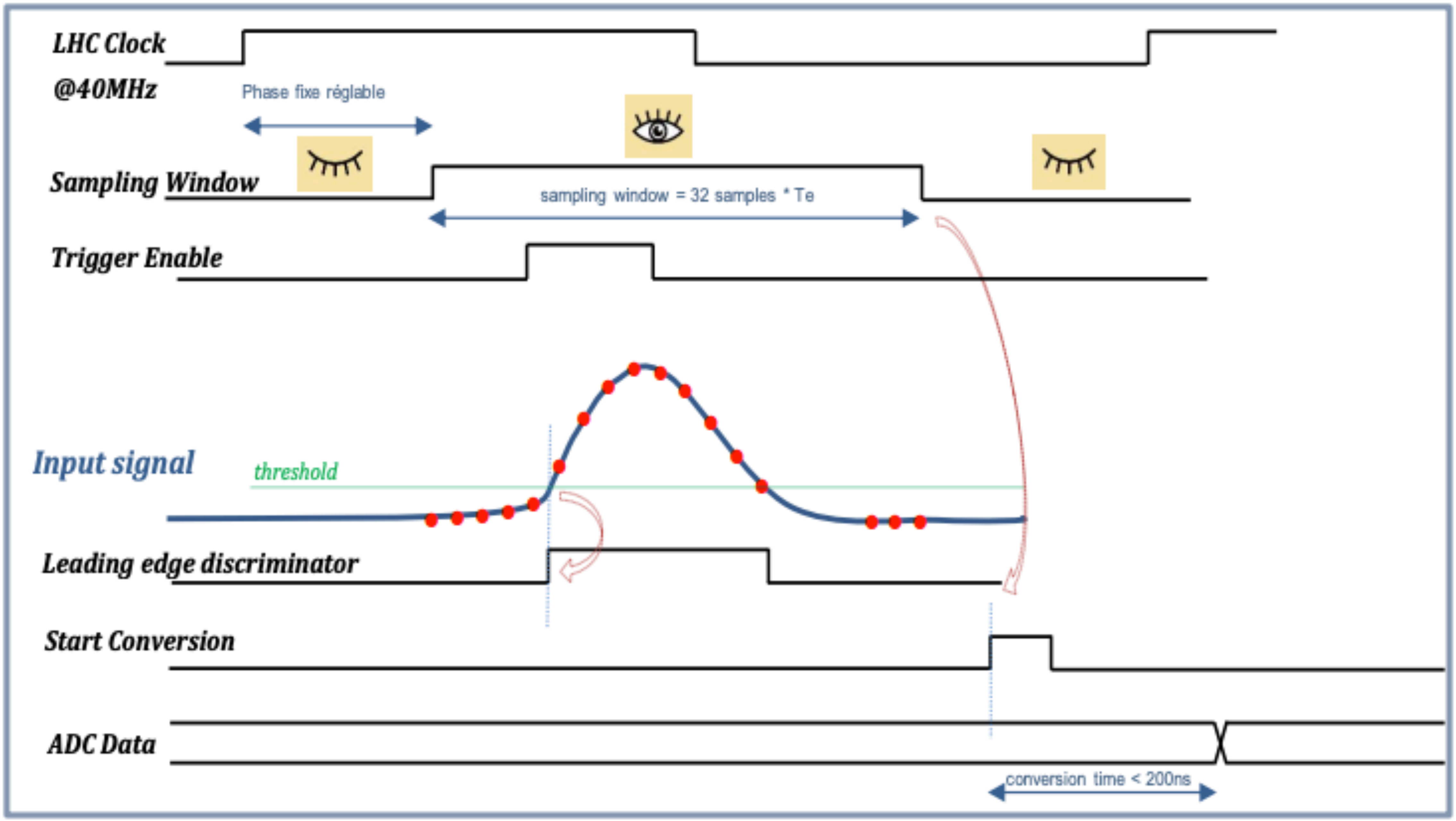
***LS3 enhancement**: innermost region equipped with 2x2 cm2 plastic scintillating fibres + W absorber







The SPIDER sampling logic



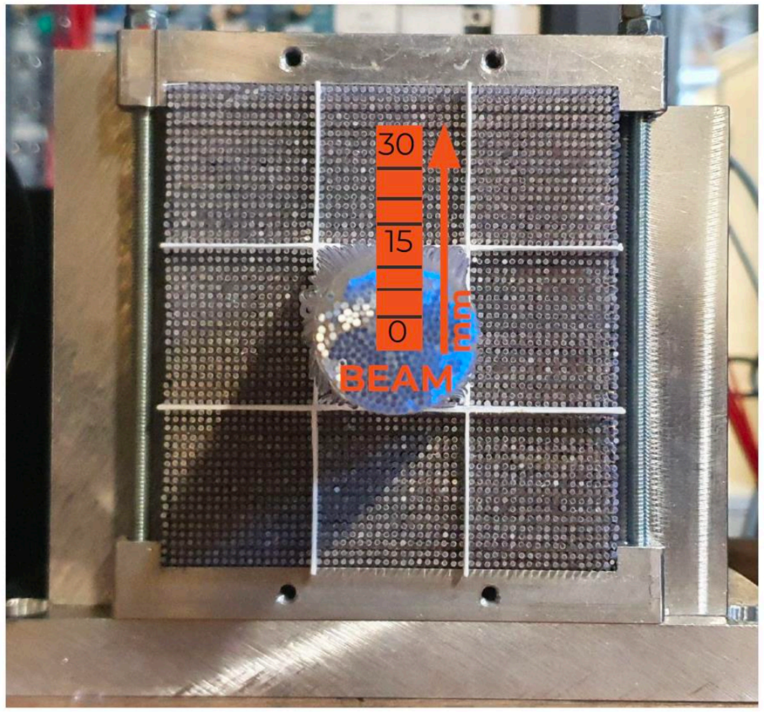
Detailed SPIDER schedule

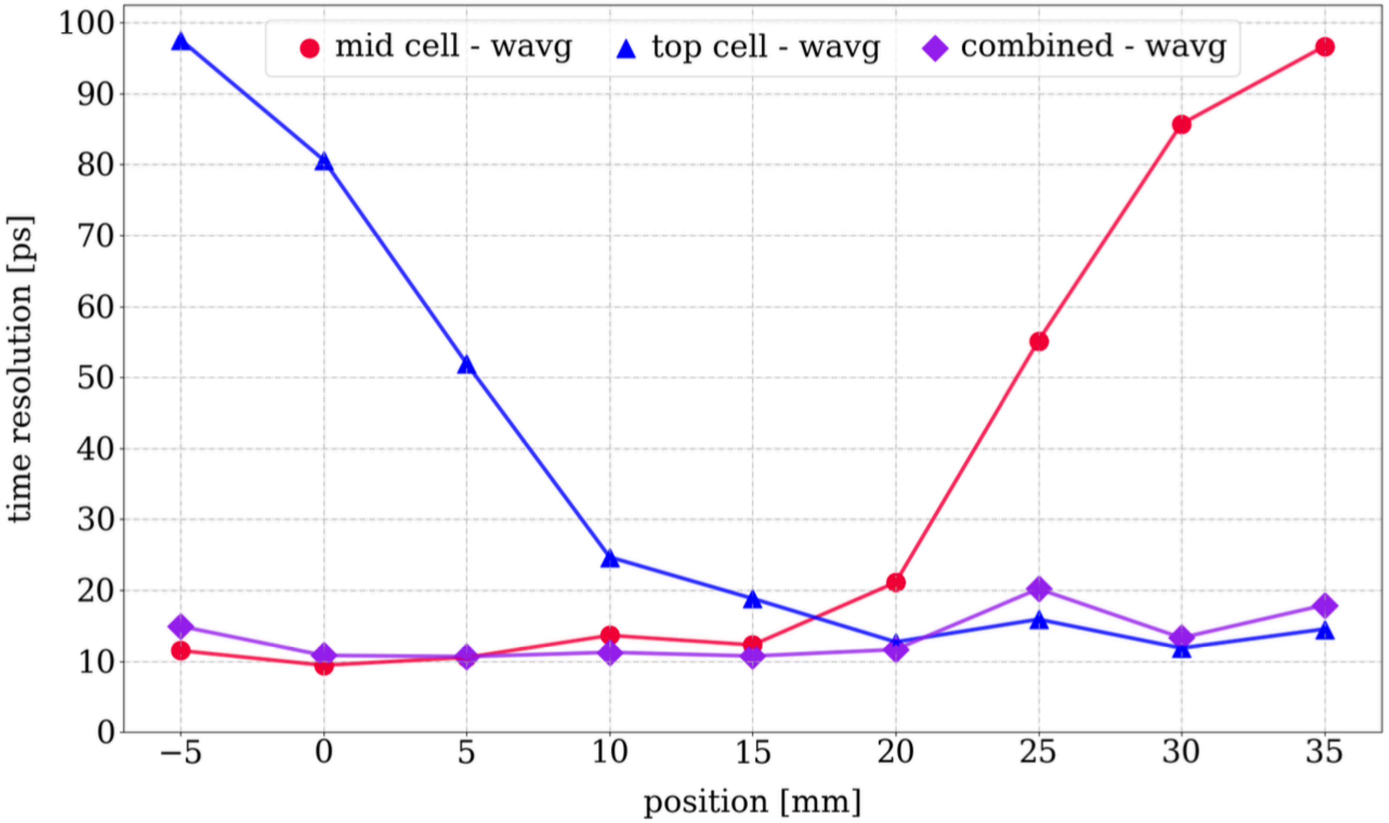
- **2024**: Design SPIDER V0 (2 channels + technology validation)
- **2025**: Characterisation SPIDER V0 and (optional) design SPIDER V1 (2 channels, in case of issues with v0)
- **2026**: (optional) Characterisation of SPIDER V1 and (not optional) design of SPIDER V2 (8 channels, rad hard)
- **2027**: Characterisation of SPIDER V2 and (optional) design V3 (V2 optimisation)
- **2028**: (optional) Characterisation of SPIDER V3 and (not optional) design of SPIDER V4 (8 channels, rad. Hard, yield)
- **2028 - 2030**: Characterisation of SPIDER V4 and pre-production design & characterisation
- **2030 - 2031**: SPIDER Production

Position dependence of time resolution

Studied in testbeam (PbPoly module, SPS with 60 GeV electrons)

- Time resolution worsens from 10 → 90 ps when moving from center to edge of cell
- Performance can be fully recovered by using neighbouring information (clustering)



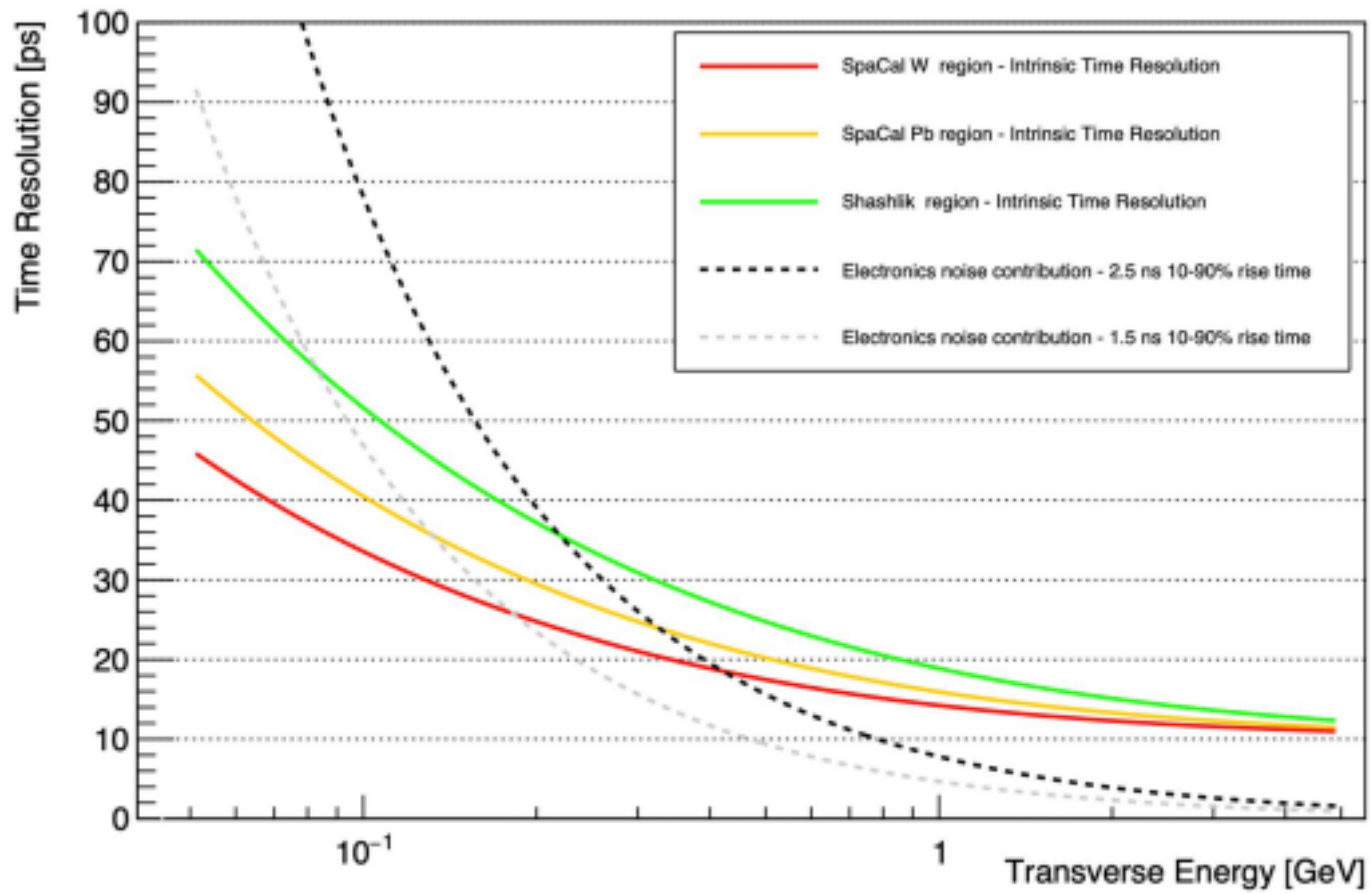


Electronics contribution to the time resolution

Reminder: $\sigma_t = \frac{t_{rise}}{SNR}$

Rise time an important parameter in the choice of PMTs and cables

Most limiting for the innermost modules (SpaCal - W)



SPIDER counting rate

- Around 40 ns reading time (BX + Peak + 8 Samples * 250MHz)
- Random occupancy and trigger distribution
- Equiprobable conversion time (10 -200ns)

- Distribution 90% (< 20ns)