Design and Testing of a Readout Chip with Integrated Sensor for High Energy Physics

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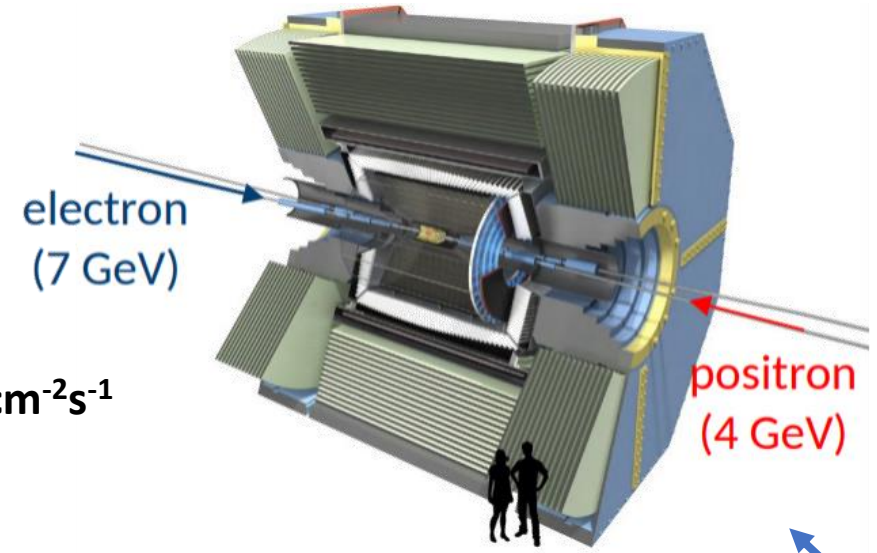
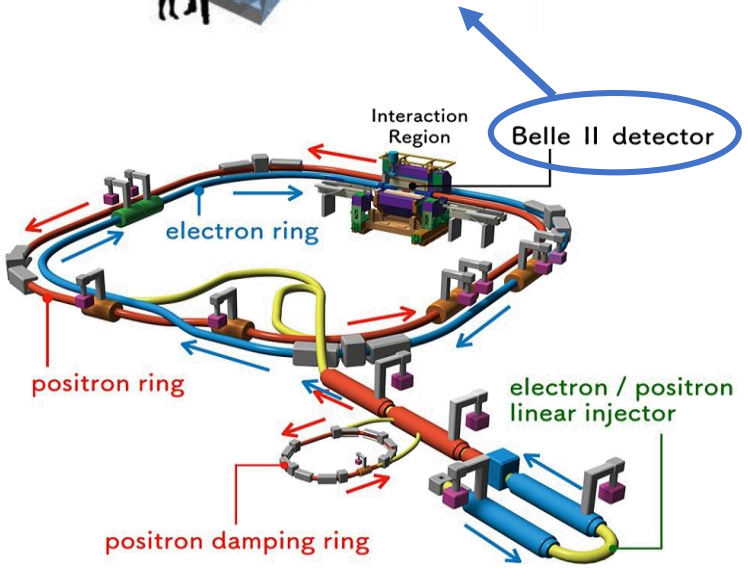
Outline

1. The Belle II Experiment
2. The VTX Upgrade Proposal
3. The TJ-Monopix2 chip
4. The OBELIX sensor : **O**ptimized **Belle**2 p**IX**el sensor
5. Summary and next steps

The Belle II Experiment

- Located at the SuperKEKB collider in Tsukuba,Japan
- Asymmetric e^+- e^- collider at 4 / 7 GeV and $\sqrt{s}$ = 10.58 GeV
- Target instantaneous luminosity of **6×10^{35} cm^{-2}s^{-1},** currently **0.47×10^{35}cm^{-2}s^{-1}**
- Target integrated luminosity of **50 ab^{-1},** currently **0.43 ab^{-1}**
  - Machine related beam background will increase with high luminosity
  - Efficiency, resolution and performance of data tracking could degrade with higher occupancy from background
  - Extrapolation to this target luminosity has large uncertainty and limited safety margins





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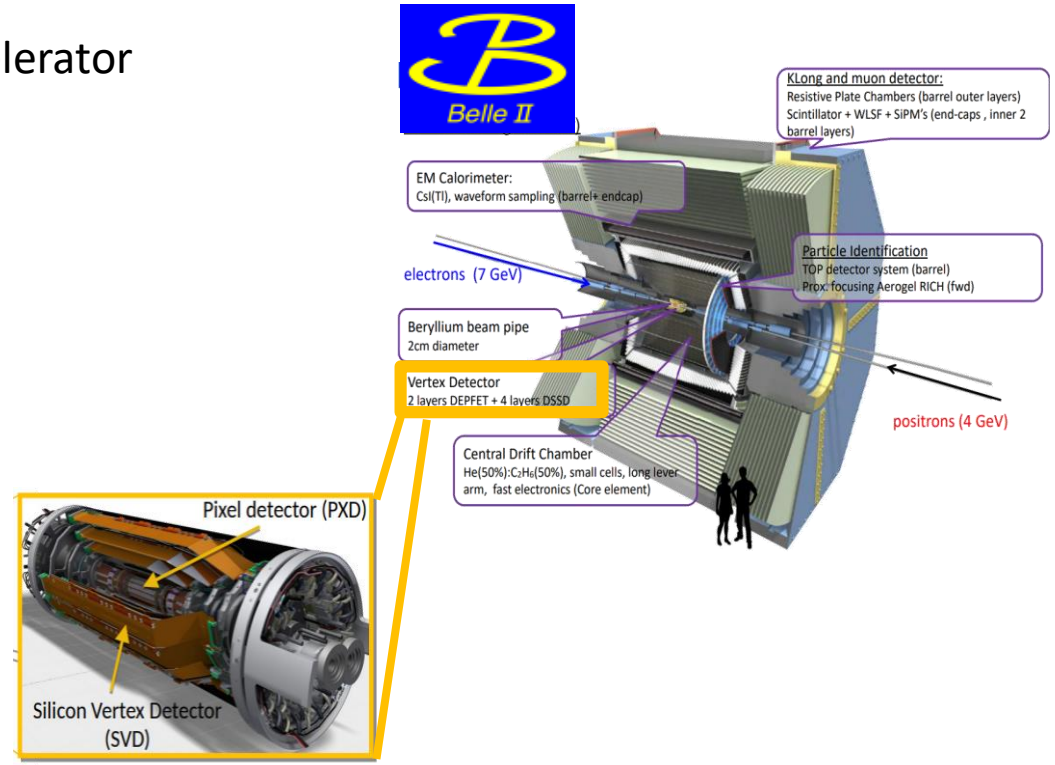
The Belle II Upgrade Motivations

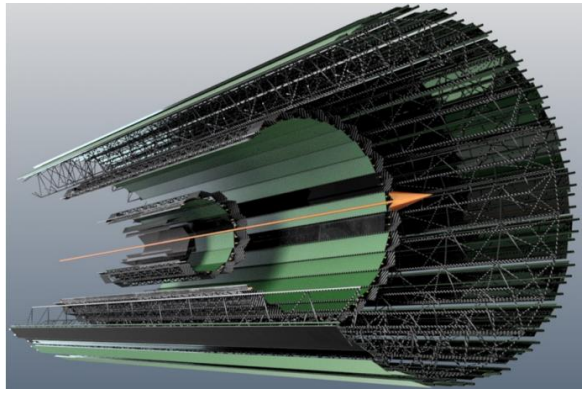
- An upgrade of the machine elements and the detector's **interaction region (IR)** is required:
  - To cope with the higher luminosity provided by the SuperKEKB accelerator
  - To improve detector robustness against high backgrounds
  - To provide larger safety factors for running at higher luminosity
  - To increase longer term subdetector radiation resistance
  - To improve overall physics performance
- Two different technologies compose the current Vertex Detector VXD:
  - Two layers of DEPFET Pixel Detector (**PXD**)
  - Four layers of Silicon Vertex Detector (**SVD**)



- A **long shutdown** is foreseen around early 2030 and provides the opportunity to install an upgraded detector

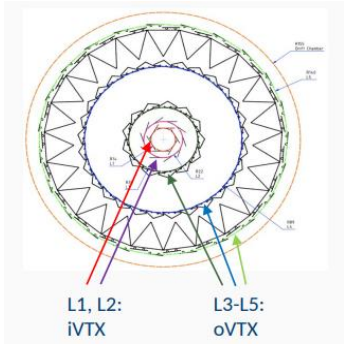
➡ **A new vertex detector concept VXD is proposed**

The VTX Upgrade proposal



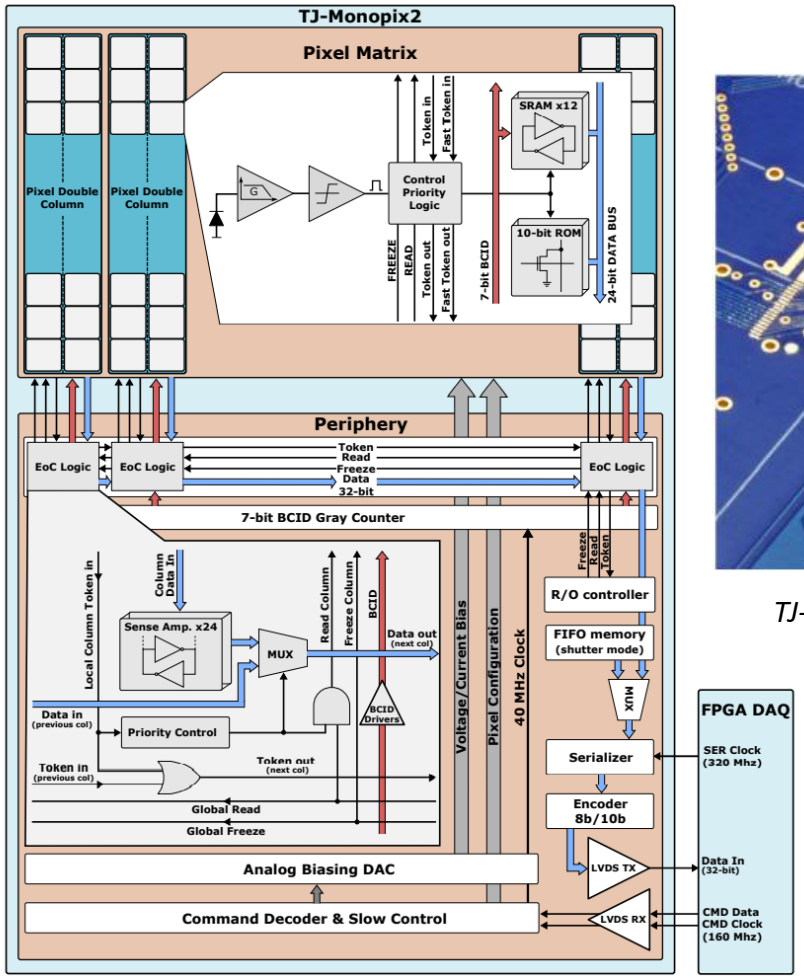
- A new fully pixelated CMOS detector to replace the VXD → VTX
- Improved tracking resolution and space-time granularity
- Reduced material budget ≈ 2%X0 instead of 3.8%X0 (sum of all layers)
- 5-6 straight layers with **D**epleted **M**onolithic **A**ctive CMOS **P**ixel **S**ensors (**DMAPS**) process
- L1 and L2 (iVTX)
  - All silicon ladders
  - Air cooling (constrains power)
- L3 to L5 (oVTX)
  - Carbon fiber support frame
  - Cold plate with liquid cooling

	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	17	40	31	
# Sensors	4	4	7	16	2 x 24	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.2	0.2	0.3	0.5	0.8	% X_0

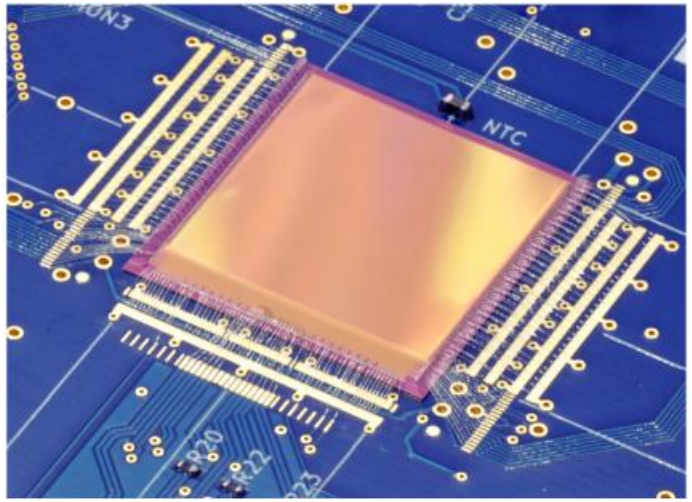


- A same monolithic CMOS pixel sensor chip for all layers : **Optimized BELLE II pIXel sensor (OBELIX)**

The TJ-Monopix2 (TJM2) as prototype



Chip architecture of TJM2



TJ-Monopix2 sensor bonded on a test board

- Developed for ATLAS experiment
  - FE derived from ALPIDE
  - 4 FE flavors
  - Column-drain R/O architecture
- DMAPS **Tower Semiconductor 180 nm CMOS**
- 2×2 cm² chip: 512×512 pixels
- Pixel pitch: 33.04×33.04 µm²
- Expected from design (simulations):
  - ~ 100 e− min. threshold
  - 5-10 e− threshold dispersion (tuned)
  - >97% efficiency at 10^{15} n_{eq}/cm²
  - ~ 5 e− noise
  - Fully efficient with hit rate 120 MHz/cm²
  - Power: ~ 1 µW/pixel

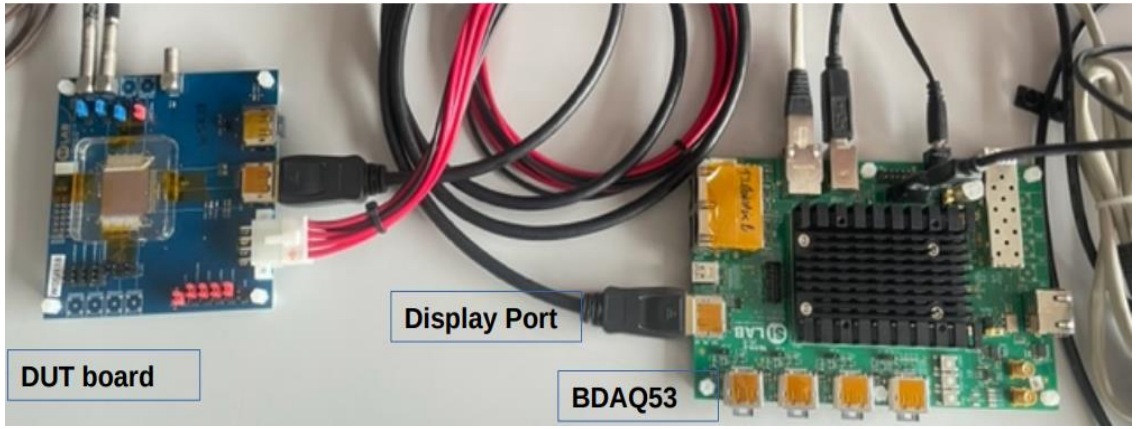
Base-line option for OBELIX design

The TJM2 Testing

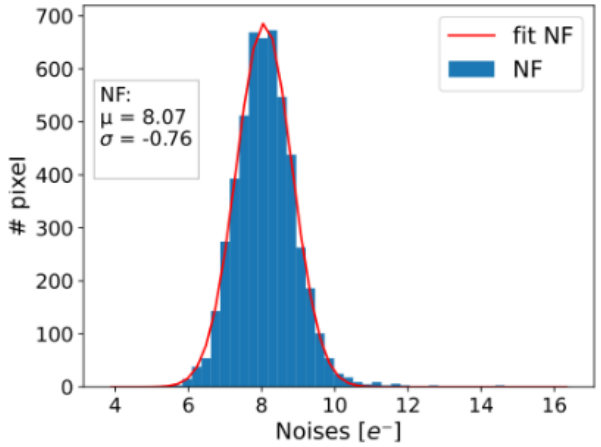
- Characterisation of TJ-Monopix2 (all FE) to validate key performance crucial for OBELIX design

- **Full characterisation** on bench:
  - Threshold scans (lowest value, dispersion)
  - Noise testing
  - ToT (Time Over Threshold) calibration

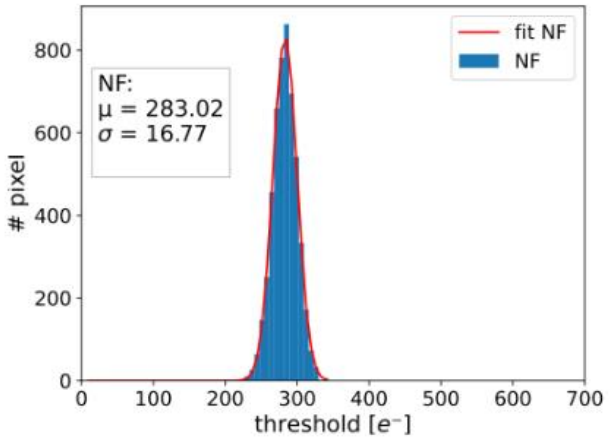
- Control and data acquisition system based on the BDAQ53 setup



TJM2 setup DAQ inherited from RD53 collaboration



Noise distribution



Threshold distribution.

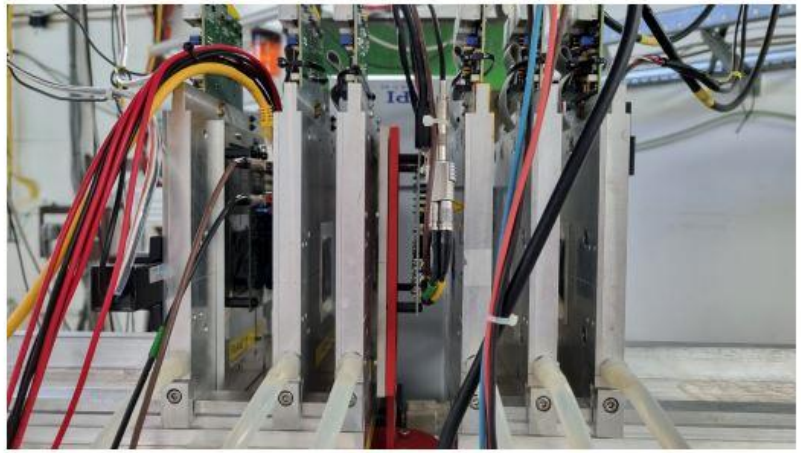
- Typical settings for operational threshold:
  - Thresholds between 200 to 300 e−
  - Average noise varies from 7 to 8 e−

- Time Over Threshold (ToT) calibration, Fe55

- Comparison with measurement and simulations
  - Measurement from monitoring pixels of the analog output signal after the FE amplifier

The TJM2 Testing

- **Full characterisation@DESY**:
  - Efficiency/Resolution measurements
  - Radiation hardness (NIEL and TID irradiation campaigns in progress)



Setup for testbeam – @Desy

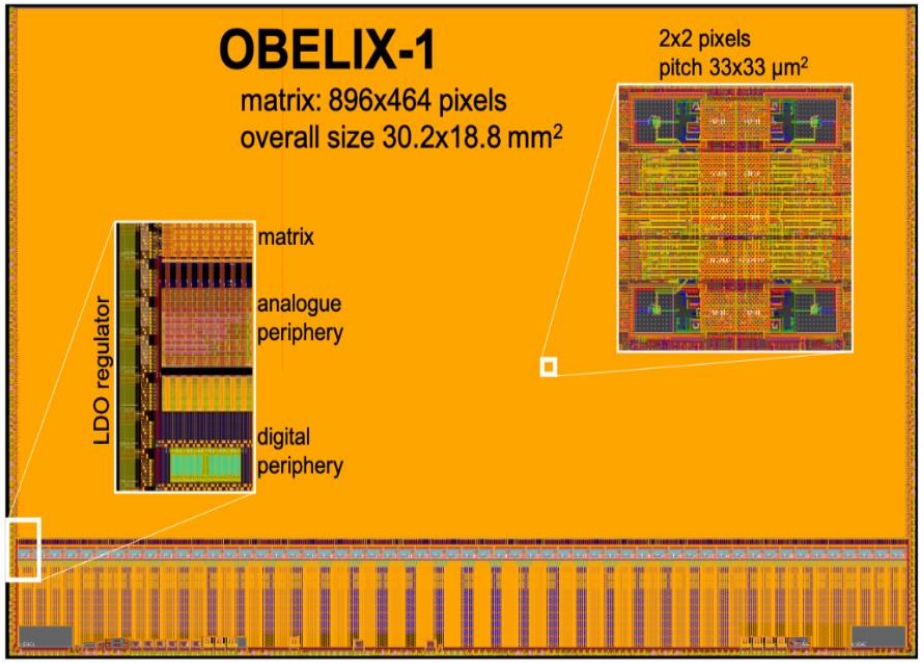
- **Several test beam campaigns (3-5 GeV e-)**
  - **July 2022:** Non-irradiated chips
    - High threshold (500 e-)
    - Hit efficiency ~ 99.54%, Cluster position residuals ~ 9 µm
  - **July 2023:** Irradiated chips at $5x10^{14}$ n_{eq}/cm^2
    - Lower threshold ~ 250-300 e-
    - Good performance and high efficiency
  - **July 2024:** Irradiated chips at $5x10^{14}$ n_{eq}/cm^2, TID of 100 Mrad
    - Good efficiency but temperature influence

→ **Another test beam planned for 2025**

The OBELIX Sensor

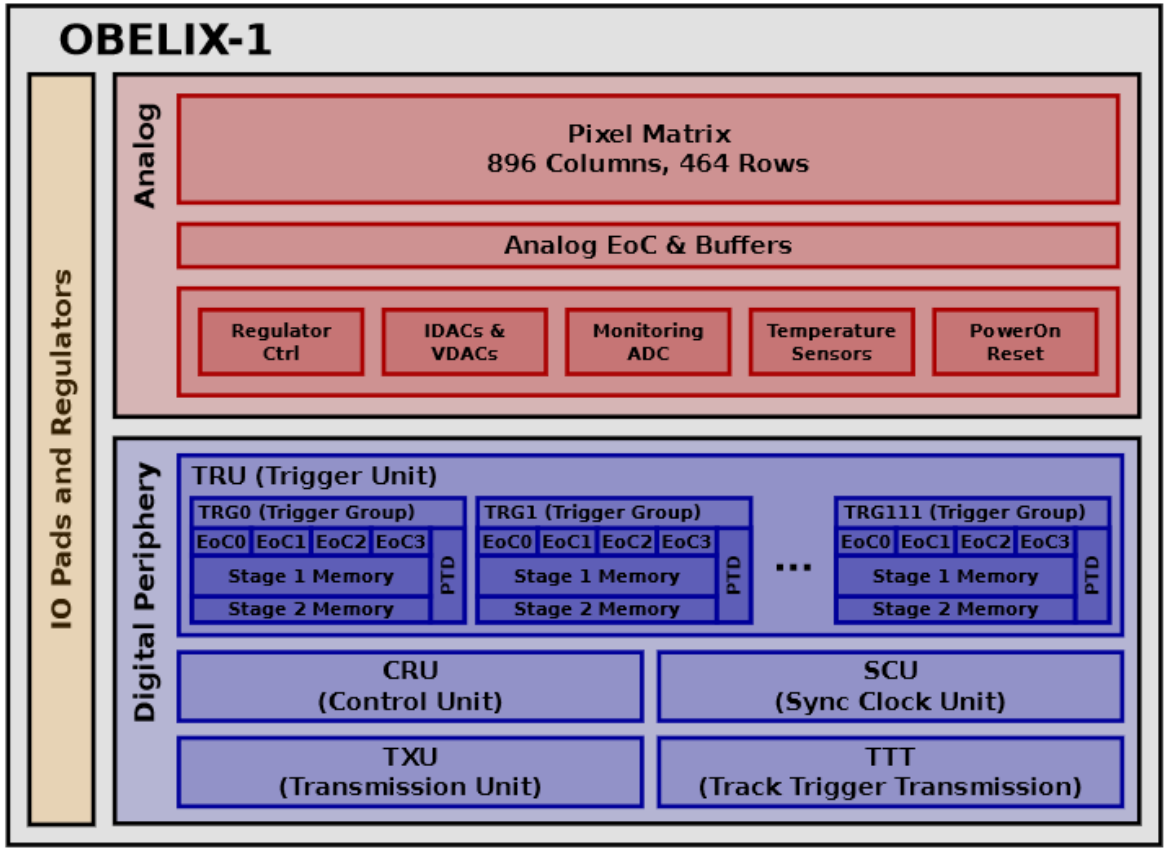
Sensor specifications:

- Tower Semiconductor 180 nm CMOS
- Hit rate up to 120MHz/cm²
- TID tolerance: 100 MRad
- NIEL tolerance: $5x10^{14}$ $n_{eq}/cm^2/year$
- Spatial resolution < 15µm
- Power < 200 mW/cm²
- Time precision < 100 ns
- Trigger at 30kHz average frequency with 5-10 µs latency



- 464 rows and 896 columns
- Overall sensor dimensions around 30.2x18.8 mm²
- Pixel pitch 33x33 µm²
- Main design is based on the **TJM2** chip

The OBELIX Block Diagram



Analog

- Pixel matrix adapted from **TJM2**
- Column drain architecture
- Monitoring ADC
- Temperature sensors

Power pads

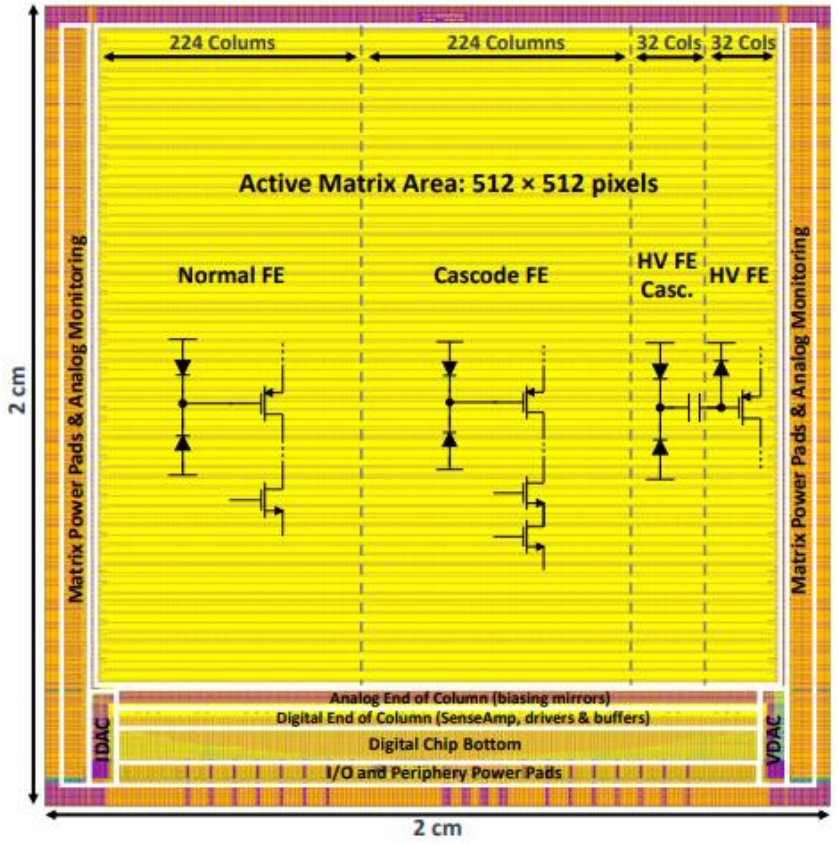
- Power regulators added
- Simplified system integration

Digital Periphery

- Main clk-in: 170MHz
- New end-of-column adapted to Belle II trigger
- Timestamped hits stored in memories
- Read-out when timestamp matched with trigger
- Single output at 340 MHz average bandwidth
- RD53 control/readout protocol

The pixel matrix of OBELIX

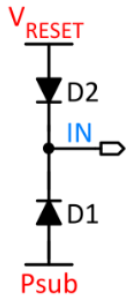
- The OBELIX sensor inherits the performance of the pixel matrix from TJM2 sensor
- The same pitch, 33 × 33 µm², with the same layout for the analog and digital parts
- The Matrix pixel of TJM2 is composed of 4 pixel flavors with differences in the Front-End (FE) amplifier and detector input coupling (AC or DC):
  - Normal FE / Cascode FE
  - HV Cascode FE / HV FE
  - **Based on current characterization and simulation results, 2 FE flavors are chosen for OBELIX on equal area:**
    - **Cascode FE**
    - **HV Cascode FE**



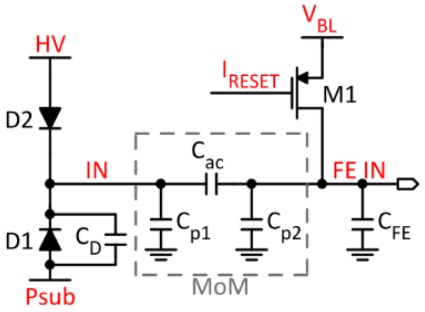
Floorplan of TJM2 sensor

The analog FE design

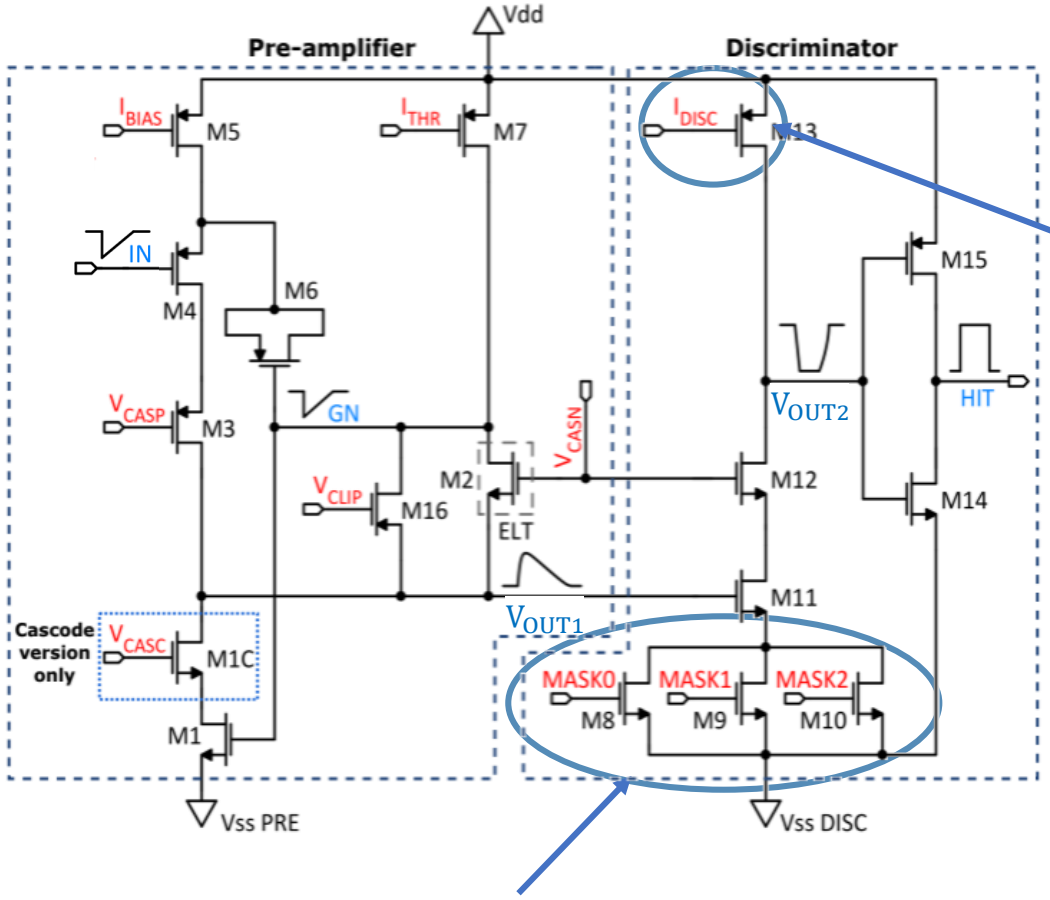
- Two flavors with a cascode pre-amplifier :
  - With an input **DC-coupling** using a forward biased diode **(Cascode FE)**
  - With an input **AC-coupling** allowing higher bias voltage above 30V (**HV Cascode FE)**



Input DC-coupling

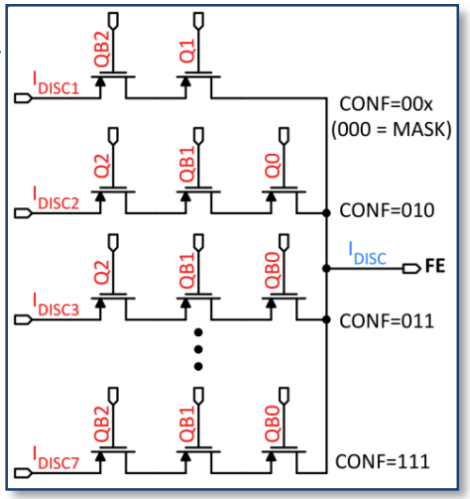


Input AC-coupling



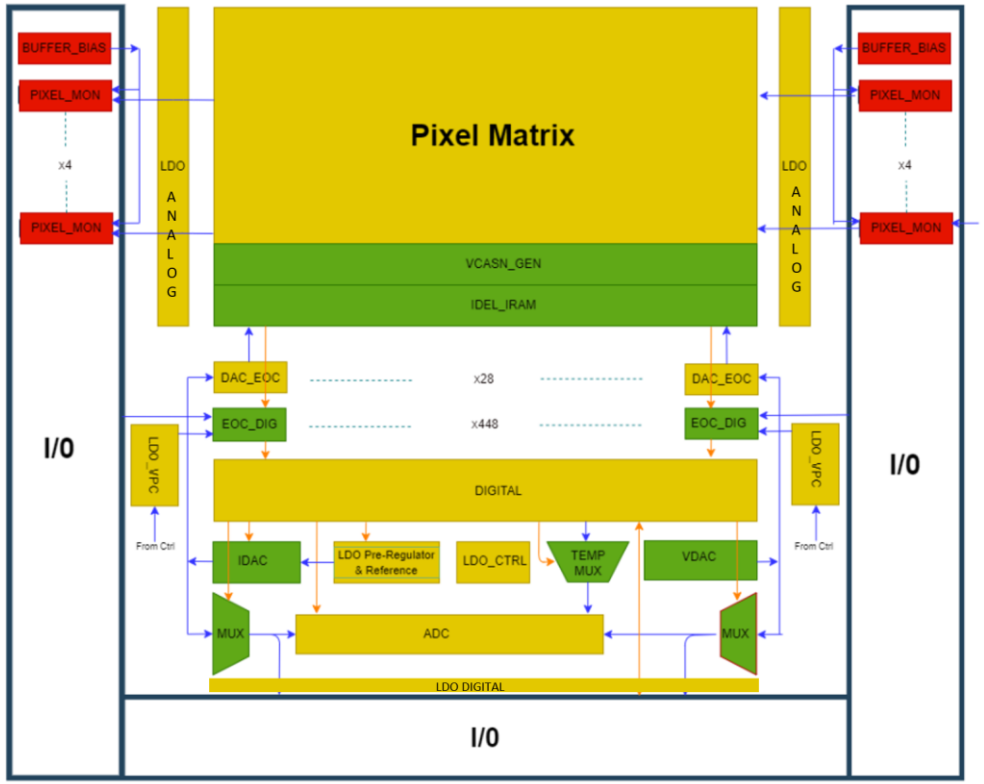
Individual pixel masking

3-bit Threshold Tuning DAC



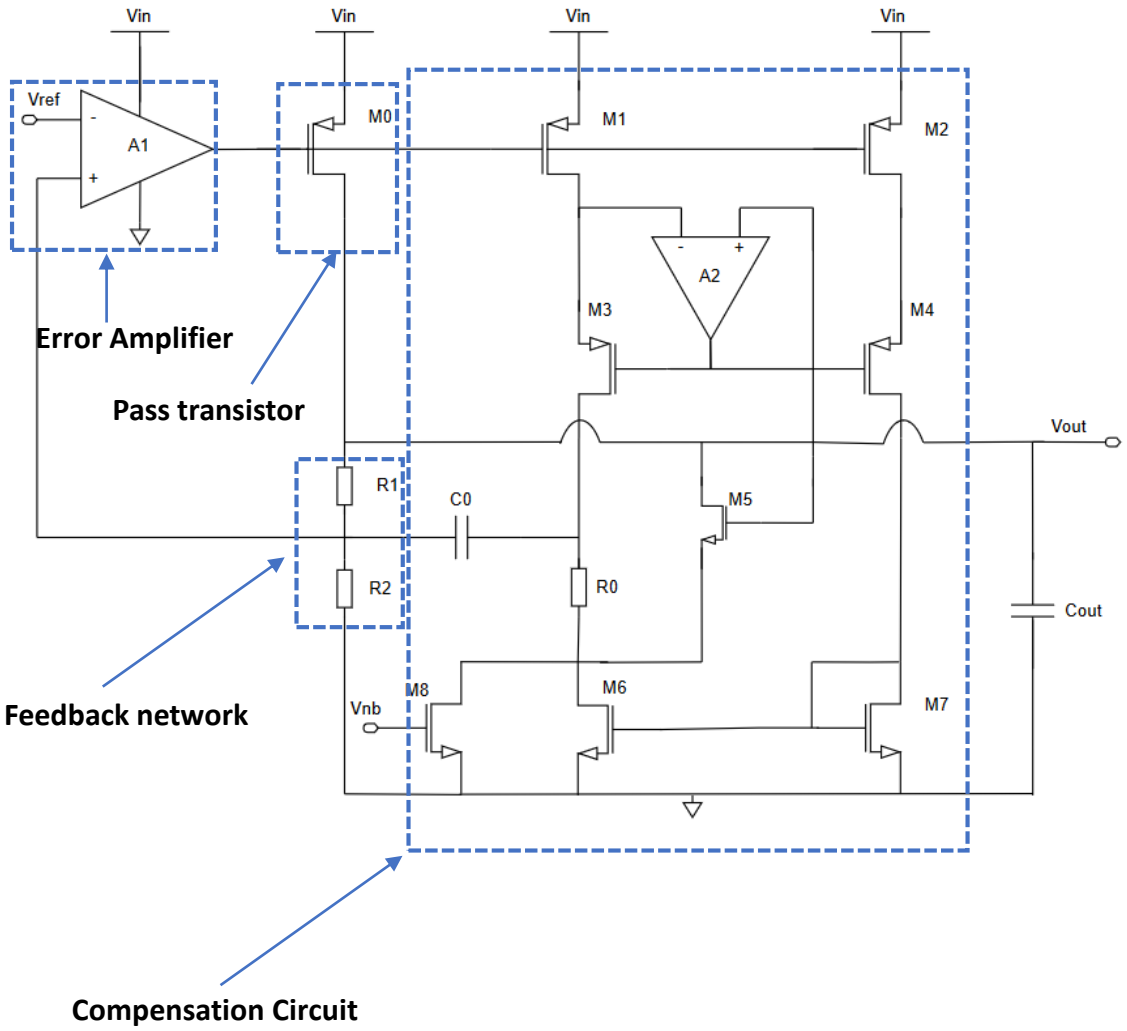
- A 3 bit threshold tuning is available at the pixel level to reduce the threshold dispersion

The OBELIX Power management



- Power distribution is a major concern as OBELIX is larger than TJM2, leading to performance degradation
- Long linear ladders ⟹ voltage drop across ladder
- On chip regulators are being developed in OBELIX to compensate the voltage drop and minimize the material budget dedicated to power distribution:
  - Two analog **LDO (Low Dropout)** regulators will be implemented to supply the matrix from both sides
  - A digital LDO in the bottom side of the chip to supply the digital blocs
  - A preregulator to supply LDO references generator
  - A VPC (Voltage pre-charge) LDO to reset and recharge bit-lines between each read cycle

The LDO regulator design



- Wide input supply voltage range of 2V to 3V
- Each LDO generates the output voltage of 1.8V ± 10% necessary for the technology to power the chip through the pass transistor M0
- Maximum load current of 500mA
- A compensation circuit is designed to ensure a stable output voltage

☑ Circuit is working within specifications

☑ Layout is done

➡ Final verifications are on going

Summary and next steps

- The SuperKEKB collider is considering a major upgrade to reach a high luminosity
- Reaching the target peak luminosity requires an upgrade of the interaction region and the Vertex Detector
- A new DMAPS VTX is foreseen to improve the performance of the Belle II vertex detector
- The OBELIX sensor based on TJM2 chip with TJ180 nm technology is under development with additional features all on-chip
- Lab testing and TB campaigns on TJM2 to validate key performance crucial for OBELIX design: **Good agreement between the measurements and simulations**

- **Next steps:**
  - Continuation of LDO design, verification and integration into the OBELIX chip which will be submitted in 2025
  - Involvement in characterization and testing of the TJM2 Chip
  - Participation in Beam Tests related to the TJM2 chip, scheduled in 2025

Thanks for your attention

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