

HGCROC Pedestals

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Procedure

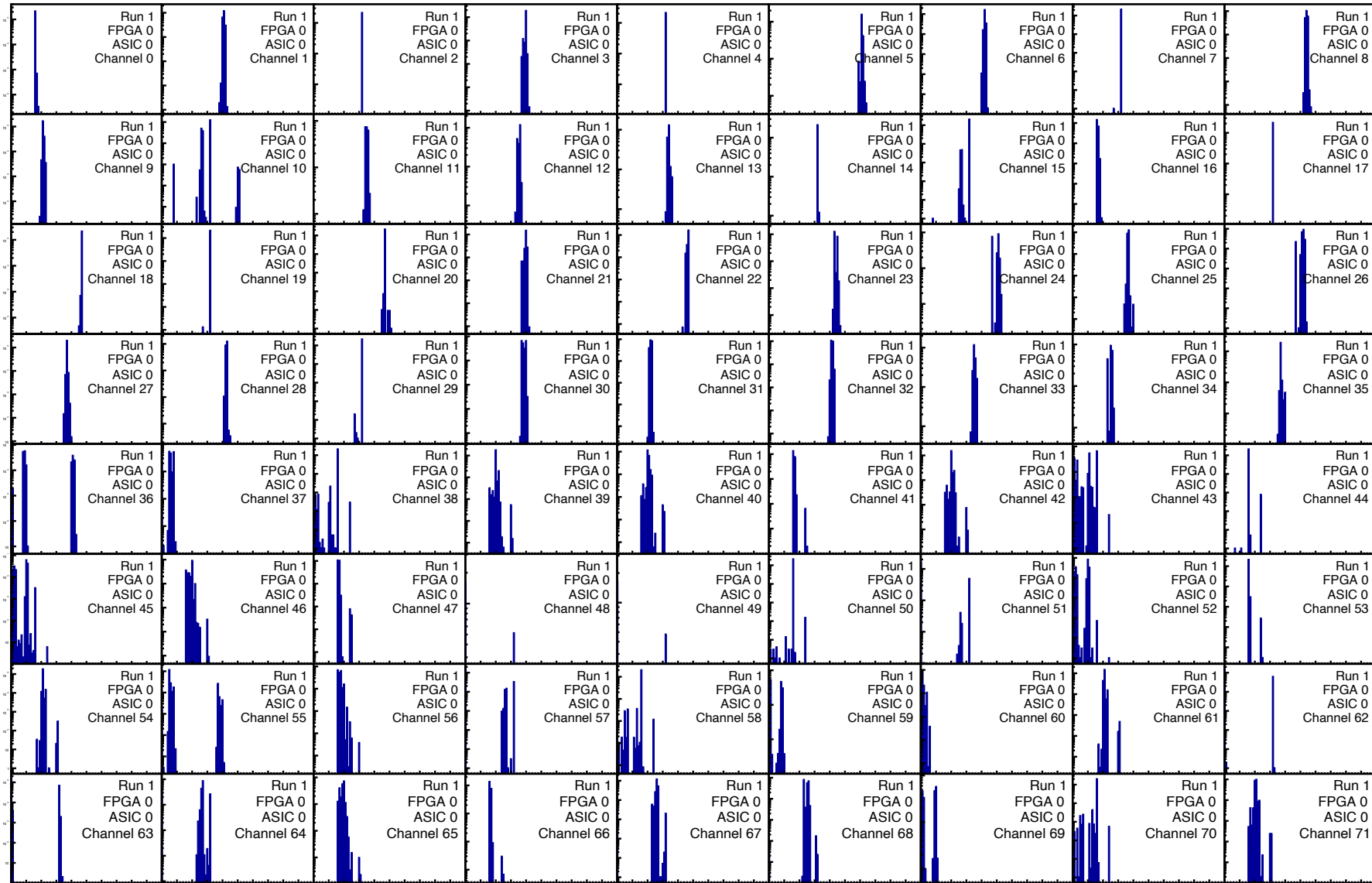
- I used ASIC 0 on FPGA 0 for these tests
- The 16 SiPM in parallel readout was attached
- Gain conveyor was switched off
 - GlobalAnalog ON_conv=0
 - GlobalAnalog gain_conv=0
 - All channel gain_conv=0
- Set inv_vref and noinv_vref
 - Inv_vref=650
 - Noinv_vref=850

Pedestal Scan

- Created config files for trim_inv values between 0 and 63
- Took 10,000 pedestal events (bias off, using config page) for 9 values
- Plotted each channels ADC spectra
 - X-axis: (0, 100) adc

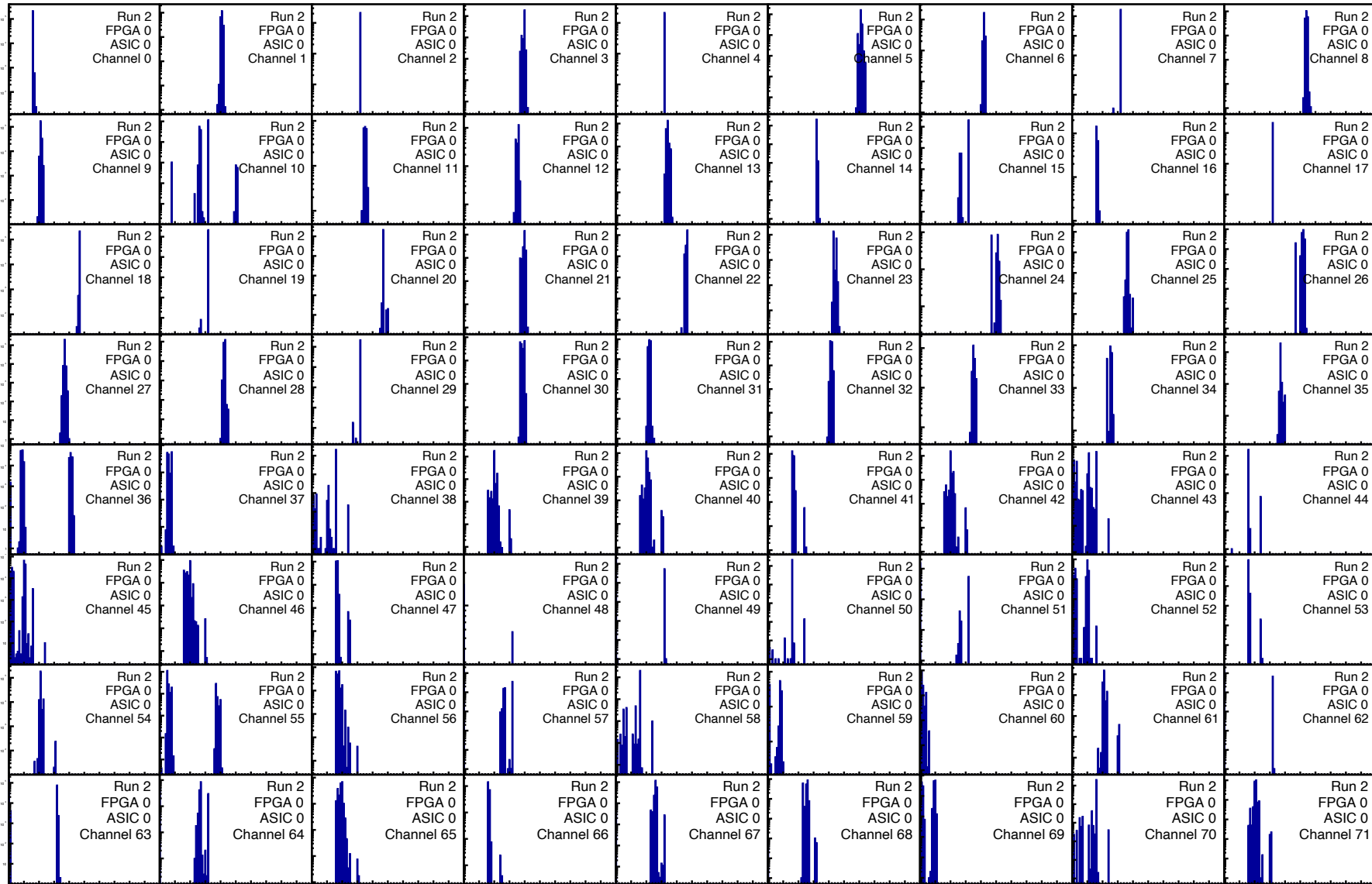
Run	Trim
1	0
2	7
3	15
4	23
5	31
6	39
7	47
8	55
9	63

Run 1, Trim 0



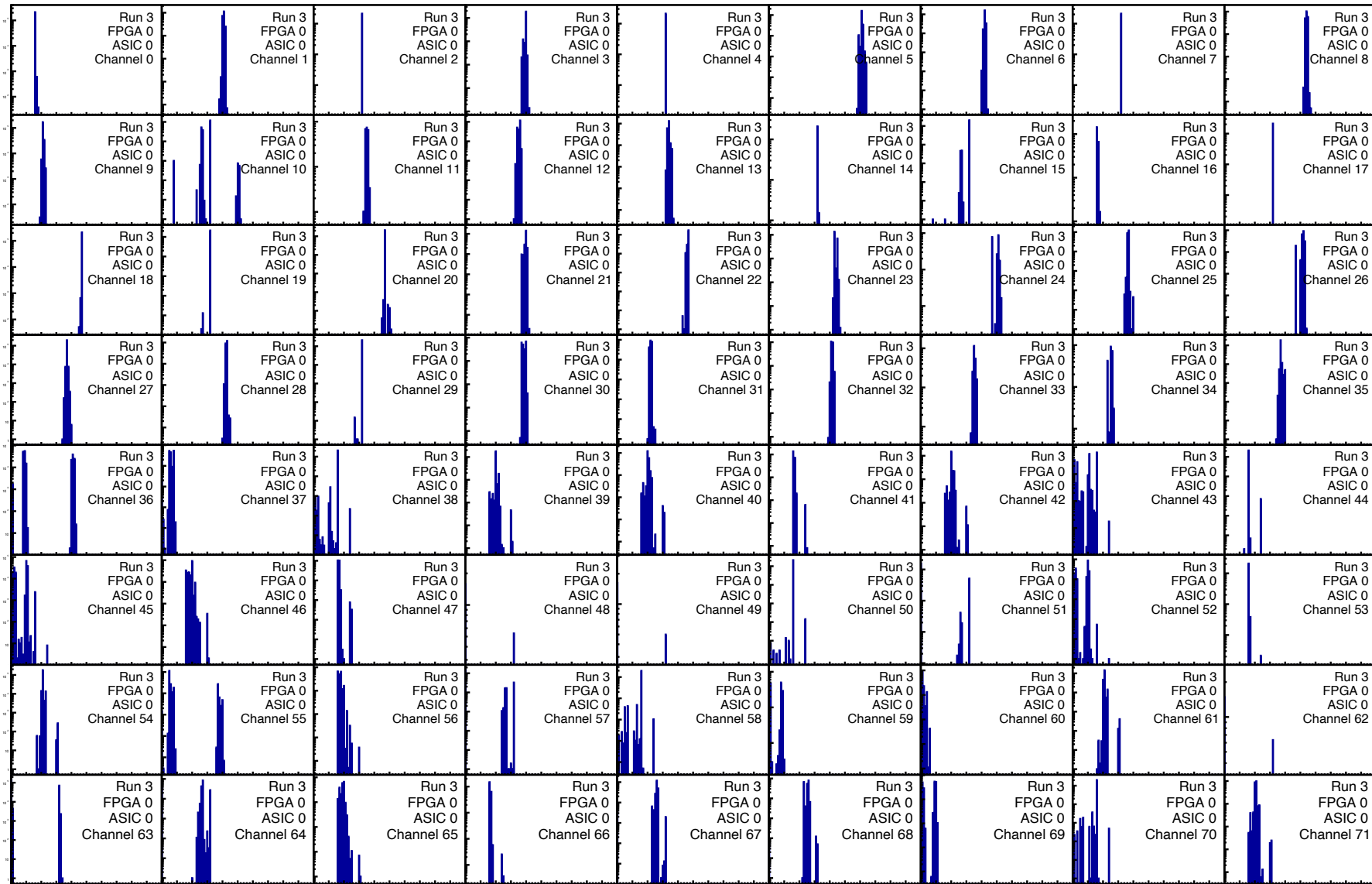
Adc 0 100

Run 2, Trim 7



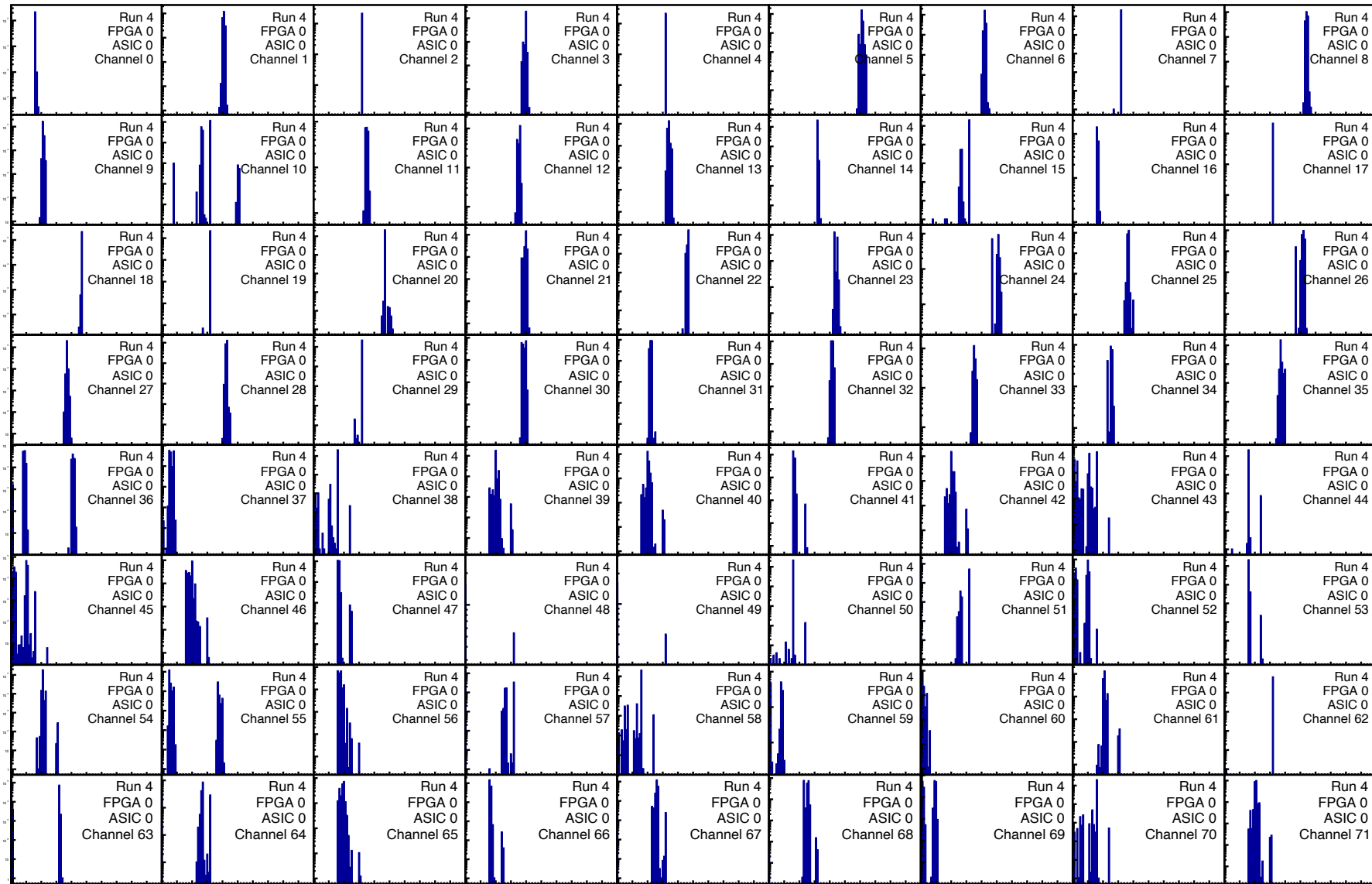
Adc 0 100

Run 3, Trim 15



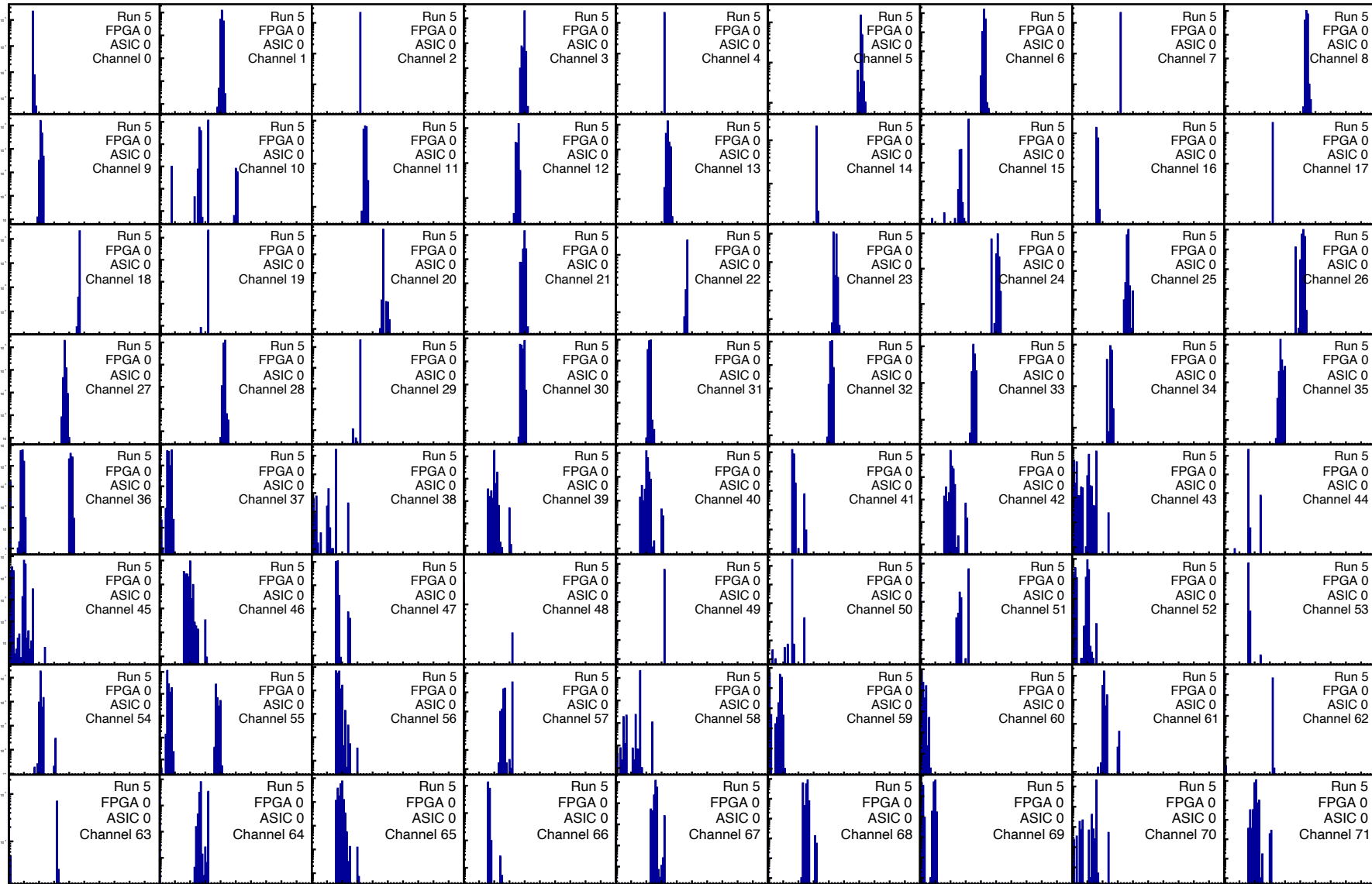
ADC 0 100

Run 4, Trim 23



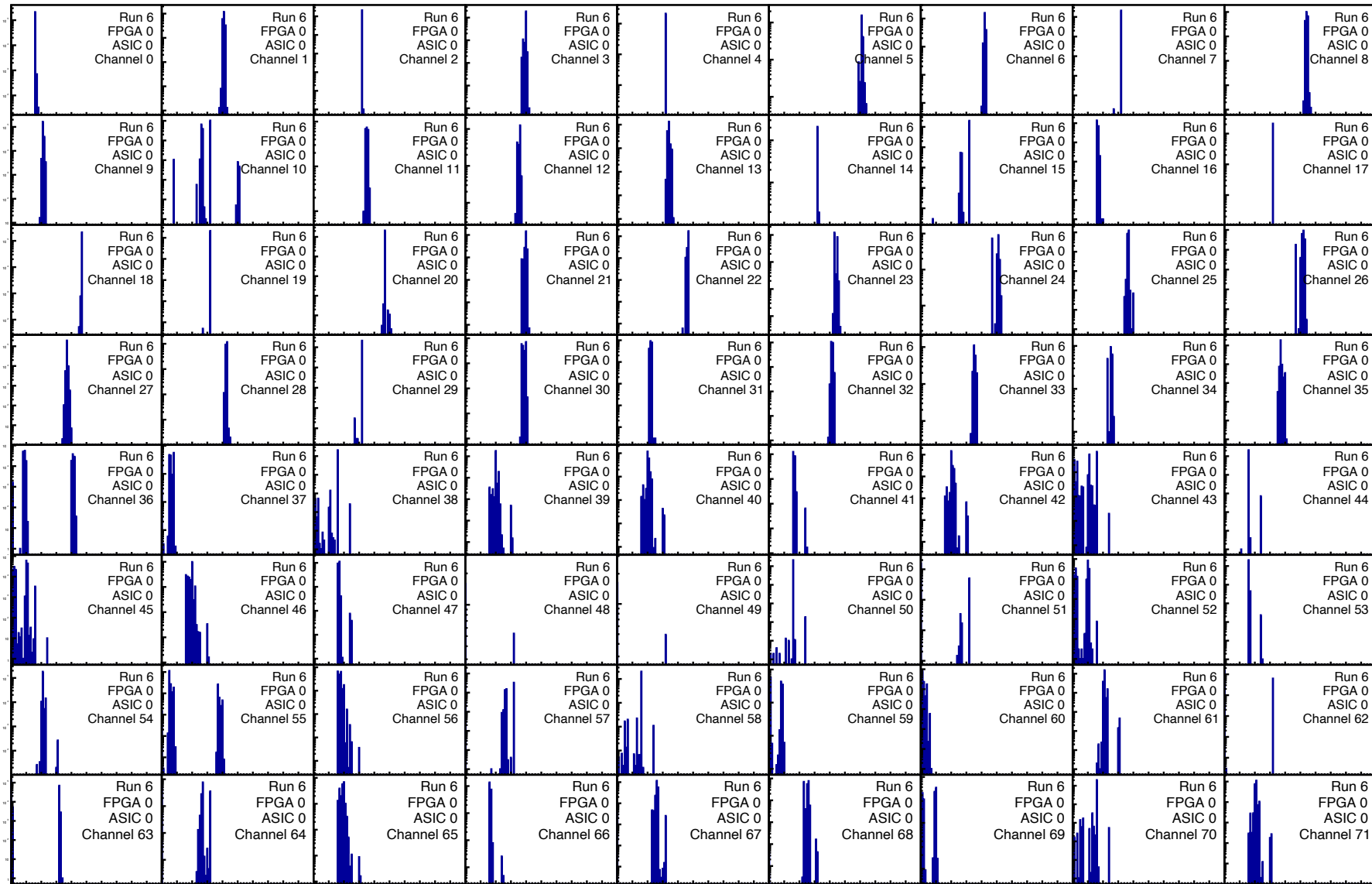
ADC 0 100

Run 5, Trim 31



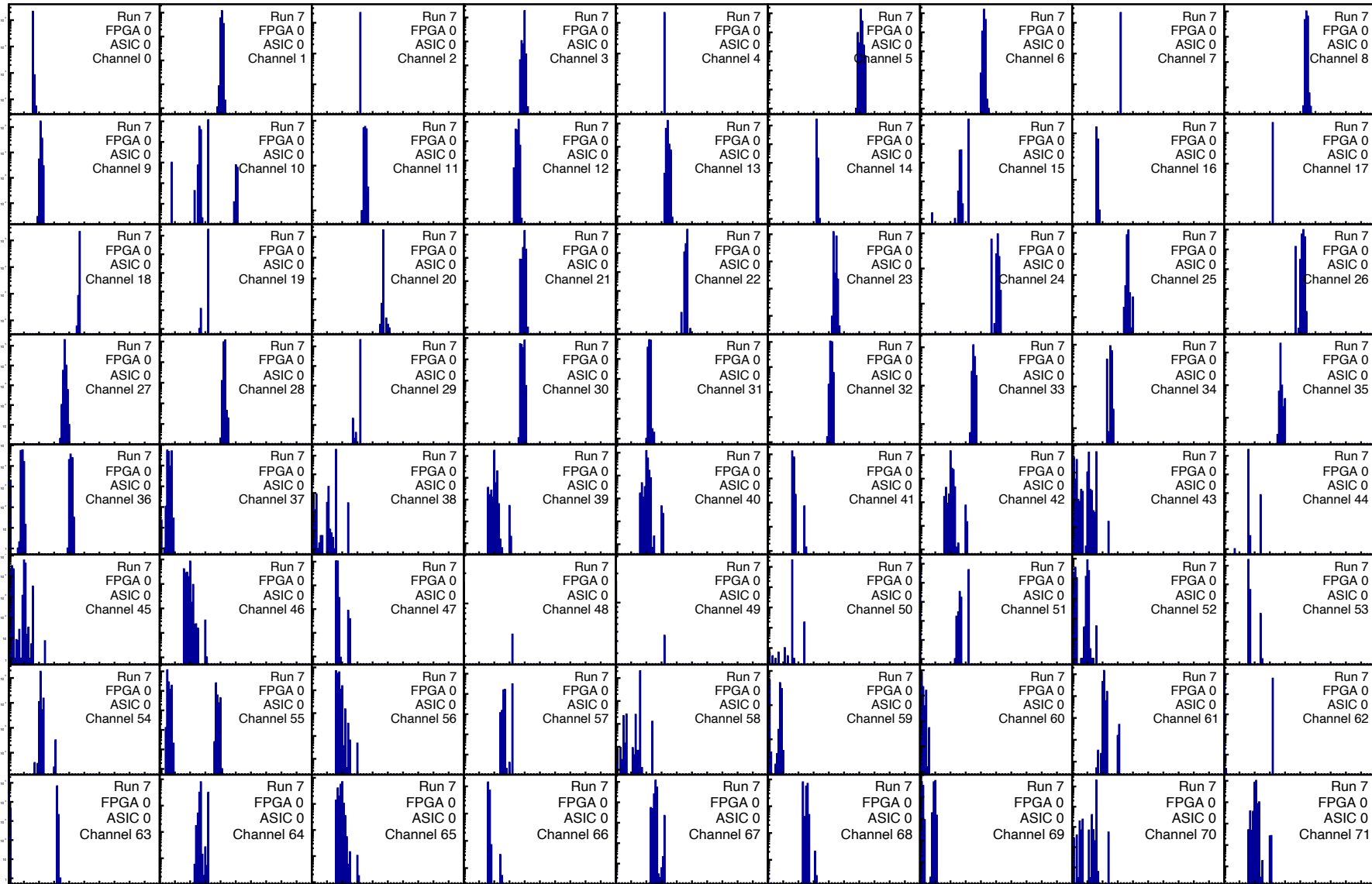
ADC 0 100

Run 6, Trim 39



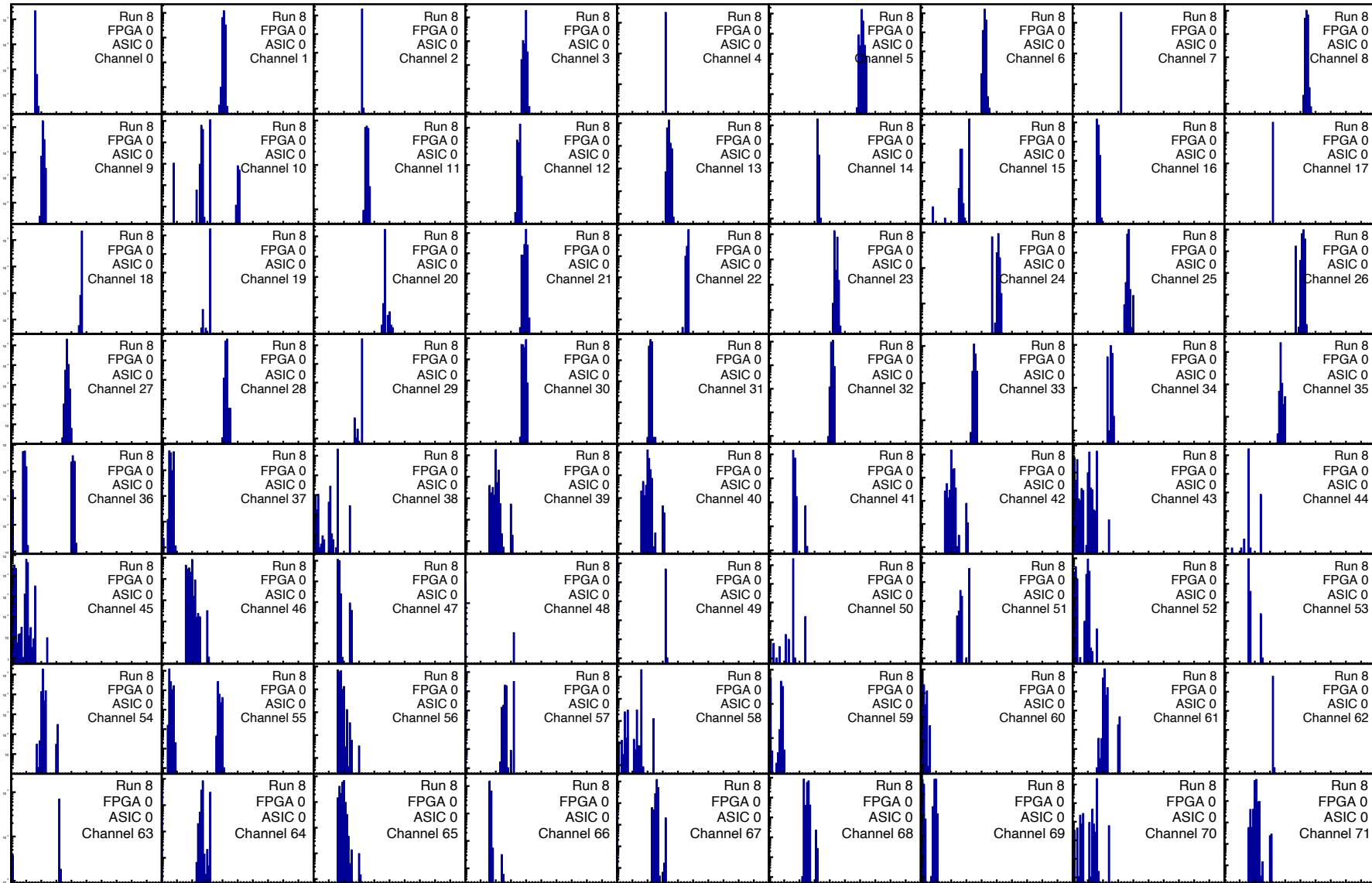
ADC 0 100

Run 7, Trim 47



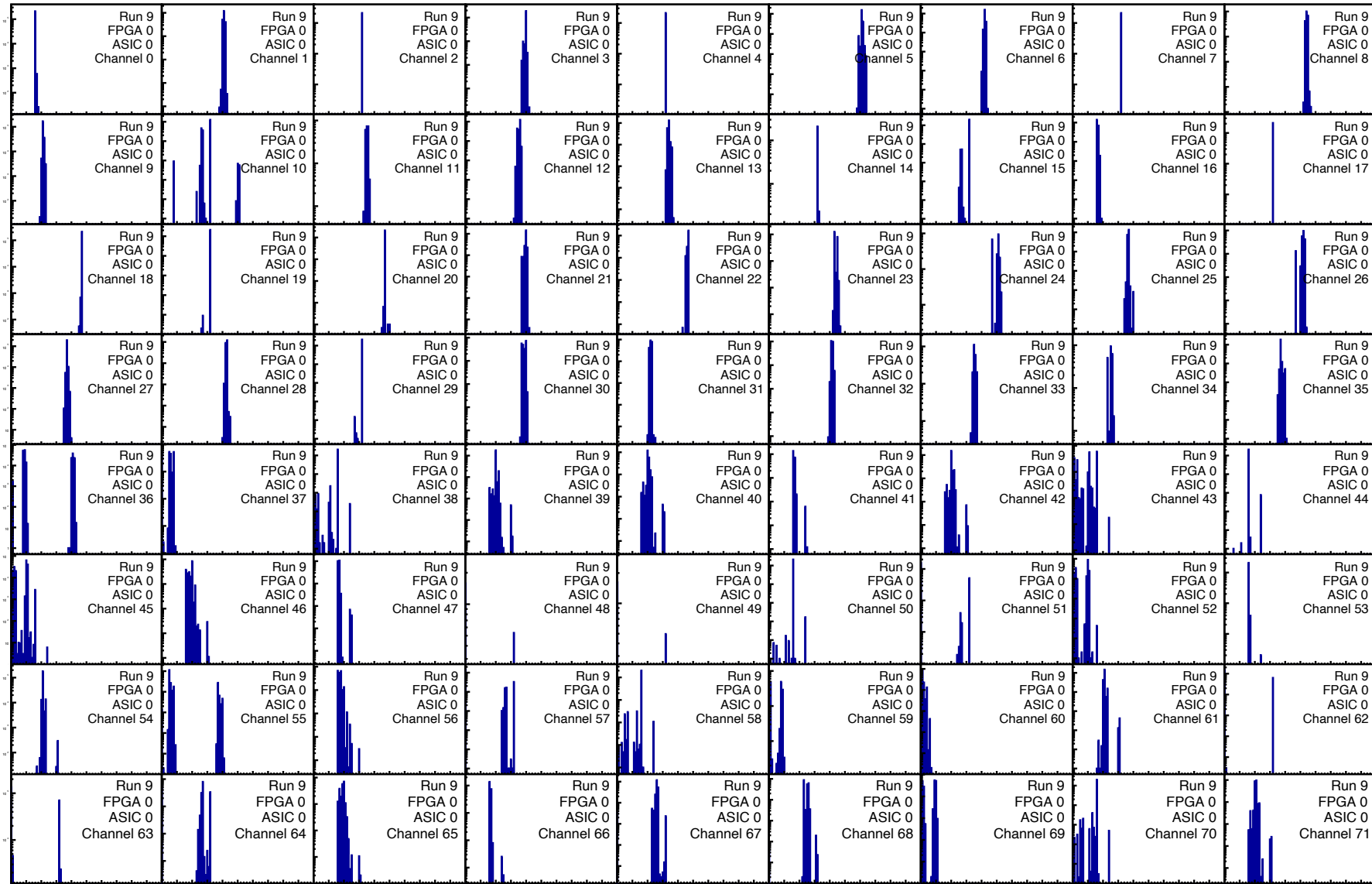
ADC 0 100

Run 8, Trim 55



Adc 0 100

Run 9, Trim 63



Adc 0 100

Questions

- The goal of this step is to minimize the dispersion, but I don't see any difference between trim_inv values
- What did we expect to see?