The commissioning and operational experience of LHCb Upstream Tracker

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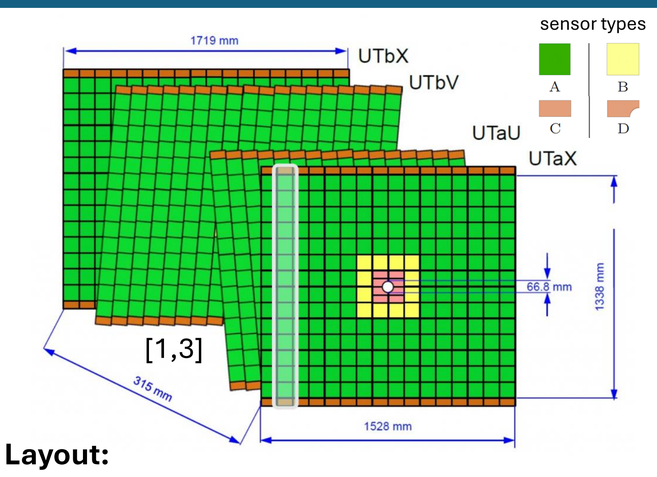
Upstream Tracker of LHCb

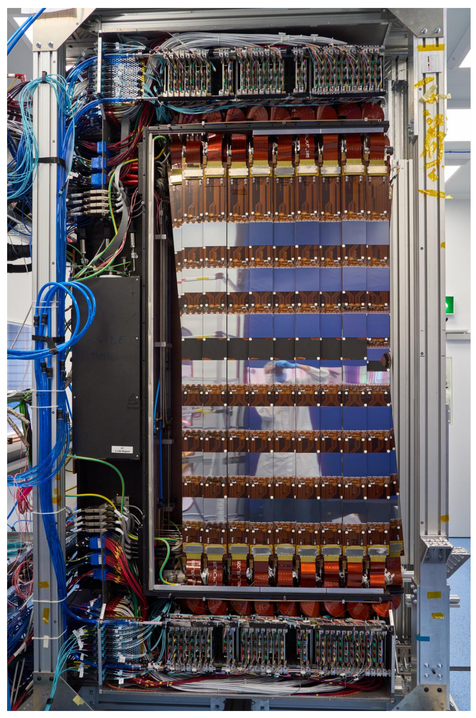


Layout:

- 536,576 silicon strips, organised in 4 planes and 68 vertical staves.
- 4 sensor types, 128-channel readout with SALT ASIC [2], 6-bit amplitude resolution.

Aims:

- Crucial for the new purely software trigger (ghost track reduction, faster track reconstruction).
- Track reconstruction of low-momentum particles and decay products of long-lived particles.

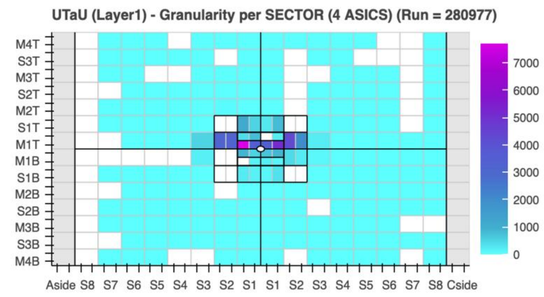


The UT box in the open position with visible staves, hybrids and PEPI box [4].

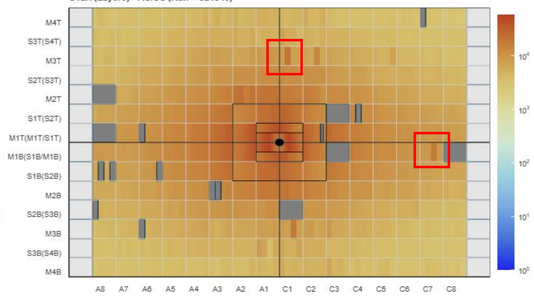
Commissioning of UT

Several obstacles were overcome during the commissioning of the UT:

- **Loss of ASICs configuration** by unstable clock signal received by the ASICs, related to the time fast control (TFC) sequence. The mitigation strategy was implemented by constant assertion of at least 1 of the 8 bits of the TFC command every clock cycle.
- **UT box imperfections** → higher humidity in the box prevented cooling to the optimal temperature. The mitigation strategy was to seal the box better.
- **Single event upsets** due to radiation produced during collisions at LHC → misconfiguration of ASICs due to flip of register bits. Mitigation strategy implemented in the detector control system.



First data collected by LHCb during the 2023 Pb-Pb collisions with the UT.

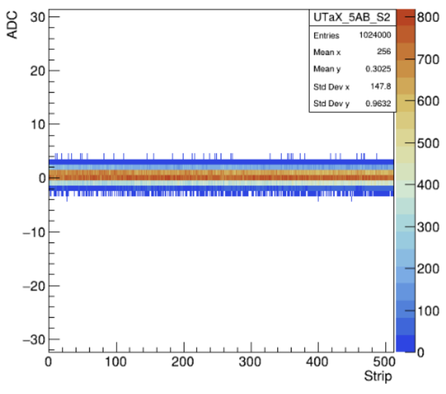


UTaX hit map with noisy ASICs after SEU, before the implementation of the mitigation strategy.

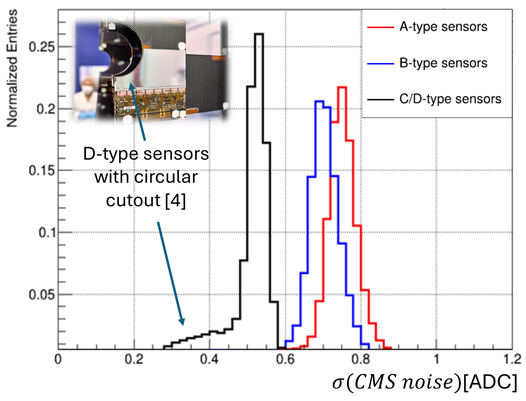
Calibration of UT

Precise calibration of the UT is required to efficiently distinguish particles' signals from noise during collisions at LHC. A dedicated VETRA software package [5] is used to perform a series of electronic calibration scans taken during no-beam time at LHC. The main components of the detector calibration covered by Vetra are:

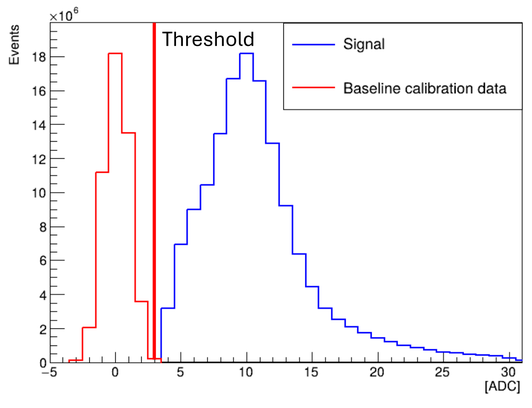
- **Analogue calibration:** precise baseline calibration using an 8-bit trim DAC register.
- **Digital calibration:** complementary baseline calibration using 6-bit pedestal register.
- **Hit thresholds calculation** based on common mode subtracted (CMS) noise level.
- Determination of noisy and faulty channels.



Distribution of ADC vs strip number for one UT hybrid taken during calibration scan after analogue (trimDAC) and digital (pedestal) calibration.



Distribution of $\sigma(noise)$ of all UT channels with the breakdown for sensor type: A-type sensors (4 ASICs), B-type (8 ASICs) and C/D-type (8 ASICs and half-length of A-type sensor + cutout for the beampipe).

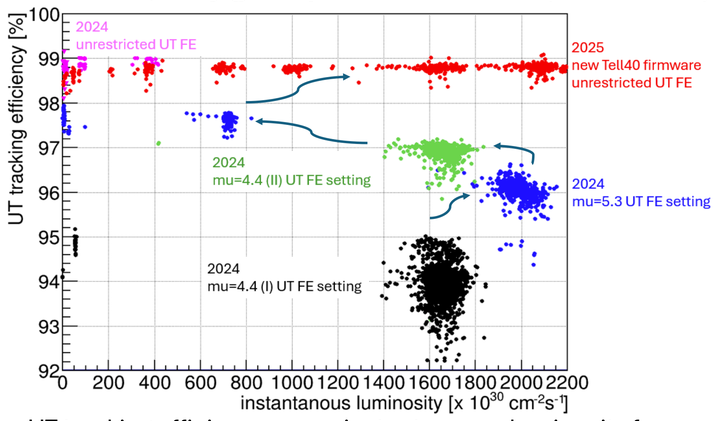


Comparison of the distribution of ADC from a physics data sample and a calibration sample for a fully calibrated detector with an indication of the discrimination threshold.

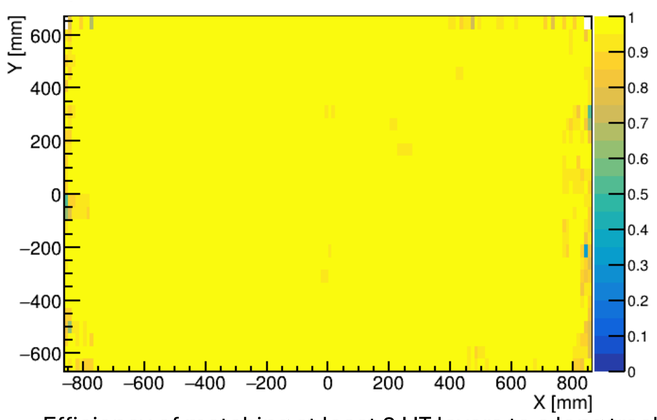
Performance across Run 3

Evolution of FE-settings and their impact on UT performance during Run 3:

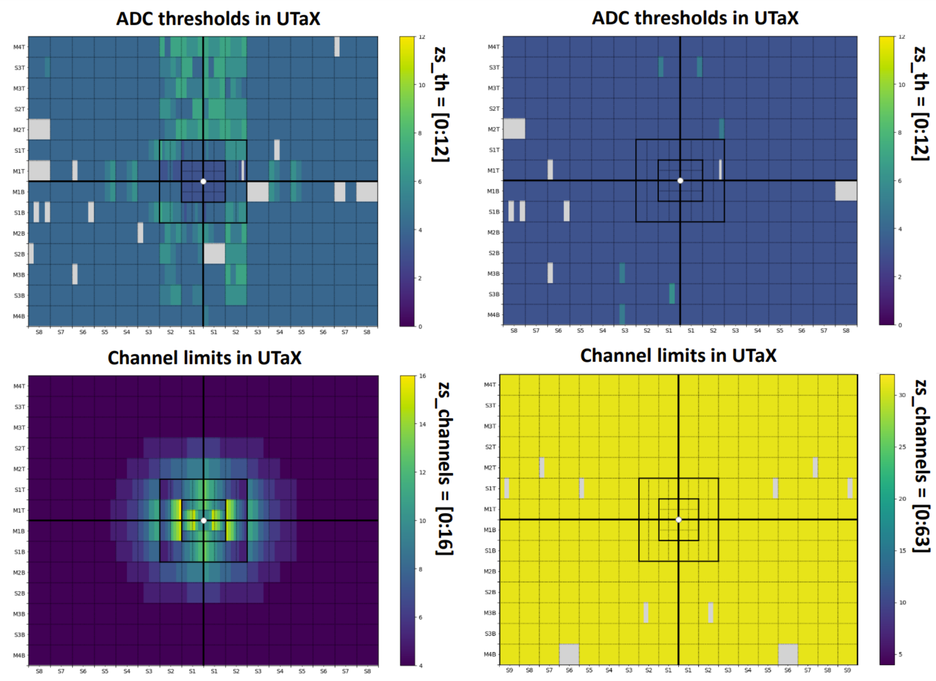
- The initial problem was the limited bandwidth of some readout boards.
- The hit rate from some ASICs was much higher than expected.
- The large hit rate asymmetry observed from some ASICs within the same readout board led to data truncation due to the protection mechanisms of the firmware.
- **2024 Mitigation strategy** – options to restrict hit rate:
  - increase ADC thresholds → removes smaller signals, high impact on signal efficiency, only as needed;
  - impose a hit limit for each ASIC → remove high ASIC-occupancy events, less harmful to physics;
  - settings were optimised iteratively for different pile-up (mu = 4.4, 5.3).
- **2025 Solution** – firmware improvement (optimisations of Finite State Machines) + decrease of sensor noise by lowering the temperature in the box. Implemented in early 2025.
- **96.3%** channels active.
- **Overall, very good performance**: Eff(>=3 UT hits)/track improved from ~93.5% in 2024 to ~**98.7%** in 2025.



UT tracking efficiency vs run instantaneous luminosity for different years of data taking and pile-up.



Efficiency of matching at least 2 UT layers to a long track as a function of track intersection with UT 4th layer.



- **Proton physics 2024:**
  - Top: Higher ADC thresholds for the problematic regions.
  - Bottom: Imposed limits on #hits for the outer region of the detector. Loose setting for the inner region to save physics events.
- **Proton physics 2025:**
  - Almost unrestricted ASIC settings thanks to firmware improvements.

Conclusions

- Long road from commissioning the detector to running with full operational efficiency at nominal conditions.
- We found that early firmware development and commissioning are essential to detect possible issues during the operation of the whole detector and data taking under nominal conditions.
- We observed a significant impact of the proper Front-End calibration on detector stability and efficiency.
- Ongoing firmware development for further improvement of the detector stability.

[1] CERN-LHCC-2014-00, LHCb Tracker Upgrade Technical Design Report
[2] Beteta, C., et al., The SALT-Readout ASIC for Silicon Strip Sensors of Upstream Tracker in the Upgraded LHCb Experiment, Sensors 22 (2021) 107
[3] The LHCb upgrade I - Aaij, Roel et al - LHCb-DP-2022-002
[4] Brice, Maximilien, LHCb Upstream Tracker (UT) in clean room, 2022, https://cds.cern.ch/record/2823998
[5] Krupa, W. (2025). VETRA software package, https://doi.org/10.5281/zenodo.15370799

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