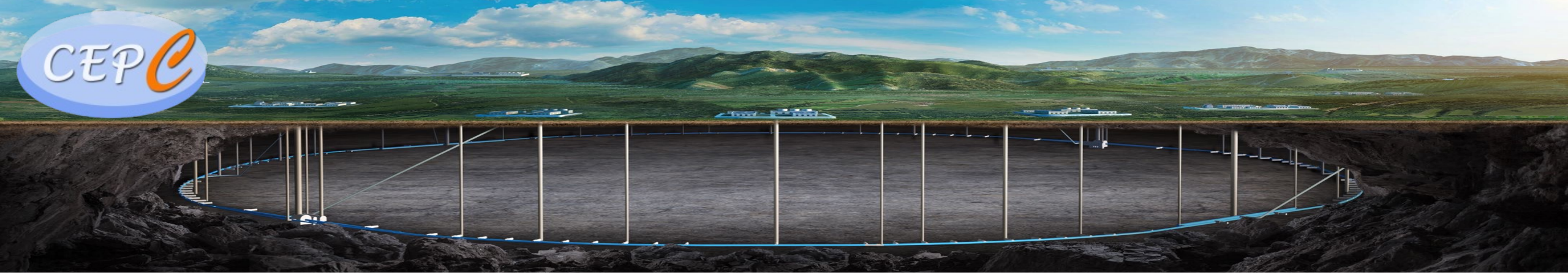


CEPC Silicon Inner Tracker and Timing Layer Detector R&D

Qi Yan

On behalf of the CEPC Silicon Tracker Group

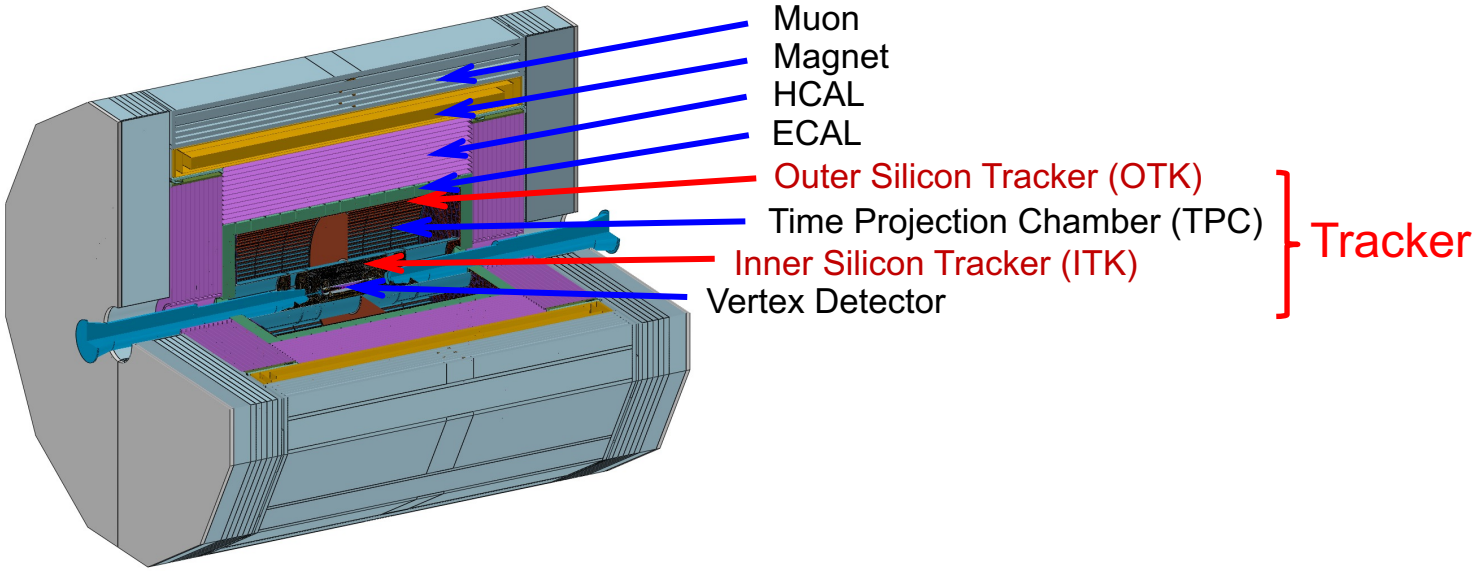
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

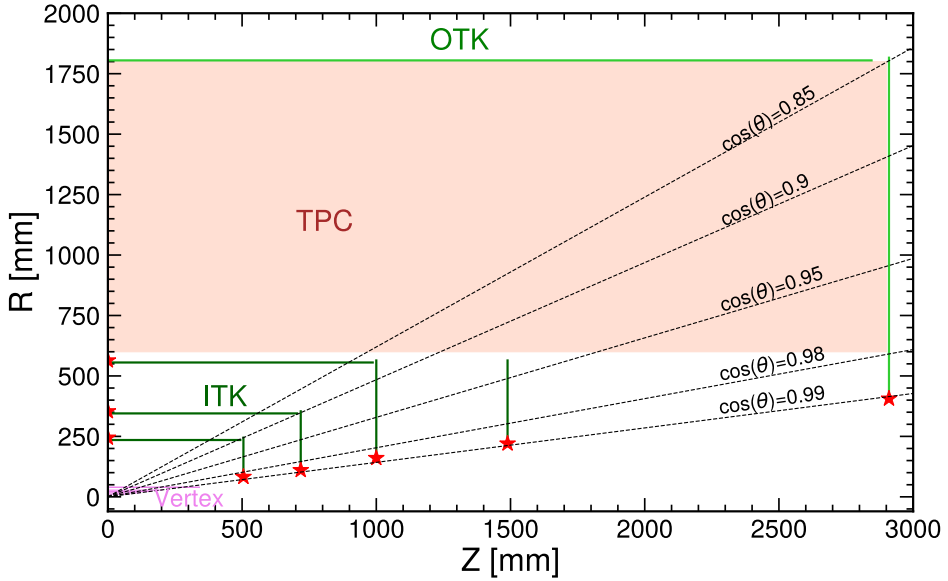
Introduction

- The CEPC tracker system includes several detectors: the Vertex Detector, Inner Silicon Tracker, Time Projection Chamber (TPC), and Outer Silicon Tracker. My presentation will focus on the CEPC Inner Silicon Tracker (ITK) and Outer Silicon Tracker (OTK).

- The ITK employs advanced CMOS sensor technology to achieve precise position measurements for accurate particle trajectory determination.

- In addition to position measurement, the OTK integrates the AC-LGAD semiconductor detector for precision time measurement of charged particles, significantly enhancing particle identification capabilities.

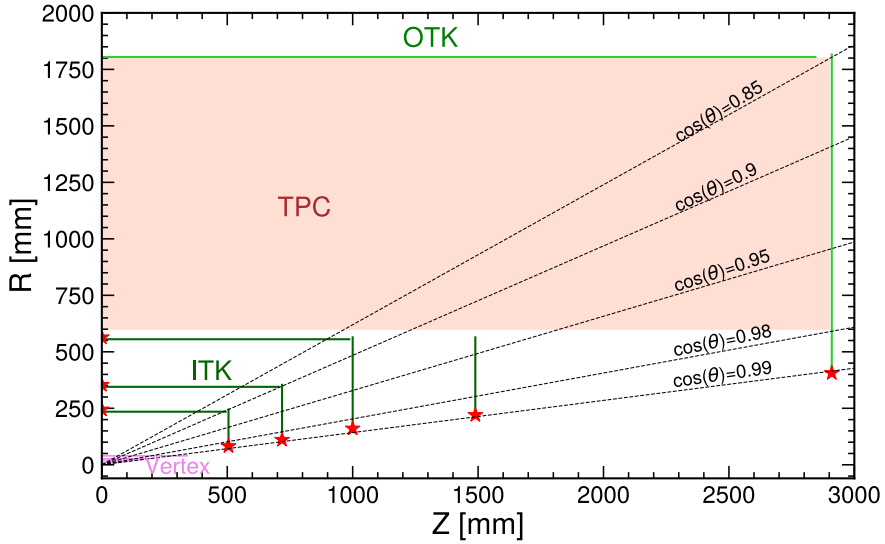




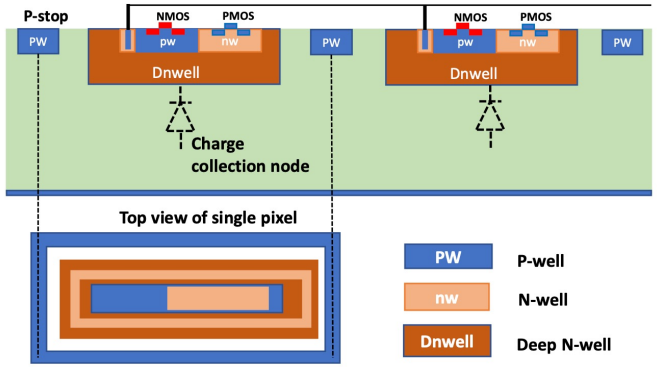
- The CEPC overall track momentum resolution requirement: ~0.1% for momenta below 100 GeV/c.

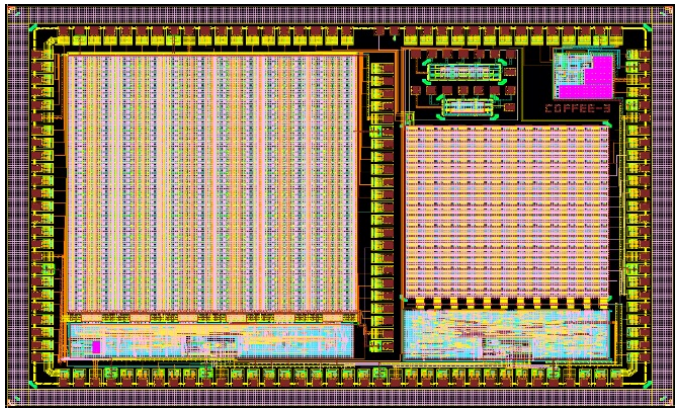
Baseline Configuration of Sensor for CEPC ITK

- Monolithic HV-CMOS pixel sensor:
  - Large depletion depth (full depletion) and large signal.
  - Good timing resolution (a few ns) to tag 23 ns bunches .
  - Radiation hard.
  - Low materials.
  - Cost effectiveness.



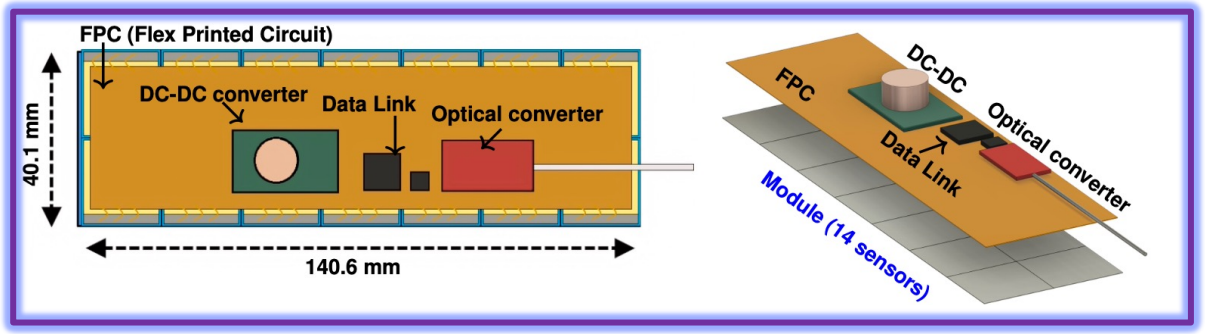
- Key parameters of HV-CMOS pixel sensor for CEPC:
  - Process node: 55 nm
  - Chip size: 2 cm × 2 cm
  - Sensor thickness: 150 μm
  - Array size: 512 rows × 128 columns
  - Pixel size: 34 μm × 150 μm
  - Spatial resolution: 8 μm × 40 μm
  - Time resolution: 3-5 ns
  - Power consumption: 200 mW/cm^2

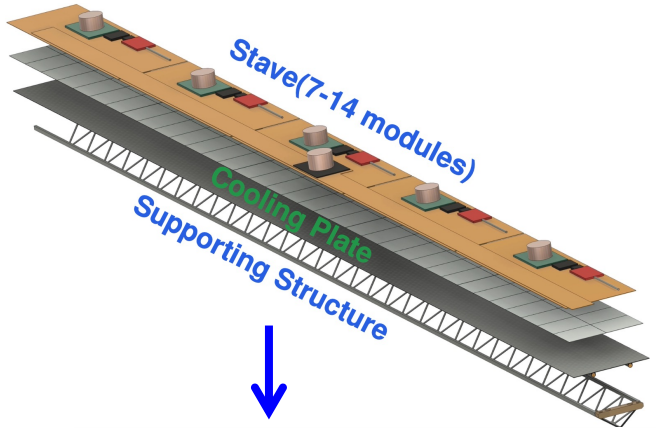




Latest HV-CMOS COFFEE3 chip (submitted for tap-out in Jan 2025)

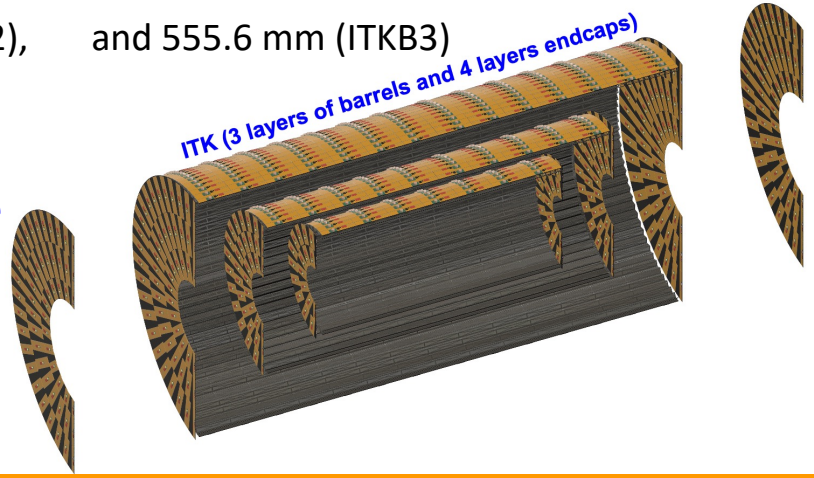
CEPC ITK Barrel Design with HV-CMOS Pixels

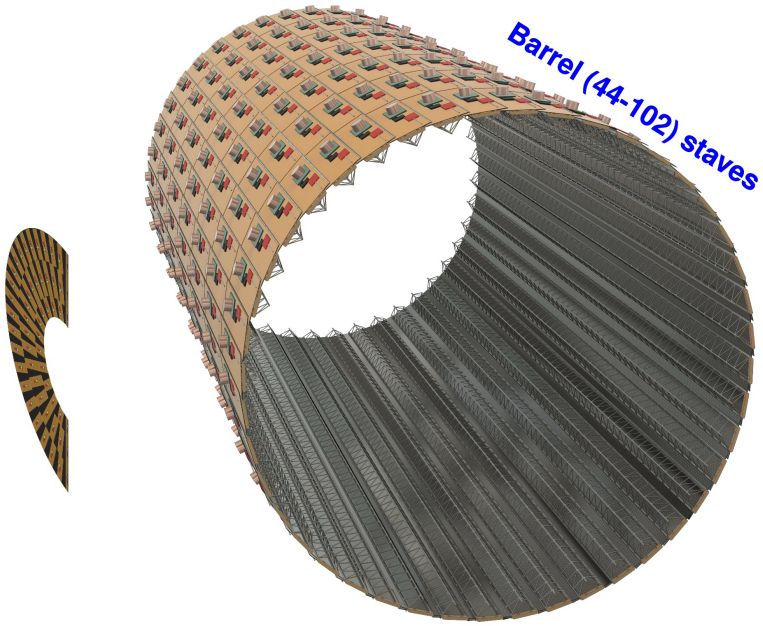




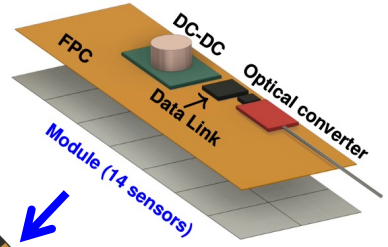
- HV-CMOS pixel sensor:
  - Sensor size: 20 mm × 20 mm
  - Pixel size: 34 μm × 150 μm (spatial resolution: 8 μm × 40 μm)
- Module:
  - 14 sensors (2 rows × 7 columns)
  - Module dimensions: 140.6 mm × 40.1 mm
- Stave length: 986.6 mm (ITKB1), 1,409.6 mm (ITKB2), and 1973.2 mm (ITKB3)
- Barrel radii: 235 mm (ITKB1), 345 mm (ITKB2), and 555.6 mm (ITKB3)

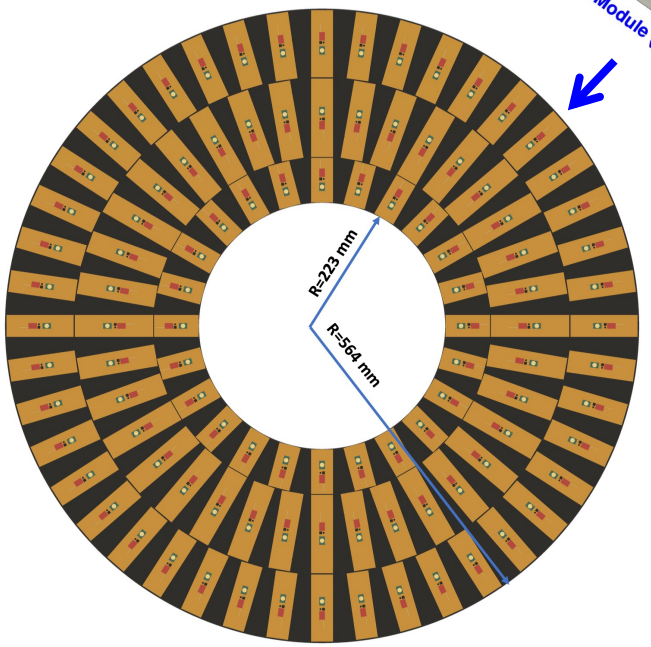
The designed 3 ITK barrel layers has a total surface area of 13 m², including 33,264 sensor chips, with a power consumption of ~27 kW.

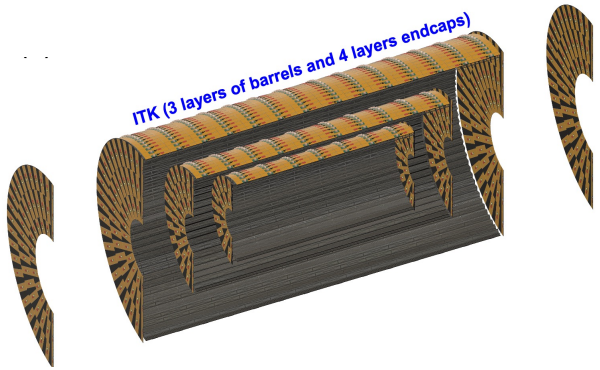




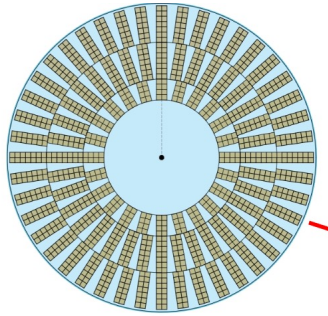
ITK Endcap Design with HV-CMOS Pixels



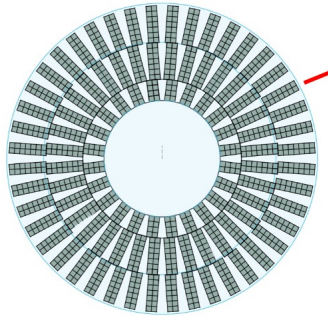




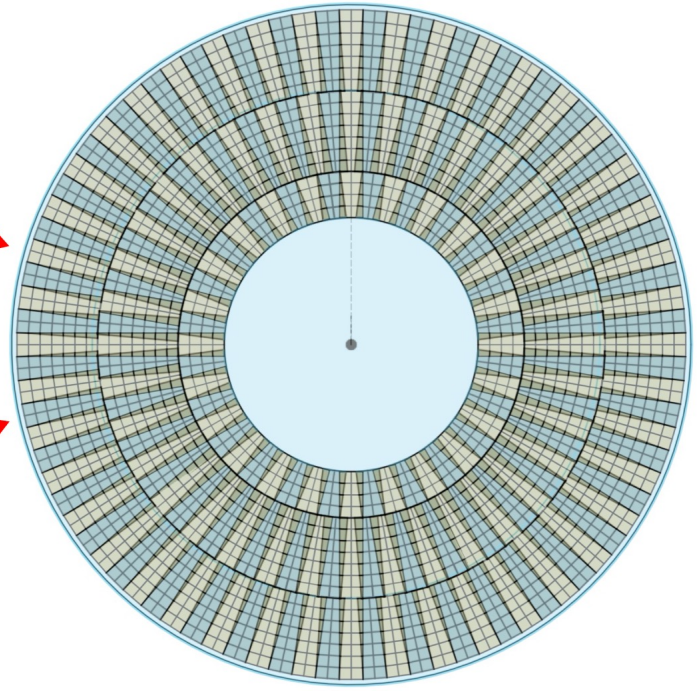
- Module:
  - 3 types of modules : 8, 12, and 14 sensors for all 4 pairs of ITK endcaps
- Endcap active area radii:
  - 81.5 mm<r<242.5 mm (ITKE1), 110.5 mm<r<352.3 mm (ITKE2), 163 mm <r<564 mm (ITKE3), and 223 mm<r<564 mm (ITKE4)



Front view of endcap



Back view of endcap



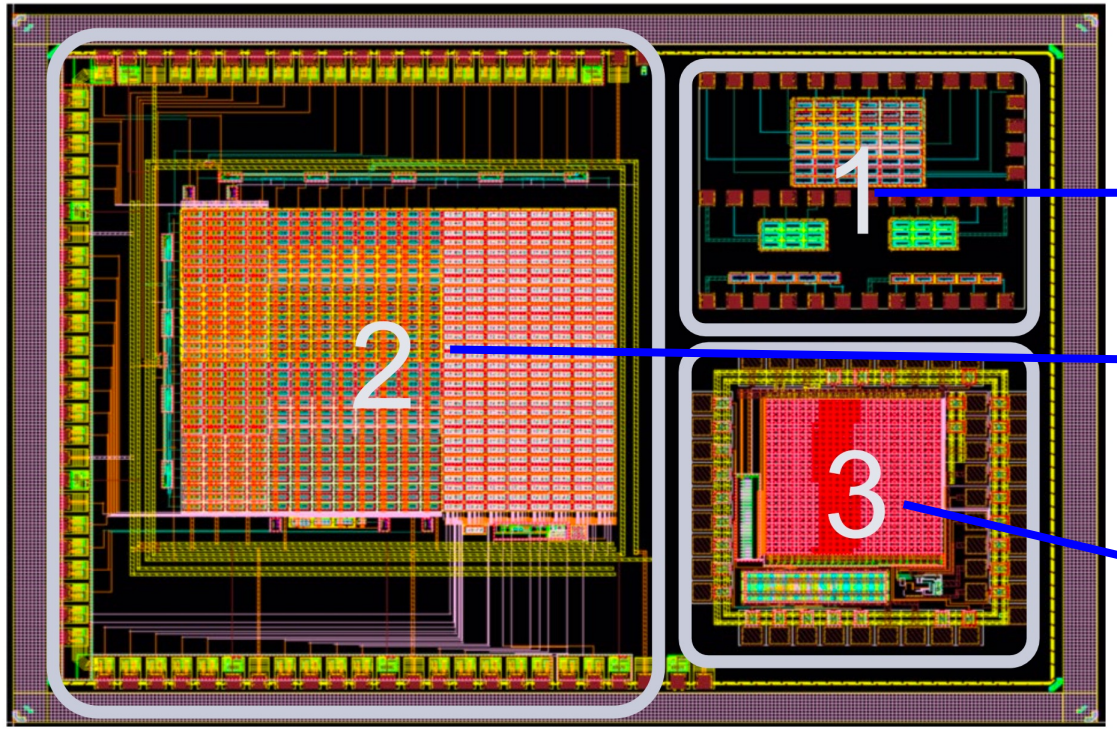
Perspective view of full endcap

Each ITK endcap features double-sided detection. Four pairs of ITK endcaps have a total surface area of 5.5 m², including 13,760 sensor chips, with a power consumption of ~11 kW.

R&D: HV-CMOS Sensor Development

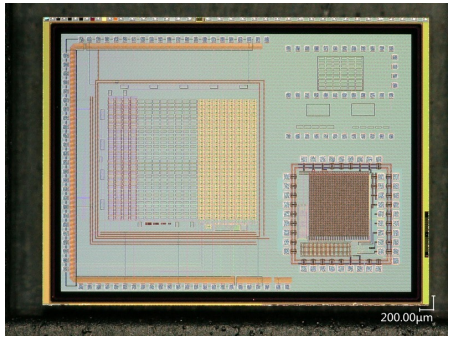
- HV-CMOS pixels (COFFEE2):

  The first sensor prototype in the 55 nm HV-CMOS process worldwide (submitted in Aug 2023, received in Dec 2023)



COFFEE

CMOS SENSOR IN FIFTY-FIVE NM PROCESS



COFFEE2

Three sections in the chip:

1: Passive diode arrays:

- Including 6 different signal collection structures for studying diodes and charge sharing.

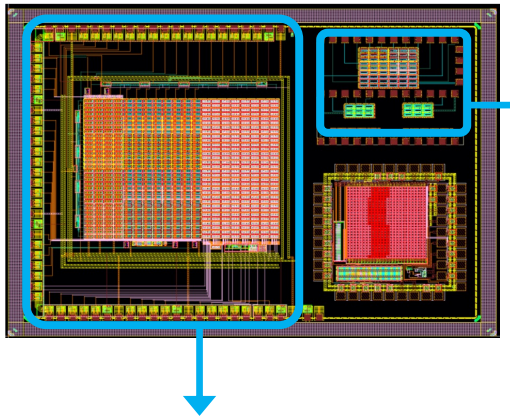
2. Pixel arrays with diodes and in-pixel circuits:

- Features 6 types of diodes and 3 types of in-pixel electronics.

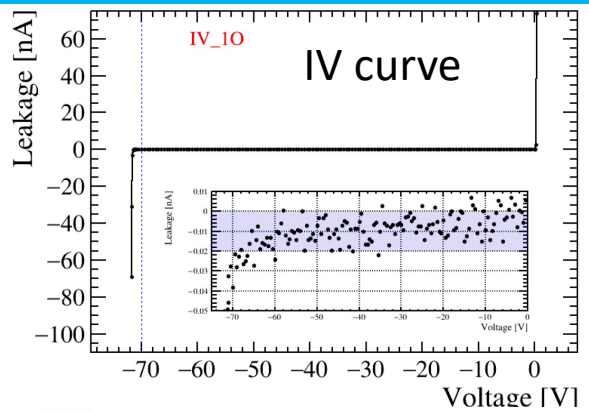
3. Pixel arrays with peripheral digital readout:

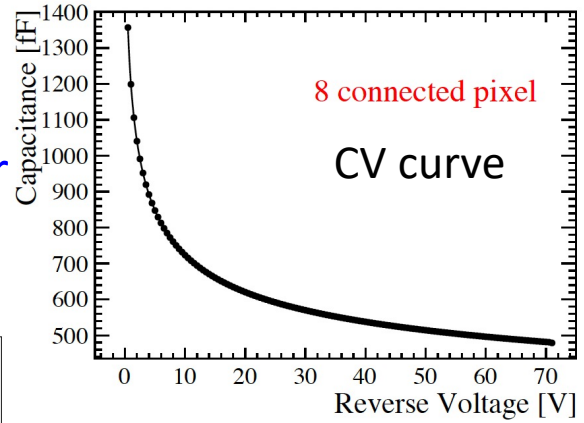
- Used for validating readout strategies for imaging application, which are not directly relevant to the CEPC use case.

HVCMOS (COFFEE2) Sensor Test



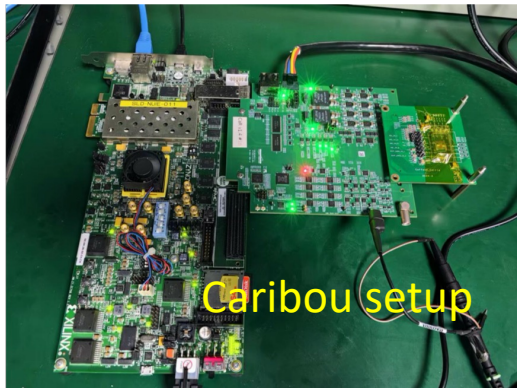
- Passive diode array test
  - IV (breakdown at –70 V)
  - CV (single pixel ~30-40 fF)
  - Leakage current increased from 0.01 nA to ~1 nA after 10^{14} n_{eq}/cm^2 radiation

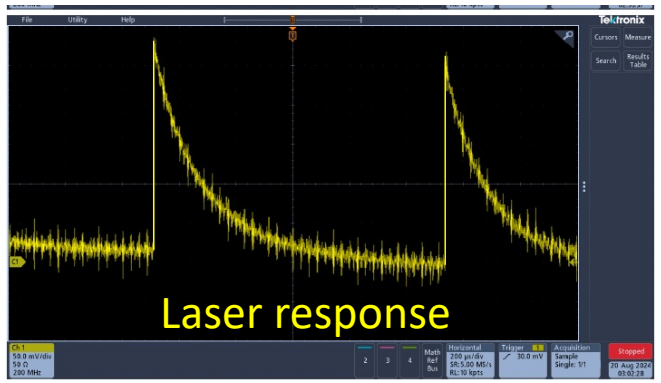


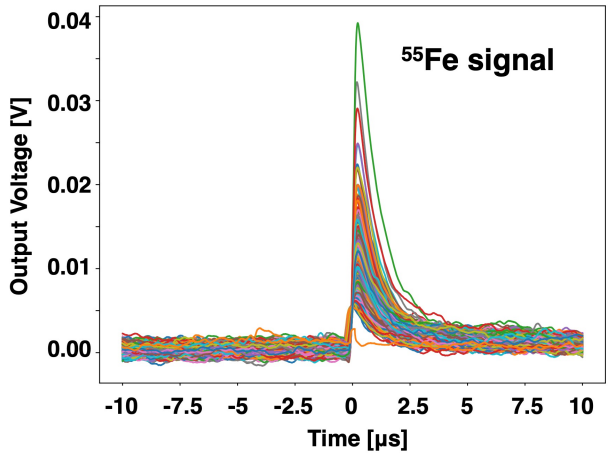


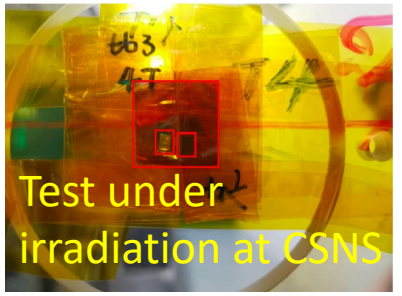
- Circuit test
  - Laser response observed
  - Radioactive source (^{55}Fe) observed

COFFEE2 has successfully verified the sensor process and in-pixel analog front-end.



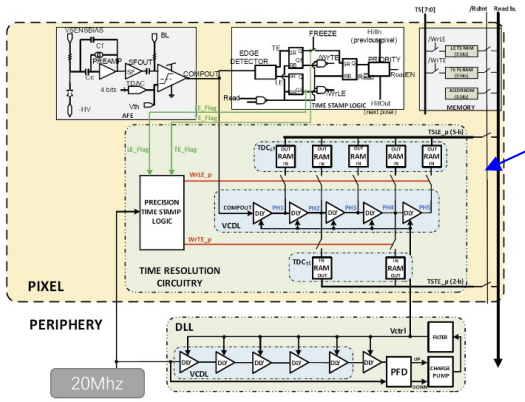




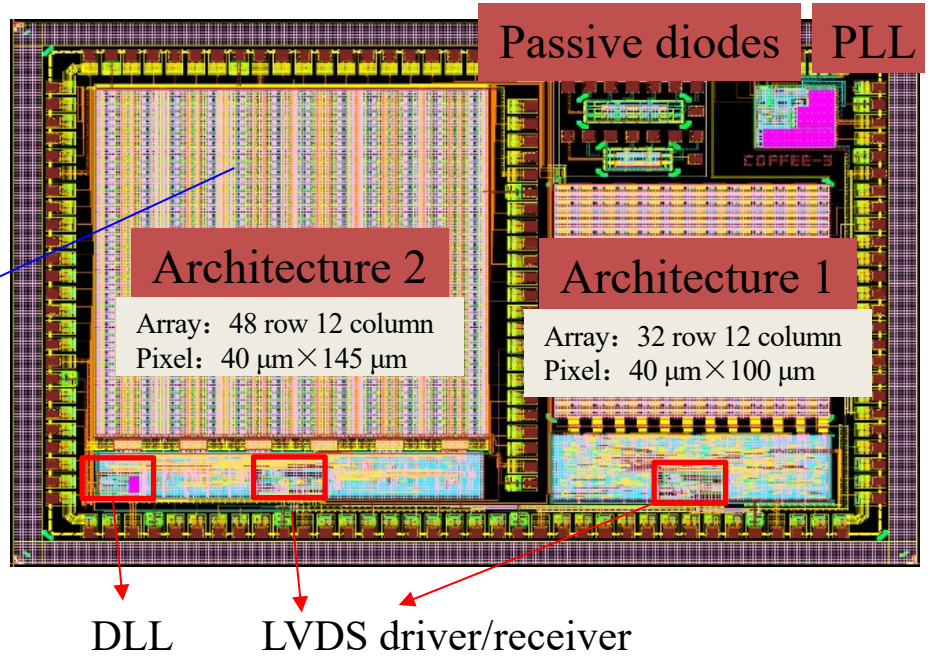


Latest Progress on HV-CMOS R&D

- HV-CMOS pixel sensor chip (COFFEE2) has successfully completed critical verification, providing important input for the next chip design and prototyping.
- The latest COFFEE3 chip design was submitted for tape-out in Jan 2025 and received in May 2025: (incorporating two readout architectures, both featuring nearly a complete ASIC readout framework, which can be extended to final chip.)

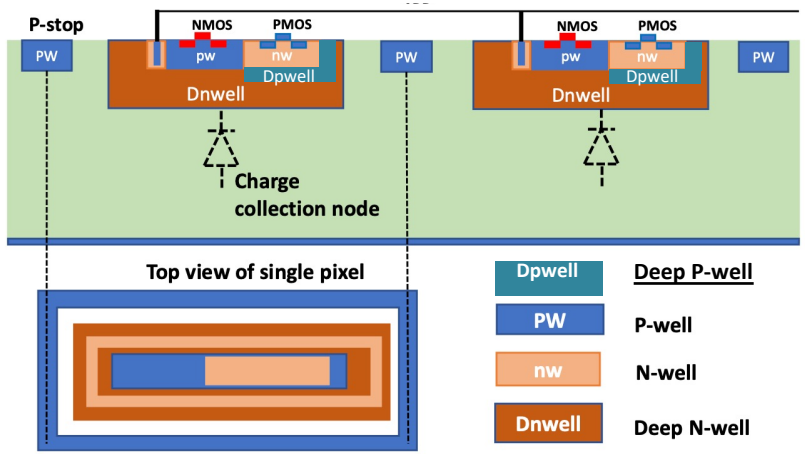


- In-pixel coarse-fine TDC



➢ **Architecture 1:** An optimized design framework based on the current process conditions (Triple-well process).

➢ **Architecture 2:** An improved solution that requires process modification (Deep P-well required) to fully utilize the advantages of the 55 nm process node.

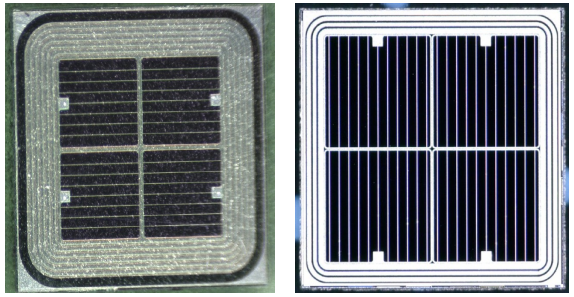


The COFFEE3 chip test is underway, and process modifications are being discussed.

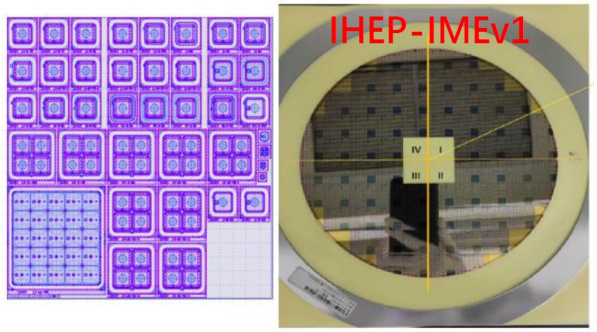
LGAD Sensor Development at IHEP

- The LGAD (Low Gain Avalanche Detector) sensor developed by IHEP achieves both precise position and time measurements under high radiation levels.

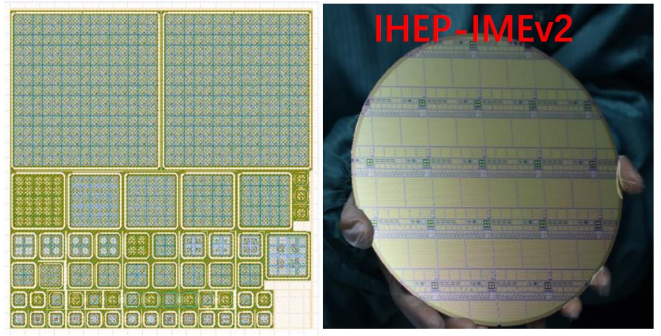
IHEP(2019)



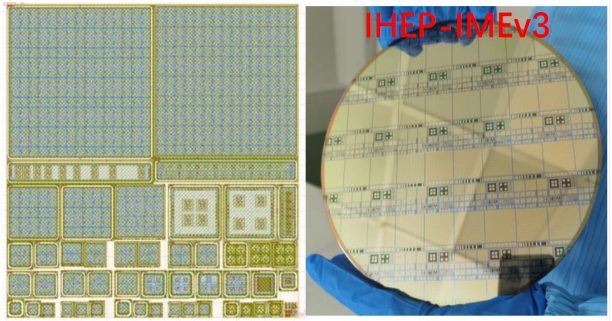
IHEP (2020.9)



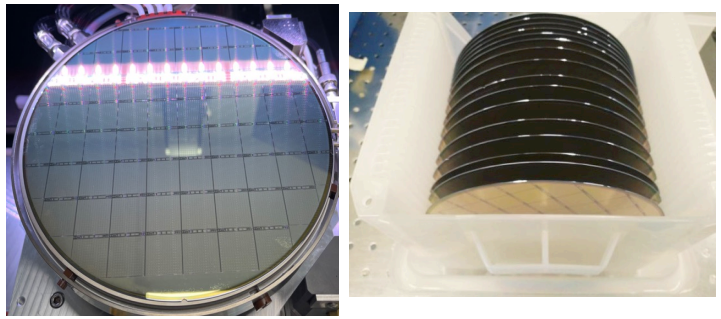
IHEP (2021.6)



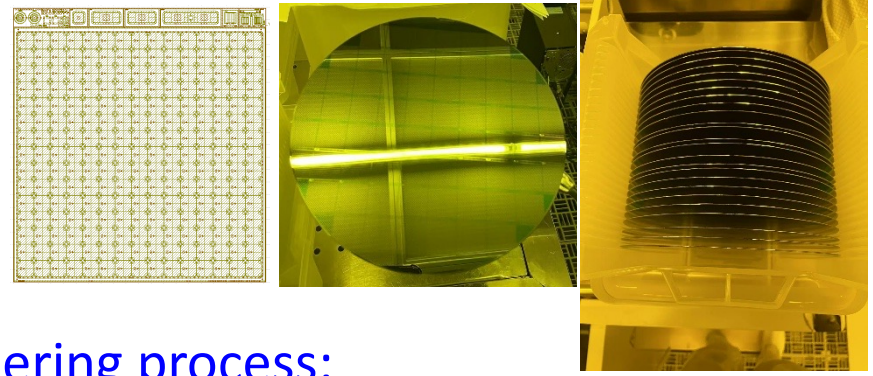
IHEP (2022.5)



Pre-production for ATLAS (2023.7)



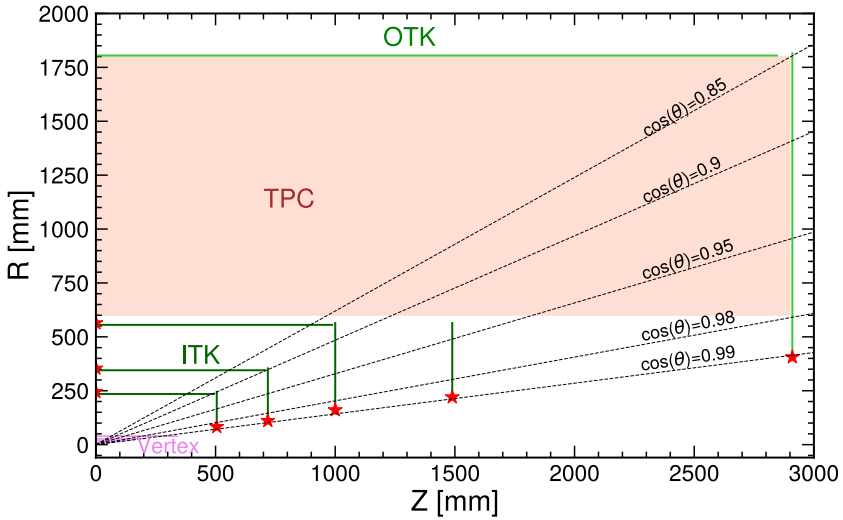
Mass production for ATLAS since 2024.6



- In May 2023, CERN selected IHEP in the HGTD sensor tendering process:
  - First time a domestic silicon sensor was chosen by CERN for an LHC experiment.

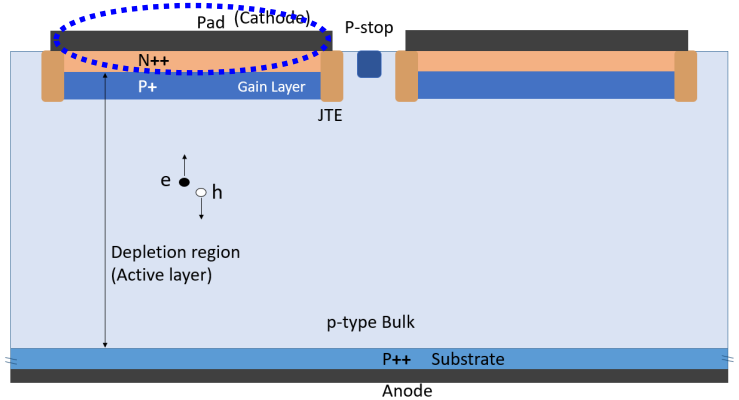
AC-LGAD for CEPC OTK with Precision Timing

- Key parameters of AC-LGAD microstrip sensor for OTK:
  - Sensor size: (3-4.5) cm × (3-5) cm
  - Strip number: 512 or 384
  - Sensor thickness: 300 μm
  - Pitch size: ~100 μm
  - Spatial resolution: 10 μm
  - Time resolution: 50 ps
  - Power consumption: 300 mW/cm^2



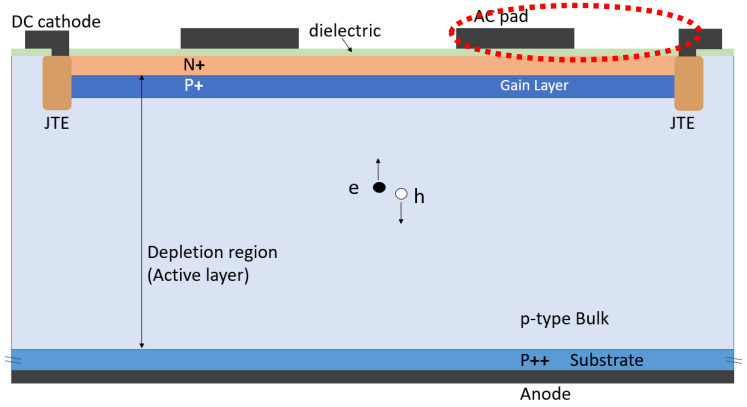
LGAD (Low-Gain Avalanche Detector)

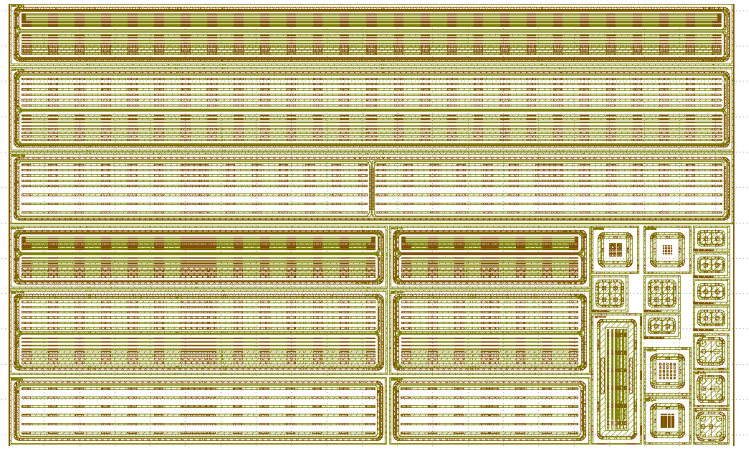
Segmented gain layer



AC-LGAD (AC-coupled LGAD)

Bulk gain layer (less dead area)



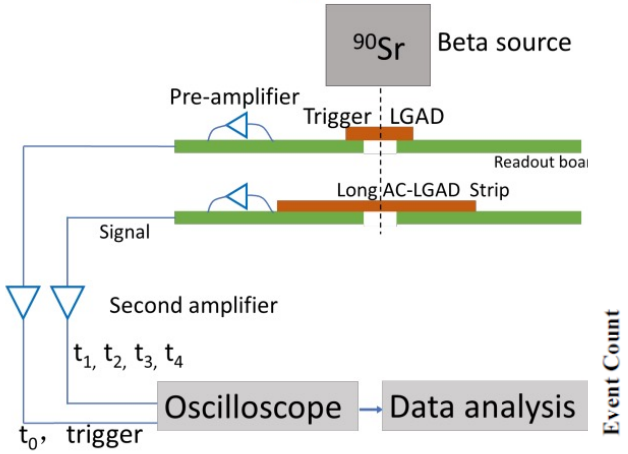


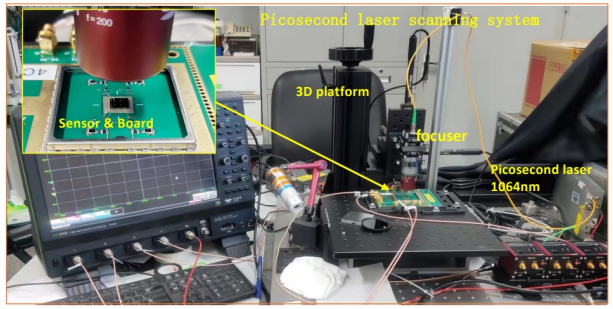
- The read-out electrode is connected to the N++ layer.
- A thin dielectric layer (Si_3N_4 or SiO_2) separates the metal AC pads from the N+ layer.

The latest AC-LGAD layout (submitted for tap-out in March 2025)

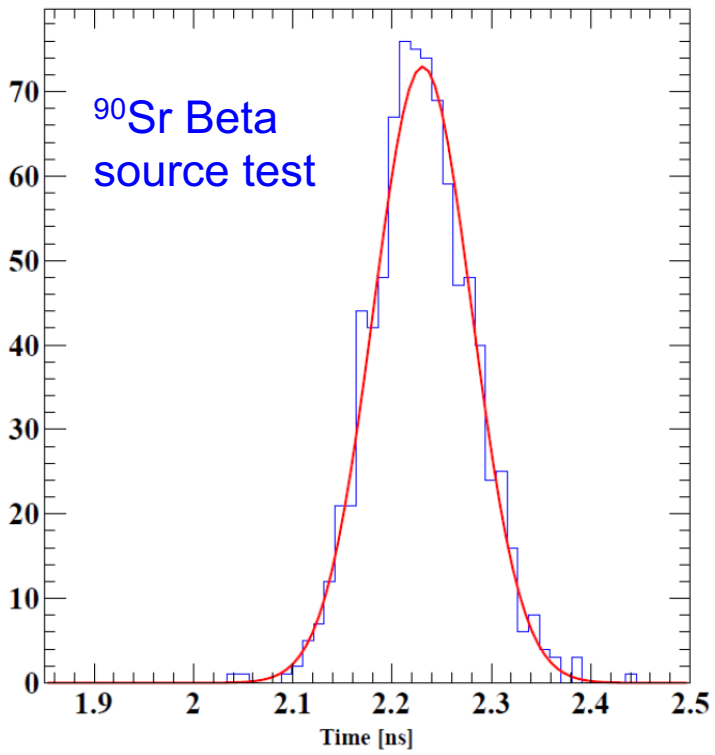
AC-LGAD Performance: Time and Spatial Resolution

^{90}Sr test setup

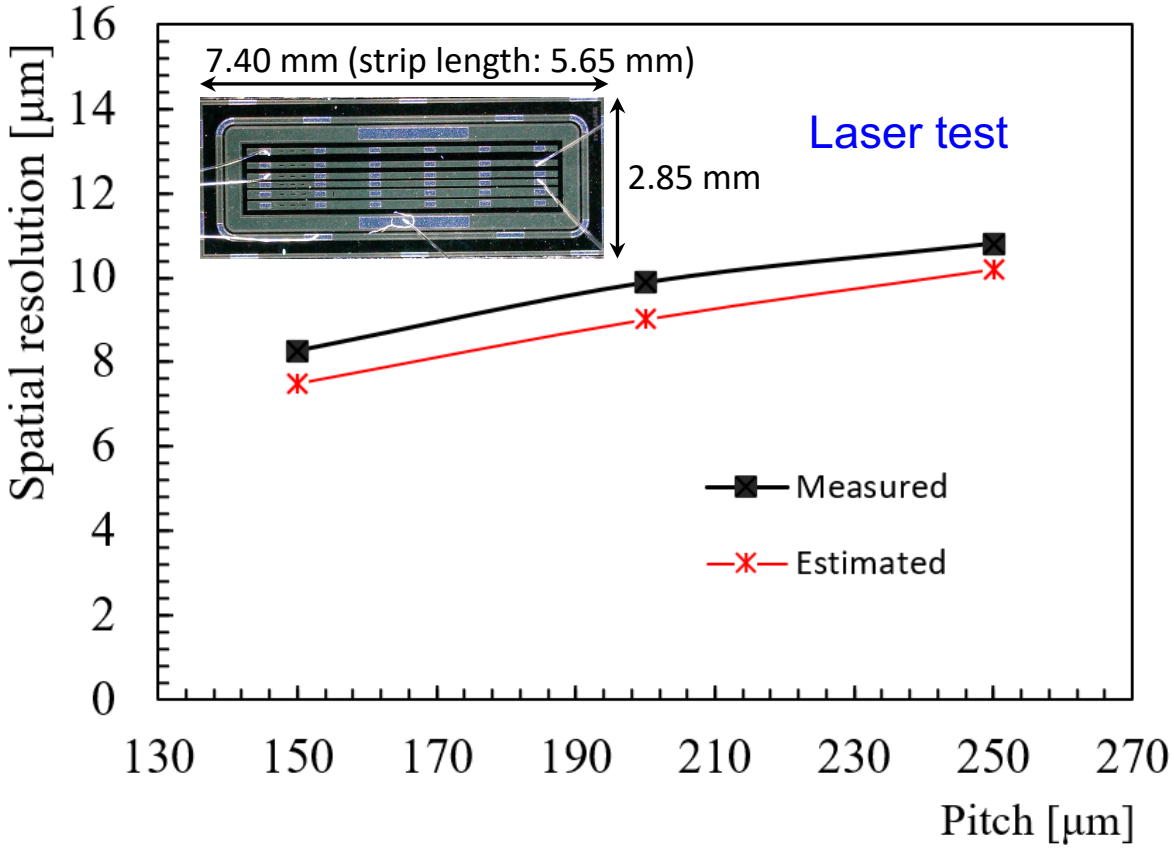




Laser test setup



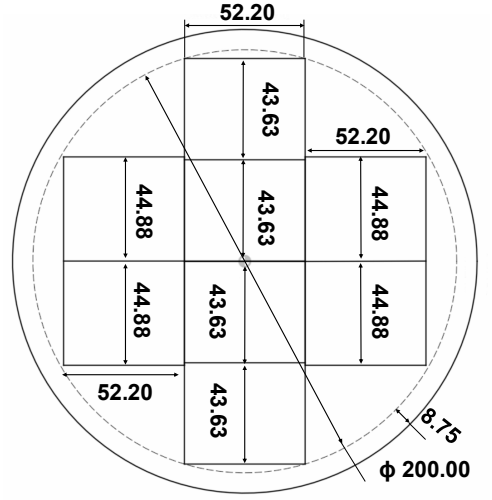
Time resolution: 38 ps



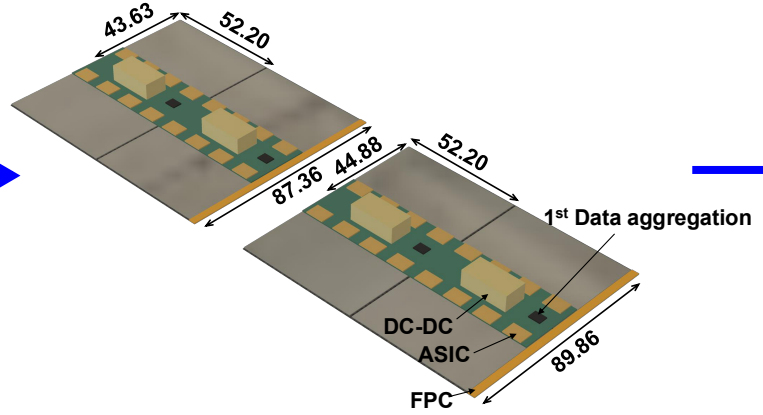
Spatial resolution: 8 μm for 150 μm strip pitch

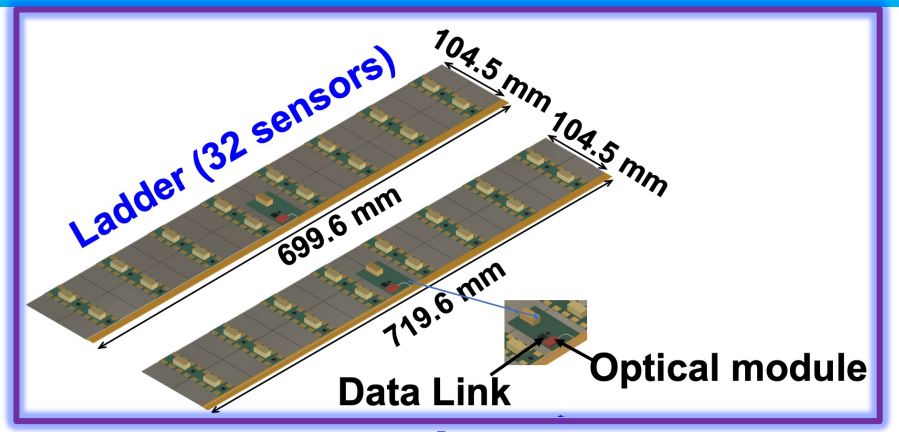
OTK Barrel Design with AC-LGAD Strip Sensor

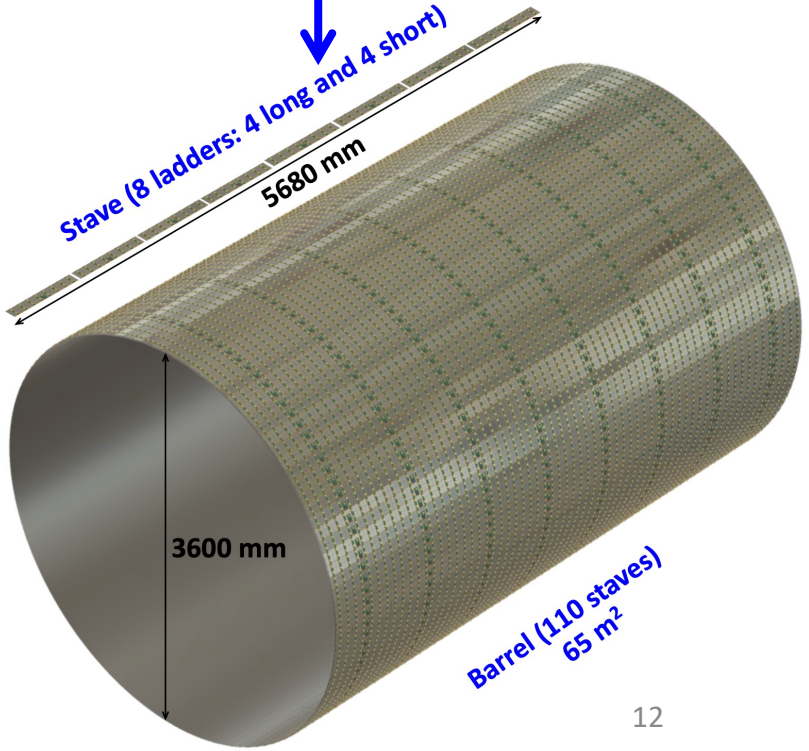
8'' wafer



Module (2×2 sensors)





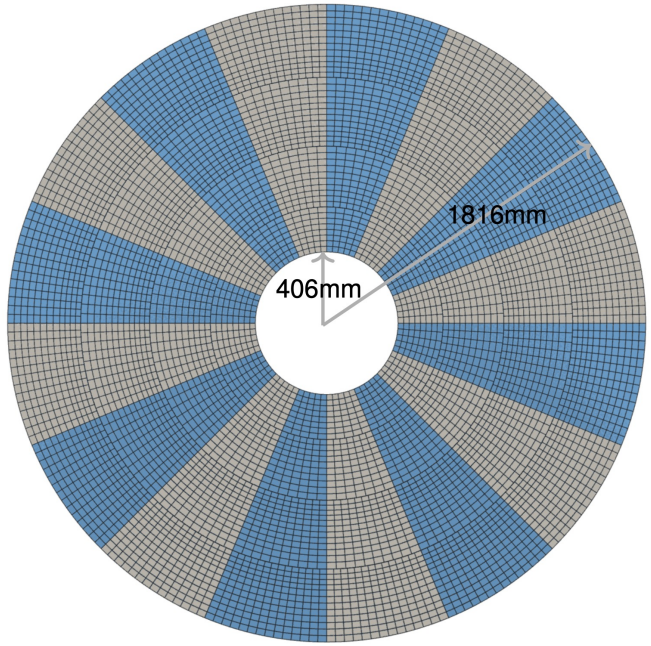


- AC-LGAD strip sensor（Each readout by 4 128-channels ASICs）:
  - Sensor size: 43.63 mm × 52.20 mm
    44.88 mm × 52.20 mm
  - Strip pitch: 100 μm (spatial resolution 10 μm)
- Module: 4 sensors (16 readout ASICs)
- Ladder: 8 modules (32 sensors)
- Stave: 8 ladders (4 short+4 long)

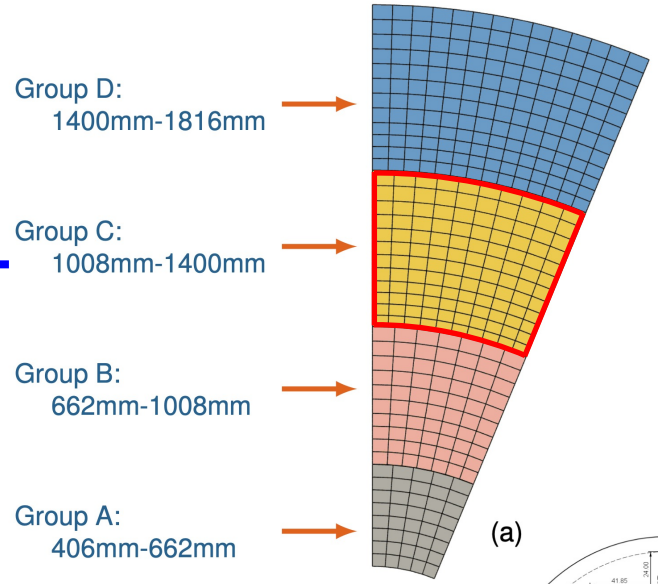
The designed OTK barrel has a total surface area of 65 m², including 28,160 sensors and 112,640 readout ASICs (LATRIC) under development by IHEP, with a power consumption of ~195 kW.

OTK Endcap Design with AC-LGAD Strip Sensor

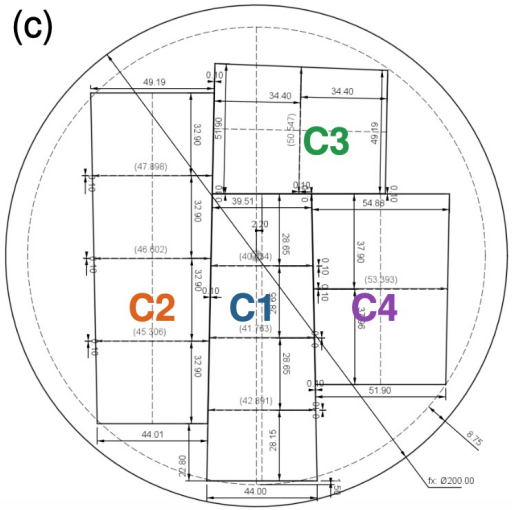
Endcap (16 sectors, 10 m^2)

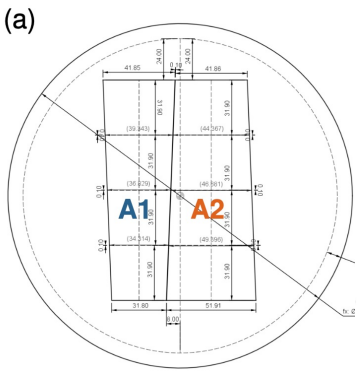


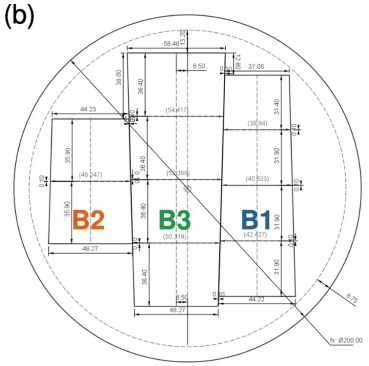
1/16 Sector

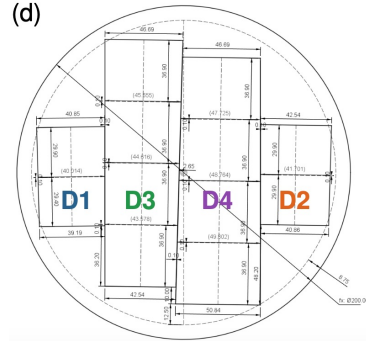


Sensor: 8'' wafer (group C sensors)









8'' wafer (group A, B, D sensors)

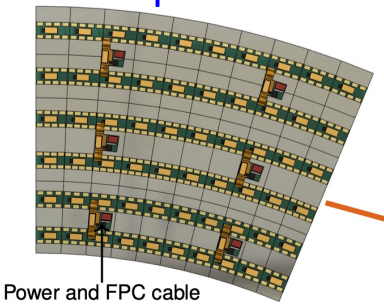
- OTK endcap consists of 42 rings, arranged into 4 groups.
- Each group contains 2-4 subgroups of trapezoid sensors, dicing from one 8'' silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
  - Strip pitch : 80.59-113.03 µm
  - Strip length : 28.1-36.3 mm

OTK endcap has a total surface area of 20 m^2, including 12,736 sensors and 46,336 ASICs, with a power consumption of ~60 kW.

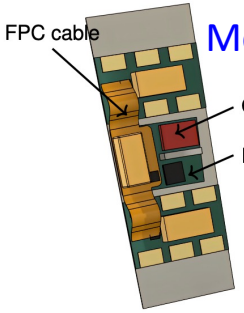
Maximize silicon wafer utilization and reduce masks (only 4 required), while facilitating detector assembly.

OTK Endcap Sensors with Readout Electronics

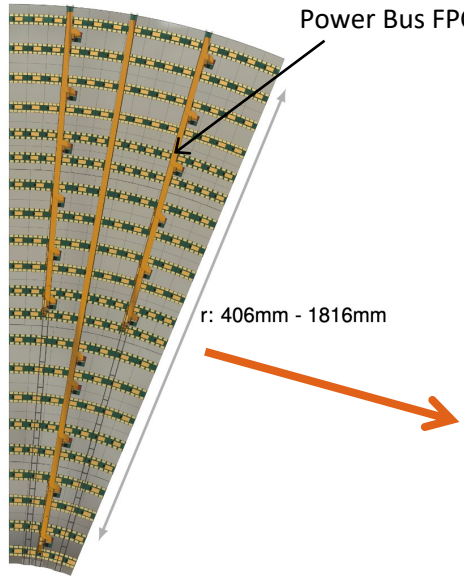
Group C sensors



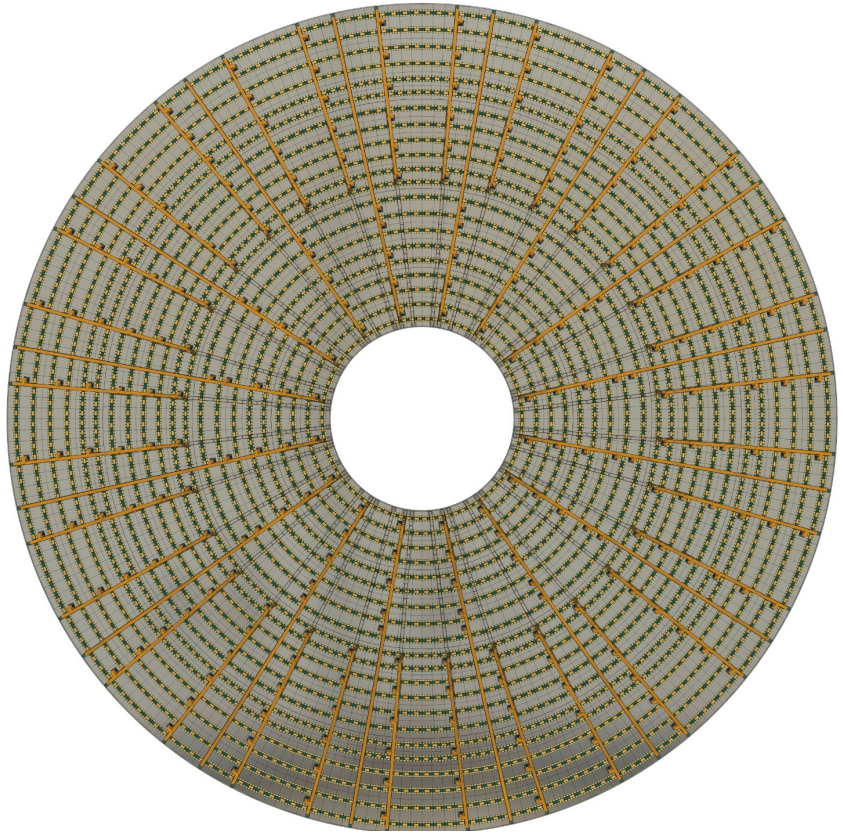
Module (2 sensors)

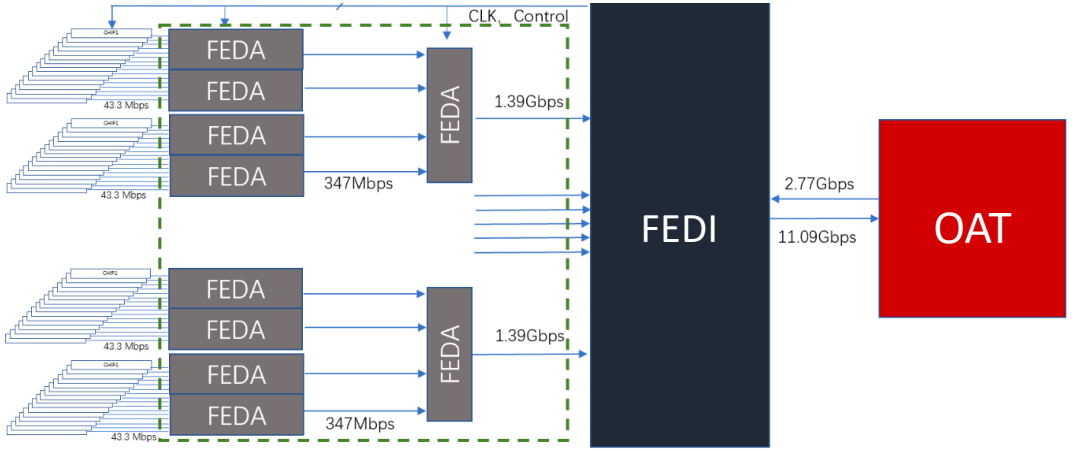


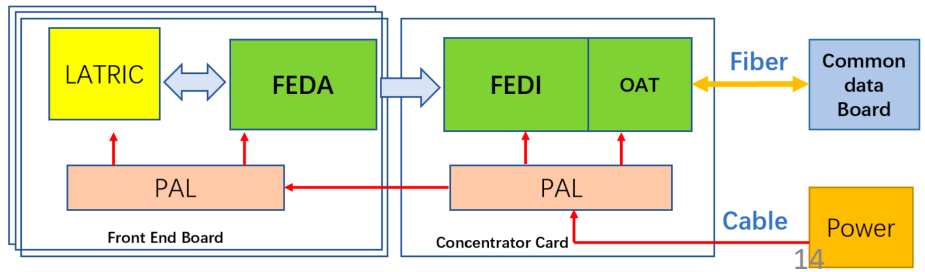
1/16 Sector



Endcap (16 sectors)



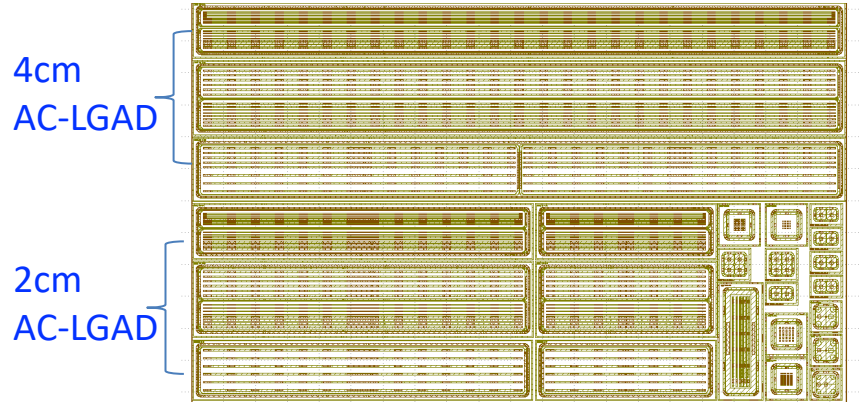




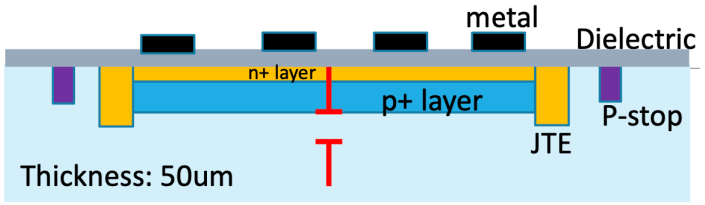
The FEDA, FEDI, OAT, and PAL chips are under development by the CEPC team.

Latest Progress on AC-LGAD Sensor R&D

- New IHEP AC-LGAD strip sensor prototype: summitted for tap-out in March 2025.
  The new layout and design include:
  - Strip lengths: 1 cm, 2 cm, and 4 cm
  - Strip pitch sizes: 100 μm, 200 μm, and 500 μm
  - Electrode widths: 25 μm, 50 μm, and 100 μm
  - Optimized isolated structure design and EPI thickness to reduce sensor capacitance (correlated with power consumption)
  - Process design optimization (n+ layer dose) for better spatial resolution

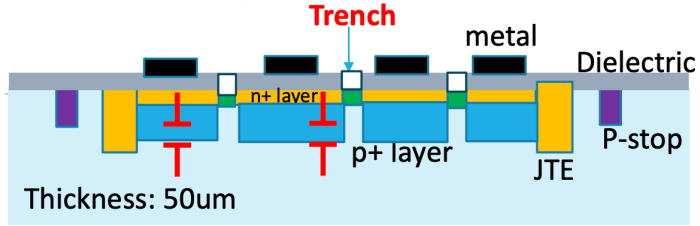


1cm AC-LGAD

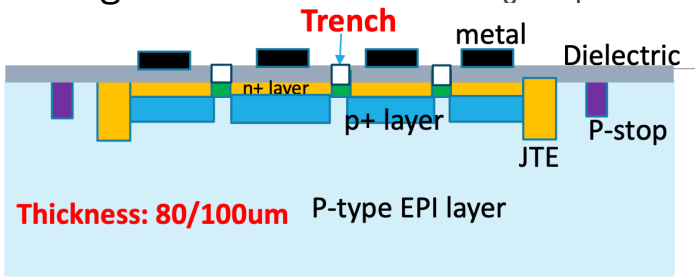


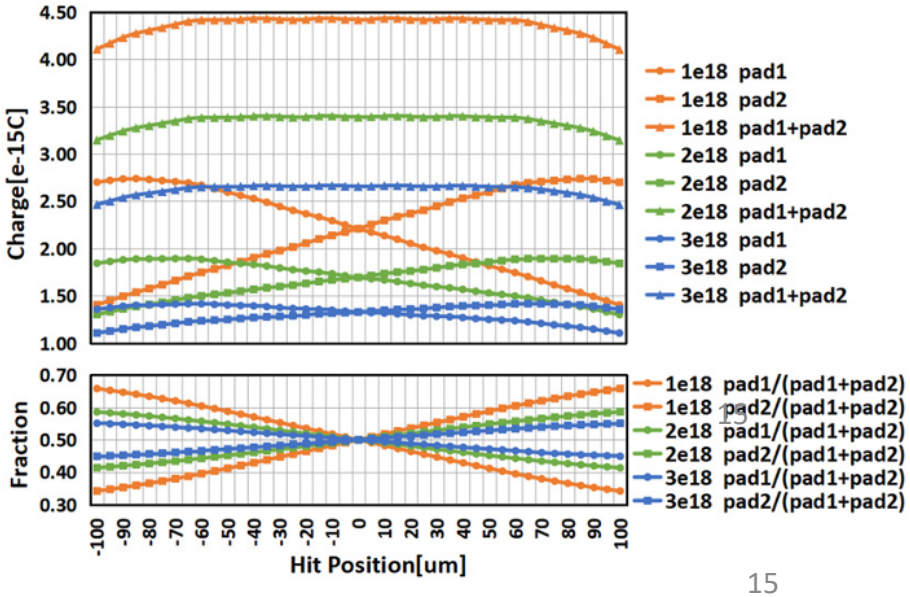
Introducing isolated structure:

$C = \varepsilon_0 * \varepsilon_r * A \downarrow / d$



Increasing EPI thickness: $C = \varepsilon_0 * \varepsilon_r * A / \mathbf{d} \uparrow$

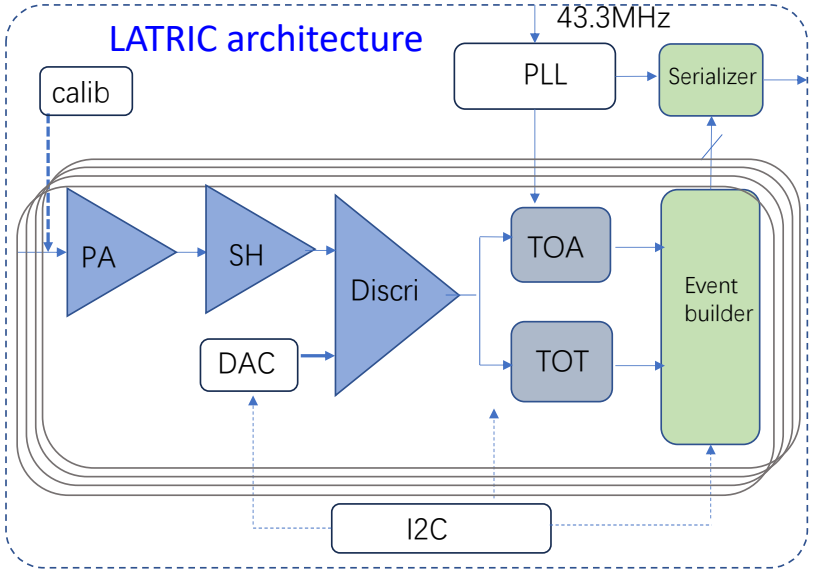


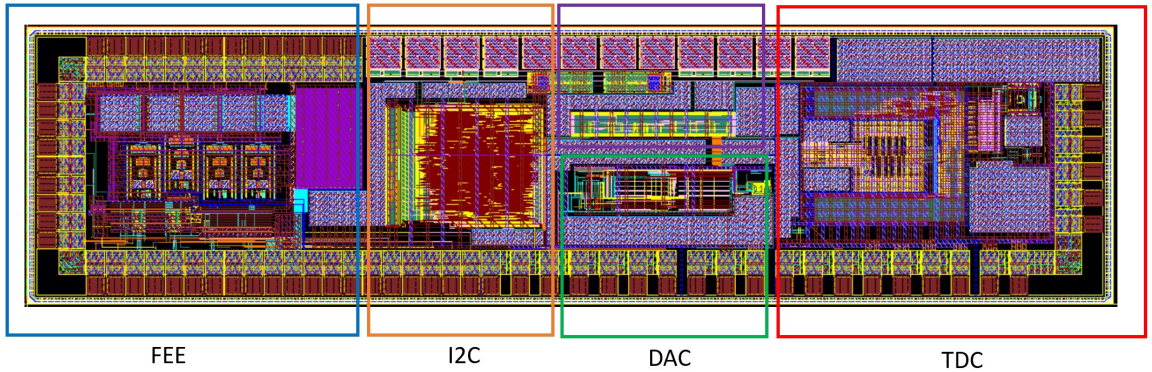


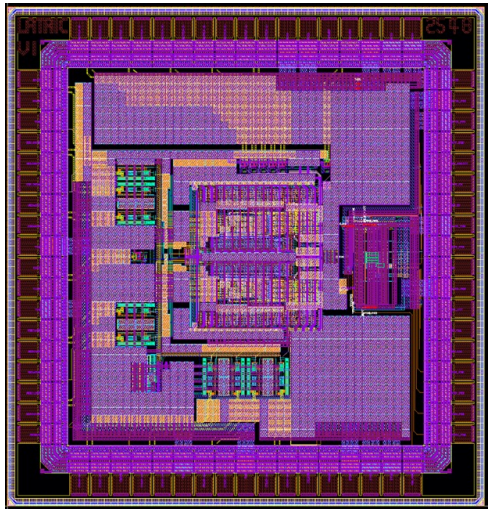
The sensor test will be launched once we received the latest tap-out.

Latest Progress on LGAD ASIC (LATRIC) R&D

- LGAD ASIC (LATRIC) development: the prototype design was submitted for tap out in April 2025.
  - Several key elements in design are shared and verified with FPMROC (10 ps) chip
    - FEE: Preamplifier+Discriminator: jitter<7.8ps @ input 2.5mV, t_r=0.1ns, Cs=0 pF
    - PLL, Serializer verified
  - I2C Slave: ASIC parameter configuration
  - 12-bit DAC: threshold and calibration
  - TDC design:
    - Event driven delay line to reduce the power consumption
    - Power consumption: average current for single event: 443 µA, static current: < 5 µA
    - Real time calibration for PVT (Process, Voltage, Temperature)
    - LSB ~36 ps based on preliminary layout post-simulation (current version)





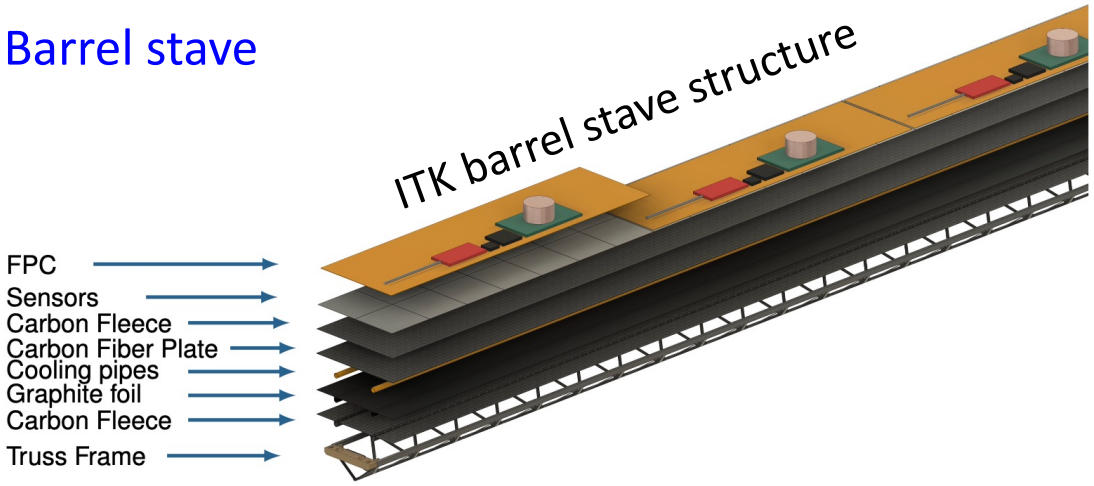


TDC delay line layout

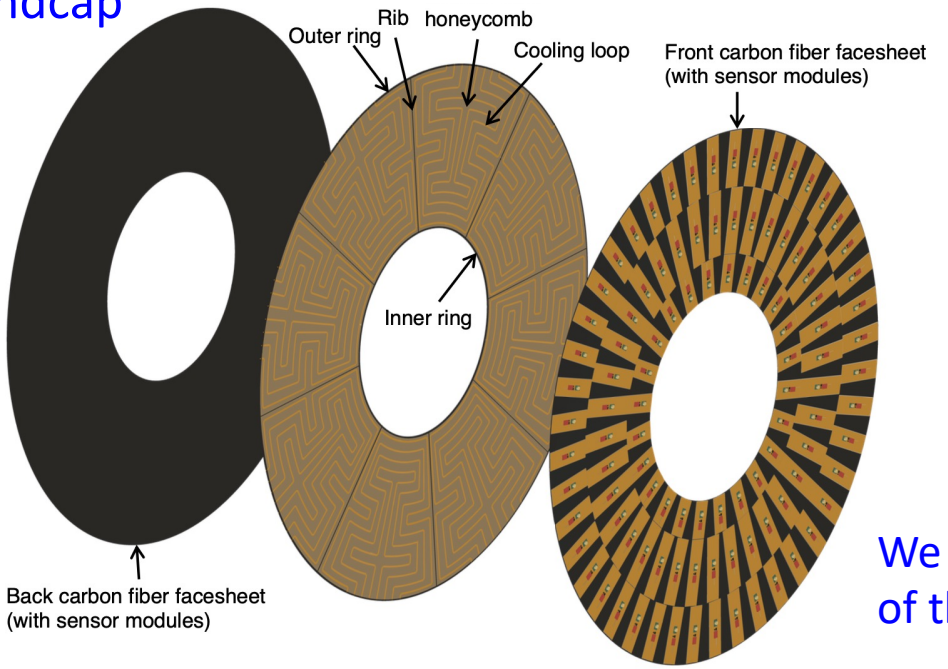
Performance testing is scheduled to be completed by the end of 2025. In Q4 2025, the new design will be enhanced by incorporating a digital logic control section. The final chip will feature 128 readout channels and provide precise measurements of both time-of-arrival (TOA) and time-over-threshold (TOT).

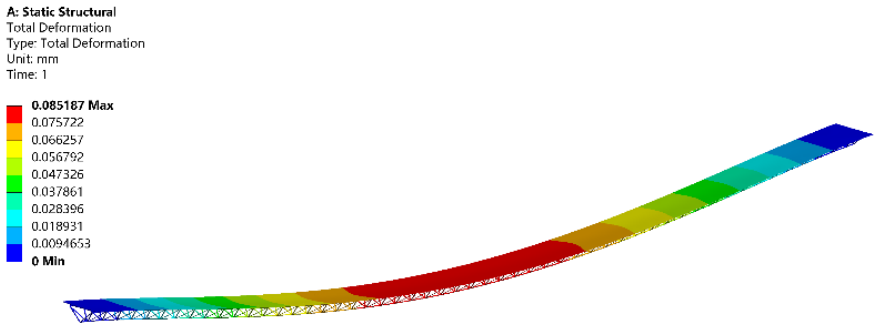
R&D on Mechanical and Supporting Structure

Barrel stave



Endcap





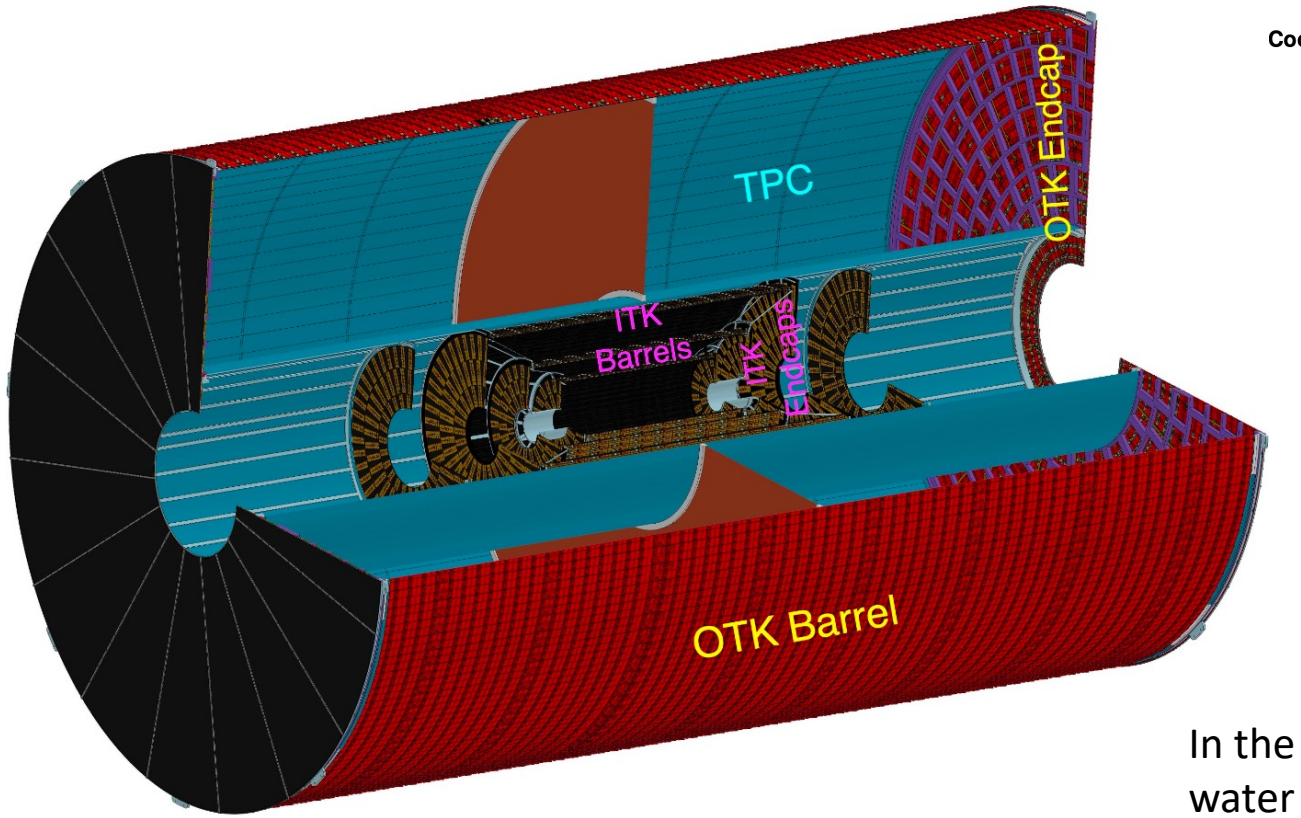
Maximum sag for first ITK barrel stave is 85 µm

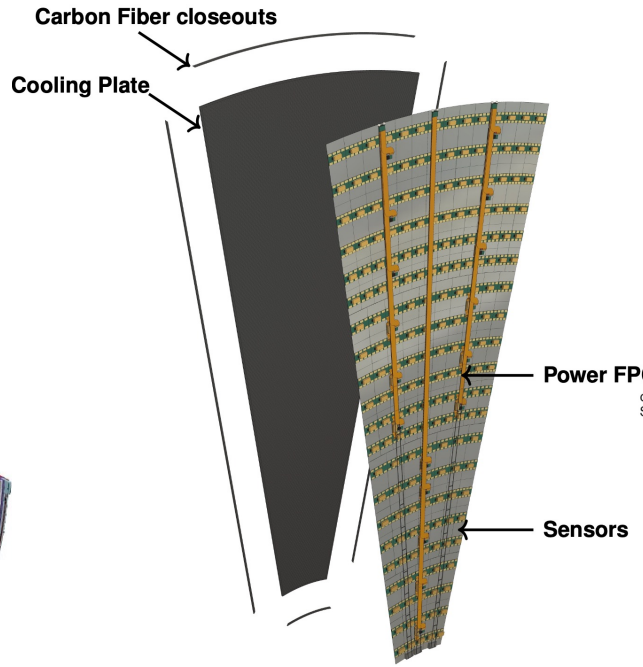
Barrel stave

Functional unit	Component	Material	Thickness [µm]	X_0 [cm]	Radiation Length [% X_0]
Sensor Module	FPC metal layers	Aluminium	100	8.896	0.112
	FPC Insulating layers	Polyimide	150	28.41	0.053
	Sensor	Silicon	150	9.369	0.160
	Glue		100	44.37	0.023
	Other electronics				0.050
Cooling Plate	Carbon fleece layers	Carbon fleece	40	106.80	0.004
	Carbon fiber plate	Carbon fiber	150	26.08	0.057
	Cooling tube wall	Polyimide	64	28.41	0.006
	Cooling fluid	Water		35.76	0.028
	Graphite foil	Graphite	30	26.56	0.011
	Glue	Cyanate ester resin	100	44.37	0.023
Truss Frame	Carbon rowing				0.080
Power Bus FPC					0.070
Total					0.677

We are collaborating with domestic carbon fiber manufacturers, and prototypes of the truss structure and other components are under development.

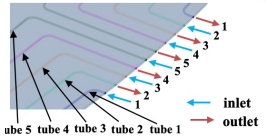
Thermal Cooling System R&D

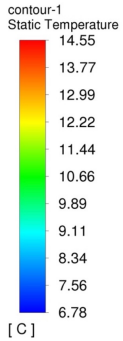


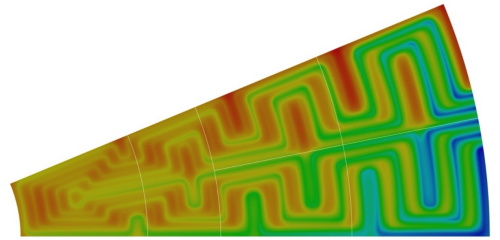


1/16 OTK endcap sector

Cooling loops







(Heat flux: 300 mW/cm^2)

In the baseline design, 1/16 sector of the OTK endcap uses 5-loop water cooling pipes with a pipe inner diameter of 2.3 mm, a flow velocity of 2 m/s, and an inlet temperature of 5°C. The sensor temperature is <15°C and senor temperature gradient is <4°C

Although water cooling was the baseline due to its overall system simplicity, We have recently also started R&D efforts for the development of CO_2 cooling system.

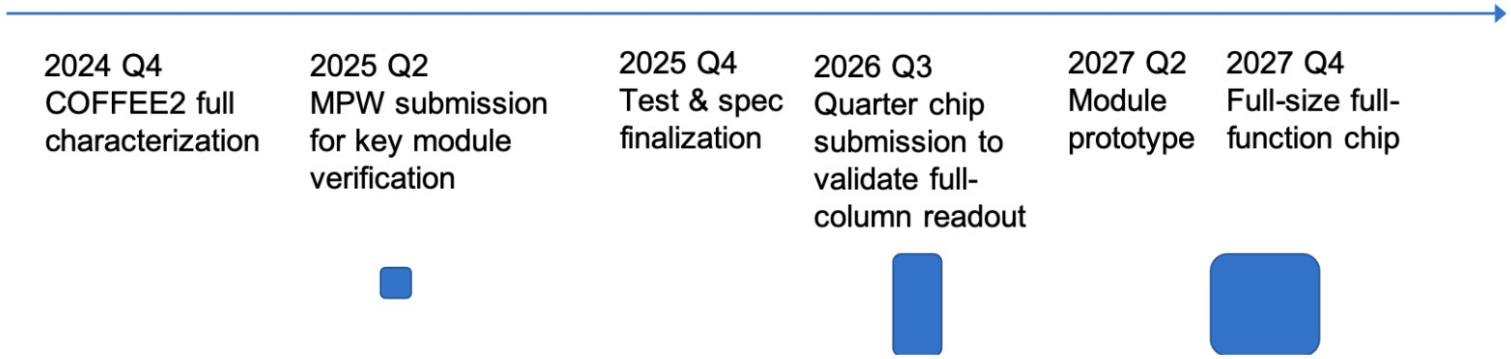
Our Research Team

- Currently active: 27 institutes, 50 staff, and 50+ postdocs & students

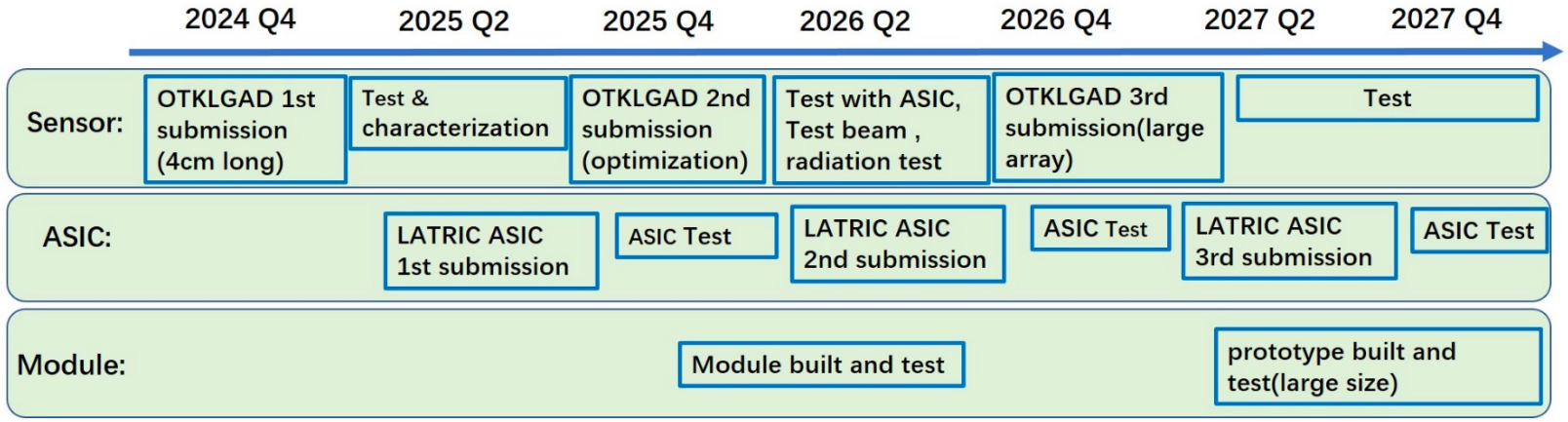
We welcome collaborations with more domestic research institutions and partners worldwide!

R&D Plan Following the Ref-TDR

- HV-CMOS pixels:



- AC-LGAD strips+ASIC:



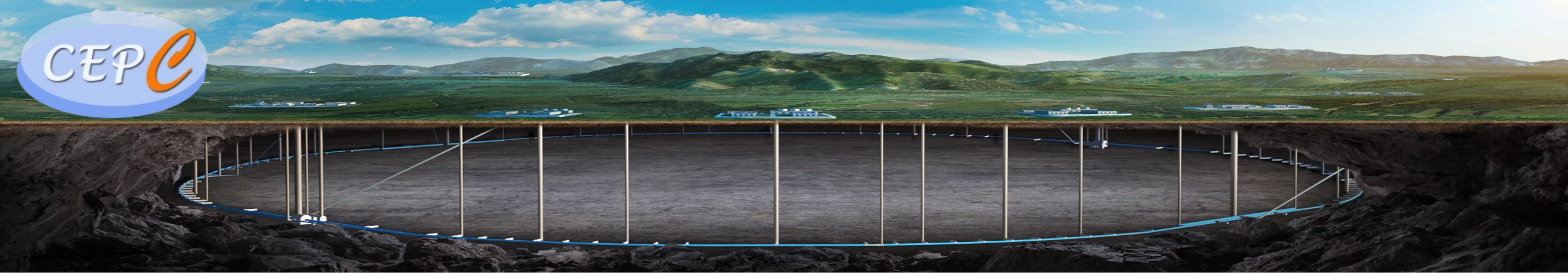
Development of the mechanical and cooling systems is progressing in parallel, with the goal of delivering a prototype detector by the end of 2027.

Summary

- The R&D progress and the complete design of the Silicon Trackers (ITK+OTK) for the CEPC Reference Detector Technical Design Report (Ref-TDR) have been presented, and the Ref-TDR will be released soon.

- Our next major focus will be on R&D. Ongoing development spans from prototype detector creation and accomplishing R&D goals.

- Continuous innovations in sensor technology, readout electronics, mechanical design, and the development of the cooling system will ensure that the Silicon Tracker meets the high demanding requirements of CEPC. These advancements will enhance tracking performance and contribute to the success of the CEPC project.

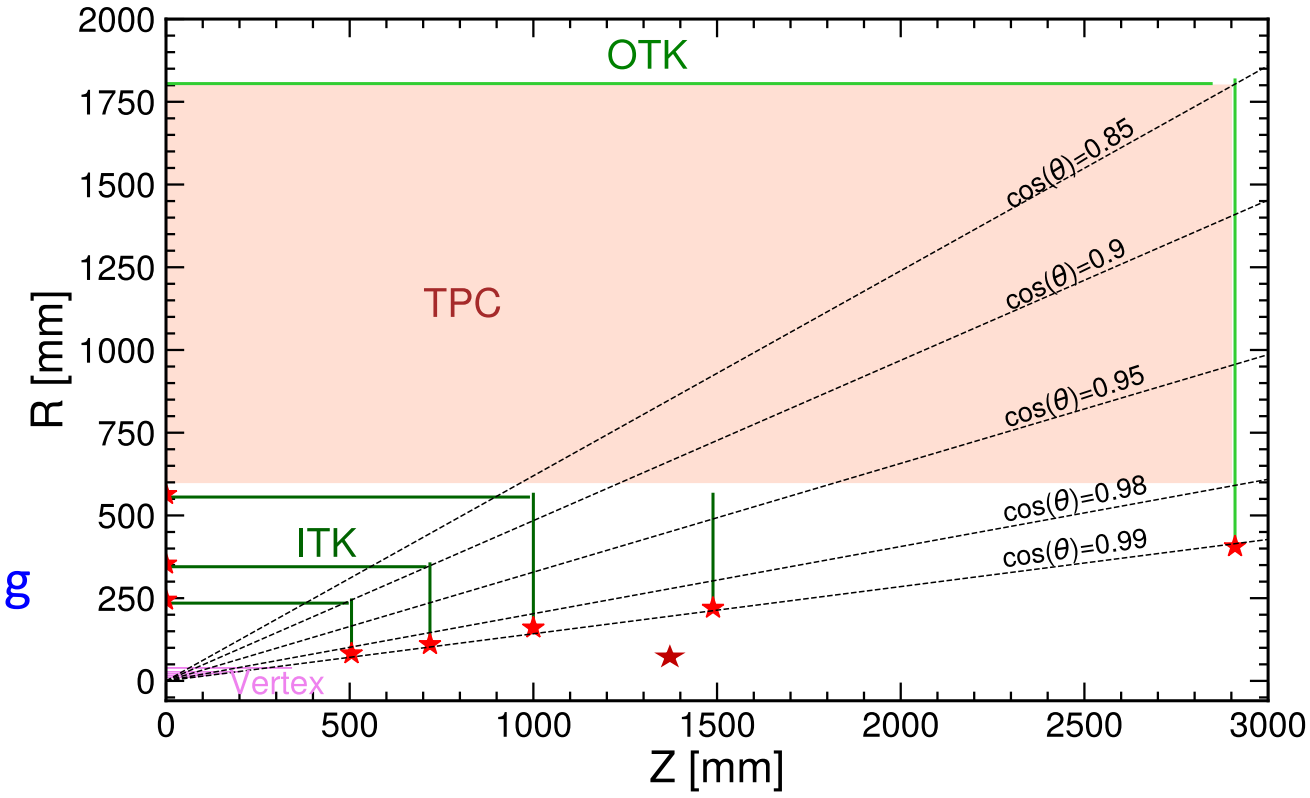


Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

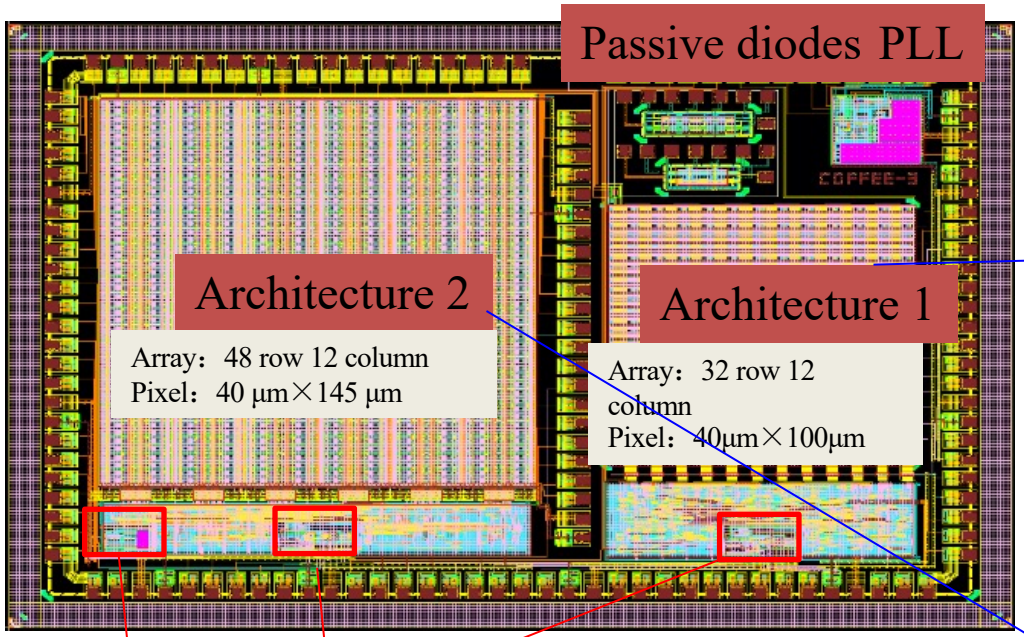
Requirements

- Inner silicon tracker (ITK)
  - Spatial resolution:
    Barrel: σ_ϕ< 10 μm (bending), σ_z< 50 μm
    Endcap: σ_ϕ< 10 μm (bending), σ_r< 100 μm
  - Material budget:
    <1% X_0 per layer
  - Operate at high luminosity Z-pole mode:
    A few ns timing resolution to tag 23 ns bunches
  - Cost effectiveness:
    ~20 m^2 area
- Outer silicon tracker (OTK) with precision timing
  - Spatial resolution:
    σ_ϕ< 10 μm (bending)
  - Material budget:
    1-2% X_0
  - Timing resolution:
    σ_t<50 ps
  - Cost effectiveness:
    ~85 m^2 area

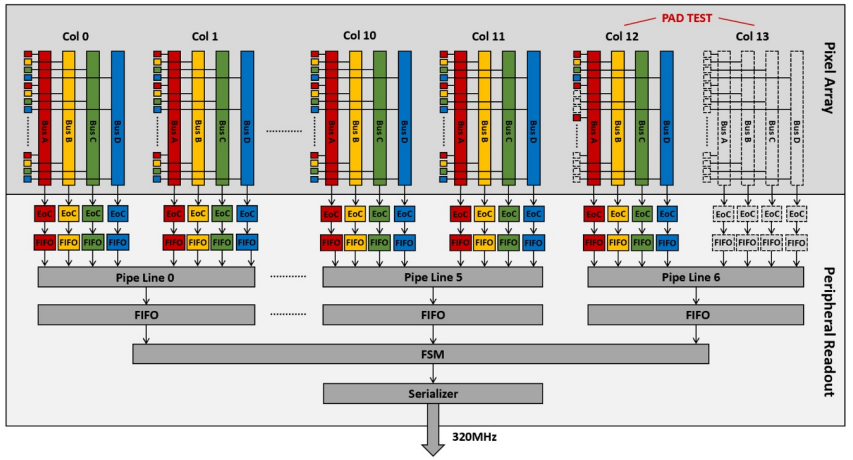


The overall track momentum resolution requirement:
~0.1% for momenta below 100 GeV/c.

Progress on COFFEE3 Development



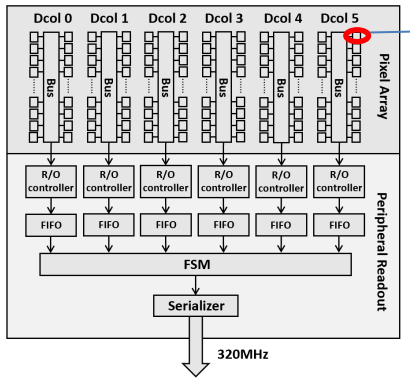
Architecture 1： NMOS Pixel Array Schematic Diagram

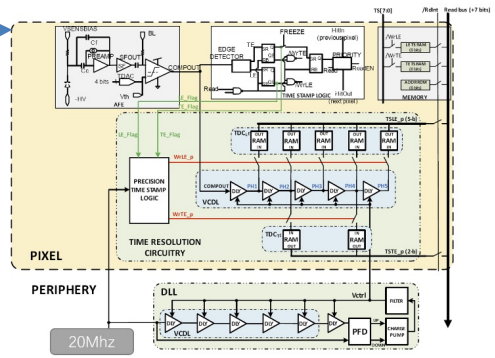


LVDS driver/receiver up to 1.28Gb/s

- In-pixel NMOS based comparator, in-pixel 4-bit DAC for threshold tuning;
- Time information （TOA, TOT…）and data formation in the end of each column;
- Improved capability to manage high incident conditions;

Architecture 2: an improved solution, fully utilize the advantages of the 55 nm process node

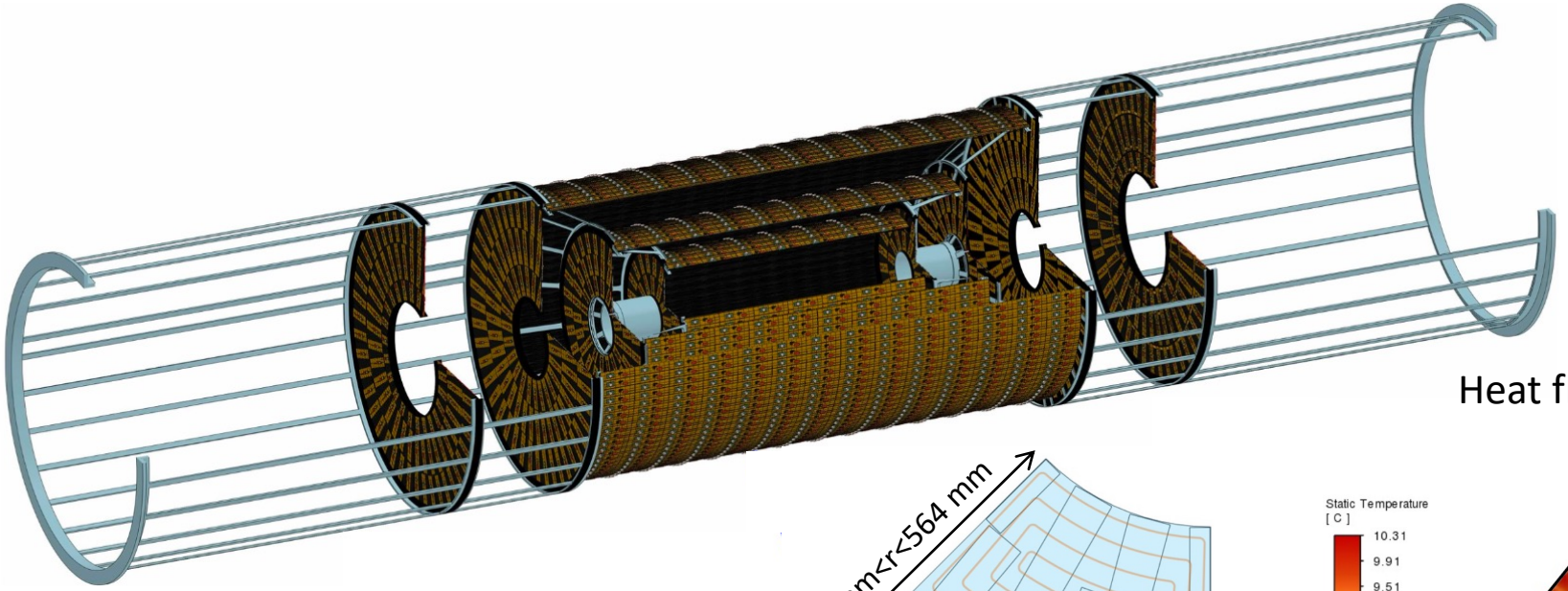


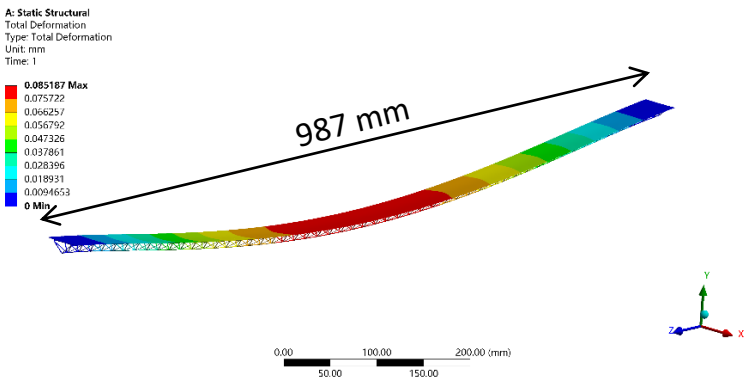


LVDS driver/receiver up to 1.28Gb/s

- In-pixel Coarse-fine TDC and 4-bit threshold tuning;
- ToA and ToT information are saved in each pixel;
- Data-driven readout;

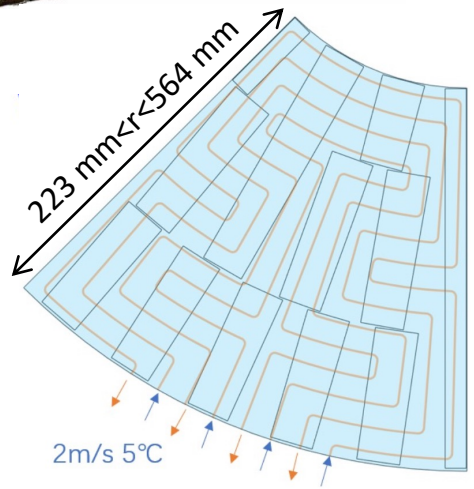
Mechanical and Thermal Analysis of the ITK

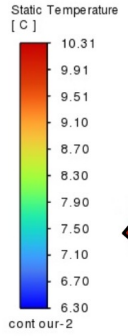


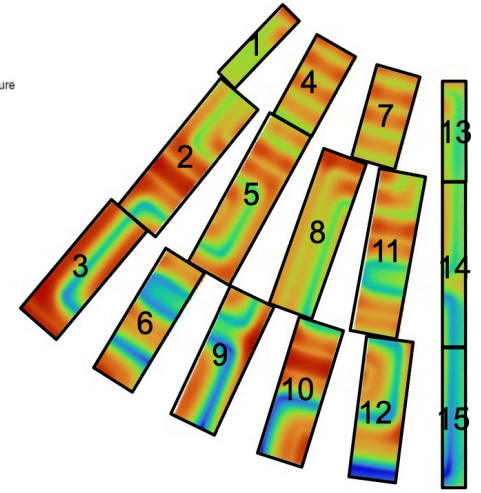


Maximum sag for first ITK barrel stave is 85 µm

Heat flux: 200 mW/cm^2



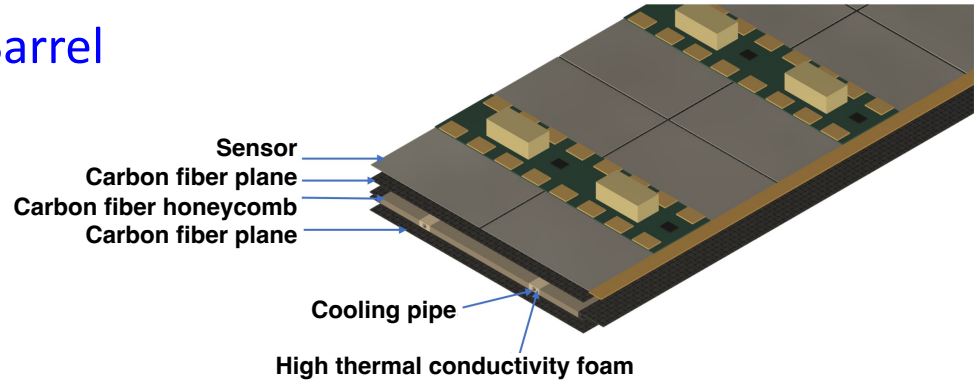




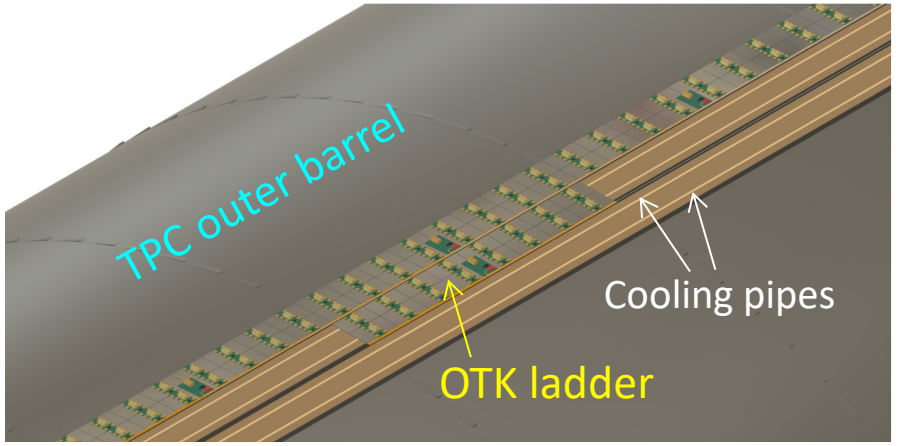
4-loops cooling for 1/8 endcap: with a cooling water flow of 2 m/s, a pipe inner diameter of 1.6 mm, and inlet temperature of 5°C, the temperature gradient across the endcap plane is <4°C, and the temperature difference for a single sensor is <2.5°C.

Mechanical and Cooling Structure of the OTK

Barrel

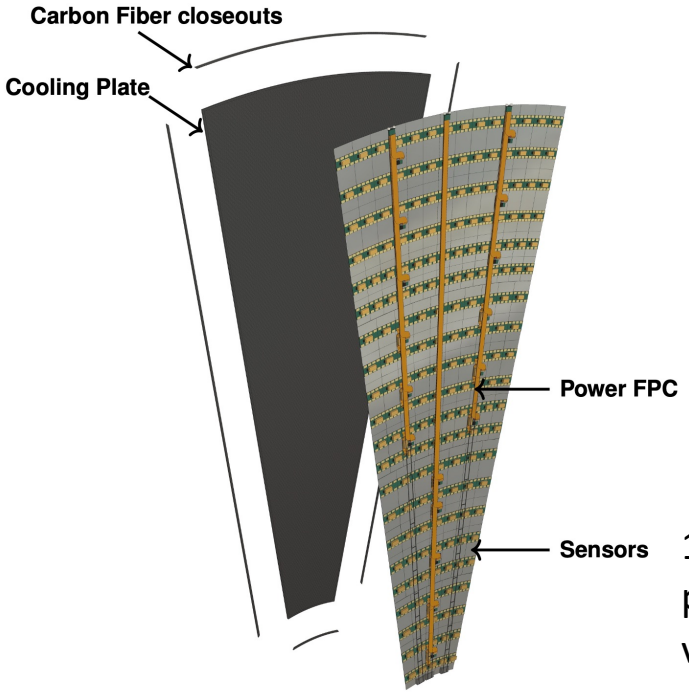


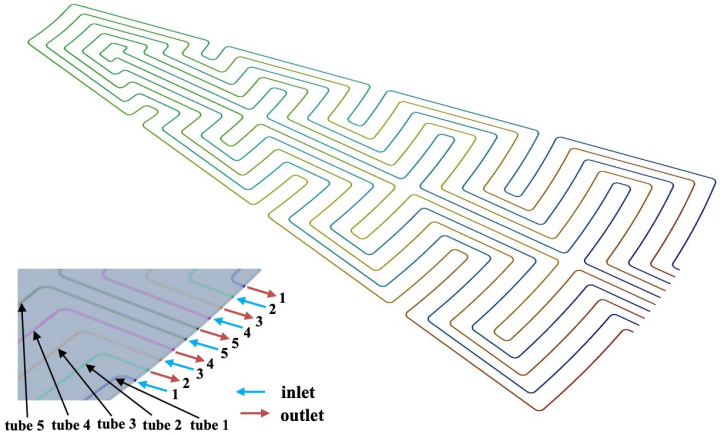
Stave Installation



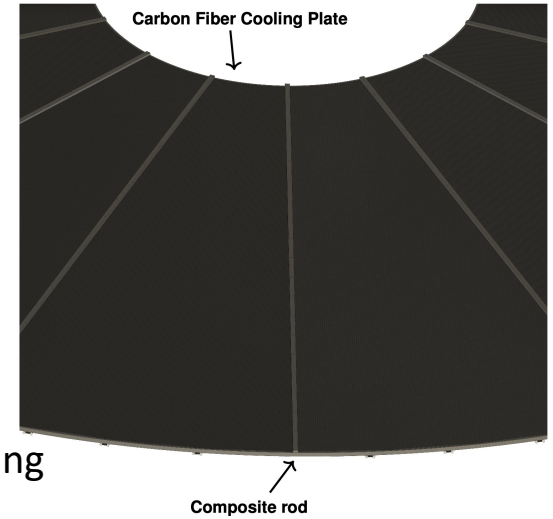
Endcap

1/16 OTK endcap sector





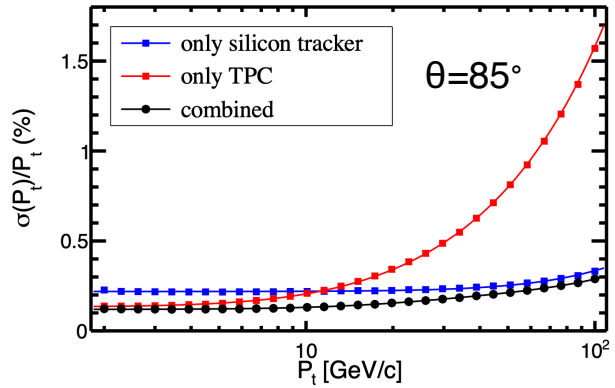
1/16 sector of the endcap uses 5-loop water cooling pipes: a pipe inner diameter of 2.3 mm, a flow velocity of 2 m/s, and an inlet temperature of 5°C.



Mounting 1/16 sectors

Simulation of the Tracker Performance

Momentum resolution in the barrel region:



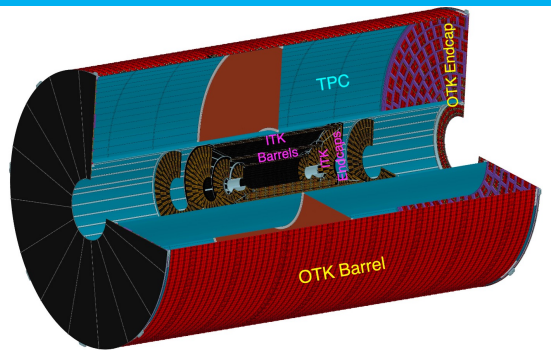
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{Si}} = ap_t \oplus \frac{b}{\beta\sqrt{\sin\theta}}$$

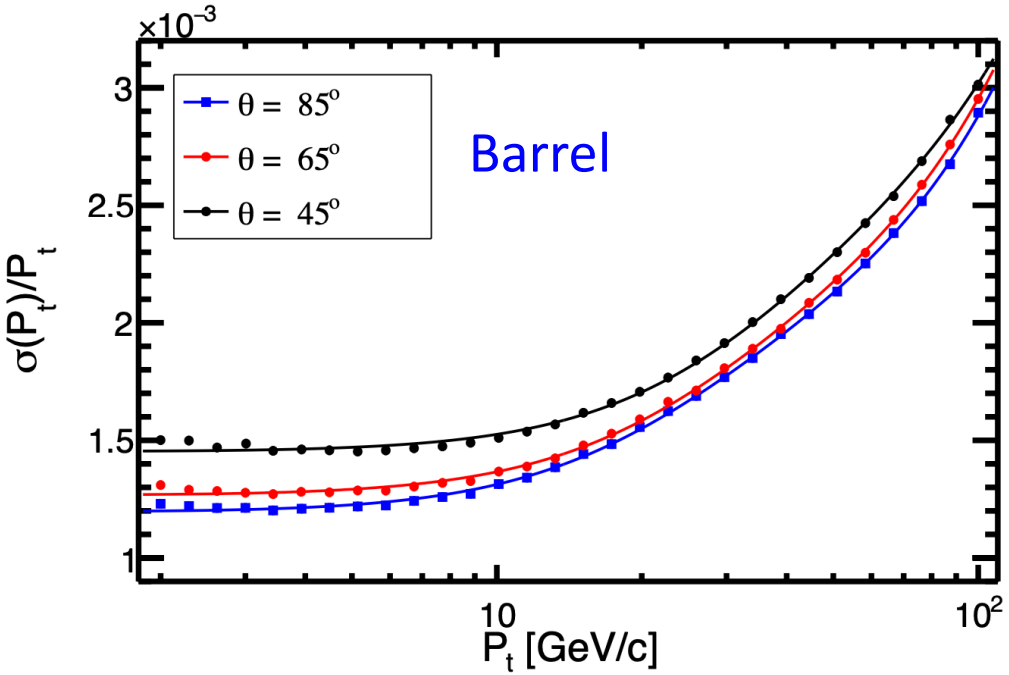
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{TPC}} = as_1 p_t \oplus \frac{bs_2}{\beta\sqrt{\sin\theta}}$$

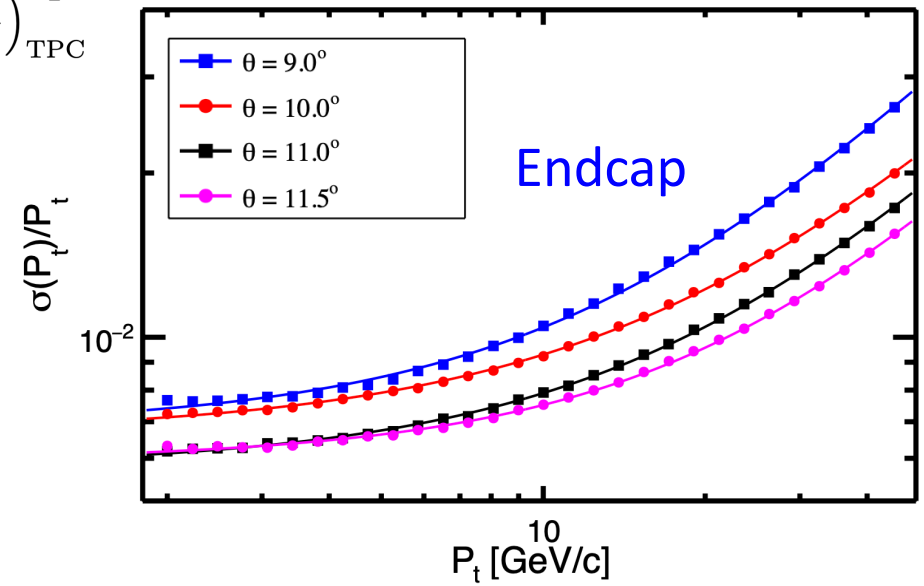
$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{Combined}} = \frac{1}{\sqrt{\left(\frac{\sigma_{p_t}}{p_t}\right)^{-2}_{\text{Si}} + \left(\frac{\sigma_{p_t}}{p_t}\right)^{-2}_{\text{TPC}}}}$$

where $a = 2.1 \times 10^{-5}$, $b = 2.2 \times 10^{-3}$, $s_1 \approx 4$, and $s_2 \approx 0.6$

Full simulation: systematic understanding of the tracker design and its performance







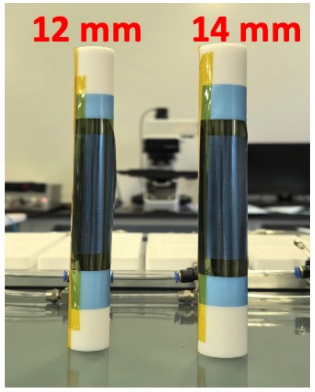
Momentum resolution in the endcap region:

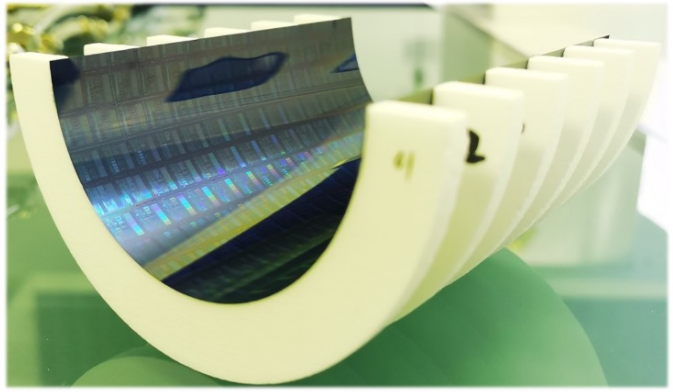
$$\frac{\sigma_{p_t}}{p_t} = \frac{a' p_t}{(tan\theta)^2} \oplus \frac{b'}{\beta tan\theta\sqrt{\cos\theta}} \oplus \frac{c'\sqrt{p_t}}{\sqrt{\beta}(\tan\theta)^{\frac{3}{2}}(\cos\theta)^{\frac{1}{4}}}$$

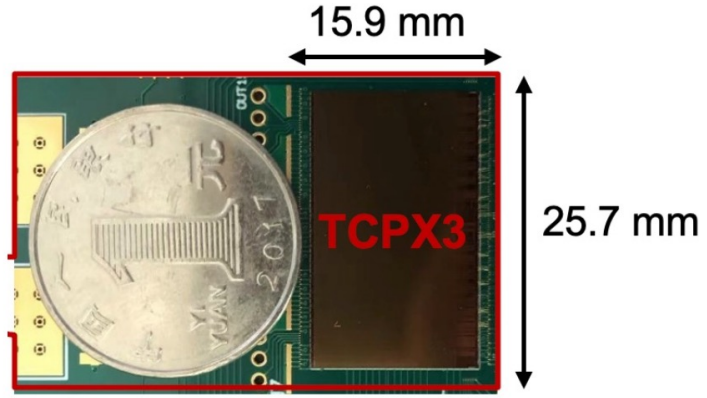
where $a' \approx 1.1 \times 10^{-5}$, $b' \approx 1.1 \times 10^{-3}$, and $c' = 1.2 \times 10^{-4}$

Vertex Detector

Baseline: curved CMOS MAPs, similar to ALICE ITS3



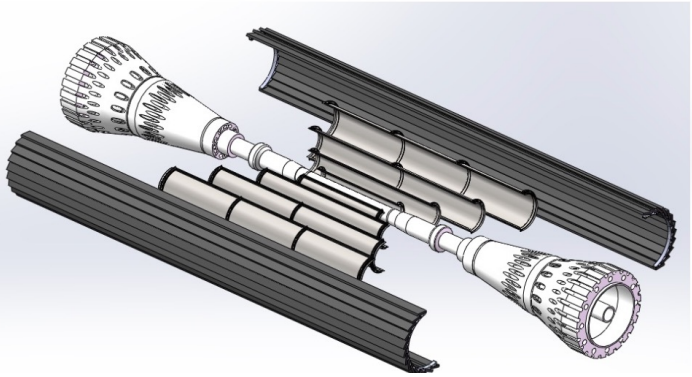


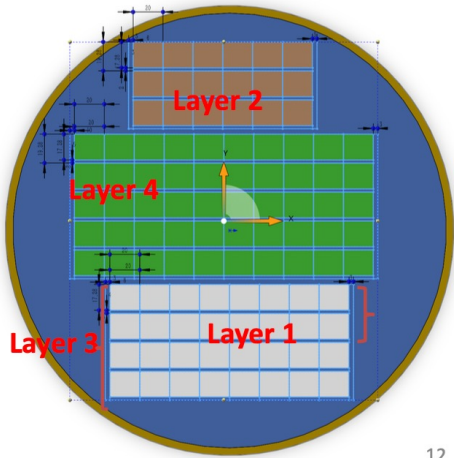


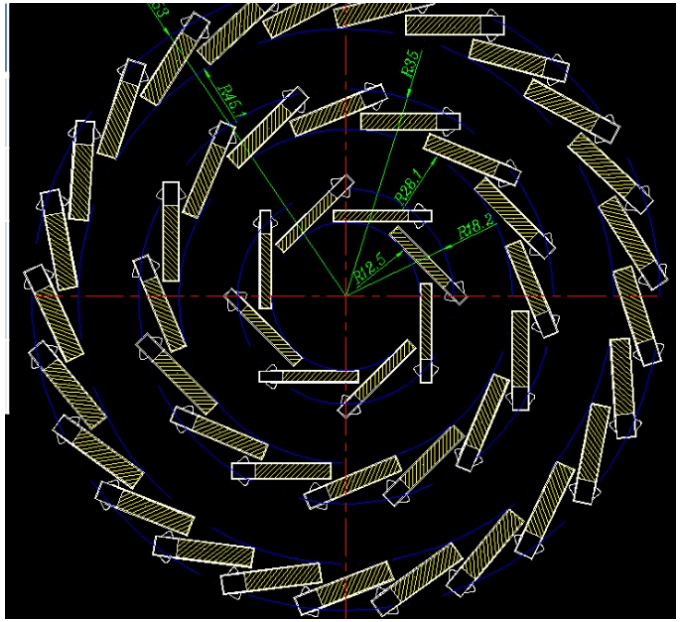
TaichuPix-3 chip vs. coin

layer	Radius	Material
Layer 1	11mm	0.06% X0
Layer 2	16.5mm	0.06% X0
Layer 3	22mm	0.06% X0
Layer 4	27.5mm	0.06% X0
Layer 5/6 (Ladders)	35-40 mm	0.33% X0
Total		0.57% X0

Long barrel layout (no endcap disk)
to cover cos $\underline{\theta}$<=0.991







Backup: long ladder