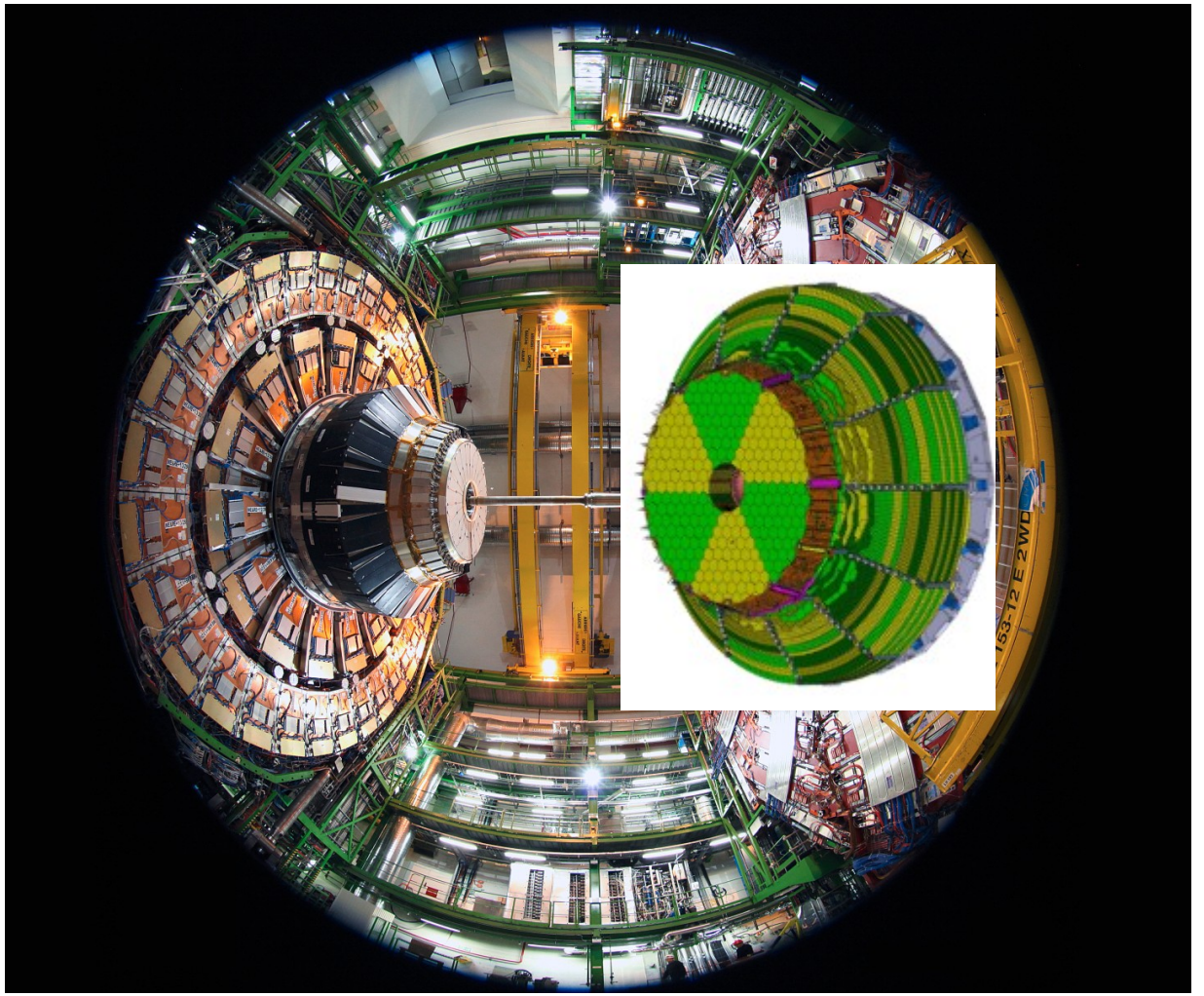
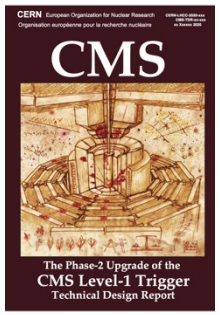
An update on the CMS High Granularity Calorimeter



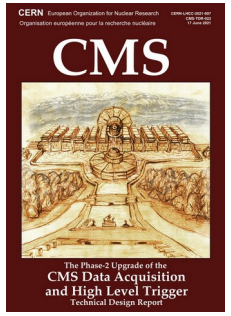
Ludivine Ceard (NTU) on behalf of the CMS collaboration

CMS Phase II Upgrades



L1-Trigger
https://cds.cern.ch/record/2714892

- Tracks in L1-Trigger at 40 MHz
- Particle Flow selection
- 750 kHz L1 output
- 40 MHz data scouting

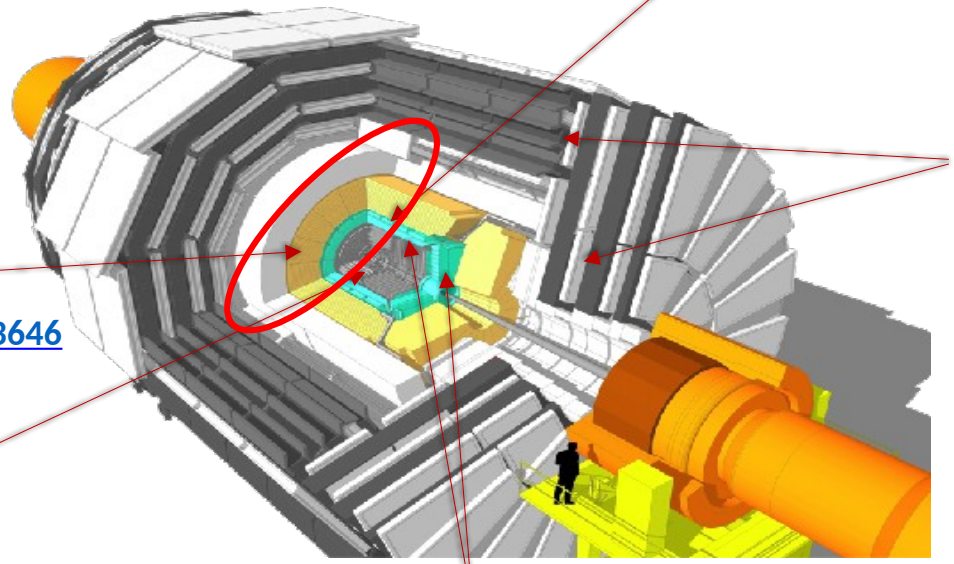


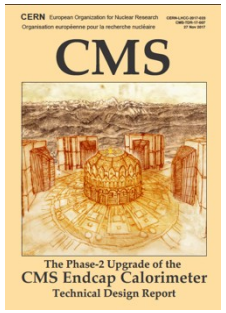
DAQ & High-Level Trigger
https://cds.cern.ch/record/2759072

- Full optical readout
- Heterogenous architecture
- 60 TB/s event network
- 7.5 kHz HLT output

Barrel Calorimeters
https://cds.cern.ch/record/2283187

- ECAL crystal granularity readout at 40 MHz with precise timing for e/γ at 30 GeV
- ECAL and HCAL new Back-End boards



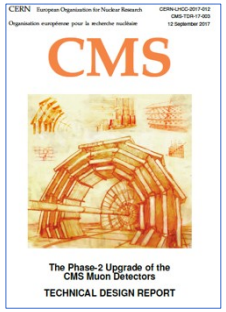


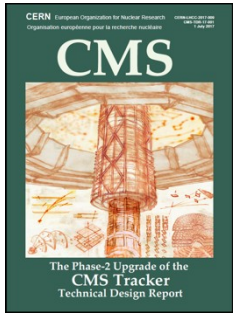
Calorimeter Endcap
https://cds.cern.ch/record/2293646

- 3D showers and precise timing
- Si, Scint+SiPM in Pb/W-SS

Muon systems
https://cds.cern.ch/record/2283189

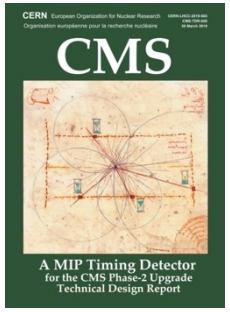
- DT & CSC new FE/BE readout
- RPC back-end electronics
- New GEM/RPC 1.6 < η < 2.4
- Extended coverage to η ≃ 3





Tracker
https://cds.cern.ch/record/2272264

- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to η ≃ 3.8



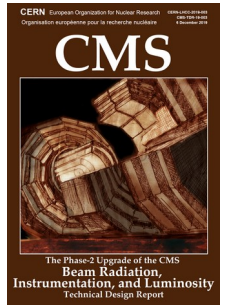
MIP Timing Detector
https://cds.cern.ch/record/2667167

Precision timing with:

- Barrel layer: Crystals + SiPMs
- Endcap layer:
  Low Gain Avalanche Diodes

Beam Radiation Instr. and Luminosity
http://cds.cern.ch/record/2759074

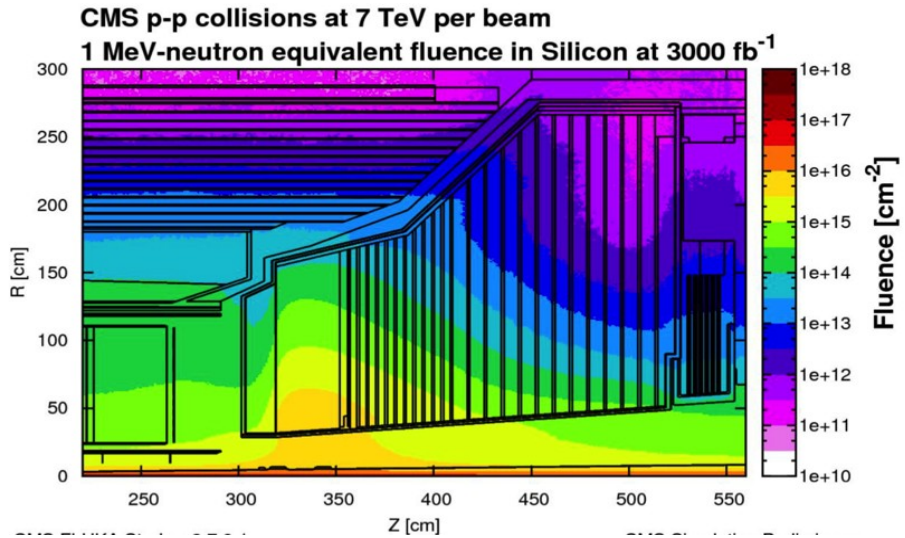
- Beam abort & timing
- Beam-induced background
- Bunch-by-bunch luminosity:
  1% offline, 2% online
- Neutron and mixed-field radiation monitors

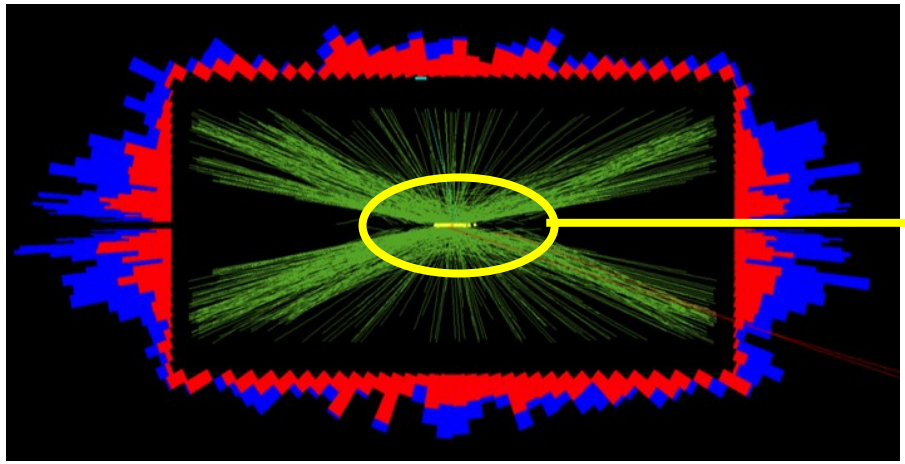


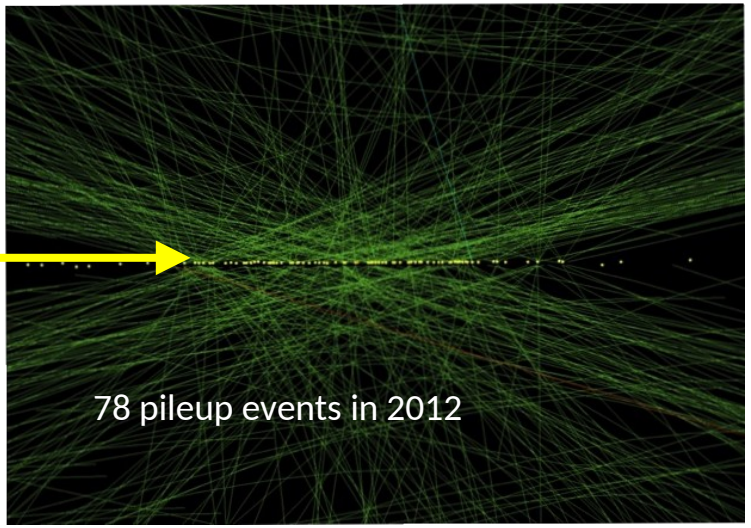
HL-LHC and Challenges

- LS3 starts in 2026
- Lumi 7.5×10^{34} cm−2s−1,
- 3000 fb^{-1} in forward calo.
- up to **200 pileup events**
  - **~10^{16} 1MeV n_{eq} cm^{-2}**
  - up to 2 MGy absorbed dose

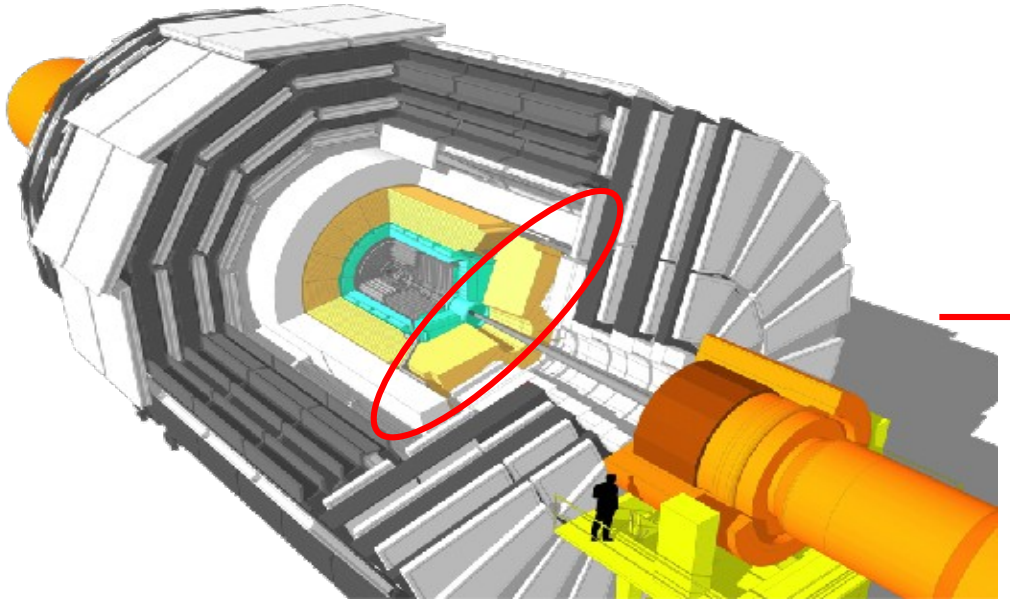
- Need to replace totally the EM and HAD calorimeter endcaps
- By a sampling calorimeter (multi layers)
- Measuring precisely:
  - Energy
  - Time
  - 3D spacial position

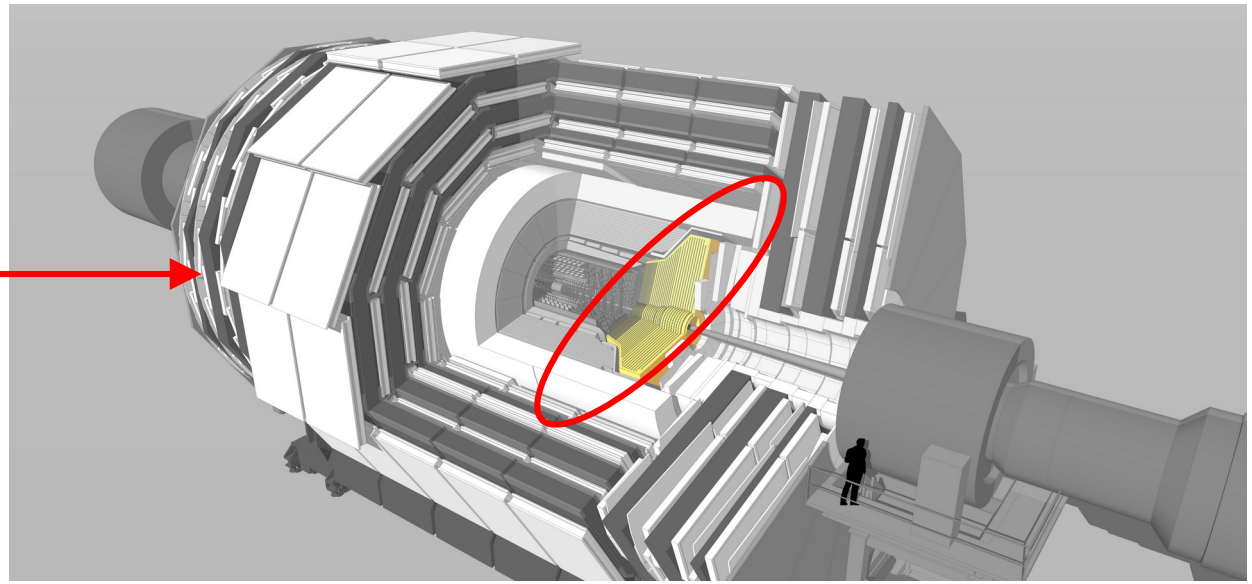






CMS Calorimeters-Endcaps Upgrade



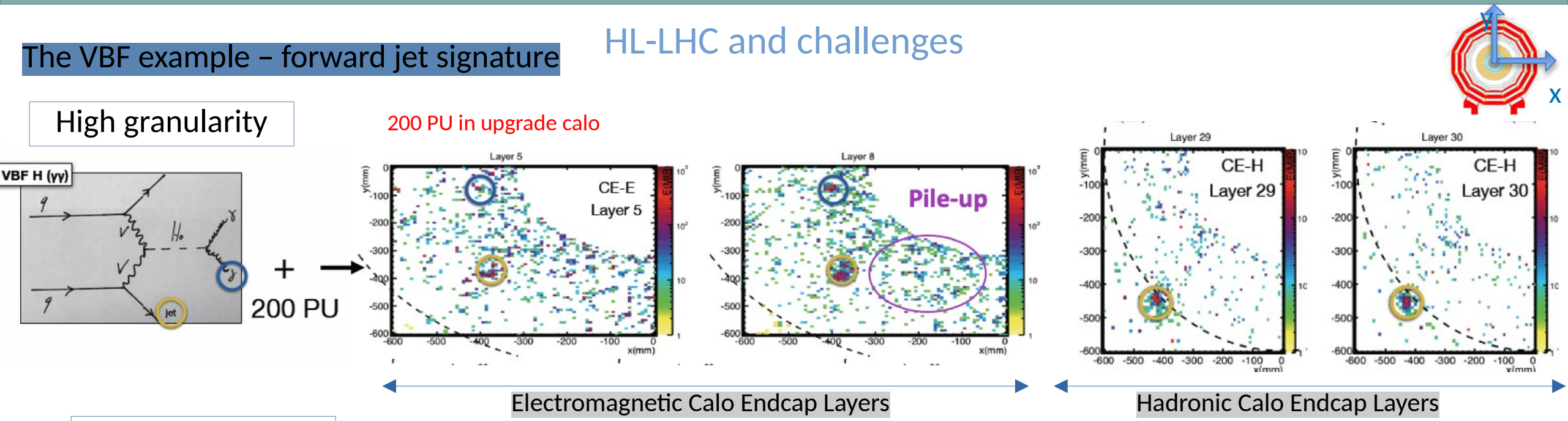


- Long time to decide what type of calorimeter
- Mitigate PU with new electronics rate, high granularity
- Able to survive the radiation, perform E and timing resolution
- Buildable and affordable too

Granularity:
Longitudinal, transverse and timing

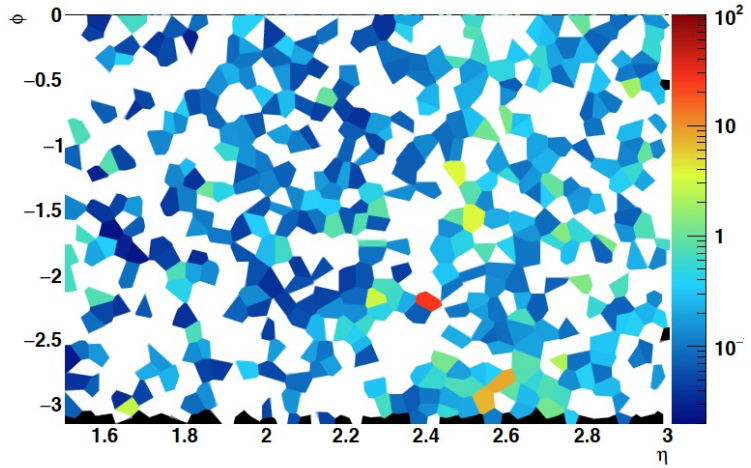
During that process we looked at one of the key process

The VBF example – forward jet signature

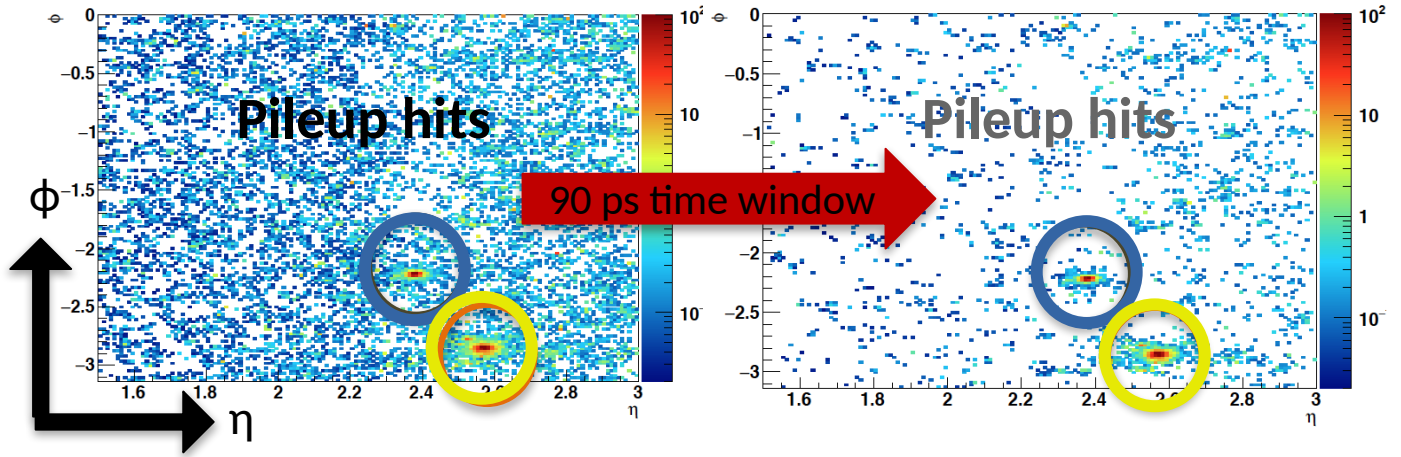


Precision Timing

200 PU in **current** calo (imagining it would not die!):



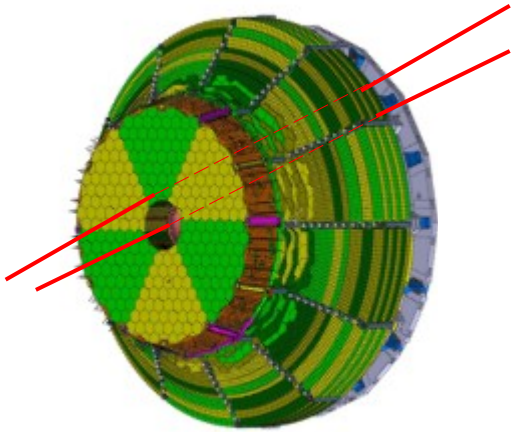
200 PU in **upgraded** calo



HGCAL's solutions and challenges

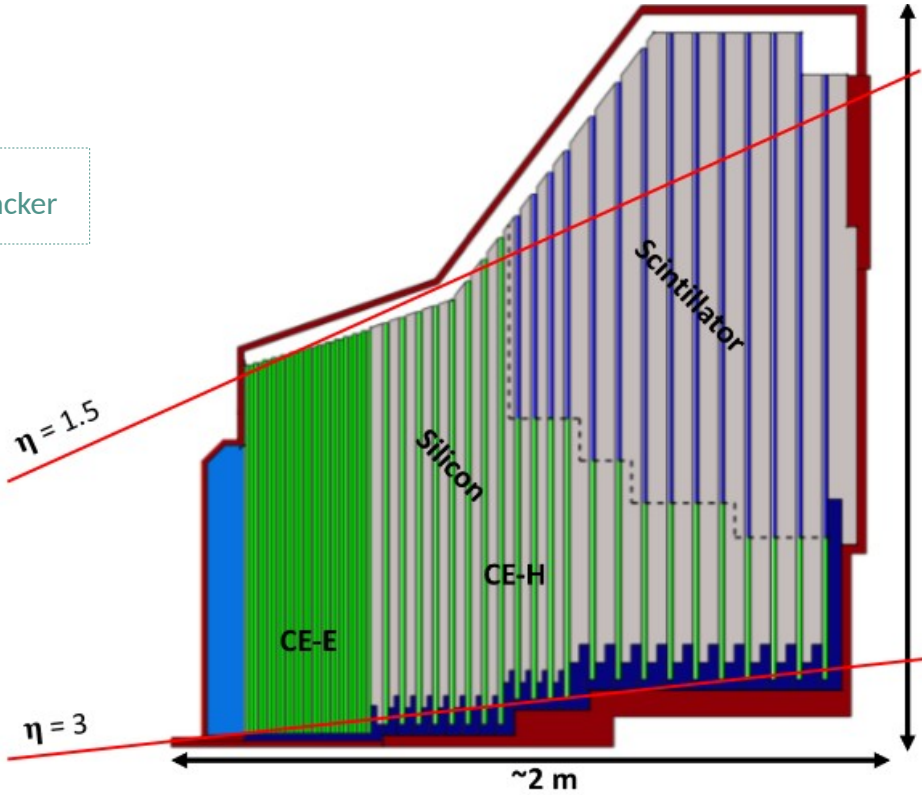
- Transverse and longitudinal granularity
- Timing precision
- Pile up mitigation
- Particle Flow calorimetry for fine structure of showers

→ Tracking in calorimeter

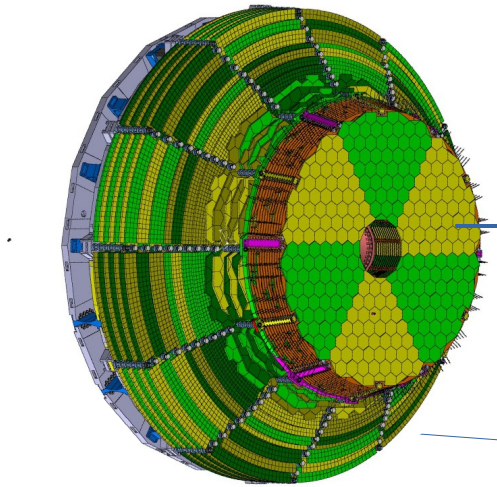


- **Key parameters**
  - 1.5 < |η|<3.0
  - 215 tones/endcap, -30 °C
  - 620 m 2 **Si sensors** – 26K modules, 6M channels
  - 370 m 2 SiPM-on-tile – 4K boards, 240K channels
  - Enables 5D reconstruction of particle showers
- **Active elements**
  - Hexagonal Si modules in CE-E and CE-H high radiation regions
  - Scintillating tiles with on-tile SiPM readout in low radiation regions of CE-H
- **Detector configuration**
  - Electromagnetic part (CE-E): Si, Cu & CuW & Pb absorbers. 26 layers, ~25X 0 , ~1.3 λ
  - Hadronic part (CE-H): Si & SiPM-on-tile, steel absorber. 21 layers, ~8.5 λ

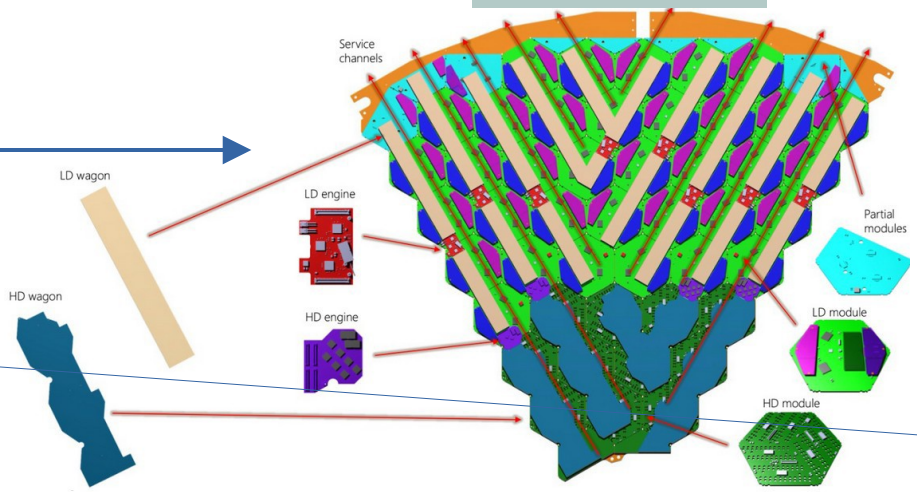
radiation hard
3 times as much silicon as in the present tracker



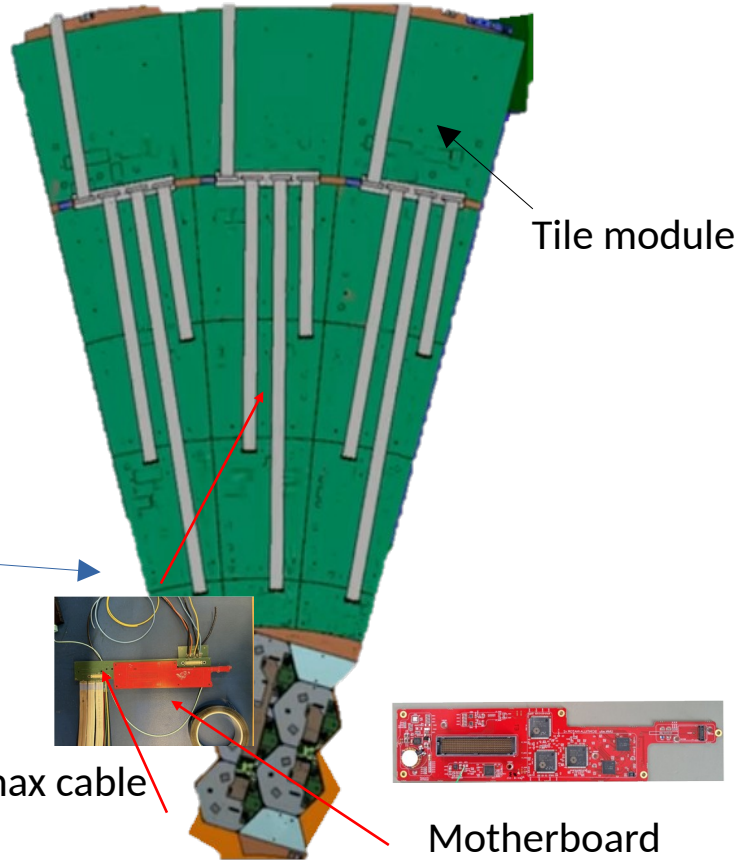
HGCAL's solutions and challenges



Silicon cassette



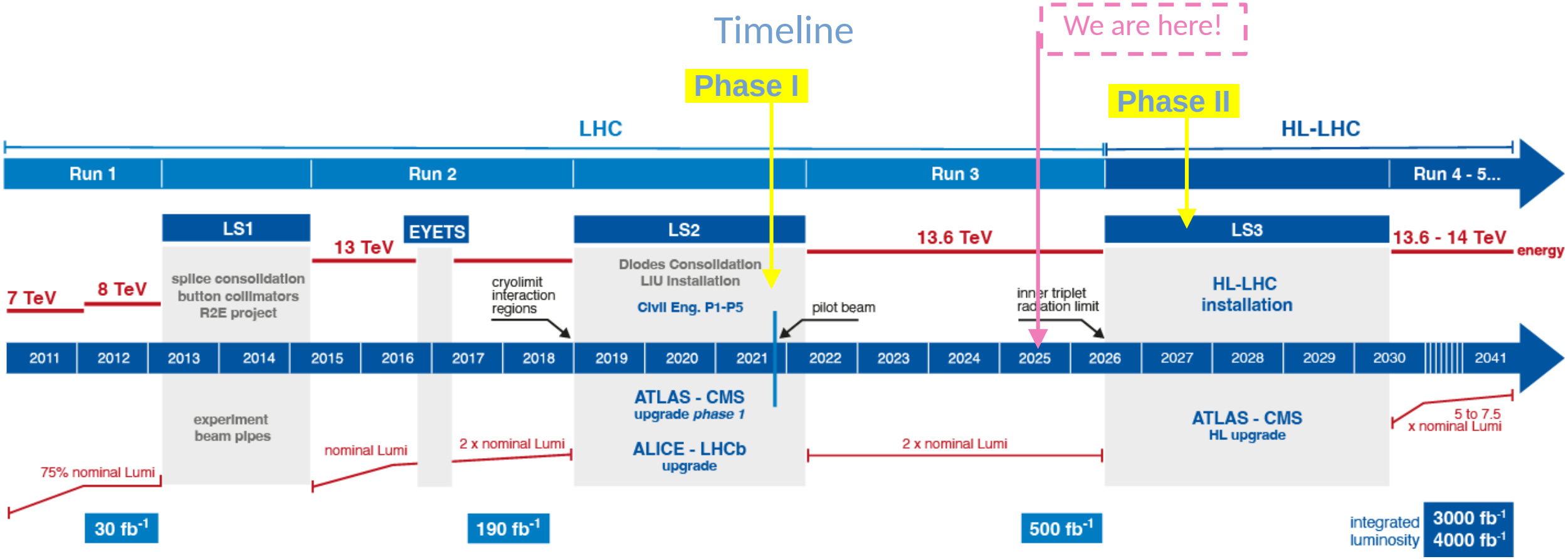
Mixed cassette Si. and Sc.



- Extremely complex, high variety of components
- Density of electronics and service ~ iphone scaled 100k!
- A large dynamic range of large dynamic ranges

Calor. energy measurement	Imaging spatial granularity	Precise timing for showers	Community backgrounds	Detector module variants	Control readout and powering boards variants	Radiation and data rates
• Calibrate on **single** MIP • O(**10^4**) MIP in particle showers • 3000 MIP/cell	• **6M** channels • in 40 m^3 • 10 channels per cell phone • Cell sizes from 0.13 to 30 cm^2	• O(**25ps**) per channel • Energy>10MIPs	• ECAL • HCAL • Tracker • Linear Collider	• 11 Silicon sensor geo. • 12 SiPM on tile geo.	• 4 engines variants • 62 wagons • 10 DCDC mezz. • 59 busbars	* EM shower max.: > 10^{15} n/cm^2 > 25 GB/s * HAD back: < 10^{11} n/cm^2 1 GB/s

Timeline

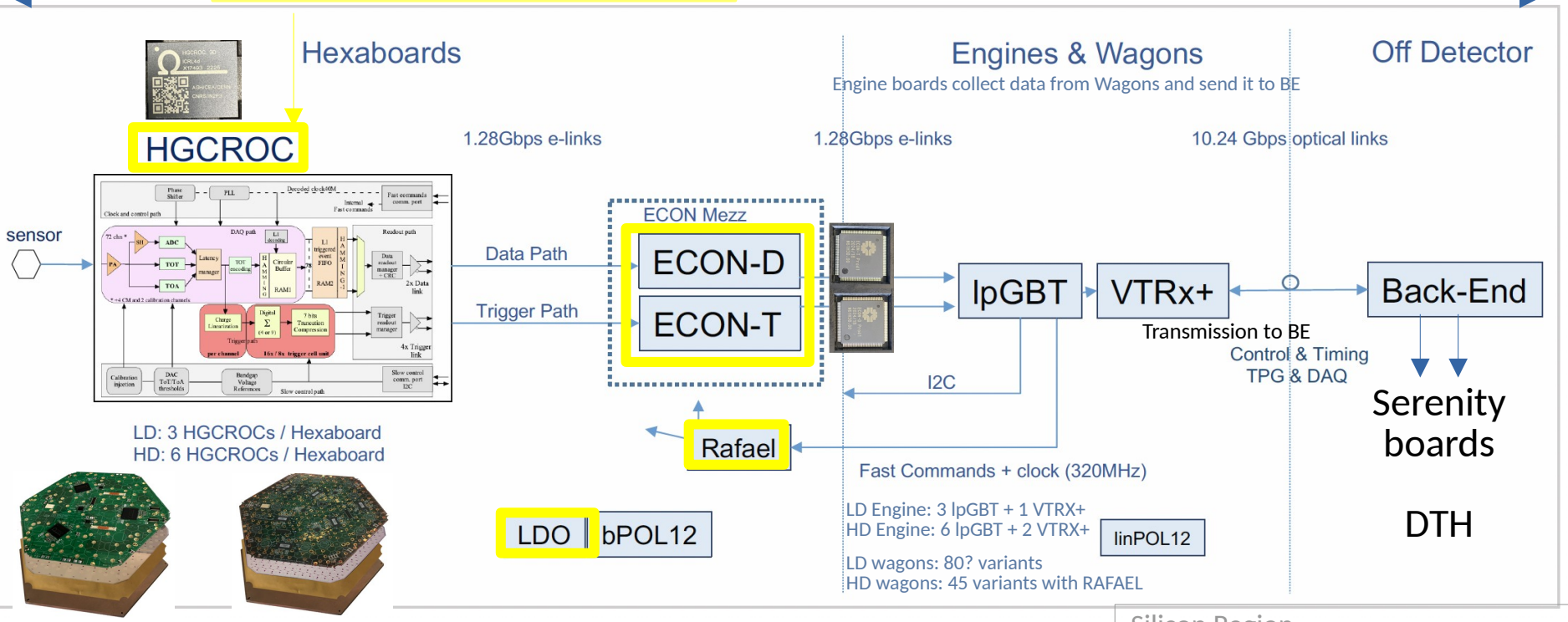


The HGCAL project is leading in parallel:

- Parts in production range from the big (200 tons) to the smalls (5mm)
- Parts going into production
- Parts' validation of final design
- Pre-serie cassette assembly exercise at the 2 CAFs (Cassettes Assembly Facilities) FNAL and CERN

- Large dynamic Range: ~ 0.2 fC to 10 pC
- 10bit ADC below ~50fC
- 12bit ToT above
- Timing information (ToA) down to 25ps

Electronic Chain



Tried to use as much CERN generic developments as possible

But had to design
- our readout and FE ASICs
- clock distribution chip
- low drop out regulator

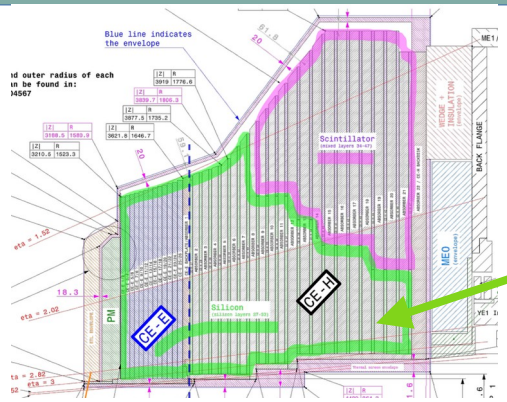
Silicon Region
Scintillator region: SiPM HGCROCs
GBT_SCA for SC
ALDO

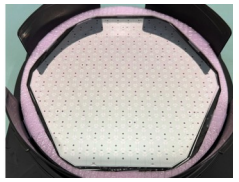
In production:
- 100k of ASICS (some already fully in hands)
- Control readout and powering PCB boards (Engines and Wagons)

Going in production:
- Engines and Wagons assembly, ECONs Mezzanine, DCDC converters, Busbars, Serenity boards

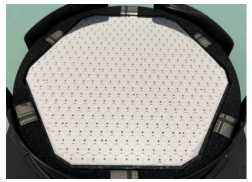
Pre-series:
- partial concentrator mezzanine

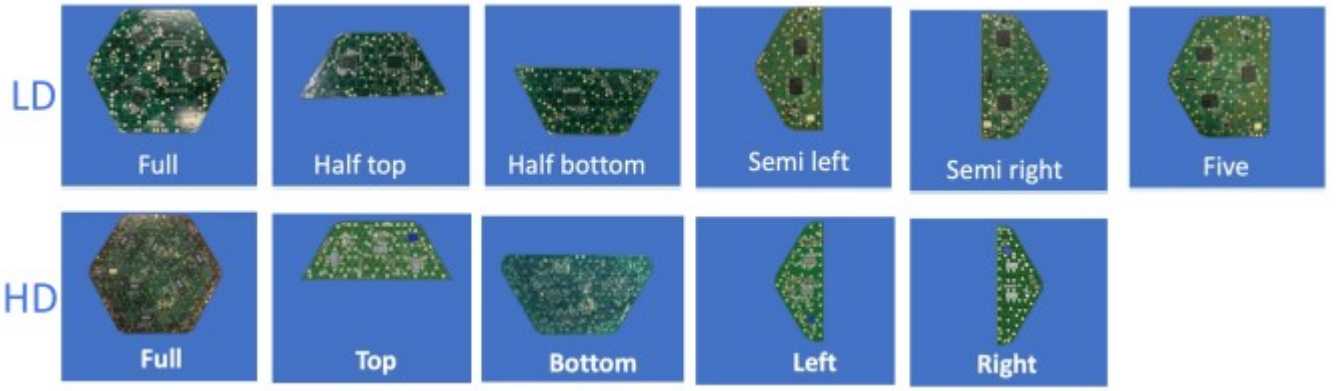
Silicon modules





20.3 cm





Completed

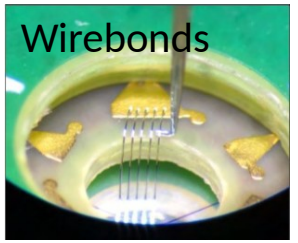
- 95% of silicon sensors delivered (consistent excellent quality)
- 5 modules assembly center (MACs) qualified + 1 being qualified
- All variant types of modules have been exercised and used to build systems

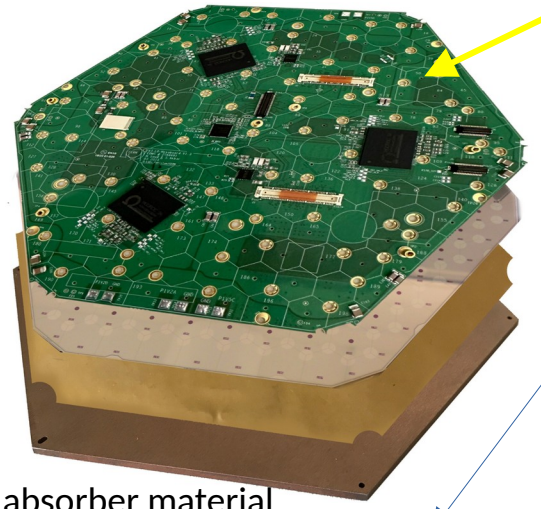
In production:

- Assembly of all hexaboards variants with electrical components
- 27k of hexaboards
- 27k of baseplates Ti for CE-H and CuW for CE-E

Going in production:

- Mass assembly at MACs





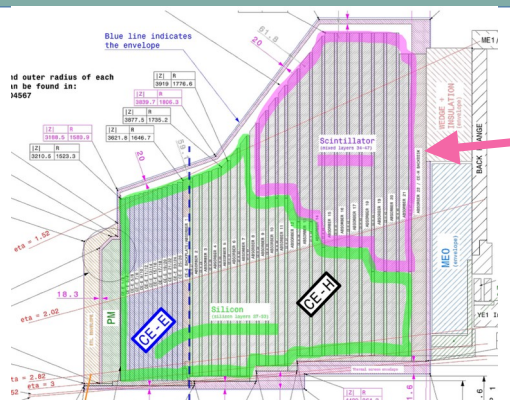
Hexaboard PCB
Hosting the readout chips

Silicon Sensor

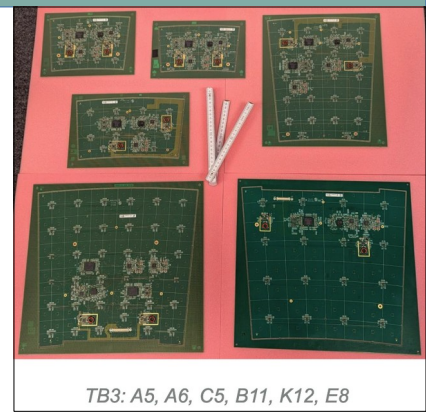
Metalized Kapton Sheet
CuW or Ti BasePlate
Rigidity, contributes to the absorber material

12 cm

Scintillator modules



Cell sizes from 4 to 30 cm^2



Tileboard PCB
Readout chips on the back

Wrapped scintillating tile
Reflective foil

Completed:

- 100% of SiPM delivered (consistent excellent quality)
- 2 Tiles Manufacturing facilities: Cast in NIU and Molded at FNAL (US)
- 2 Tiles Assembly Facilities Qualified: DESY (DE) and FNAL (US)

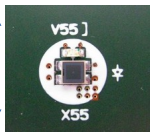
In production:

- Molded tiles
- Cast tiles machining
- Bare tileboards
- Tile wrapping DESY (including all special tiles)

Going in production:

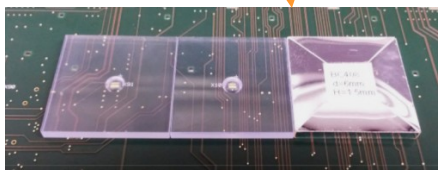
- Tile wrapping NIU
- Tileboards assembly with HGCROC
- Tile modules assembly
- Wing-boards and Twinax cables

0.4 cm



Si Photomultiplier (SiPM)
Calibration with LED

2 cm



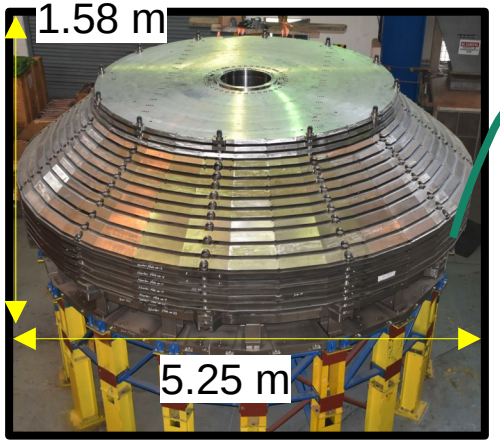
Scintillator tiles

Mechanics and Engineering

Completed

First endcap CE-H1 absorber! In PAEC/HMC3

- absorber disks, support cylinders, split rings, wedges assembly
- Swivel test done ! Equivalent to swivel a 200 tons iphone!
- then partial disassembly and shipping to CERN



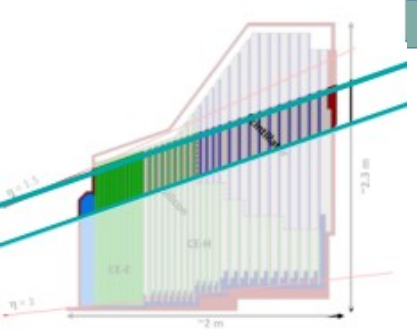
In production:

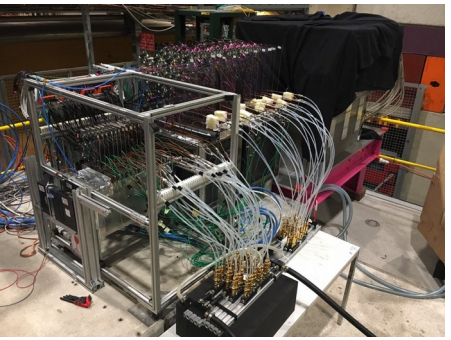
- CE-H endcap 2 absorber machining
- CE-E back plates machining
- Thermal screen
- On-detector CO_2 manifold
- Tooling for CE-E assembly

Going in production:

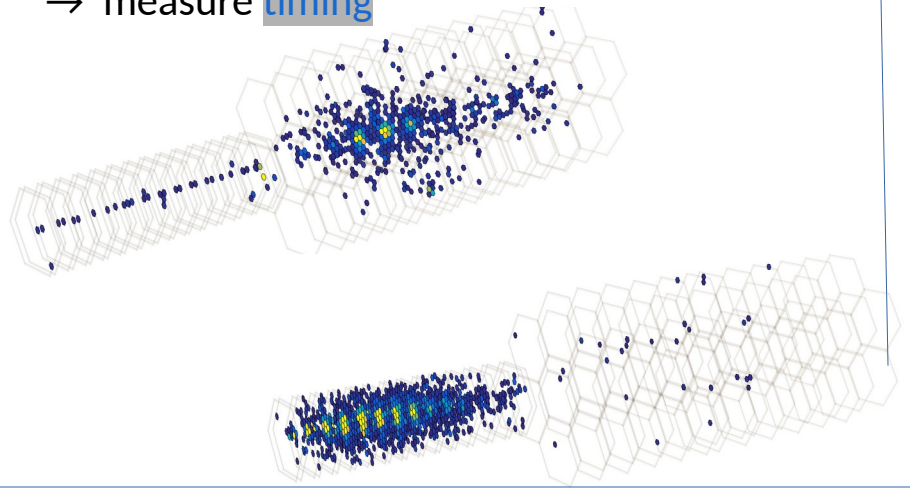
- CE-E lead/stainless steel absorbers
- YE1 CO_2 Cooling distribution manifolds

System testing: beam test and others

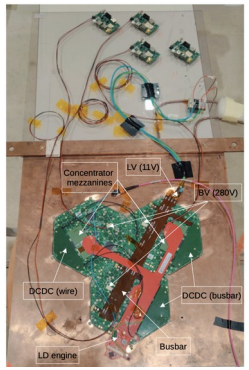


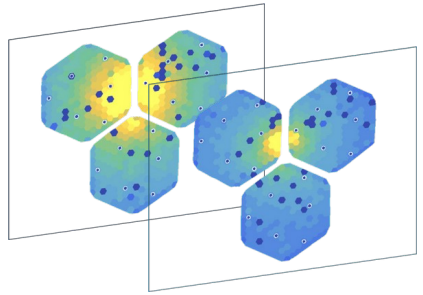


- 2016-2018 : **100 modules calorimeter**
  → measure E and resolution EM and HAD
  → measure timing

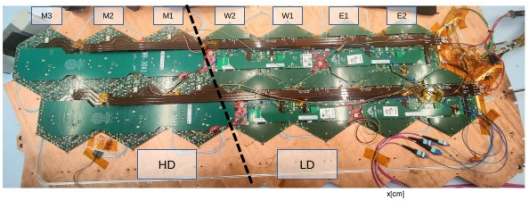


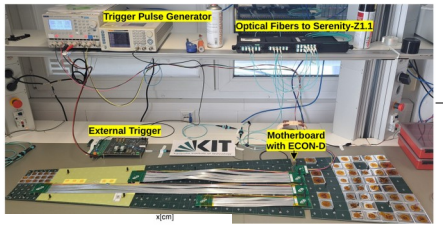
- Since 2021 **electronics closer and closer to final** electronics
- 2023 1st test with full electronic chain
- 2024 scaling up

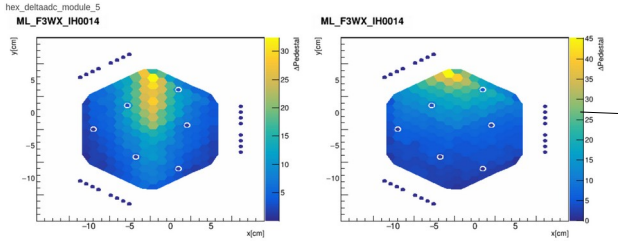




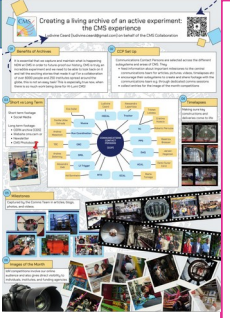
Poster #893 in 14A





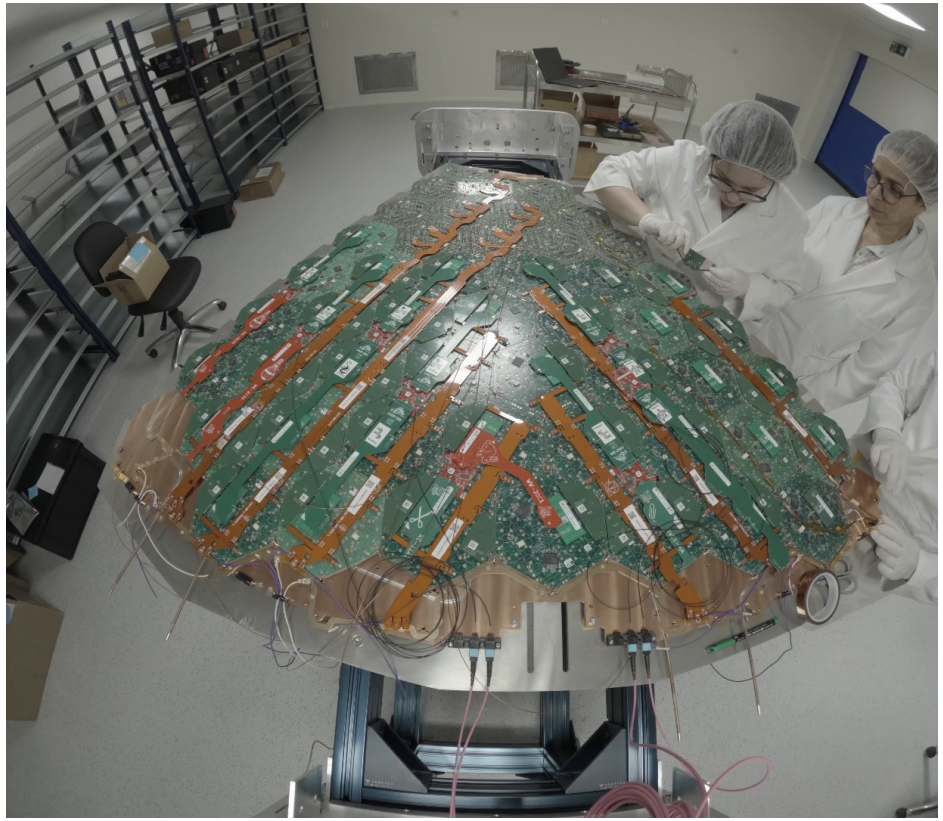


Validation of with "ESR2" silicon system	Basic functionalities Clock distribution Noise measurement Trimming and Calibration will V3 system High rate tests
Validation with single train systems	Cold tests With partial hexaboards
Beam test with magnetic field	MIP and S/N Timing performance Comparison of DAQ and TPG data

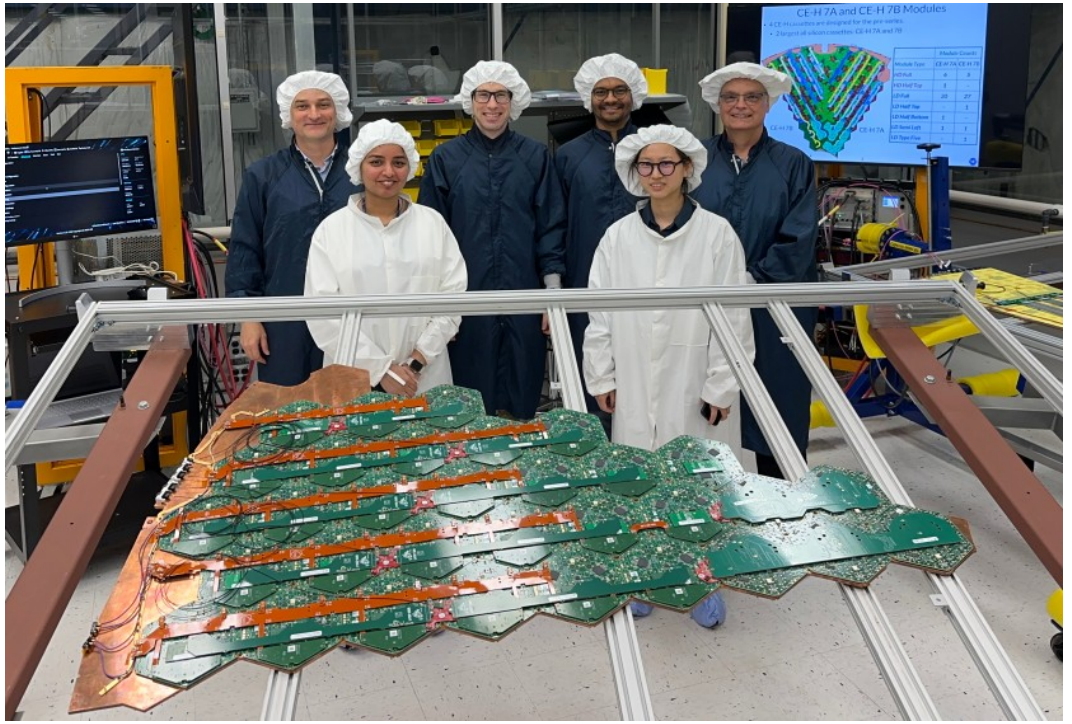


Poster #439 in 21C

CEE and CEH cassette assembly



CE-E Layer 25 at CERN

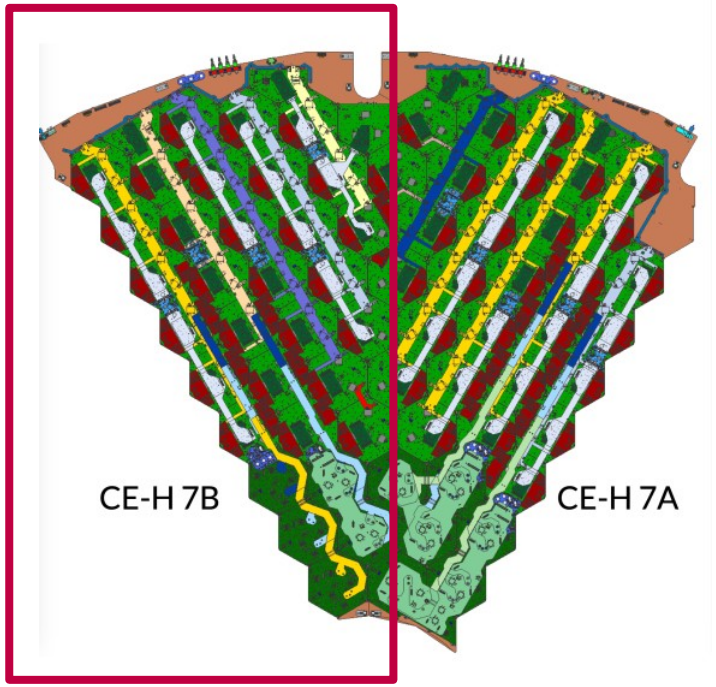


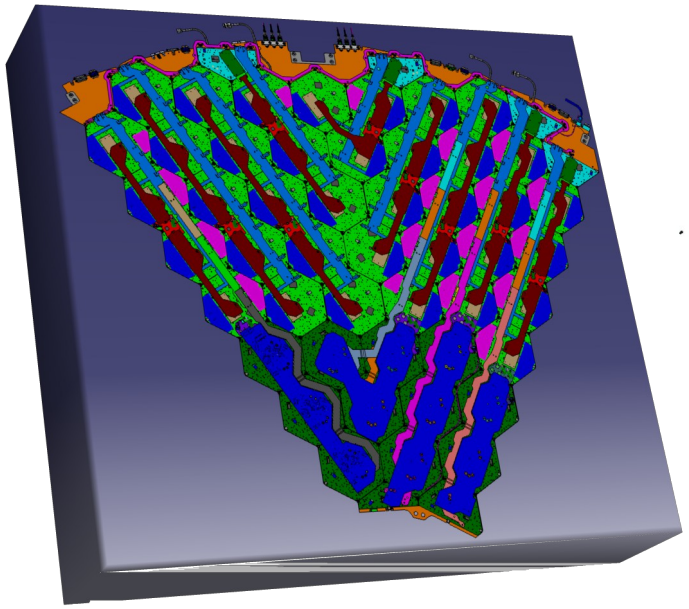
CE-H 7B at FNAL

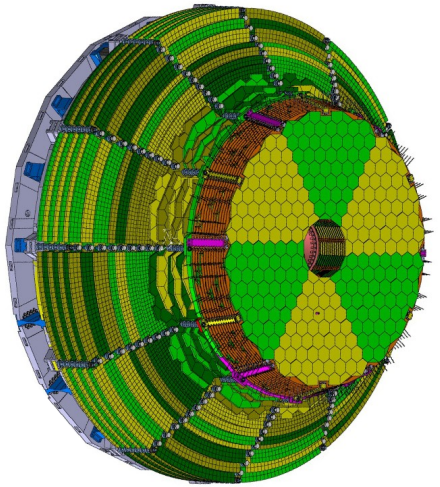
- Assembly in clean rooms at CAFs
- Majority of components
- Integration check , powering check

Wrap-up and future

From concept

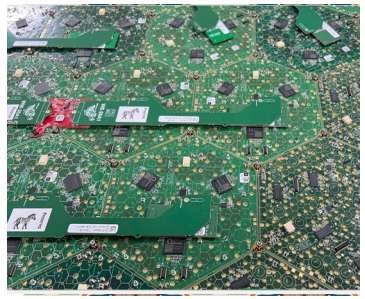


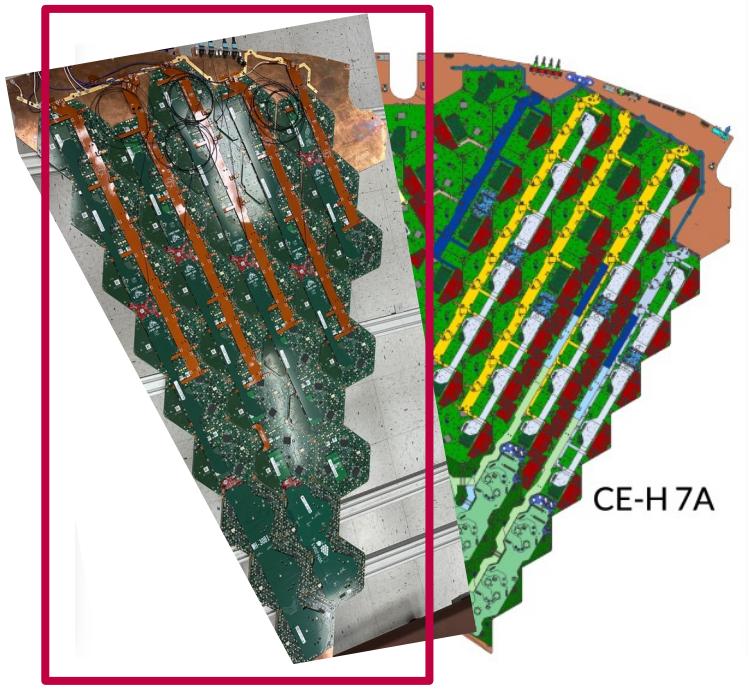


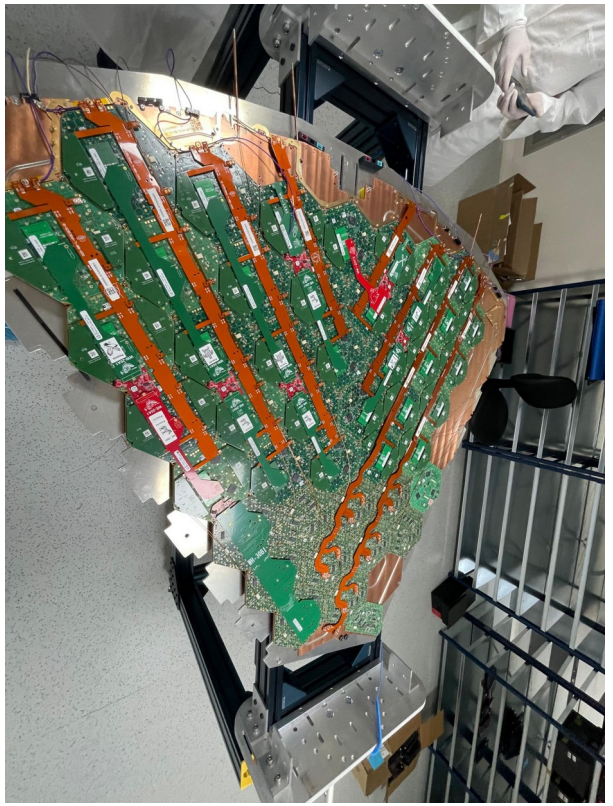


Wrap-up and future

To reality

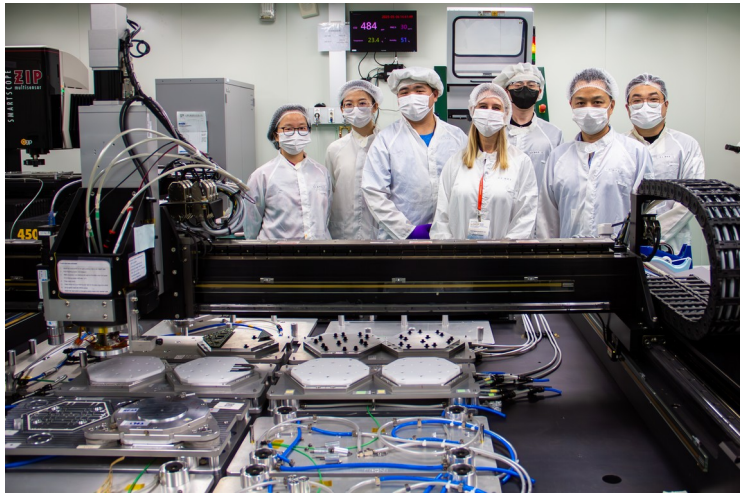




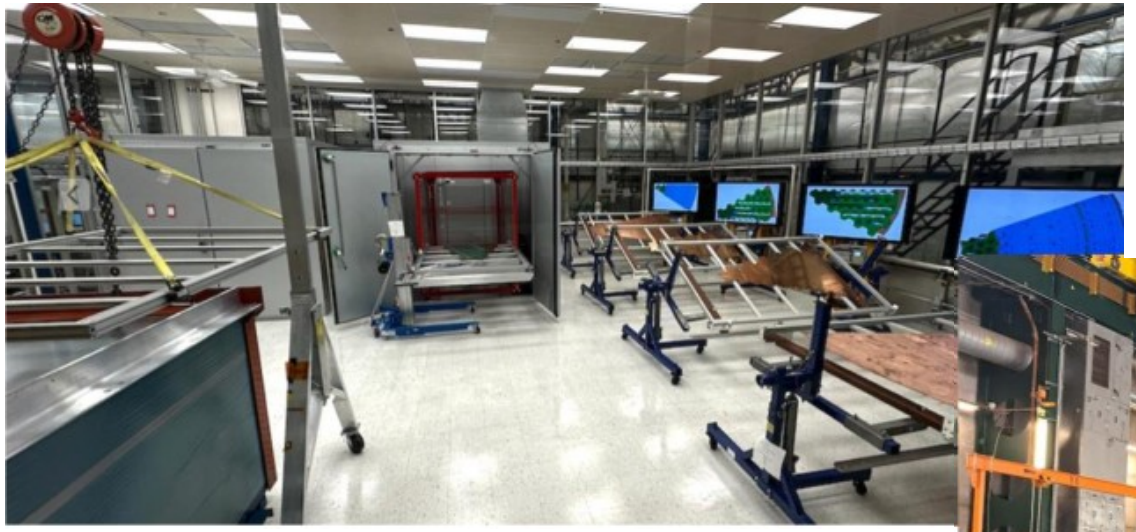


Wrap-up and future
#LifeWithHexagons

- We are in production of an unprecedented detector kind
- We are learning to build and operate it
- Exciting times ahead!



Module Assembly Center NTU

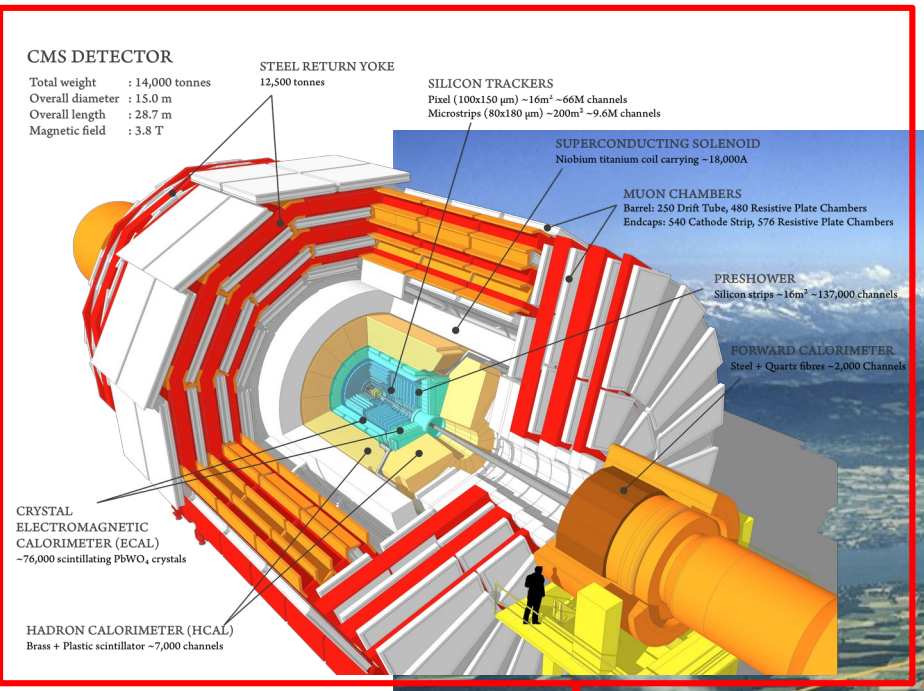


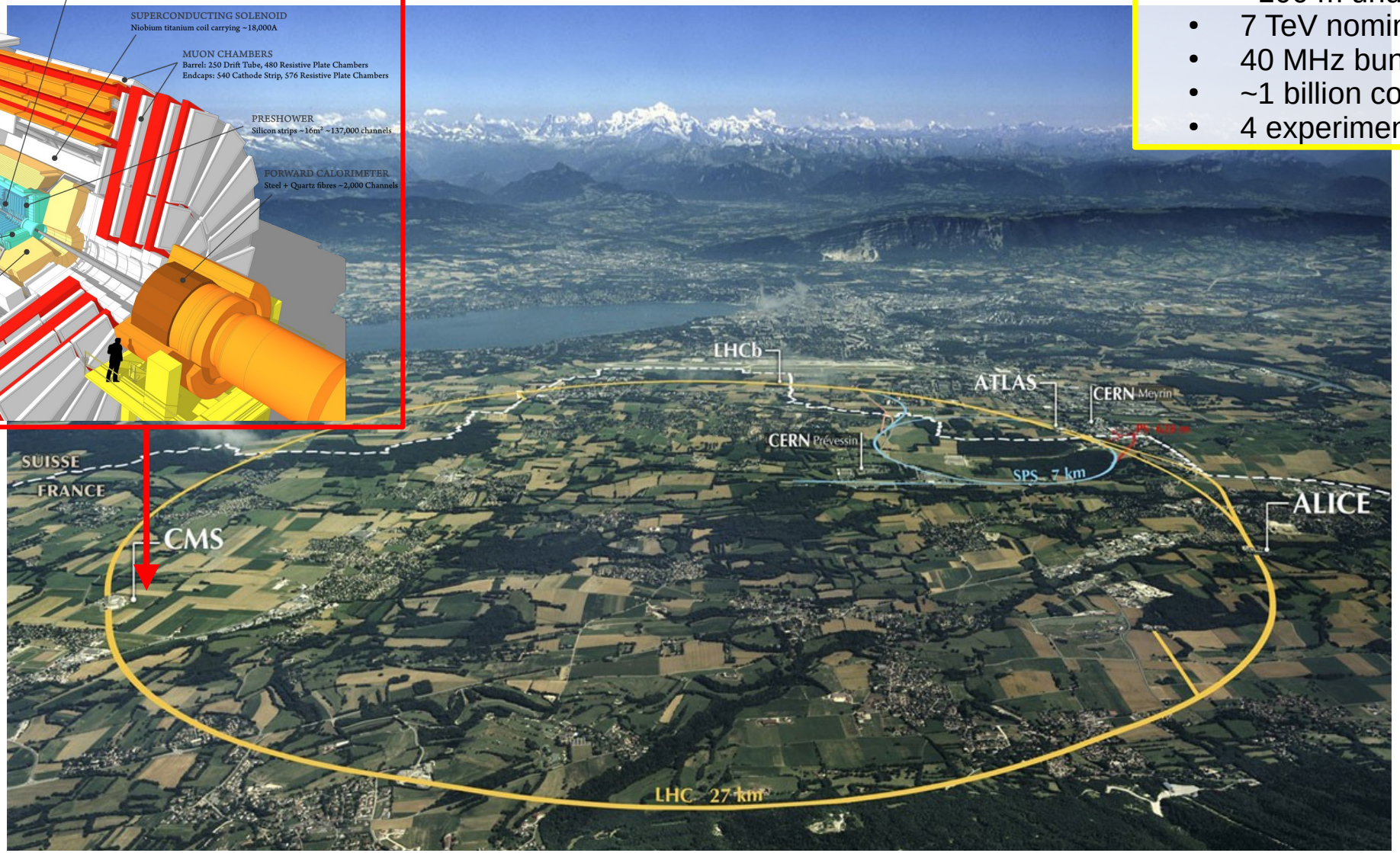
Clean room FNAL

Assembly Hall CERN

BACK UP

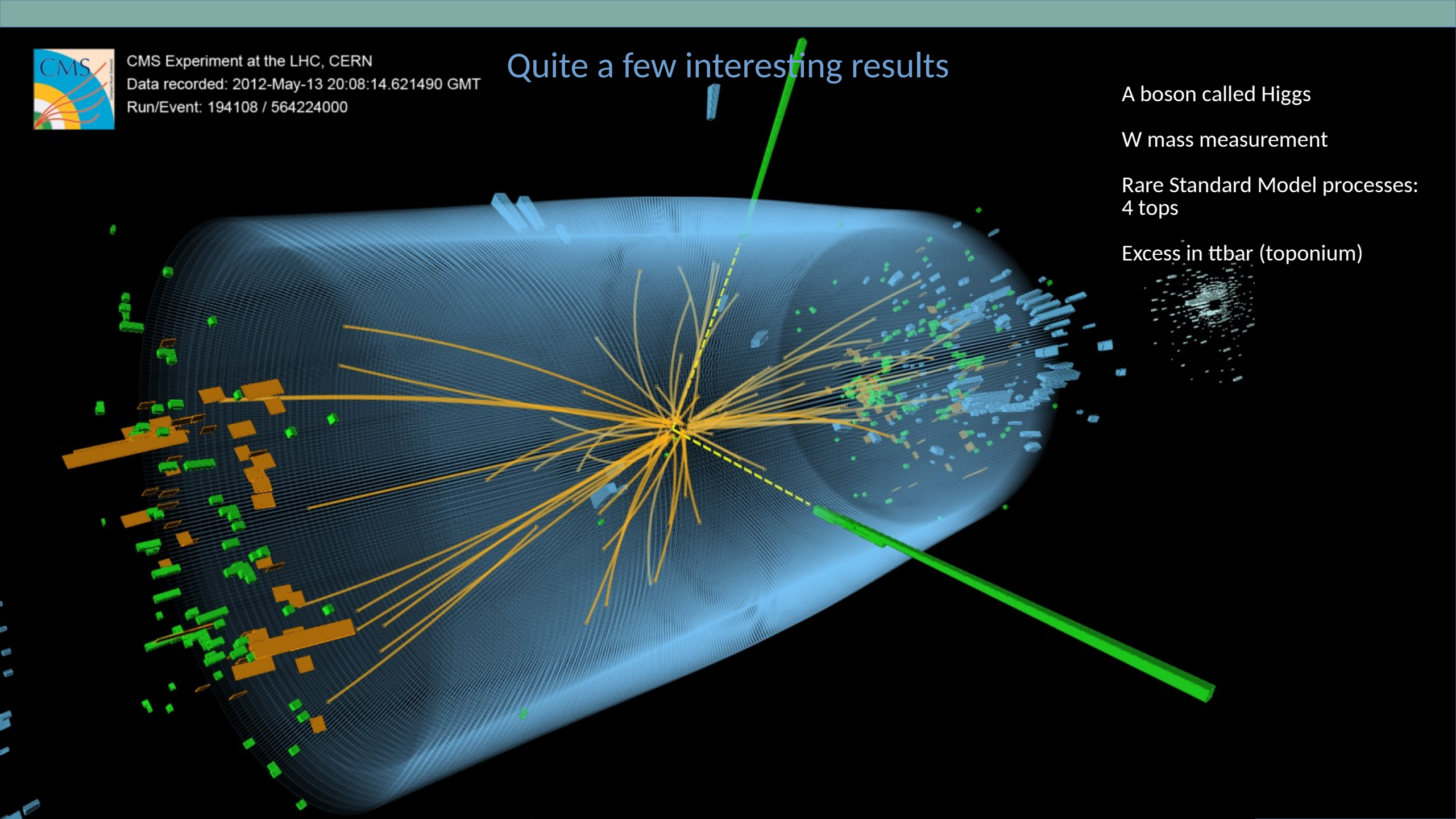
The LHC and CMS





- 27 km circumference
- ~100 m underground
- 7 TeV nominal beam energy
- 40 MHz bunch crossing rate
- ~1 billion collisions / s
- 4 experiments

Quite a few interesting results



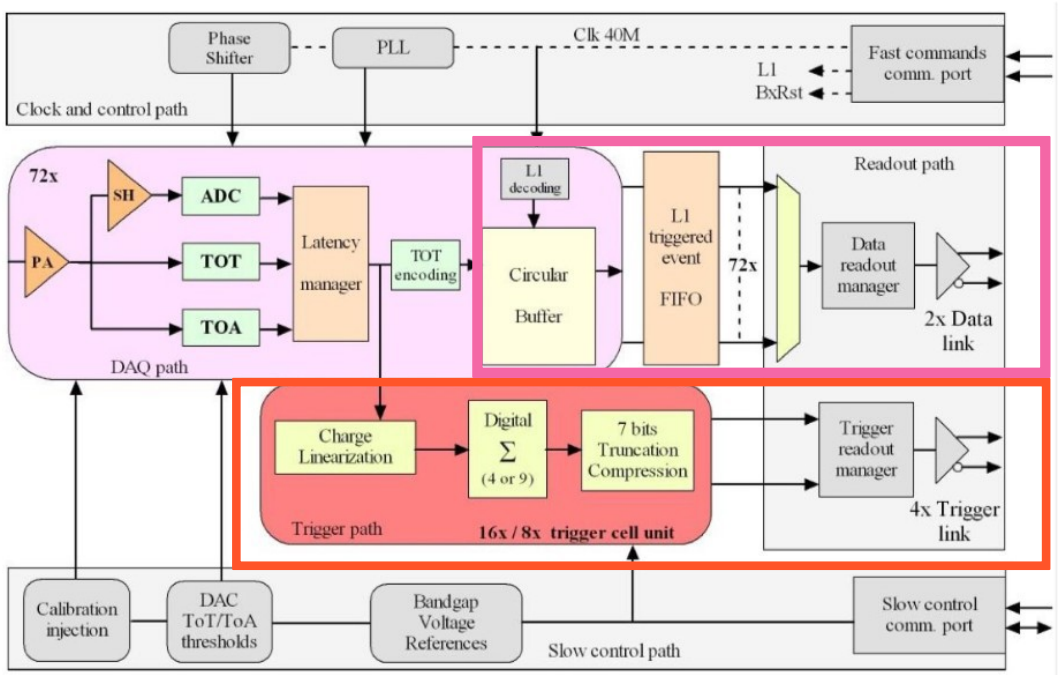
A boson called Higgs

W mass measurement

Rare Standard Model processes: 4 tops

Excess in ttbar (toponium)

Electronic Chain



Synchronous fast control @ 320 MHz

DAQ path
Data packets after LV1A

Trigger path
Trigger primitives @40 MHz

Asynchronous slow control I2C

HGCROCs versions details

HGCROC

3b packaged devices @ Omega Feb 2024

HGCROC3b used in system tests, test beams and performance studies.

Some 3b Issues related to the TDC
1, TOT Hole
2, TOA & TOT Outliers
3, SEE – Digital I pulses (FIFO Tri-state driver conflicts)
4, SEE – Analog I pulses (TDC not working)
5, SEE – TOA Gray Encoder errors
I2C
ESD

Deep Dive with CEA/Omega & ESE/Chips
Goal: To examine each item in the list together with their possible design solutions. Make suggestions where appropriate on simulation techniques or additional tests that would be useful.
Summary documentation on the HGCROC Deep Dive.
https://indico.cern.ch/event/1429271/

HGCROC3c submitted in July/August 2024
Metal fix only changes

The review involved Jorgen, Kostas, Jan and Xavi

3c packaged devices @ Omega Nov 2024
Function and SEE tests in Dec. 2024
The 3 most serious 3b issues were solved in 3c (TOT hole, Outliers and I2C).
In fact all issues solved except bug 5.

Bug 5 now affects both TOA and TOT whereas in HGCROC3b it only affected TOA.

HGCROC3d & HGCROC3e designs

HGCROC3d > Quick metal fix to keep all successful changes from 3b but to restore bug 5 to the 3b condition.
HGCROC3e > Full engineering run to replace the asynchronous counter with a synchronous counter with TMRG.

HGCROC3d could be submitted quickly but HGCROC3e would need more time and not be available for the initial stages of module production

HGCAL HGCROC Operations and Physics Impact Task Force
Goal: To understand the physics impact and operational impact at system level of HGCROC3c and HGCROC3d

HGCROC Task Force - Summary & Conclusions

Summary:

- HGCROC3x is a series (a,b,c,d,e) implementing the full HGCAL TDR architecture
- The current version in our hands and in our test systems in HGCROC3c.
- HGCROC3c works well but suffers from SEU induced errors on both TOA and TOT.

- 2 additional versions are in the design flow.
- HGCROC3d …… Designed to be robust against SEU errors on TOT but they will remain for TOA (6.5ns jumps)
- HGCROC3e …… Designed to be robust against SEU induced errors on TOA and TOT.

- HGCROC Task Force …. Set up to examine the operational and performance impact of using HGCROC3c in the back of CEE and CEH.
- This is to allow Hexaboard and module assembly to begin and not to have an impact on our module assembly schedule.

- The HGCROC3c behaviour can be summarised by a state diagram with 3 states (S0, S1 & S2).
- Transition between the states can be induced by SEUs.
- S0 & S1 have no errors for TOA & TOT. S2 is a problematic state which can produce errors on TOA & TOT.

- The probability to reach S2 can be greatly reduced by I2C procedures we call “inoculation”.
- If a chip reaches S2 it can be reset to S0 via a power cycle during the ”inter-fill” gaps.
- Inoculation and power cycling can reduce the number of chips in the problematic S2 state to negligible numbers

- The impact on Physics & Trigger Performance has been studied in worse case conditions, assuming no inoculation or power cycling:
- The errors are manageable and the impact on HGCAL performance considered as “mild”.

Conclusion:

- The inoculation & power cycling procedures are very powerful, they can reduce the number of chips in the problematic S2 state to negligible numbers hence negligible impact on HGCAL.

- Even without inoculation, the physics performance impact on HGCAL is considered “mild” providing 3c only used in the CEE and CEH back layers.

- The HGCROC Task Force (whilst still on-going) has verified our strategy of proceeding with hexaboard and module production using HGCROC3c and their deployment in the back layers of CEE and CEH. HGCROC3d and 3e designs continue in parallel and will be inserted into the production flow when verified and available.

- This strategy avoids negative impact on the HGCAL module production schedule

ECON D

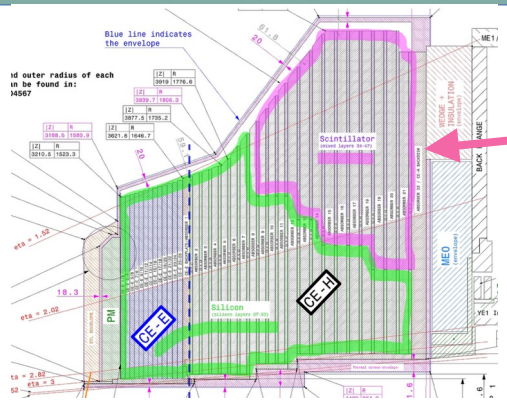
S-RAM error particularly BIST (Built in Self Tests) which fails n some fraction of chips at a higher supply voltage than observed on prototype batch

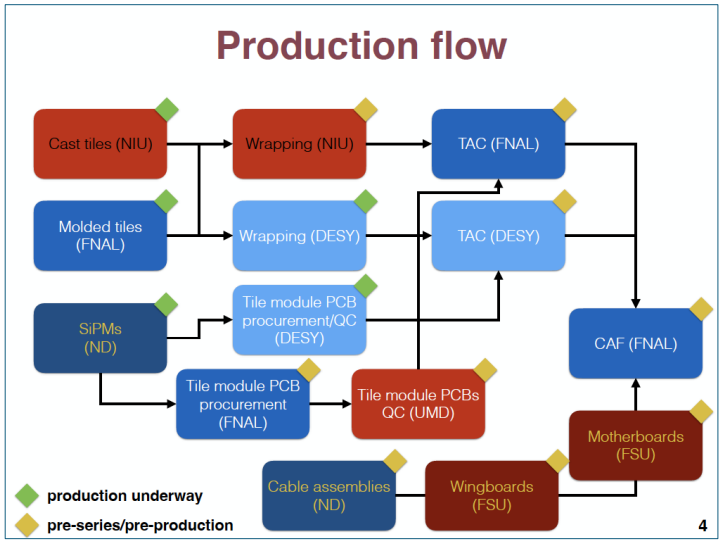
This can be considered a yield issue = many spare should be available

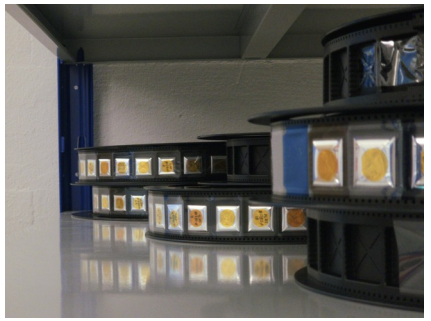
Critical voltage T and D dependent so need to carefully define the margin for acceptance

TID test up to 660 Mrad

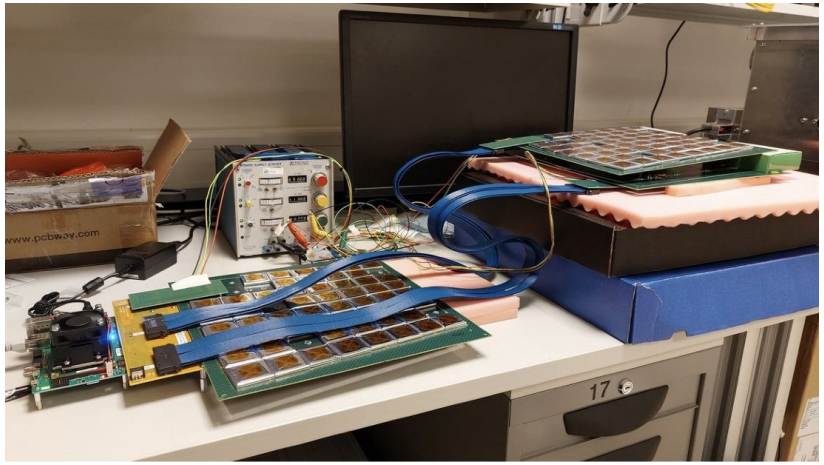
Scintillator modules



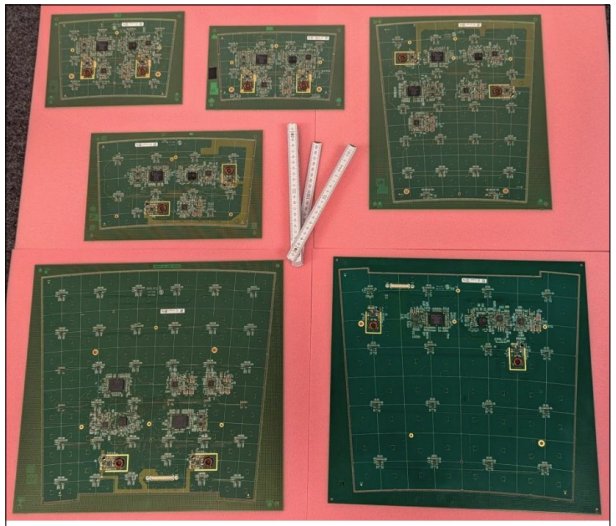




FNAL TAC pick-and–place machine for tile-module assembly



Tile-module test stand at DESY



TB3: A5, A6, C5, B11, K12, E8

System testing: others

ESR2 system : integration test, clock quality, noise
Similar syst cold test
Calibration and operation

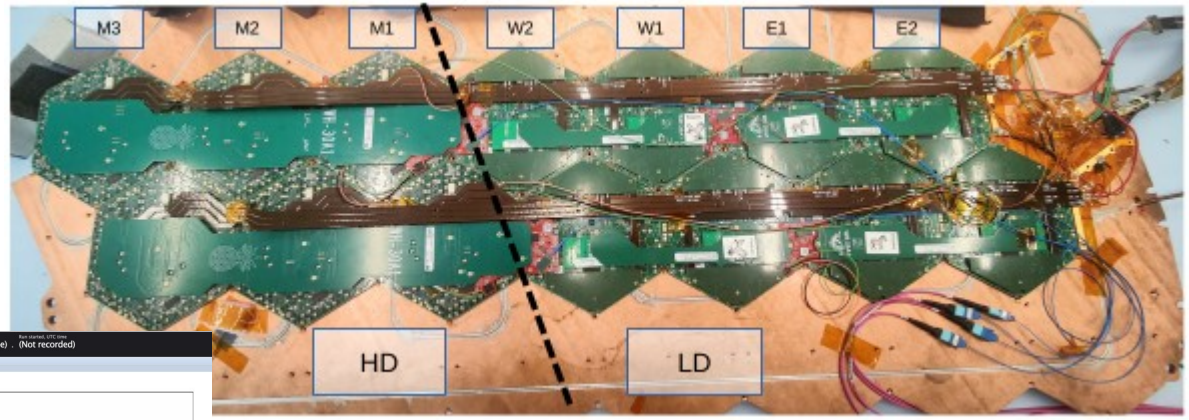
SiPM on tile system chain with Serenity BE operating at KIT

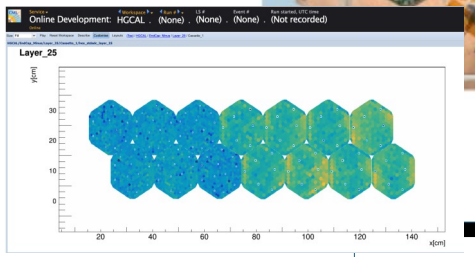
Multi-train si module system test cat CERN with HGCROCsv3C, LD and HD
(14 module son pre-serie cu plate) silicon full electronic chain

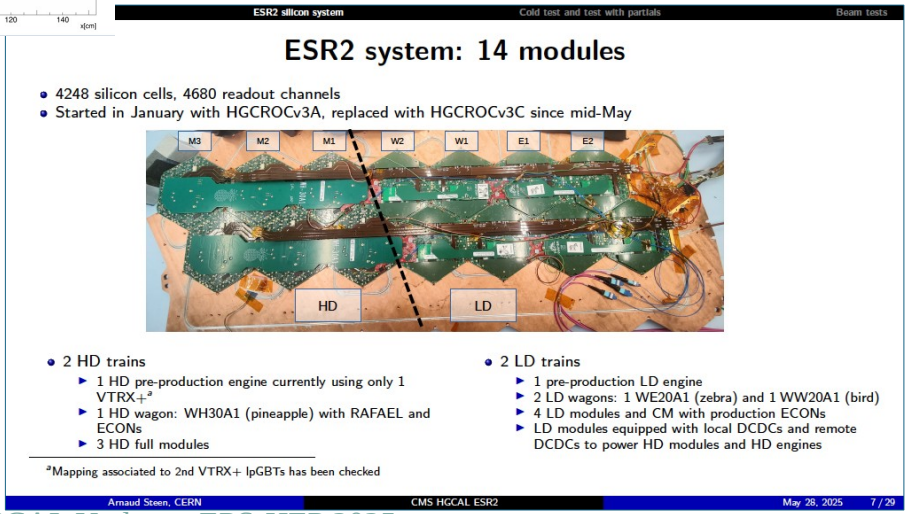
Magnet test up to 3T: to test HD trains → results

Sep/Oct: high purity electron beam with small calorimeter stacks
EM shower with trim and calib in situ + synchronised readout of Si and SiPM with latest BE boards

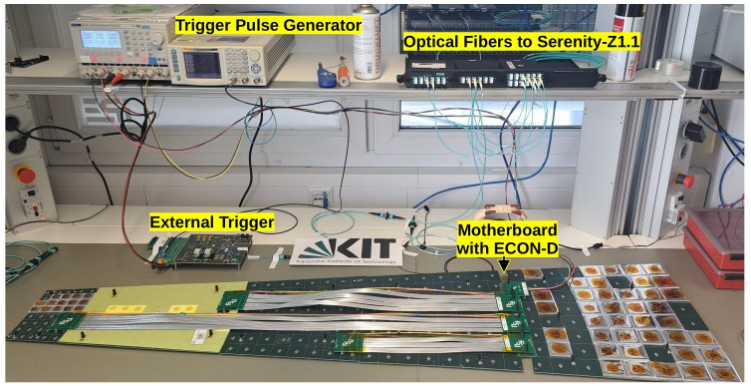
Testing system boards for all variants of si modules







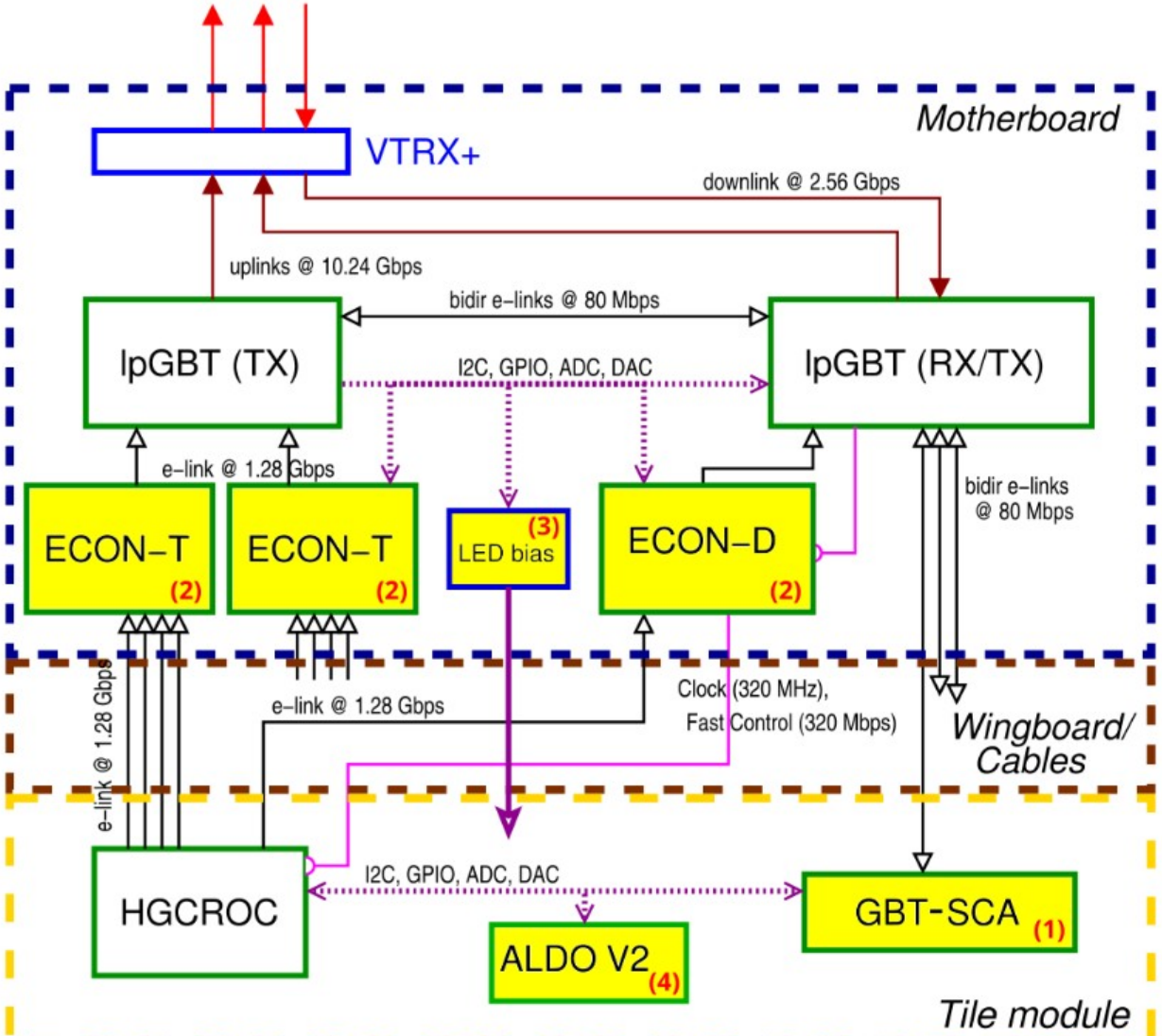
Wrap-up and future



Next steps in validation of the SiPM-on-Tile system

- Tests with realistic power supplies, cable lengths, grounding scheme (KIT, CERN)
  - Copper plate for 10° sector being manufactured right now
  - Once setup is at CERN: clock jitter, eye diagrams of links
- New readout system with Serenity-S and DTH (KIT, CERN)
  - Repeat some tests mentioned above with higher rates or more events
  - Utilize DPG tools (DQM)
- Cassette integration tests (FermiLab)
  - Tests with silicon modules and tile modules on one plate
  - Operation in cold environment (-35°C)

Scintillator front-end (and where it's different)



1. GBT-SCA on the tile modules
   → tile modules were part of ESR1
2. ECON's are on the motherboards
3. LED system to calibrate the SiPMs
4. ALDO to adjust SiPM voltage
   → ALDO was part of ESR1

Cassettes assembly at FNAL