Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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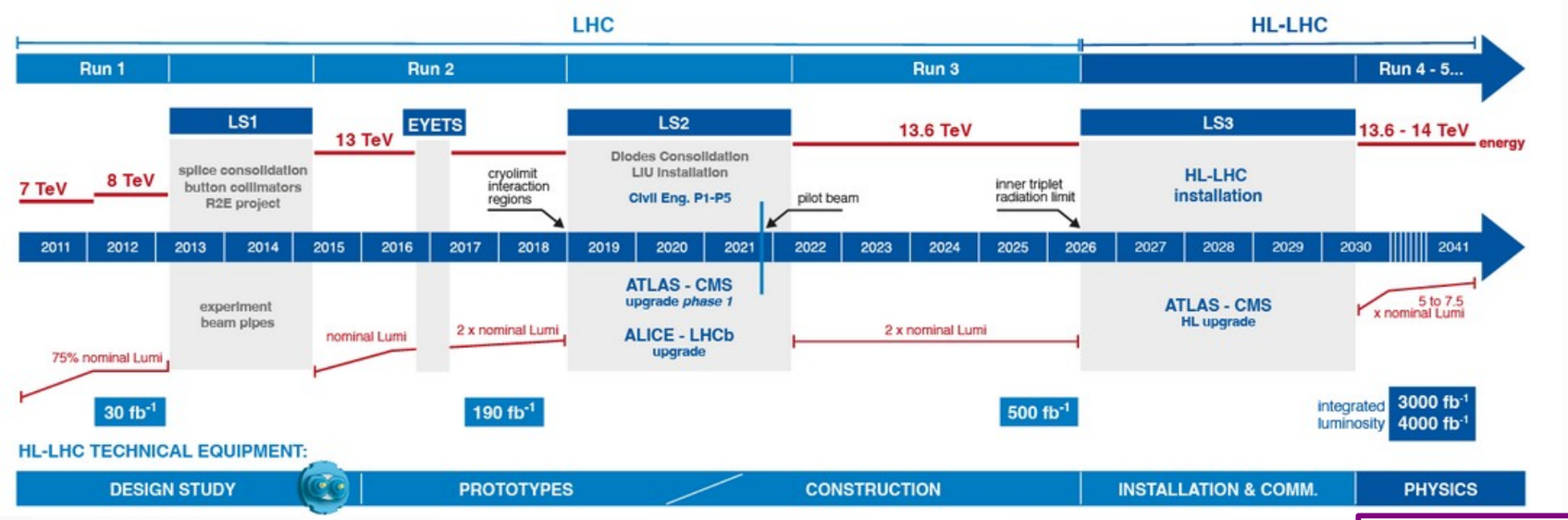
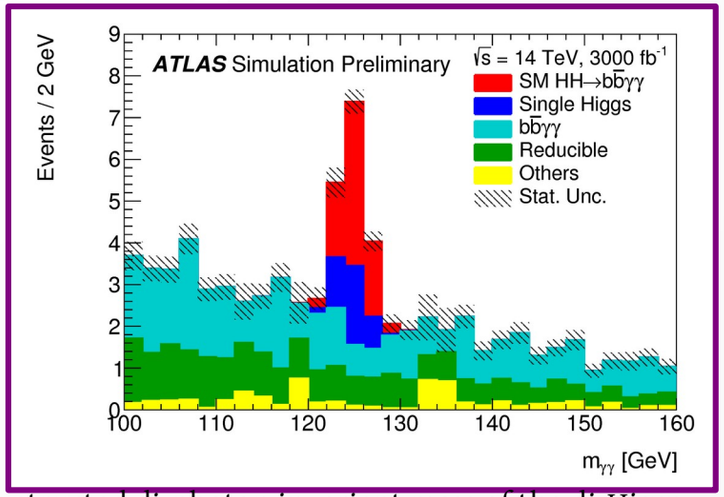
High Luminosity (HL)-LHC



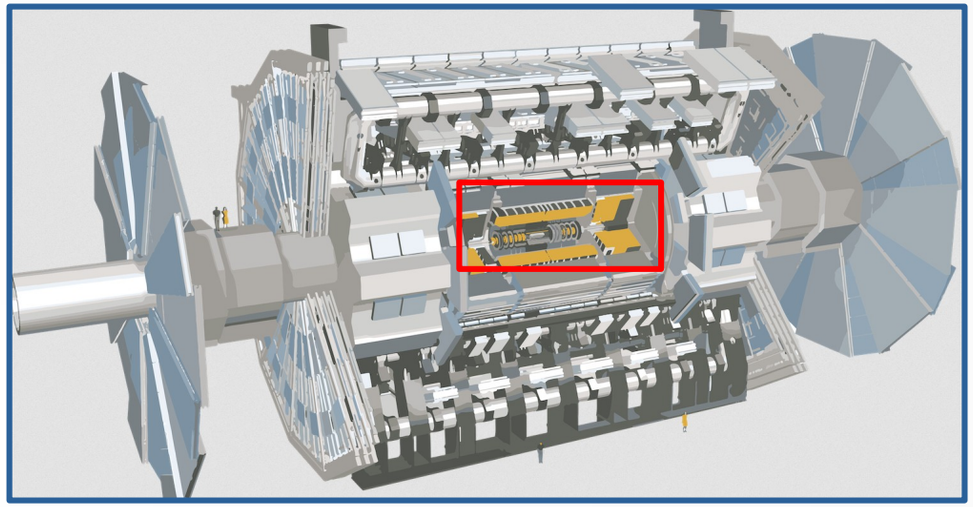
- Increase the instantaneous luminosity by up to a factor 7.5 (for up to a 10 time increase in the total collected data)
  - More possibilities to **study ultra-rare processes** thanks to the increase of number of collisions
- Increase in luminosity will lead to higher pile-up and radiation → changes are needed for the detector at the HL-LHC
- **LAr calorimeter** is the key detector for the **photons**, **electrons** and **jets** reconstruction by precise energy computation with high spacial granularity

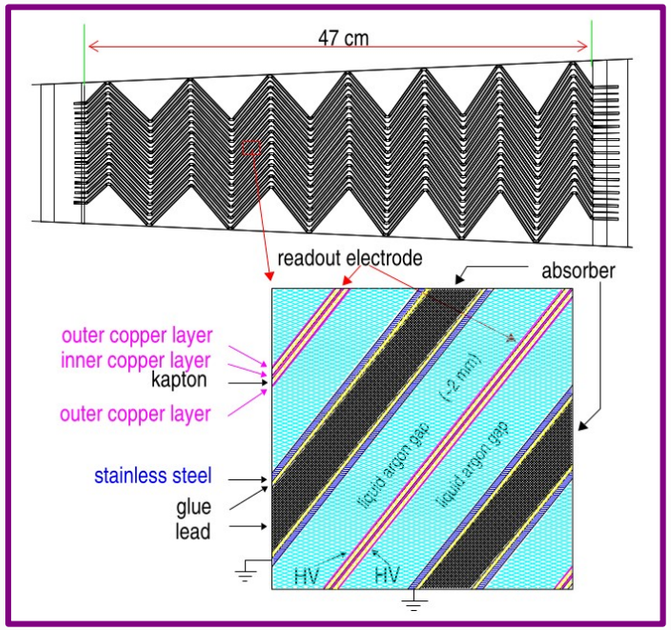


Reconstructed di-photon invariant mass of the di-Higgs production in the γγbb channel with the HL-LHC dataset [ATL-PHYS-PUB-2018-053]

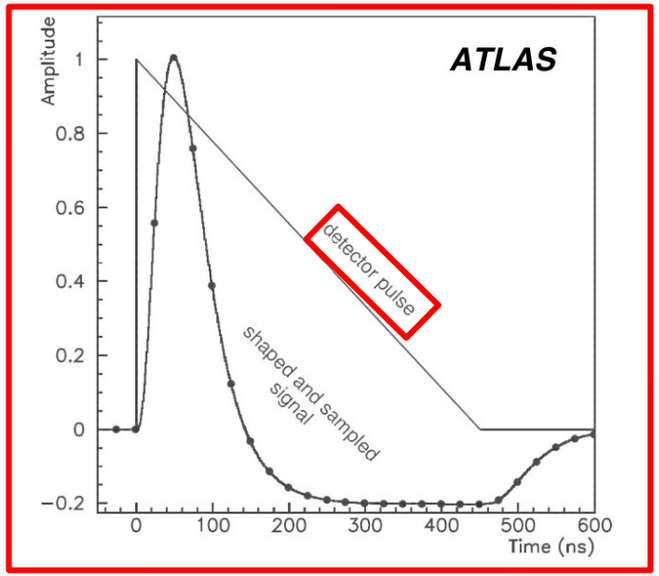
The Liquid Argon (LAr) Calorimeter in ATLAS

- Sampling detector with active (LAr) and passive (Pb, Cu, W) layers in **accordion geometry** (parallel plates for HEC and thin LAr gaps parallel to beam for FCAL)
- A total on 182,468 cells read at collisions rate off 40MHz (every bunch crossing)

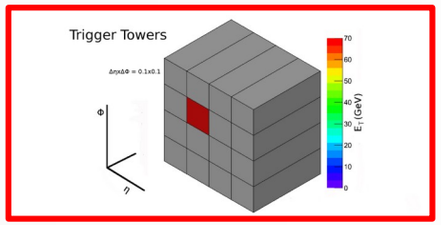


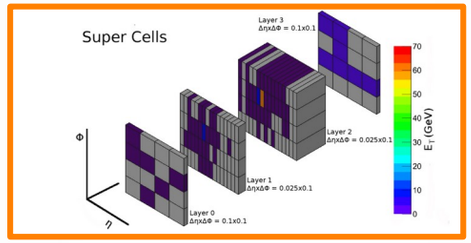


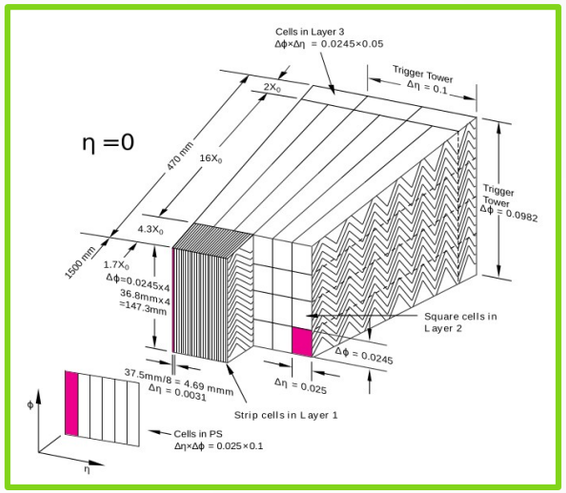
- Drift of the charged particles will create a change in the current creating the **detector pulse signal,** which is later amplified and shaped



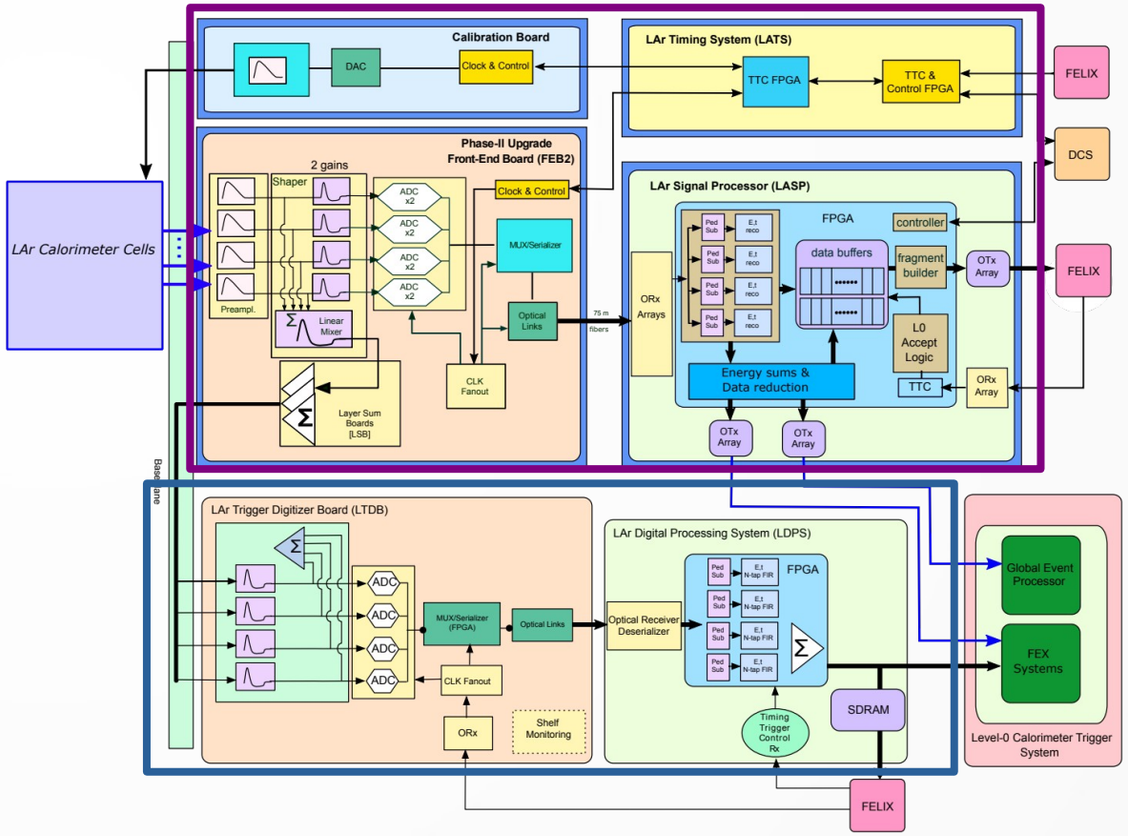
The upgrade scheme for LAr





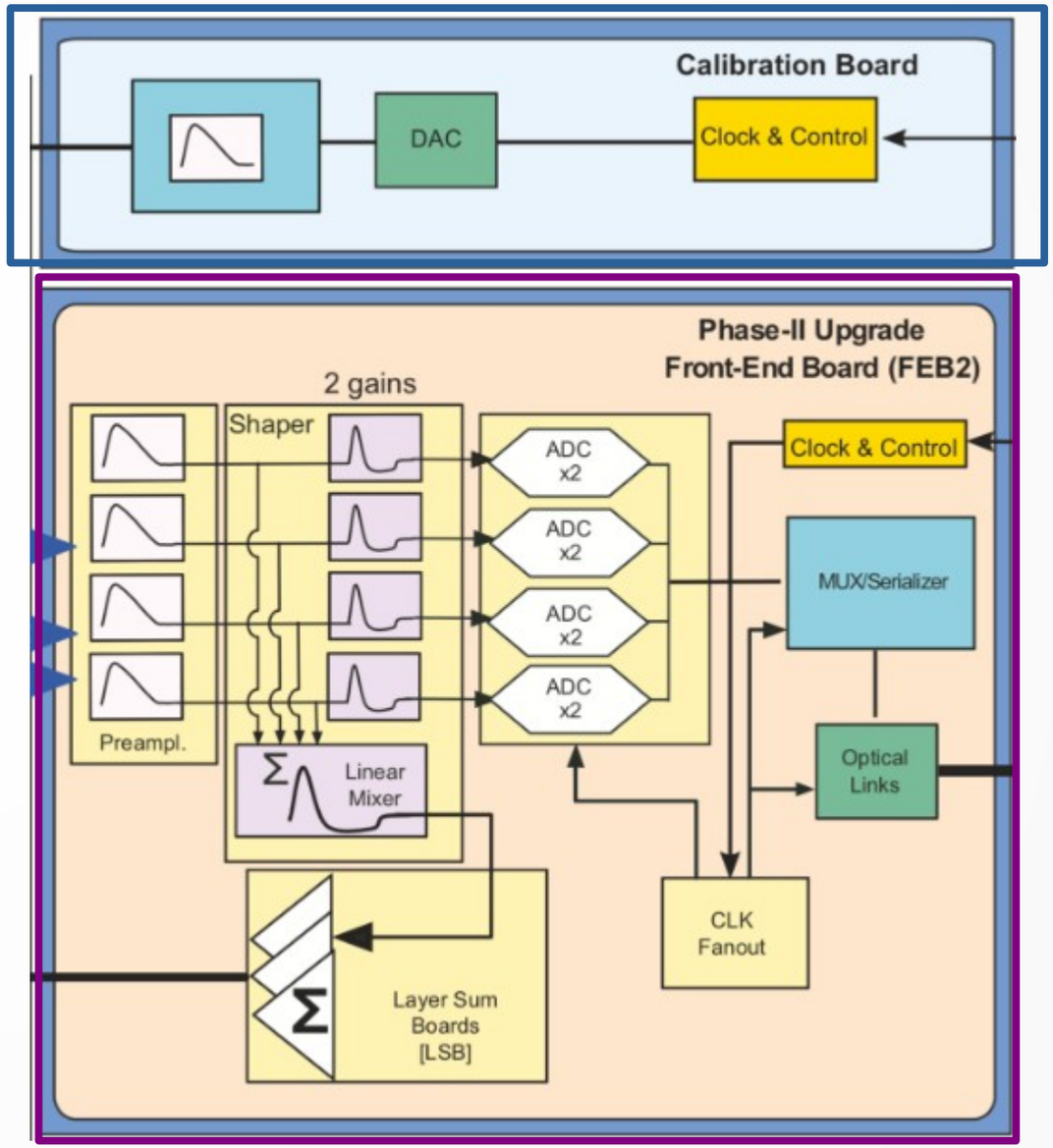


- Detector will stay unchanged, all readout electronics will be changed (except the cold readout in HEC)
- Two steps procedure :
  - Phase-I (Run 3)
    - Digital trigger with more granularity (super cells) than in first 2 runs (Trigger towers)
    - Commissioned and operated successfully in Run 3
    - Will be kept as input to phase-II trigger system
  - Phase-II (HL-LHC)
    - Send full granularity data off detector
    - 2 gains with 16-bit dynamic range
    - Increased radiation tolerance of front-end electronics

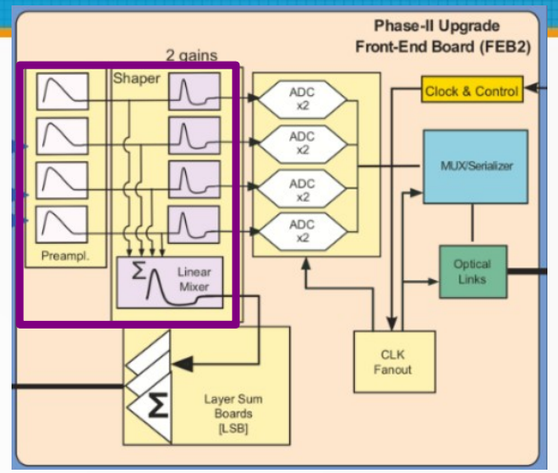


On-Detector electronics

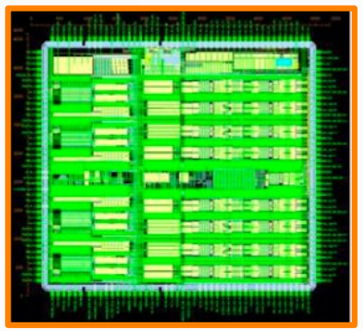
- **FEB2**
  - Amplify, shape and digitize the signal
  - Send 345 Tbps of data to the off-detector
- **Calibration board**
  - Send calibration pulse precise in amplitude
    - Non-linearity < 0.1%
    - Non-uniformity < 0.25 %
  - Send calibration pulse precise in time
    - Pulse rise time < 1ns
- Functionality should be stable under irradiation:
  - Until 1.4kGy (TID)
  - $4.1*10^{13}$ 1MeV n_{eq}/cm^2 (NIEL)
  - $1*10^{13}$ h> 20MeV $/cm^2$ (SEE)

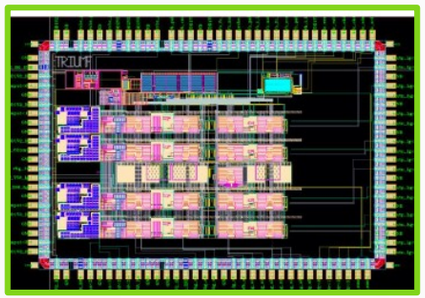


FEB 2 (Pre-amplifier and Shapers)

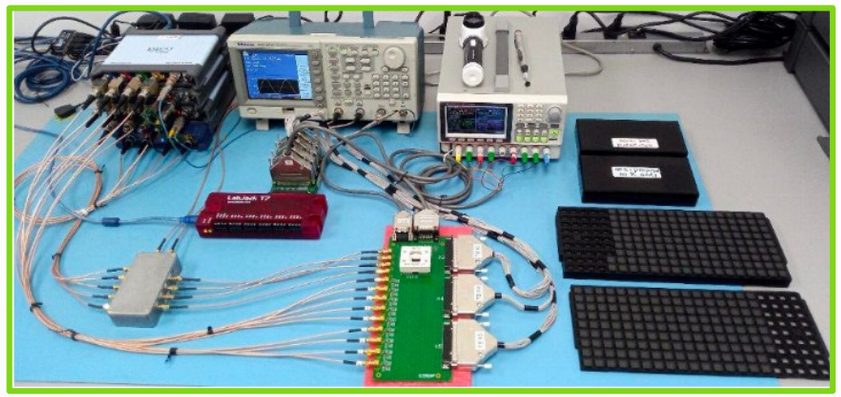


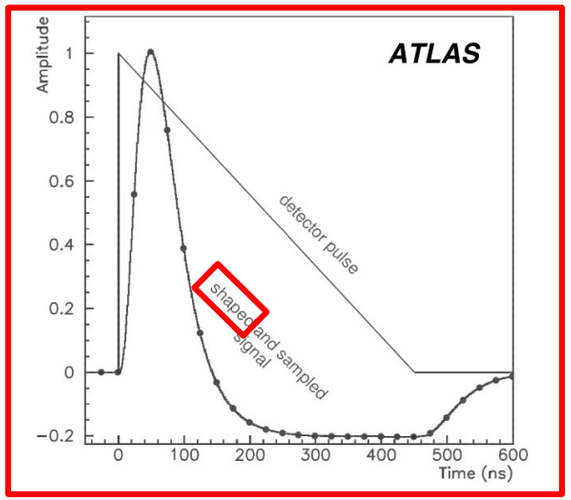
- **ALFE2 (for barrel/End-Cap/FCAL) and HPS (Hadronic End-Cap)**
  - Custom ASICs designed in 130 nm CMOS, pre-amplifier replaced by pre-shaper for HPS
  - 4 input channels (calorimeter cells) per chip
  - Amplification of signal and **differential shaped** output with **two-gain** (~25 ratio between gain)
  - **1 sum** of the 4 channels for the **Digital Trigger (Phase-I) datapath**

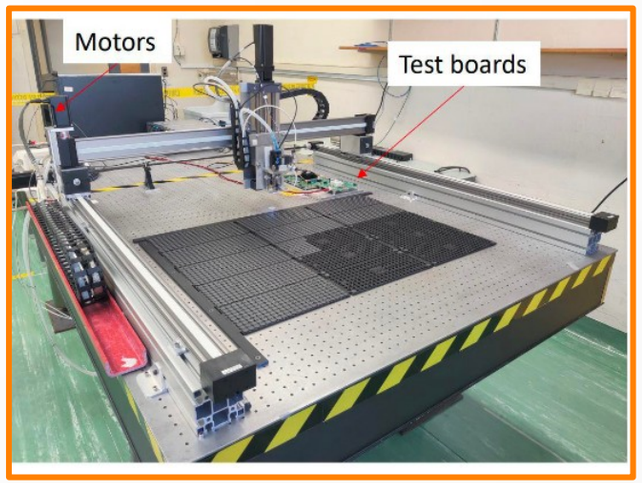




- ~ 80k chips are being produced (~2700 for HPS)
  → **robotic test (ALFE)** needed **(manually for HPS)**
- **Radiation test complete** for both chips

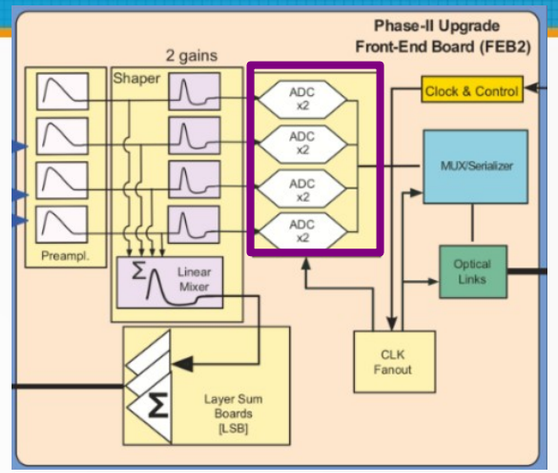


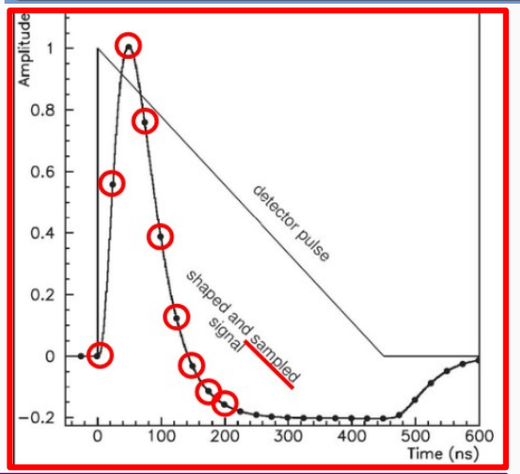


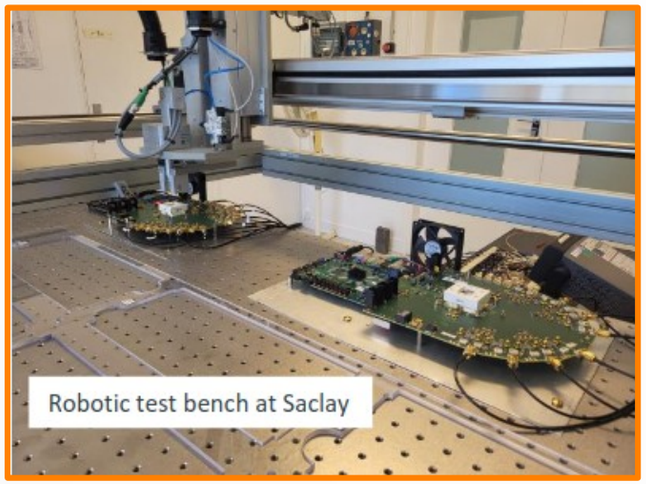


COLUTA ADC

- **COLUTA ADC**
  - Custom ADC ASIC designed in 65 nm CMOS
  - **Sampling:** Digitize shaper output for both gains and 4 channels at 40MHz with 14-bit dynamic range
  - 3-bit Multiplying DAC (MDAC) + 12-bit successive Approximation Register (SAR)
  - Digital Data Processing Unit (DDPU) applies calibration and transmit data (15 bits data of ADC and 1 overflow) at **640 Mbps**
  - Add sampled timing information (Bunch Crossing ID)
  - Interface to lpGBT (optical transmission off-detector)

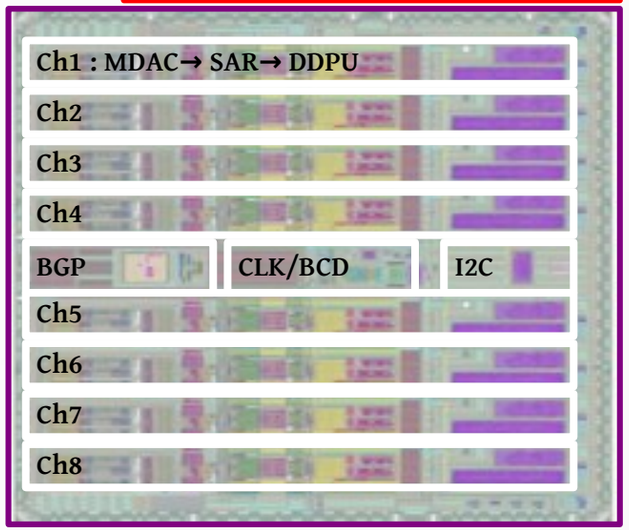




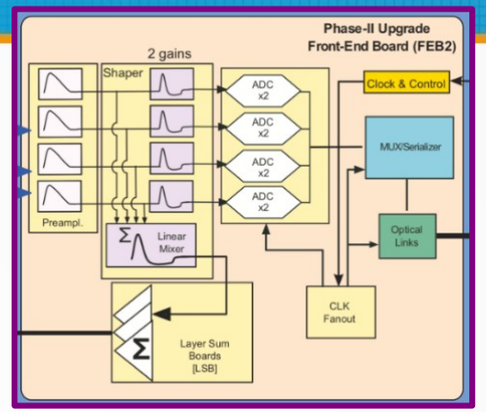


- ~ 80k chips are produced (production complete)
  → **robotic test** underway
- Radiation, vibration and thermal test completed

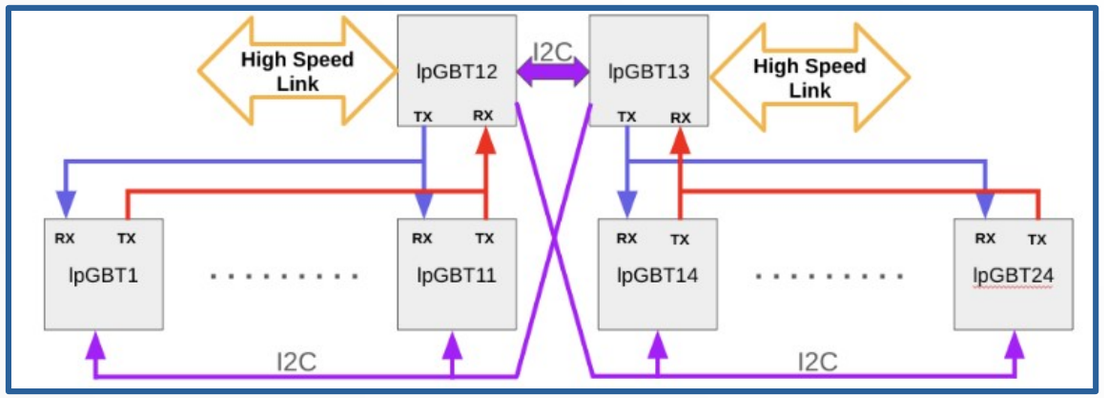
  → Production Readiness Review held this June

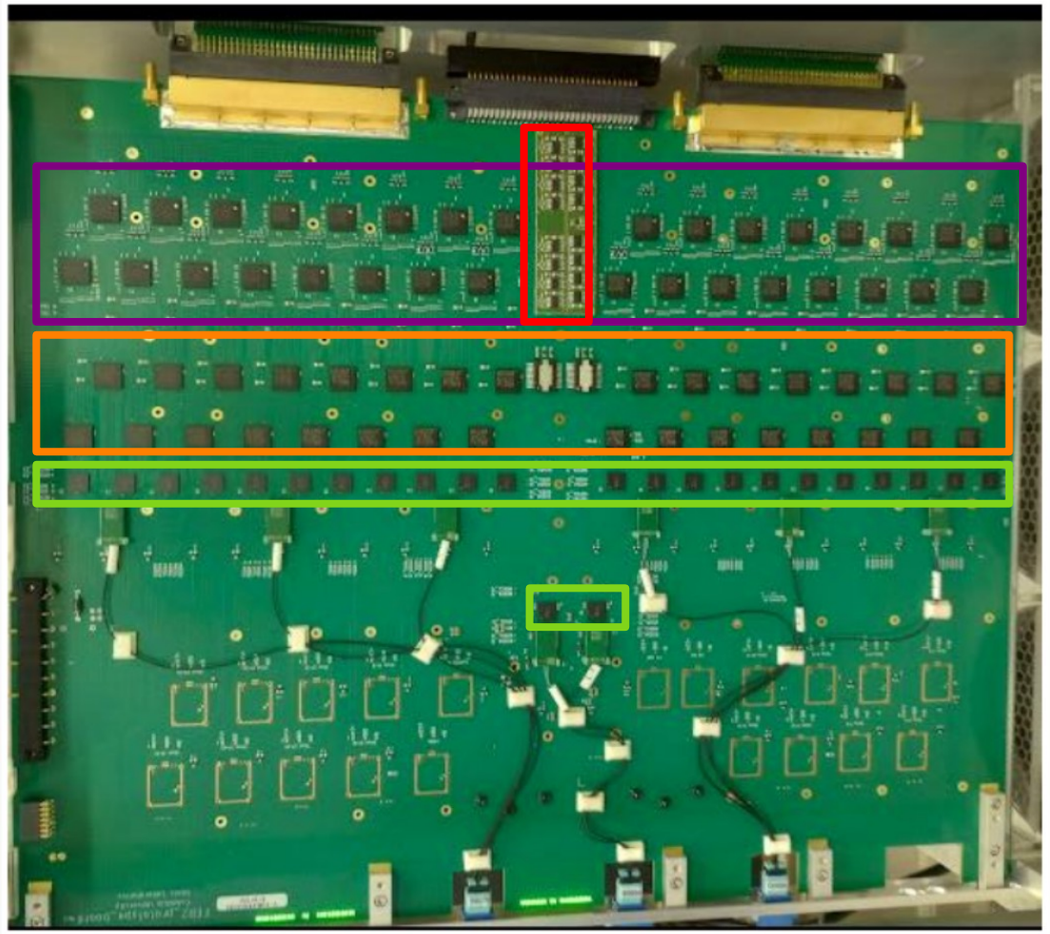


FEB2



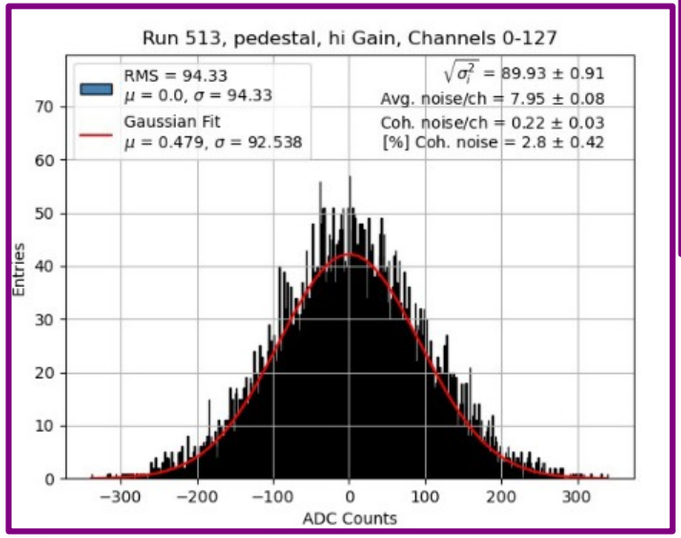
- Digitize and read out LAr calorimeter with full precision and full granularity for every LHC bunch crossing at 40 MHz
- 1524 to be installed on detector need to be radiation hard, actively cooled with a water cooling system
- 128 cells are read out by each FEB2 using:
  - **32 ALFE Preamp/shapers**
  - **32 COLUTA ADCs**
  - **24 lpGBT chip (2 for monitoring and configuration)**
  - **Mezzanine Layer Sum Board** (send analog trigger to Phase 1 trigger system)

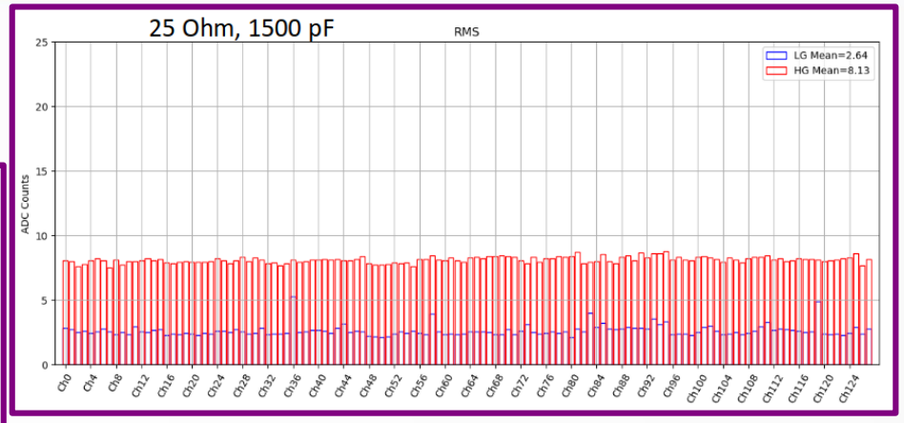


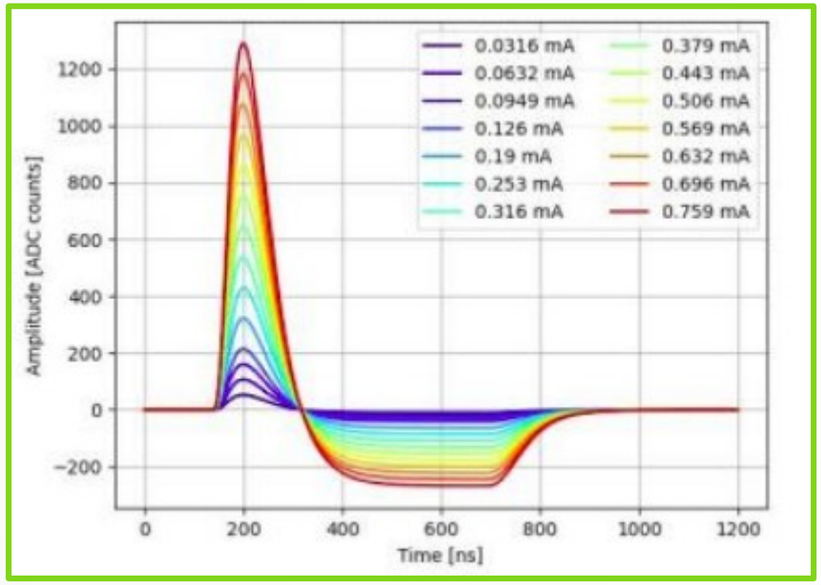


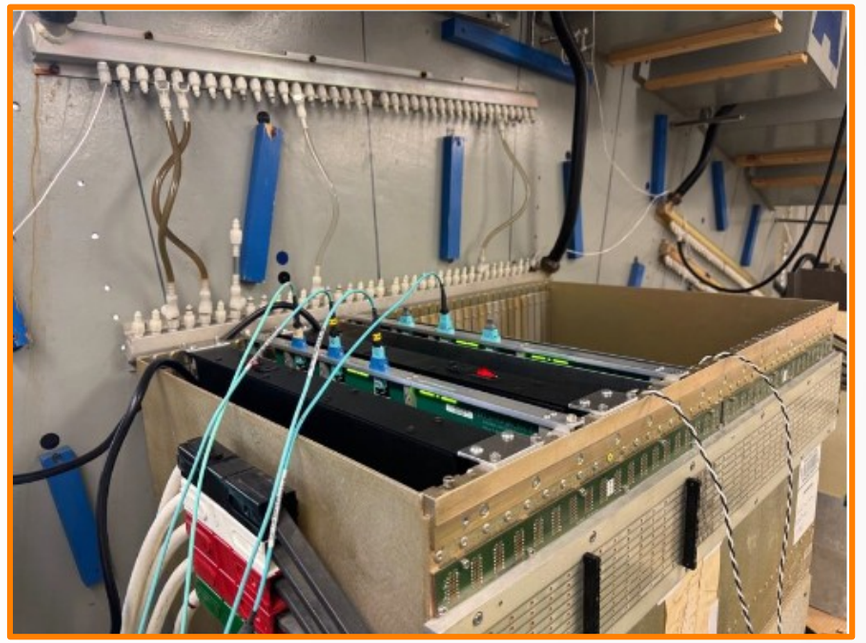
FEB2 test

- Board being tested in stand-alone and integration stand
  - **Pedestal values tested** and study over long stability test
  - Fast-Fourier transform and coherent noise study
  - Correlation noise study between the different FEBChannel
  - **Pulse** and linearity study of the signal



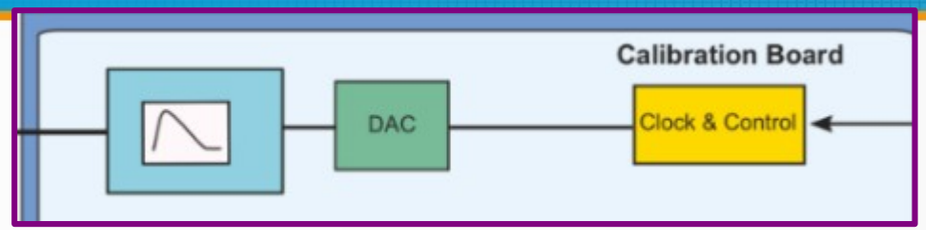




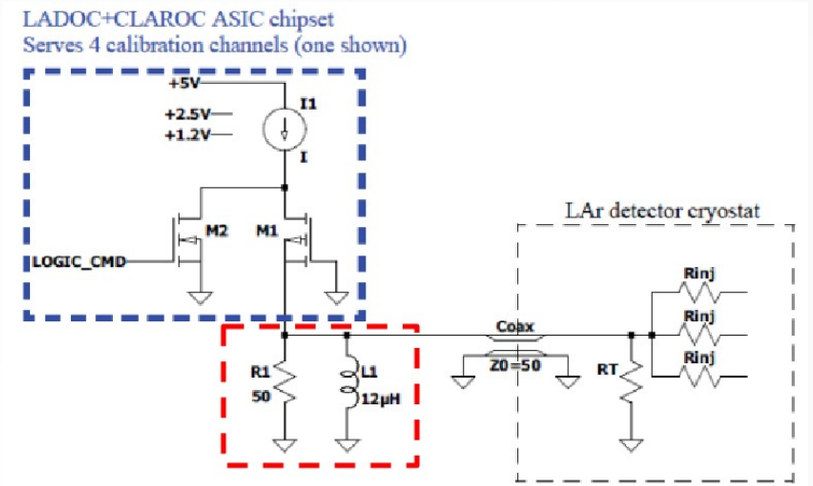


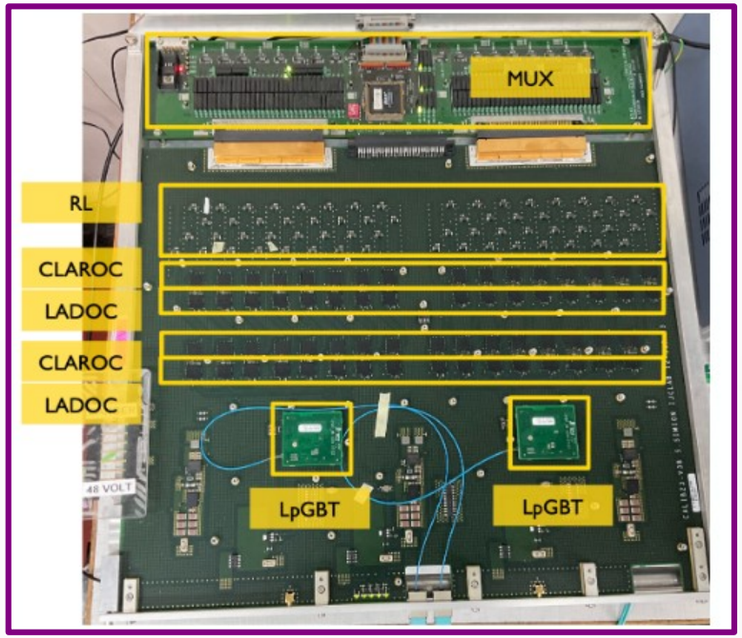
- Integration test planned for validation of coherent noise inside a **Front End Crate system** (14 FEB operated simultaneously in a production-like system)

Calibration boards

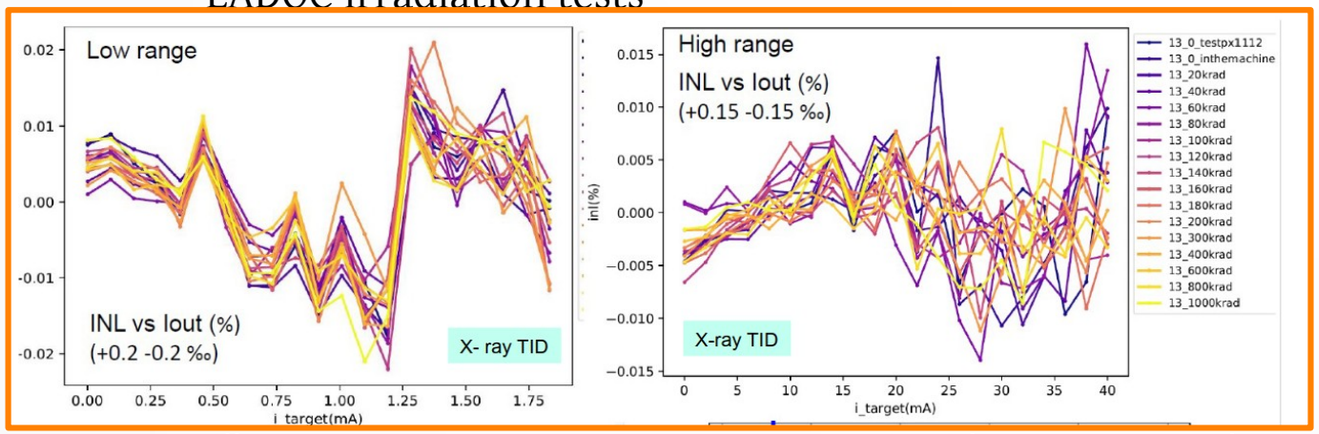


- Calibration board
  - **Two ASICS :**
    - **LADOC** (130 nm TSMC): precise DC current and used for slow control
    - **CLAROC** (180 nm CMOS): high frequency switches which is opened with a command pulse
  - Pulse built from precise DC current using inductor **(L1)** and precise resistor **(R1)**
  - 32 LADOC and 32 CLAROC per board
- Will be able to pulse 128 calibration channels per board with at 16-bit dynamic range
- 122 boards to be installed on detector (~12 FEB2 board pulsed per calibration board)
- **Radiation test passed** → production of the chips starting soon → robot test in preparation
- Ongoing integration test of a prototype board at CERN



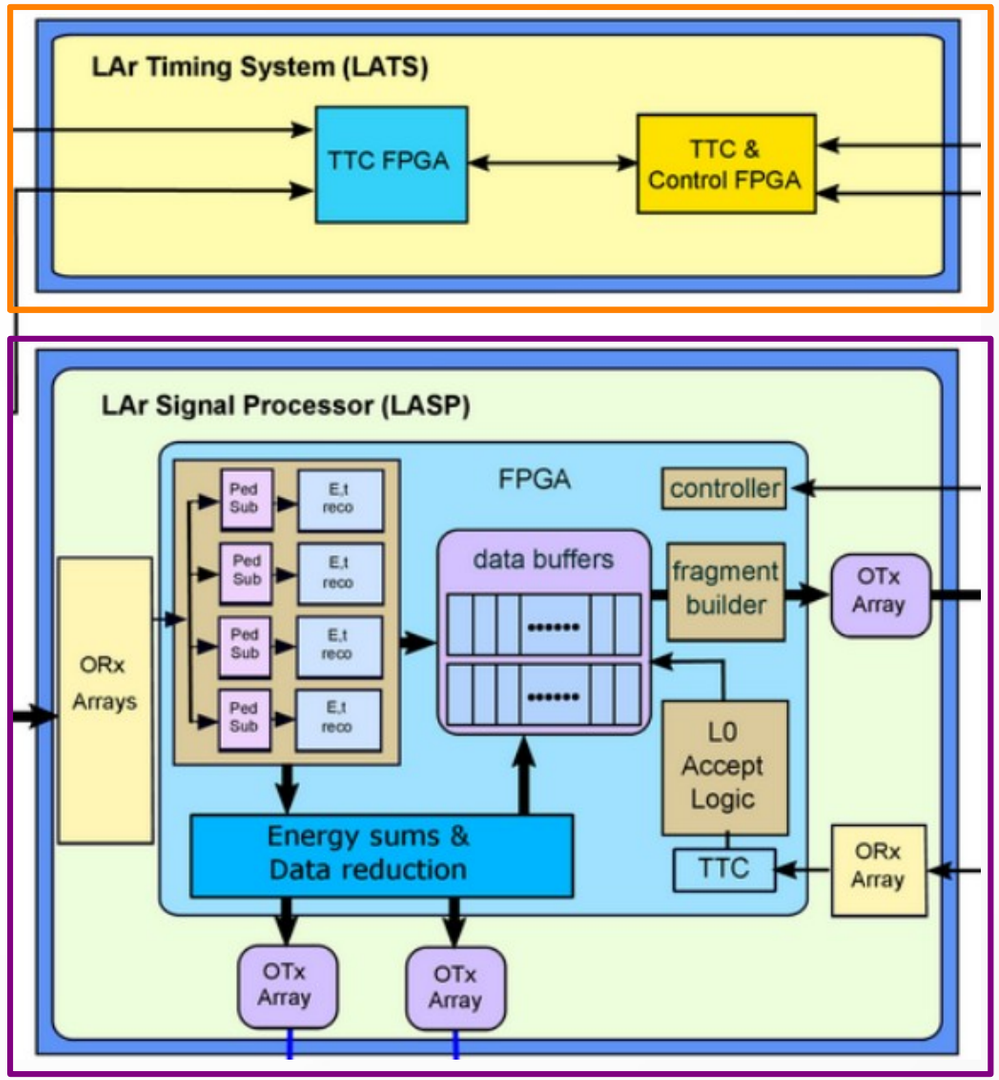


LADOC irradiation tests

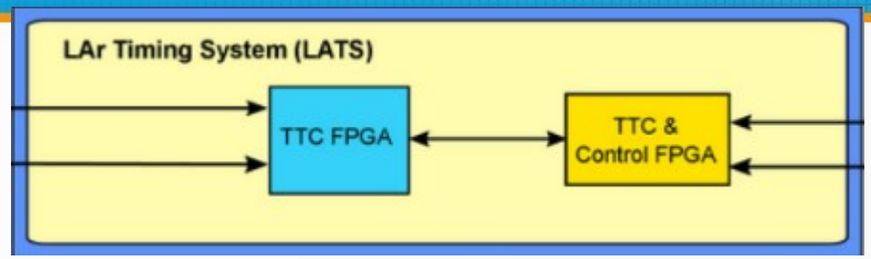


Off-detector electronics

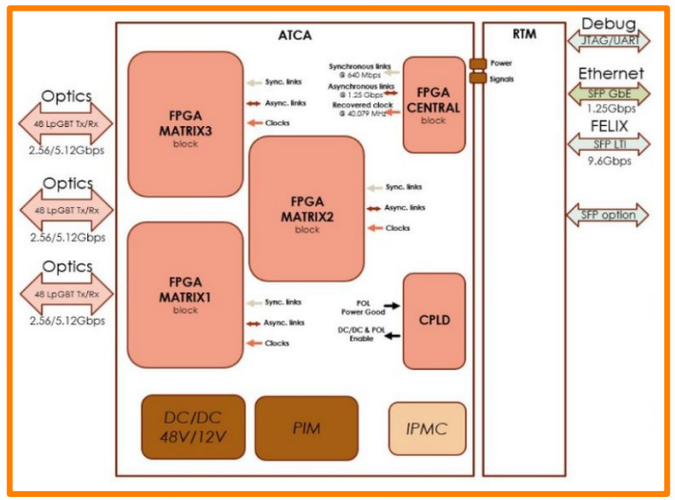
- LATS :
  - Synchronize, configure and monitor the on-detector boards
- LASP :
  - Total of ~33000 incoming links at 10 Gbps (345 Tbps total from front-end)
  - Perform energy and time reconstruction at 40MHz
  - Process data to be send to the trigger and data acquisition systems and buffer until trigger accept signal

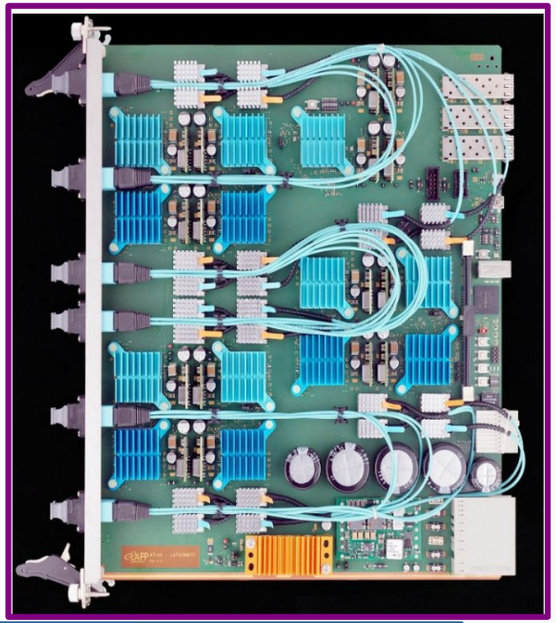


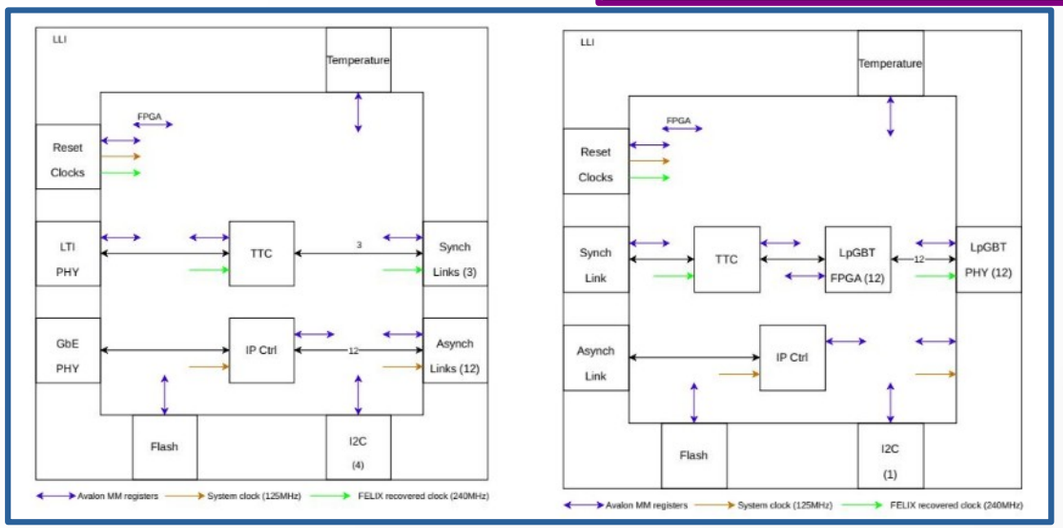
LATOURNETT and configuration



- **LATOURNETT** is our board implementation of the LATS
- Up to 72 board (FEB2 and Calibration board) monitored, synchronized and controlled per LATOURNETT
- 13 Cyclone10 GX FPGA
  - 1 CENTRAL FPGA : connected to GbE (to timing and control software)
  - 12 FPGA split in 3 blocks of 4 MATRIX FPGA : Connected to the Front-End boards
- **2 different firmware** versions for CENTRAL and MATRIX FPGA
- Prototype passed preliminary test and now included in integration test

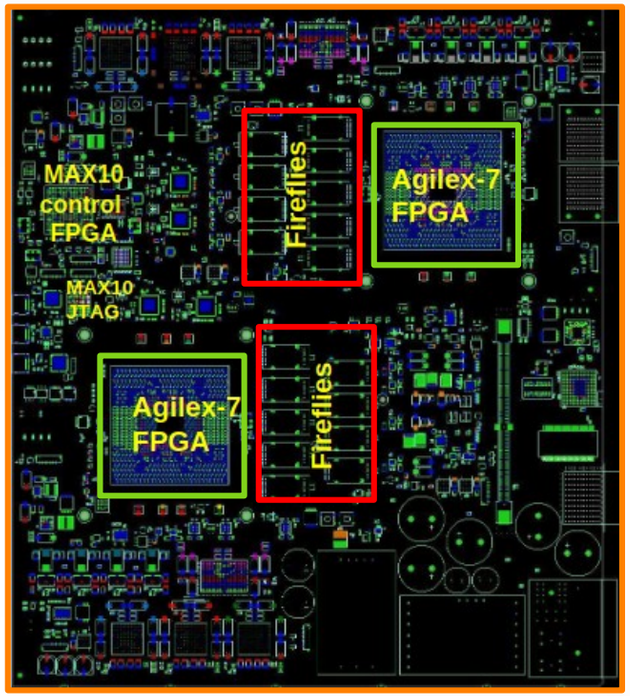


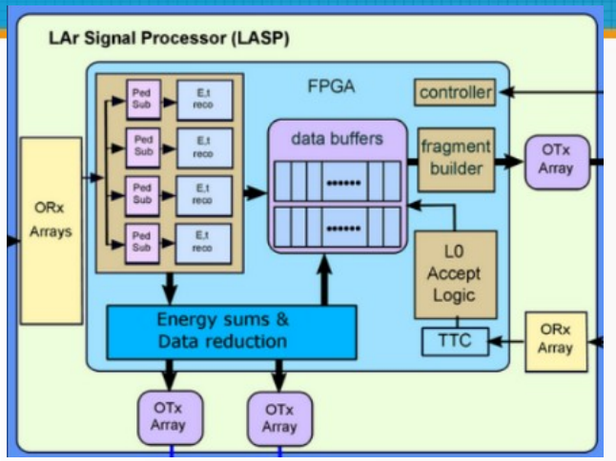


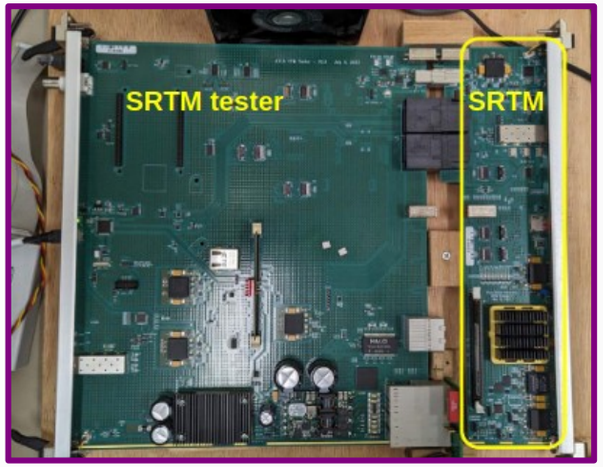


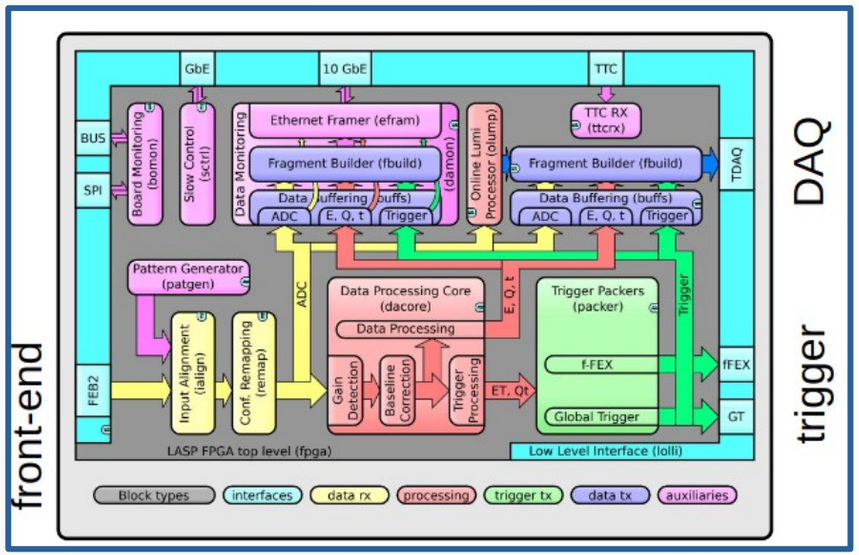
LASP system

- **The LASP main blade**
  - 2 Agilex 7 FPGA per blade reading data input from 3 FEB each
  - Read the 10 Gbps input link (lpGBT protocol) from FEB through custom SamTec Firelflies
- **The SRTM (Smart Rear Transition Module)**
  - Implemented Xilinx Zync Ultrascale FPGA
  - Timing Trigger and Control (TTC) input at 10Gbps
  - Interface with Data Acquisition output at 25 Gbps
- 278 LASP+SRTM will be installed



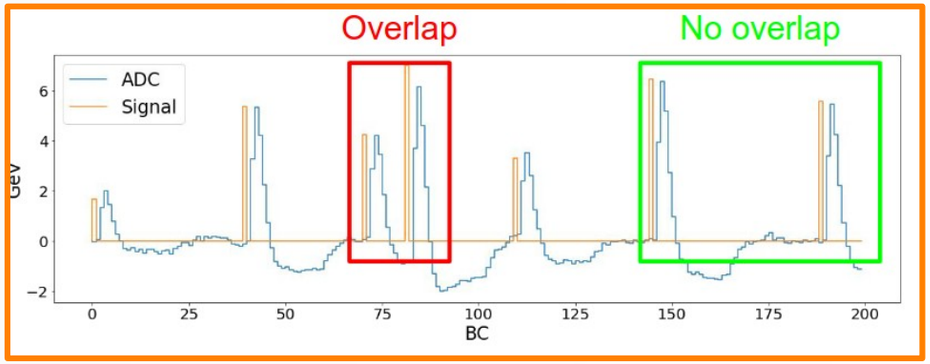


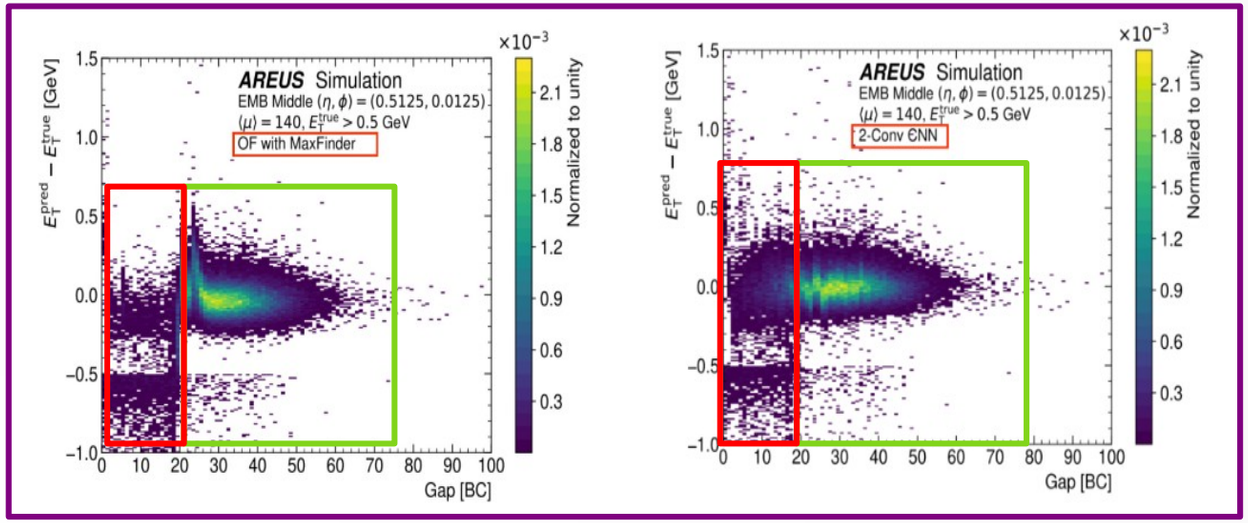




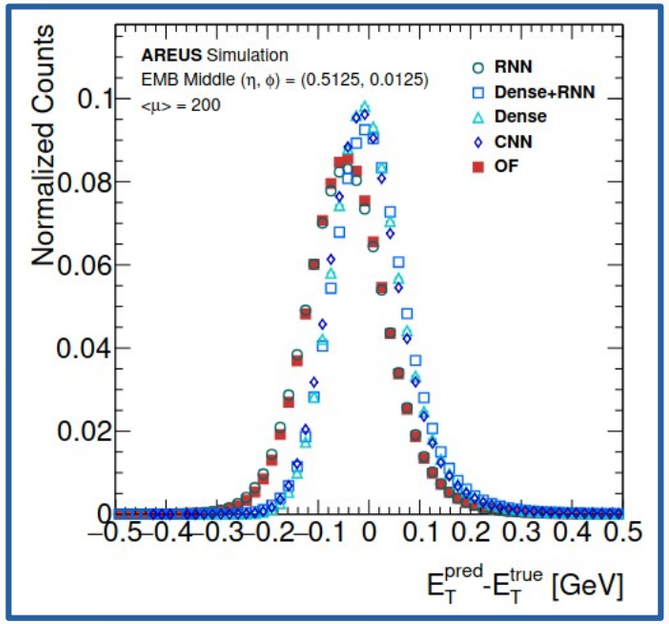
- **LASP Firmware:**
  - Receive and synchronize digitized data from FEB2
  - Compute signal time and energy on each calorimeter cells
  - Transmit all cell energy to global trigger system at 40MHz
  - Buffer the data until trigger response at 1MHz and transmission to DAQ

Energy and time extraction





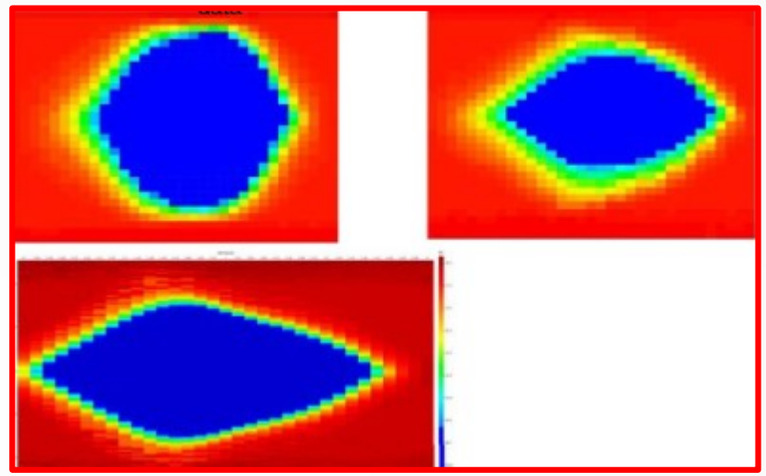
- Usage of the Optimal Filtering (OF) algorithm to reconstruct the energy
  - Weighted sum of samples around the pulse peak
  - Max finder to select the peak BCID and reconstruct the time
- Increase of the luminosity will **increase the pile-up** → **degradation of the Optimal Filter** performance
- **New promising methods** are being tested:
  - Extended OF approach with forward correction: Wiener Filter+OF
  - Extended OF approach with more samples before and after the energy deposit
  - Convolutional Neural Network
  - Recurrent Neural Network
  - Dense layer Neural Network



For more information see
[presentation from Raphaël Bertrand]

LASP system test

- Ongoing SRTM test (power, temperature, infrastructure, **eye scan**)
- Ongoing LASP testbench development for hardware validation
  - Planned for the final production board
  - Testing all specifications of the board :
    - Use of an **INGUN interface** for access to all test points
    - JTAG, IPMC and clock distribution test
    - Preparation of optical test with injector and SRTM
- LASP prototype soon available for validation of the test bench → SRTM connection with prototype will be tested
- LASP test-boards are used in test-bench and integration setup

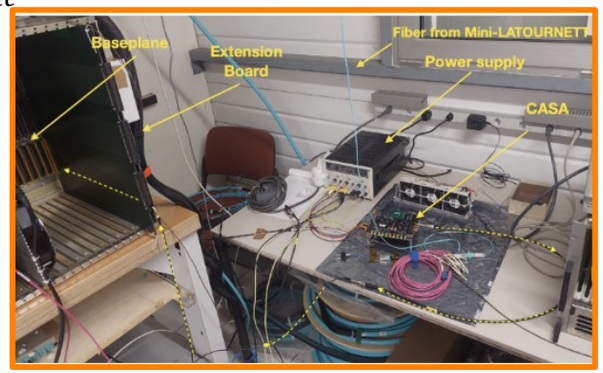


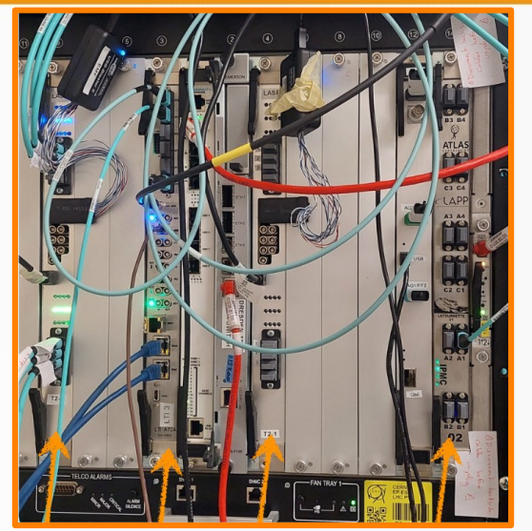
SRTM eye scan

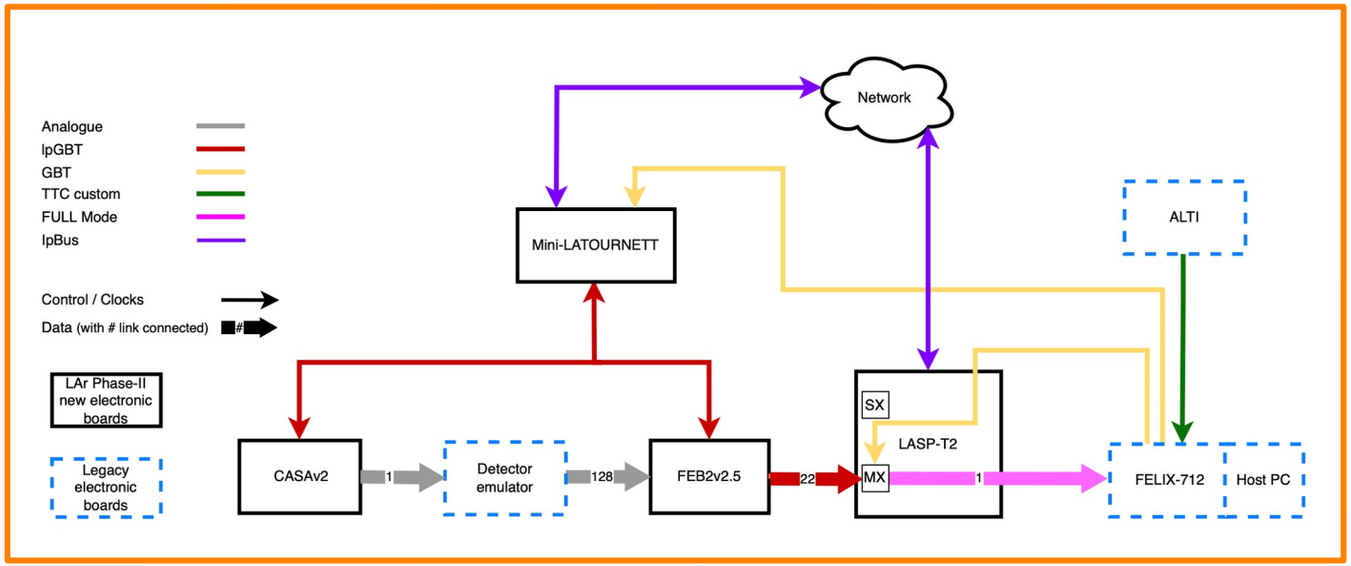
INGUN interface for LASP

Integration setup at CERN

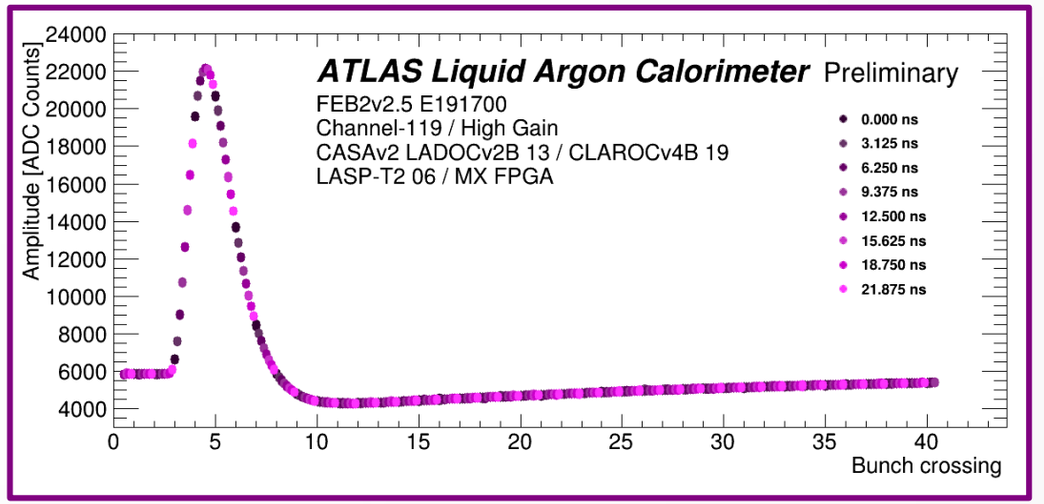
- More complete (with all hardware needed) **integration setup** being developed at CERN
  - For hardware and firmware (link, protocol)
  - For online software (Control, monitoring, safety)
  - For offline software (reconstruction and analysis)
  - For continuous development all along the HL-LHC
- **Successful test of calibration pulsing and data acquisition**
- Lots of other tests ongoing (FEB noise measurement, protocol test, calibration ramp)







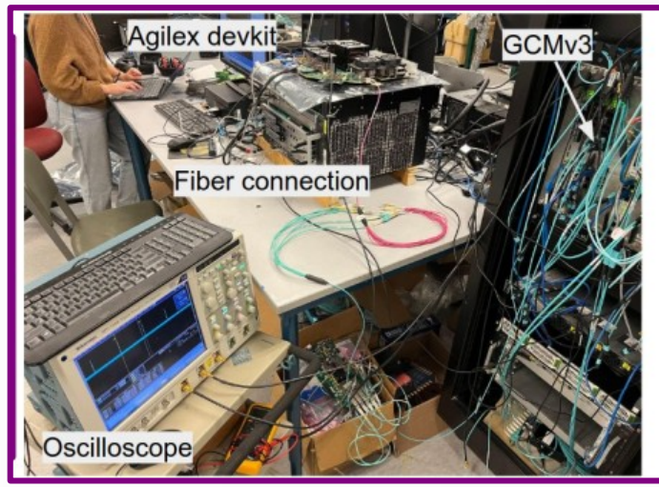
Scheme of the setup at CERN

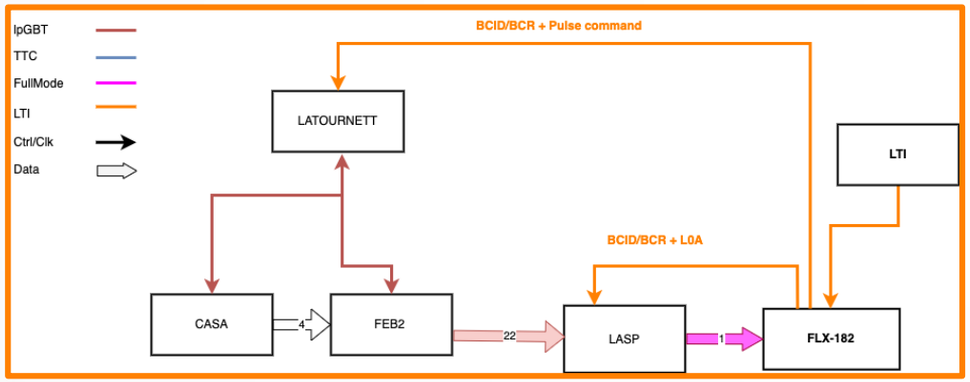


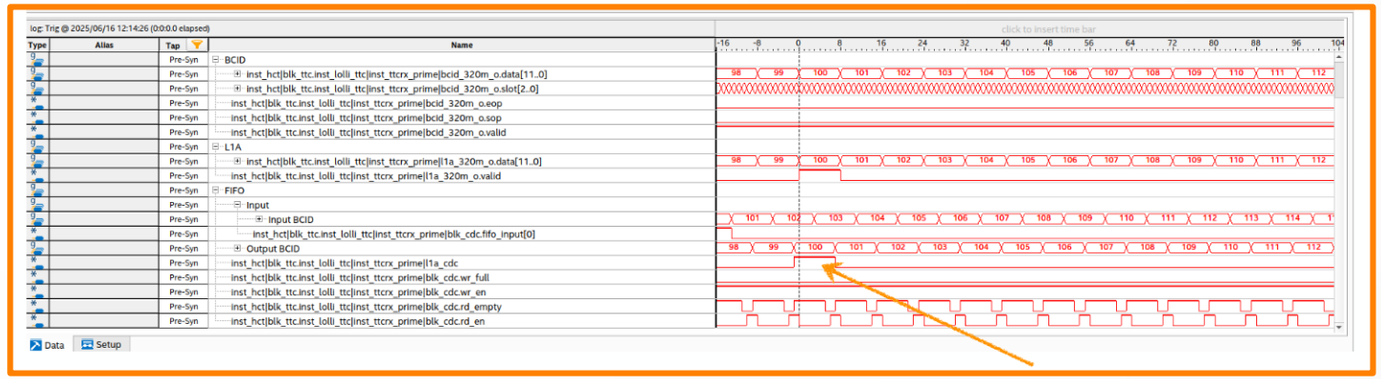
Reconstructed pulse with the setup

Integration with trigger and DAQ systems

- Interlaken (25Gb/s) Core 1990 protocol
  - Agilex Devkit to Global (main trigger path) GCMv3 Xilinx VP180 data transfer tests
    - Demonstrated stable transmission of 576b/BC







Trigger signal properly decoded by the LASP firmware

- Test with new ATLAS Local Trigger Interface (LTI) protocol and hardware
  - Protocol properly decoded and propagated by the LASP and the LATTOURNETT
  - Full data path tested showing proper synchronization by the system and effectiveness of pulse command system (through LTI and LATOURNETT)

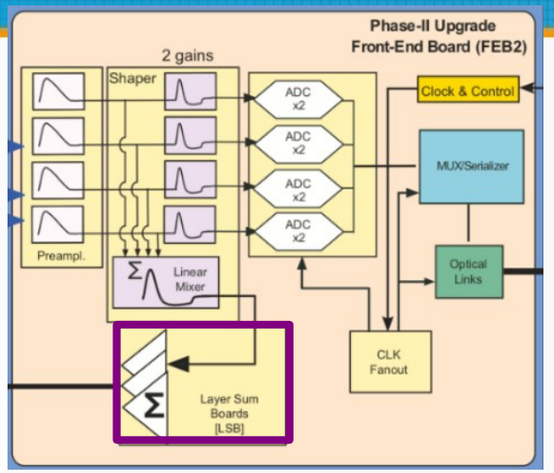
Key points

- All (except HEC cold electronics) ATLAS LAr calorimeter electronics will be upgraded for the HL-LHC
- Good progress is made in every aspect of the upgrade
  - All radiation tests are done for on-detector ASICs chips
  - Performance tests of ASICs chips are done
- Integration progressing well :
  - A whole readout chain made of new LAr electronics is functional and routinely used
  - Integration ongoing with trigger and DAQ systems
- On schedule for the decommissioning (July 2026) and the installation inside the cavern (in 2027) to be ready for the HL-LHC Run 4 (in 2030)

Thank you !

ATLAS Liquid Argon team during a workshop at Montreal in June 2024

Layer Sum Boards (LSB2)



- First summing done in pre-sample chip
- Plug-in mezzanine implemented on the FEB2 in order to provide the next step of the summation
- Summation done via analog circuit design using COTS
- Send out the output to the Digital Trigger path