ATLAS ITk Pixel Detector Overview

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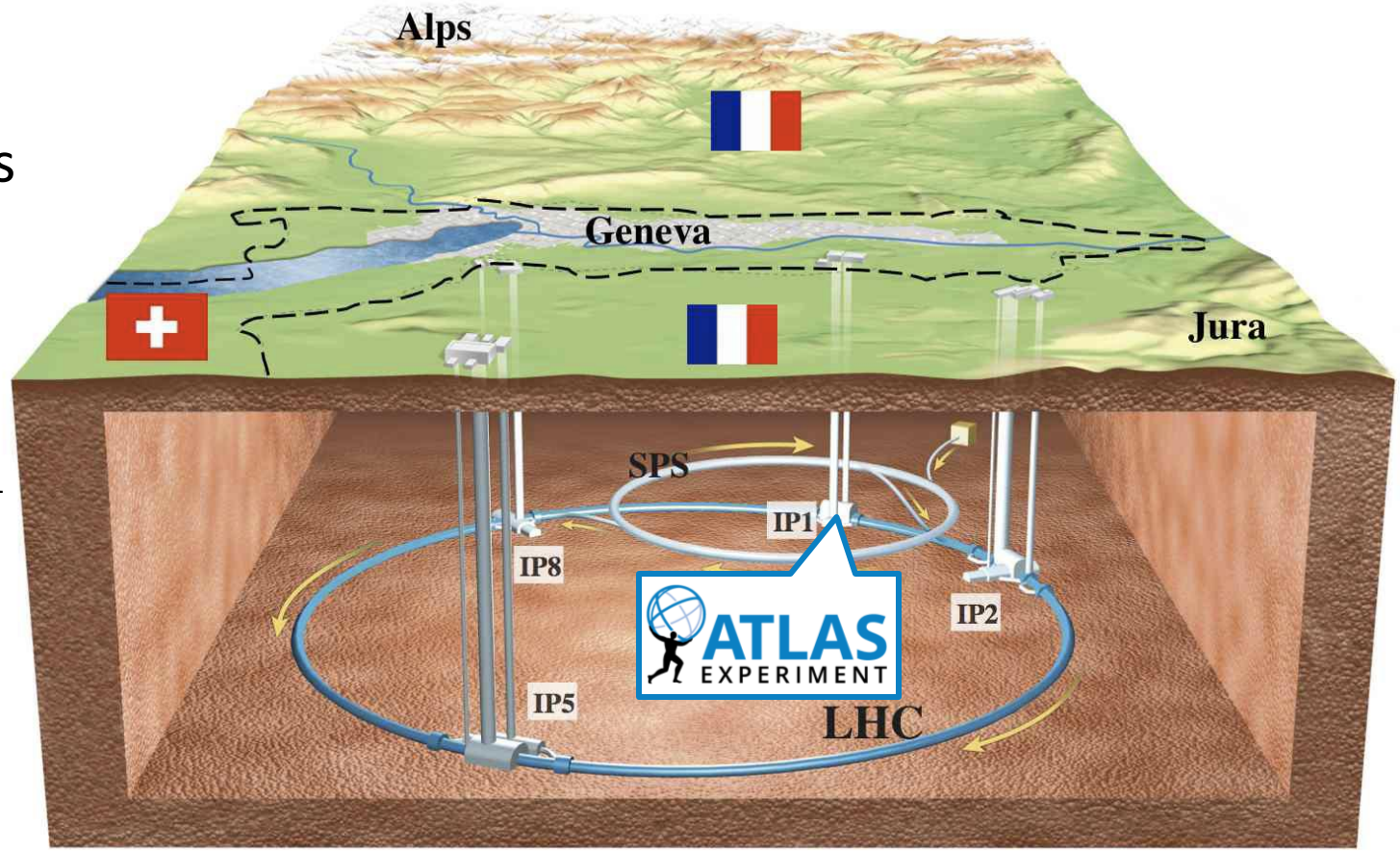
Large Hadron Collider Upgrade

- Large Hadron Collider (LHC)
  - Circumference: 27 km
  - pp and (heavy) ion collisions
- High Luminosity (HL) Upgrade
  - Physics run from mid. 2030
  - Peak luminosity:
    $2 \rightarrow 5\text{–}7.5 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
  - Integrated Luminosity:
    $500 \rightarrow 3000\text{–}4000\ \mathrm{fb}^{-1}$
  - Collision energy:
    $13.6 \rightarrow 14\ \mathrm{TeV}$

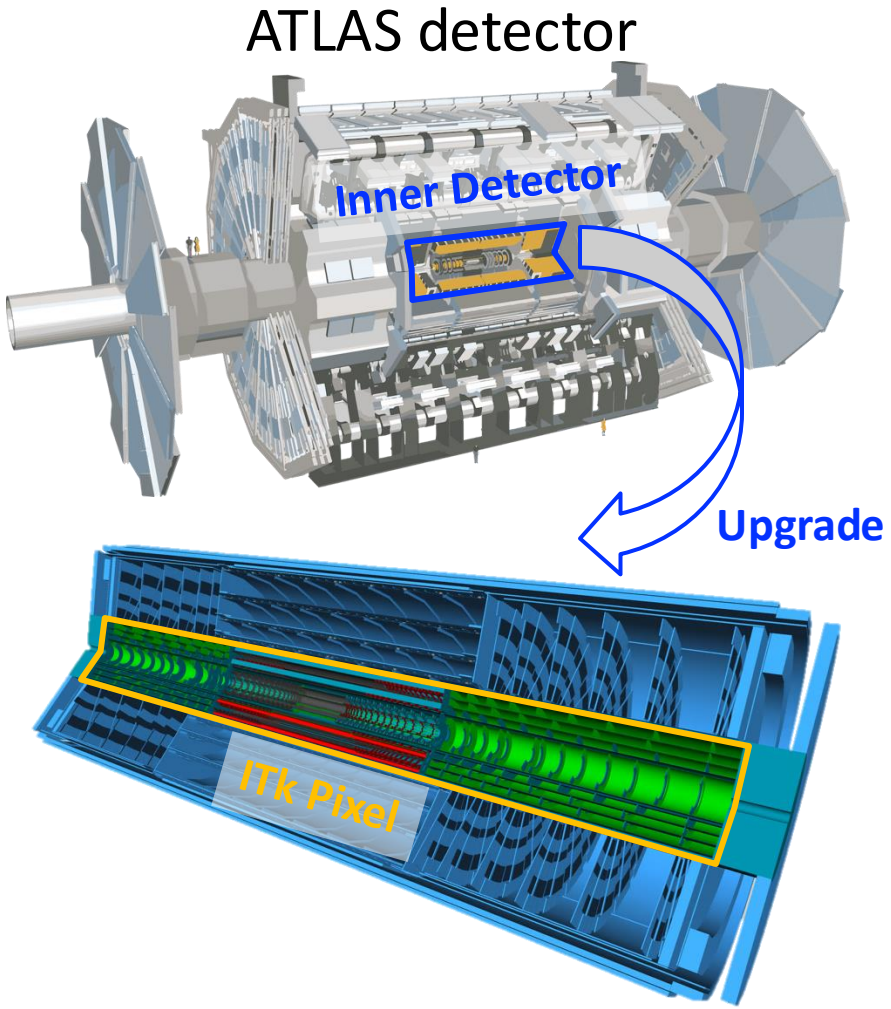
CERN-ATS-2012-064



ATLAS Tracker Upgrade

- ATLAS in HL-LHC
  - pile-up events: $\langle\mu\rangle = 64 \rightarrow 140\text{–}200$
  - need more granularity
    rate capabilities
    radiation hardness

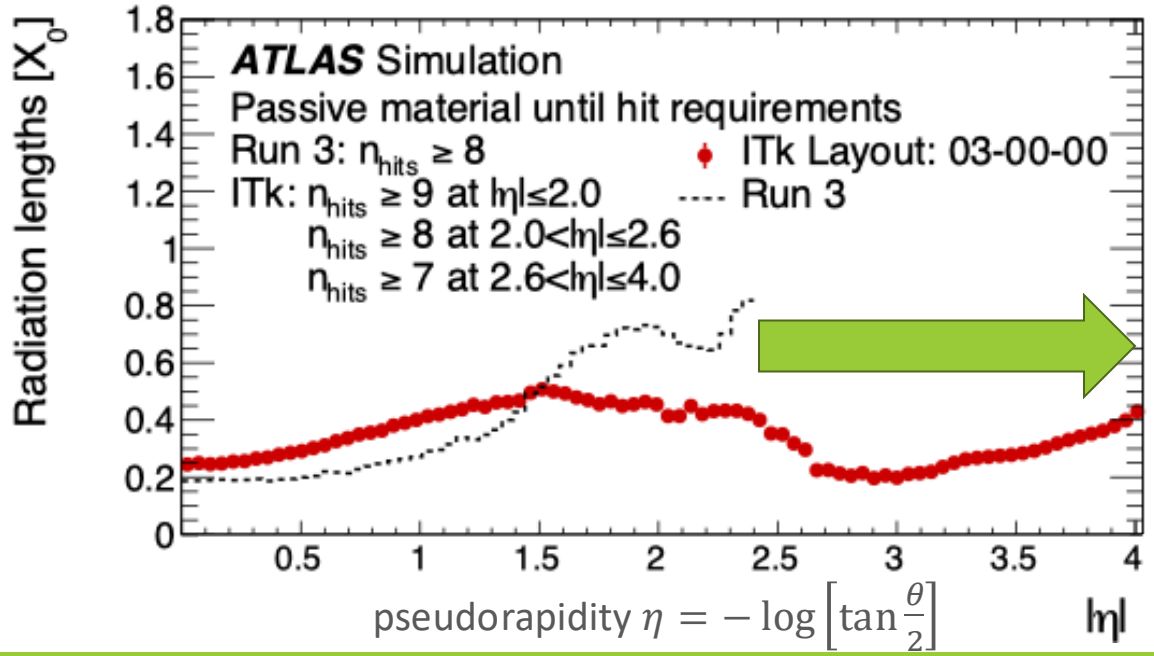
- Inner Tracker (ITk)
  - 9-layer all silicon detector
  - inner 5-layer Pixel + outer 4-layer Strip



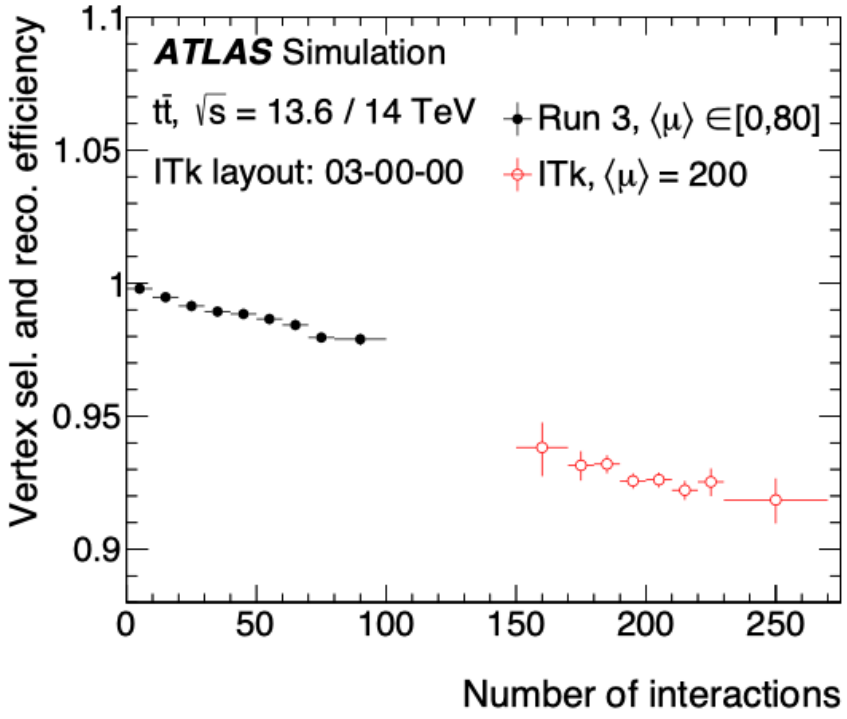
ATLAS Tracker Upgrade

JINST **20** P02018

- ITk Performance
  - Improved forward acceptance
  - Reduced material budget
    - Low-mass support material
    - Power/Data cable reduction

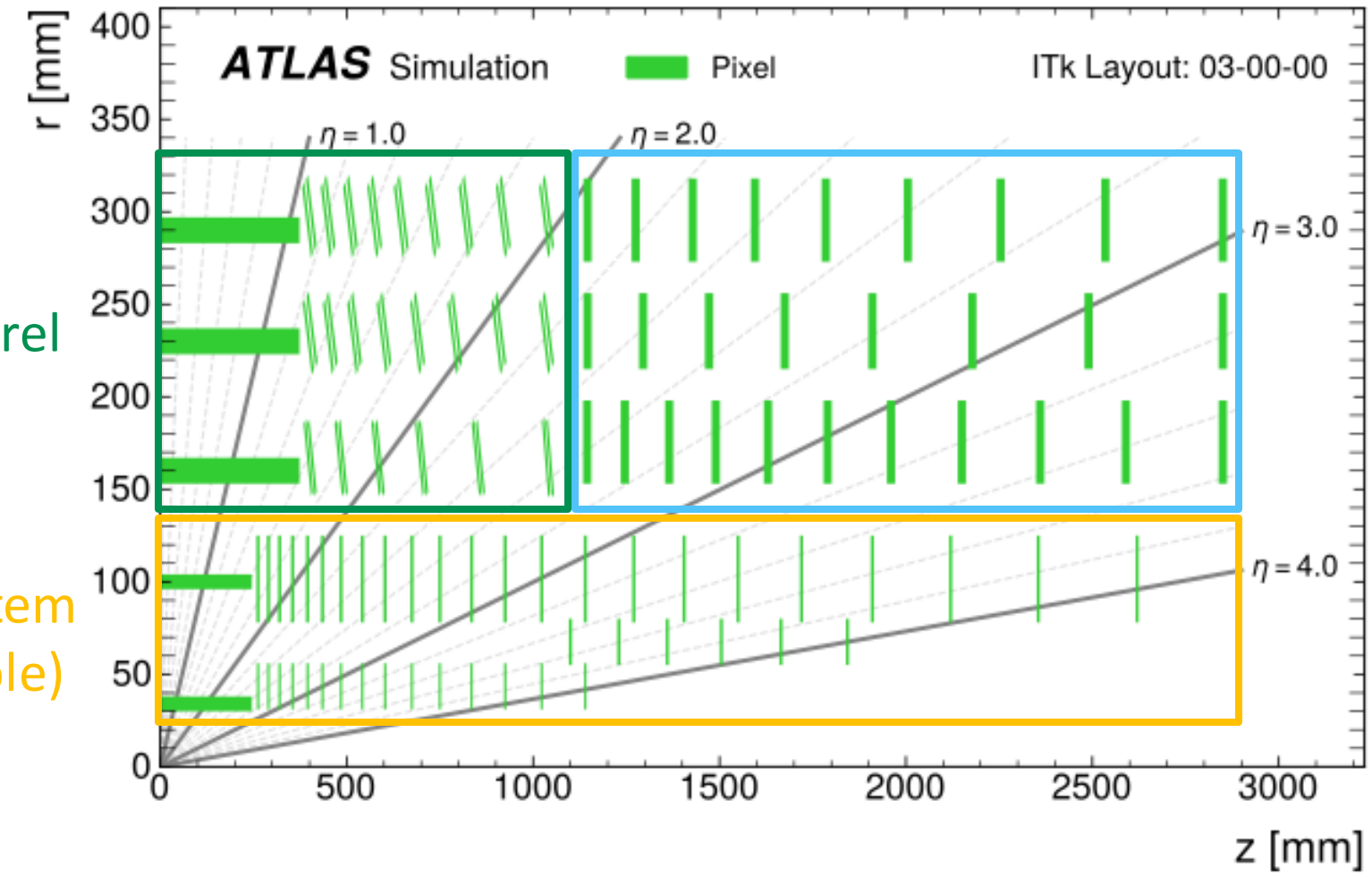


- Keep primary vertex reconstruction efficiency > 90% even in 200 pile-up



ITk Pixel Structures

JINST **20** P02018



Outer Barrel

Inner System (replacable)

Outer Endcap

ITk Pixel Structures

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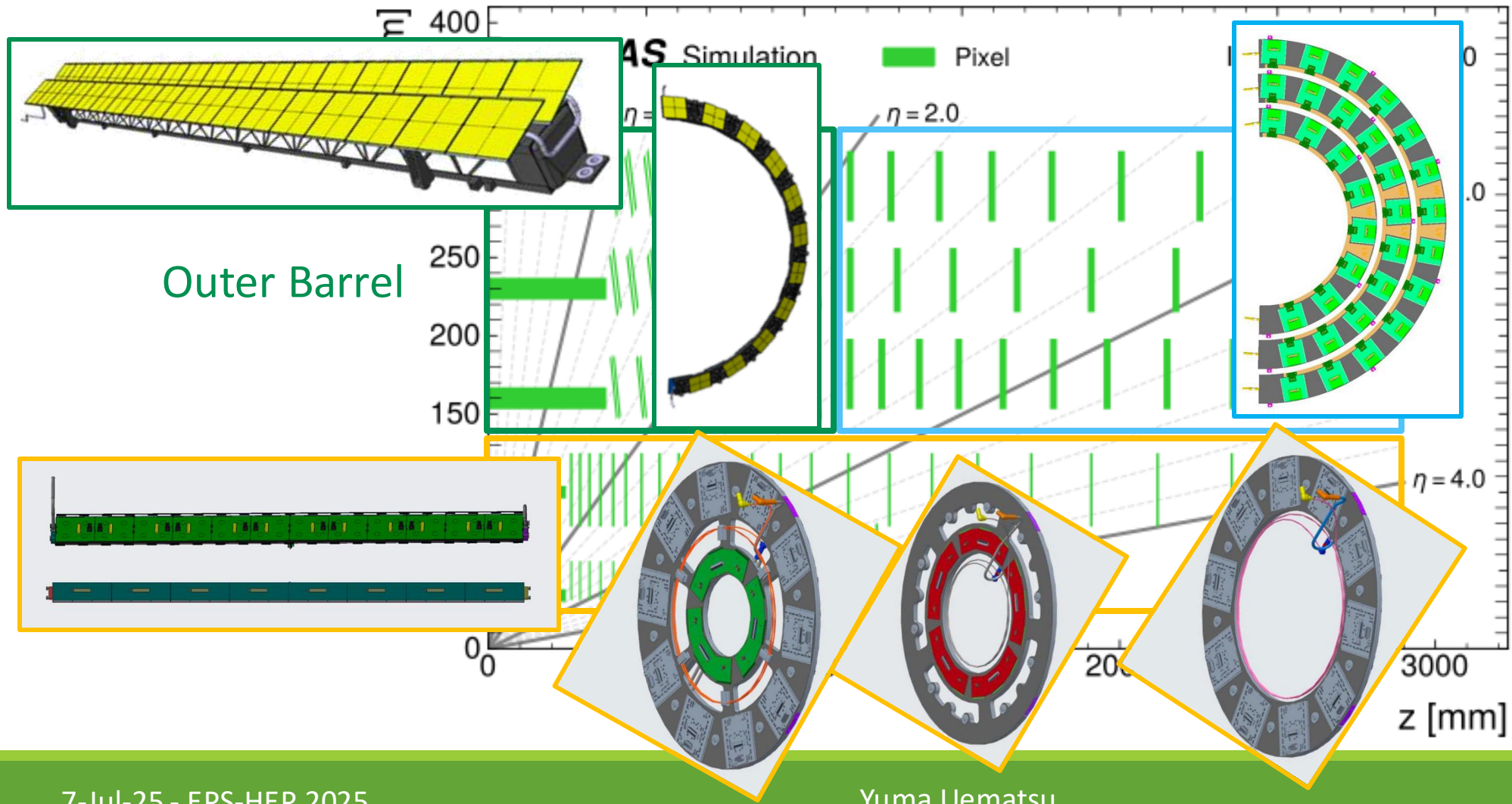
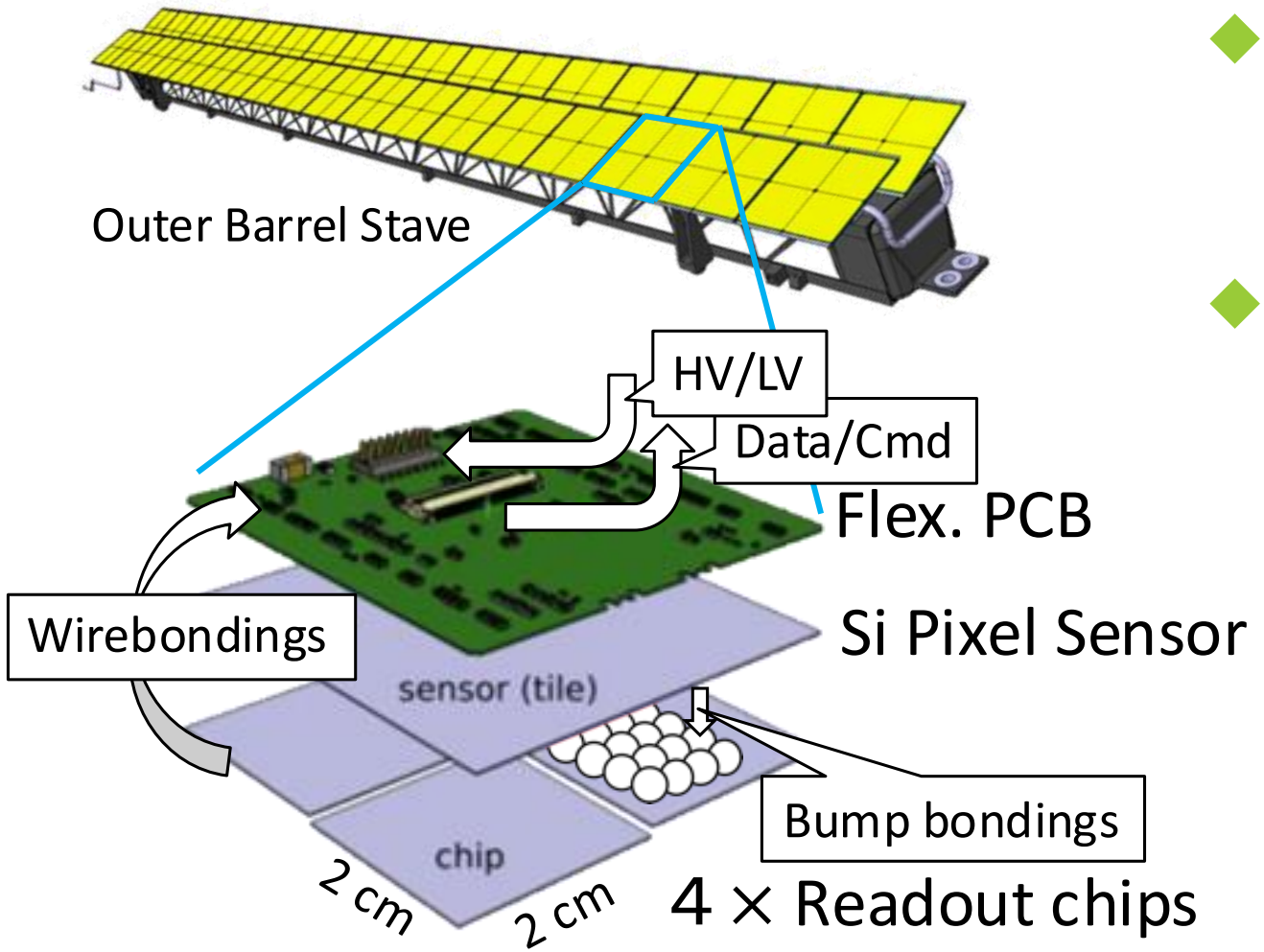


Outer Barrel

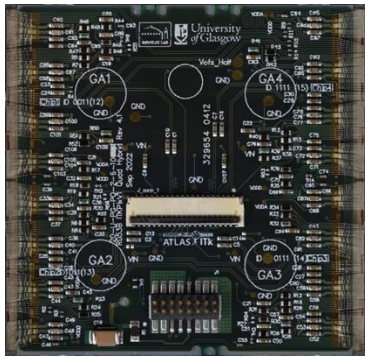
Outer Endcap

ITk Pixel Module

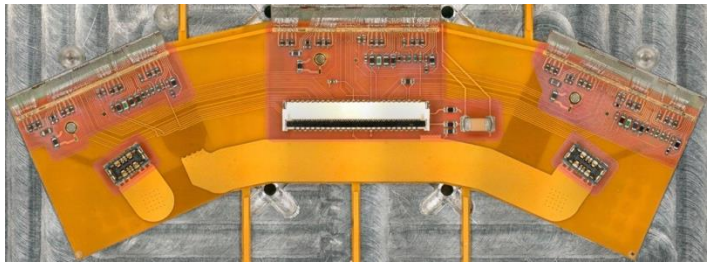


- Detector = Compilation of Module
  - Module = Unit detector component
  - Full detector needs 8372 modules
- Module Flavors
  - Layer-1 – 4: Quad = 1 sensor + 4 chips
  - Layer-0: Triplet = 3 (small sensor + chip)s

Quad Module

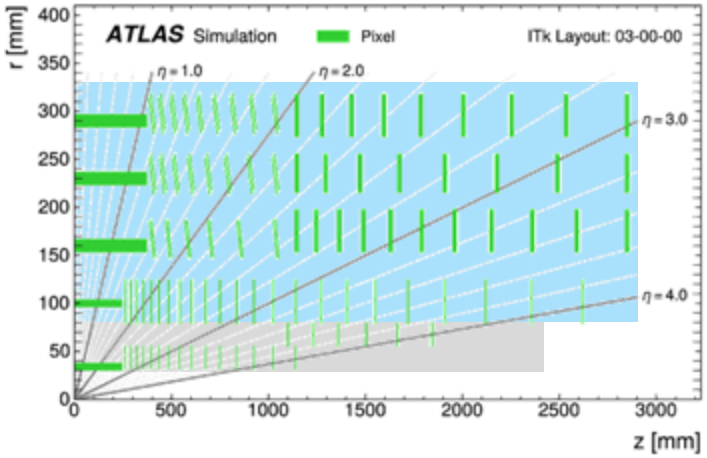


Triplet Module (Layer-0.5 ring)

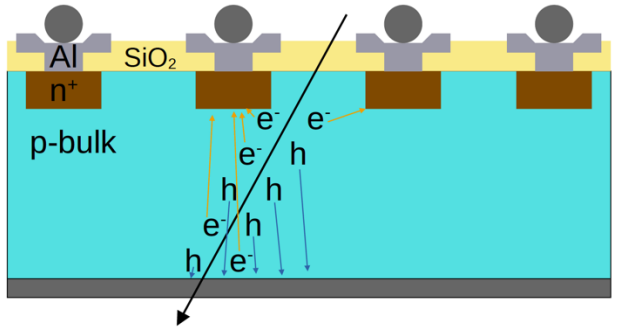


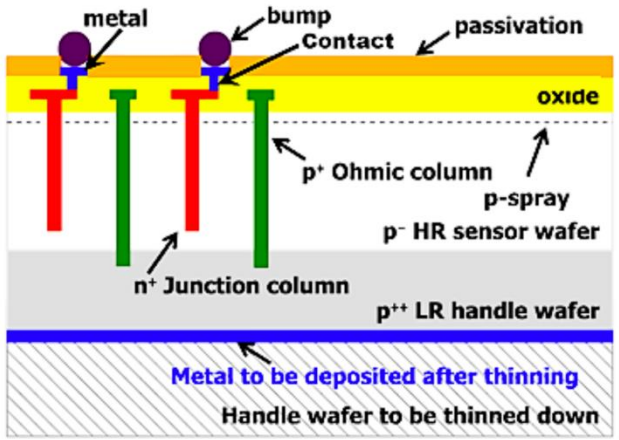
Sensor Technologies

planar (Quad)



3D (Triplet)





Y. Tian, ICHEP2024

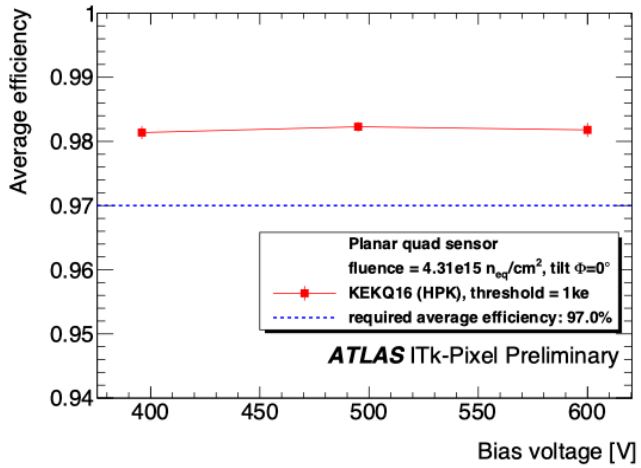
- n^+-in-p
- $50 \times 50\ \mu m^2$ pitch
- $150\ \mu m$ thick
  - Layer-1 Barrel: $100\ \mu m$ thick (FBK)
- HPK/Micron

- $50 \times 50\ \mu m^2$ pitch
  - Barrel: $25 \times 100\ \mu m^2$ (FBK)
- $150\ \mu m$ thick active layer
- $100\ \mu m$ thick support layer
- FBK/SINTEF

Irradiation Study

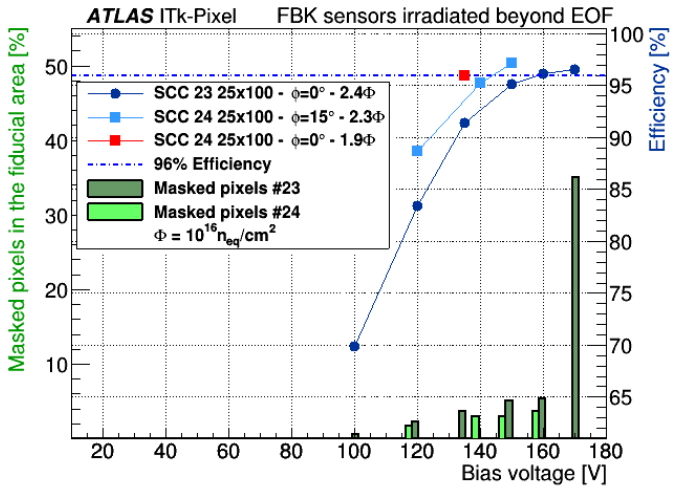
planar (Quad)

ITK-2023-005



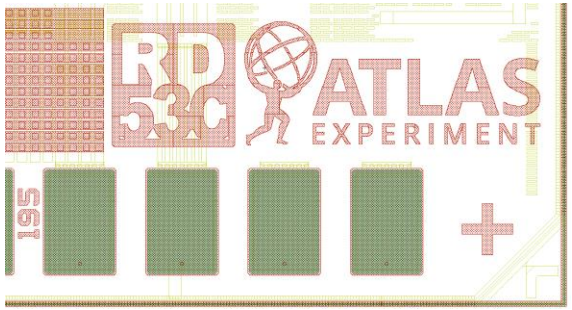
3D (Triplet)

ITK-2023-003



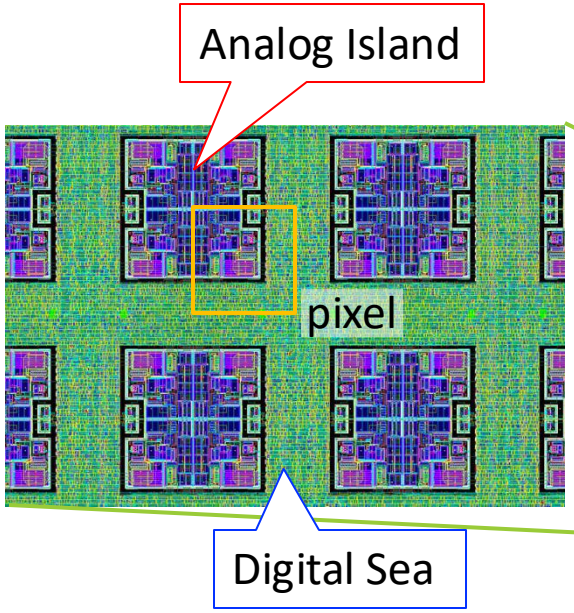
- HPK Planar
  - Layer-1: $4 \times 10^{15} n_{eq}/cm^2$ @4000 fb^{-1}
  - Irradiated $4.31 \times 10^{15} n_{eq}/cm^2$
  - Efficiency > 98% with 400/500/600V
- FBK 3D
  - Layer-0: $1.8 \times 10^{16} n_{eq}/cm^2$ @2000 fb^{-1}
    - replacement at halfway
  - Irradiated up to $2.4 \times 10^{16} n_{eq}/cm^2$
  - Efficiency > 96% with 140V for 1.9Φ

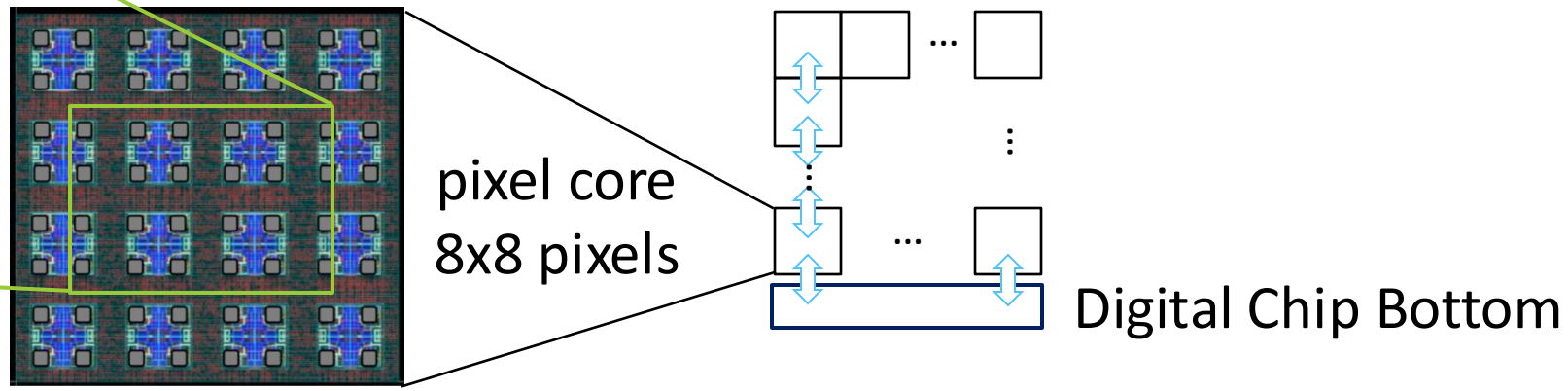
Readout Chip



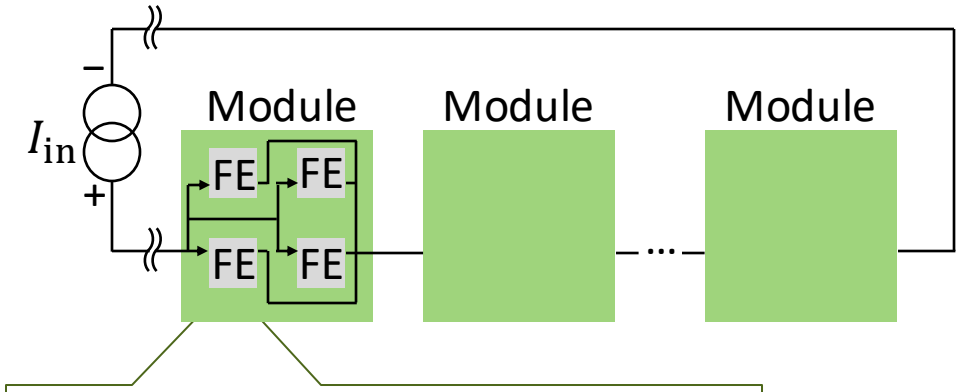
JINST **20** P03024

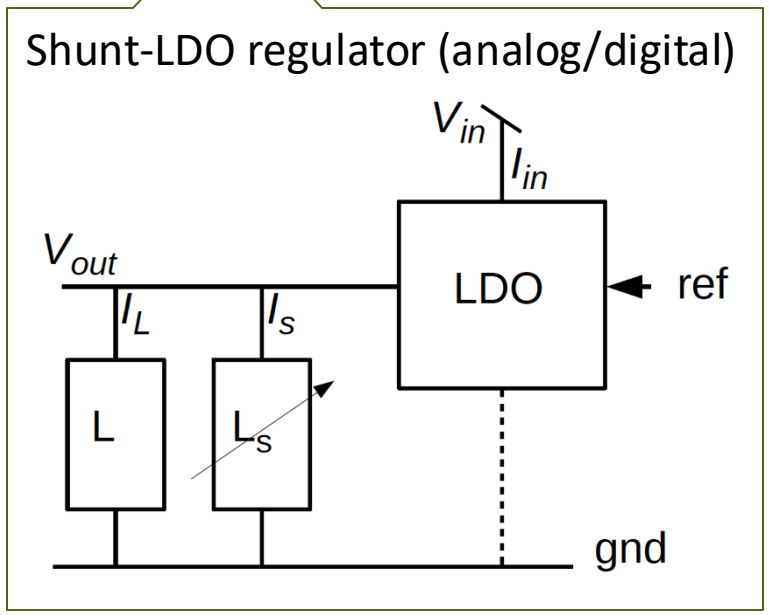
- ITkPix V2
  - ATLAS implementation of RD53C design by RD53 collaboration
    - Differential analog frontend
  - 65 nm CMOS technology
    - $2 \times 2\ \mathrm{cm}^2$; 384×400 pixels; $50 \times 50\ \mu\mathrm{m}^2$ pitch
    - $0.56\ \mathrm{W/cm}^2$
  - Radiation hardness up to 1 Grad
    - Low threshold operation @$1000e^-$ with low dispersion ~ $100e^-$

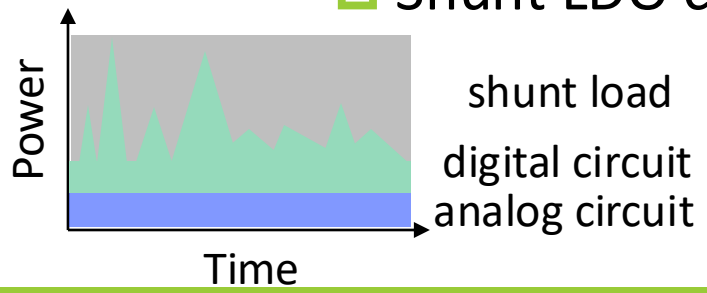




Serial Powering







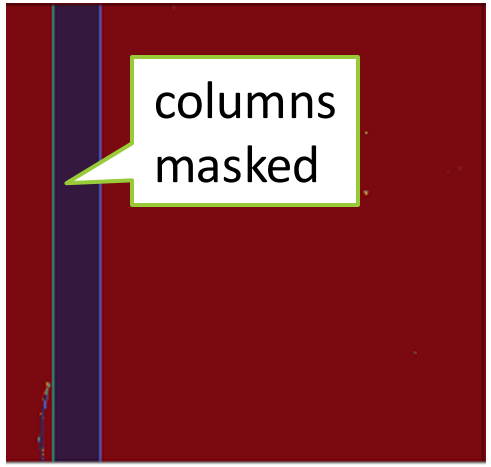
JINST **20** P03024

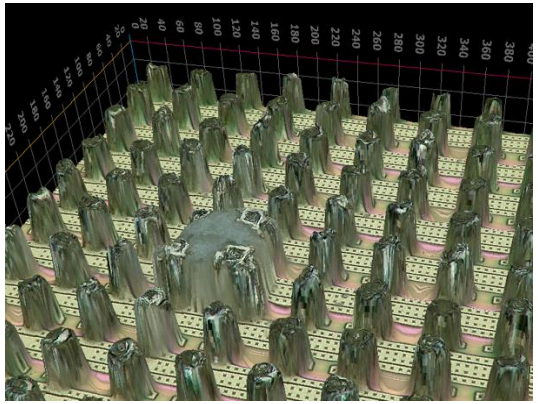
- Serial powering
  - Reduce power cables
  - Also reduce loss in power cables
- Realization
  - Chip power consumption depends on activity
  - Power supply follows voltage change, but with delay due to cable inductance
    → Voltage transients in chain
  - Shunt LDO circuit stabilizes chip impedance

Production Status

- Module production started!
  - > 300 modules assembled
- Bump-bonding has been a challenge in assembly process
  - Bump disconnection/merging
- Recent study suggests another criticality during bonding
  - We see difficulty in reading out some modules
  - Workaround is to disable pixel core columns
  - Higher shunt LDO failure rate in such cases
  - Delamination study → Si debri in masked region!
    - Debri looks large enough to damage chip during bonding
  - → Further care is taken in dicing/bonding (WIP)

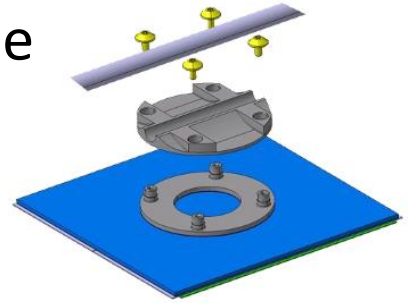
L. Meng, TREDI 2025

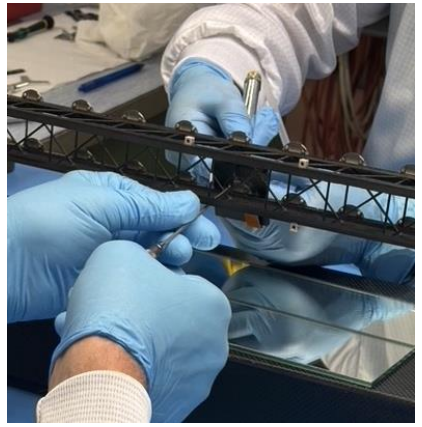




Testing Close-to-Real Demonstrator

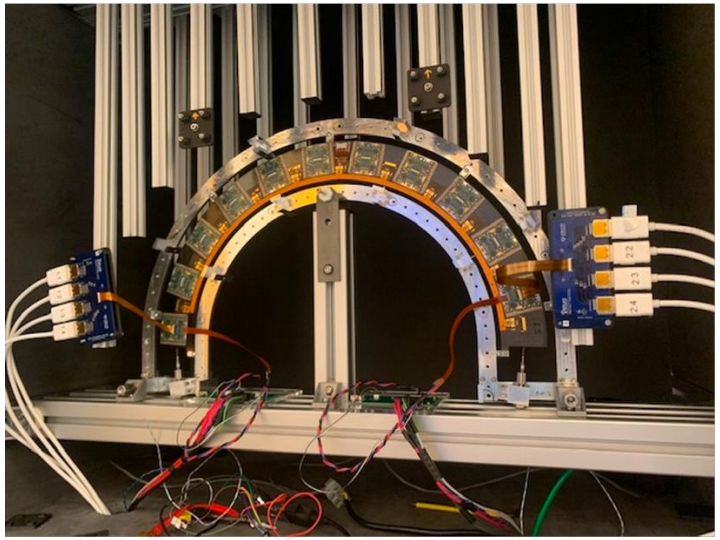
- Pre-production Integration (Outer Barrel)
  - Attach PGT + Cooling Block to backside of module
  - attach to support structure with screws



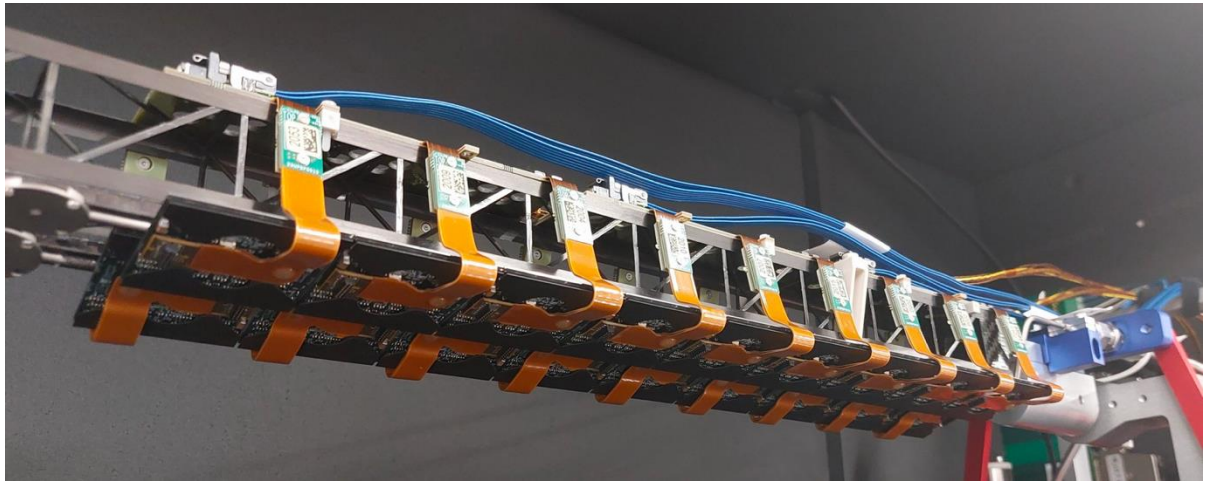


- Readout Test

Outer Endcap



Outer Barrel

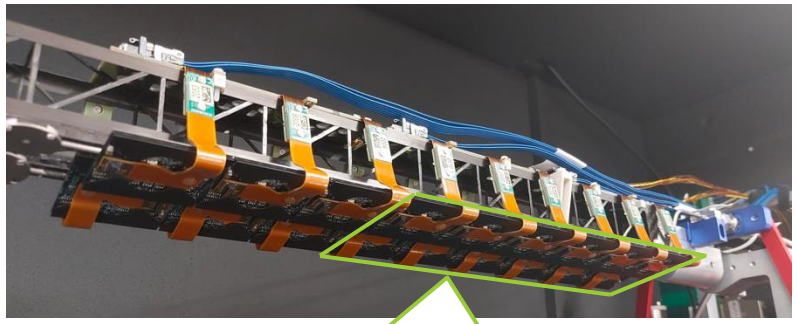


Testing Close-to-Real Demonstrator

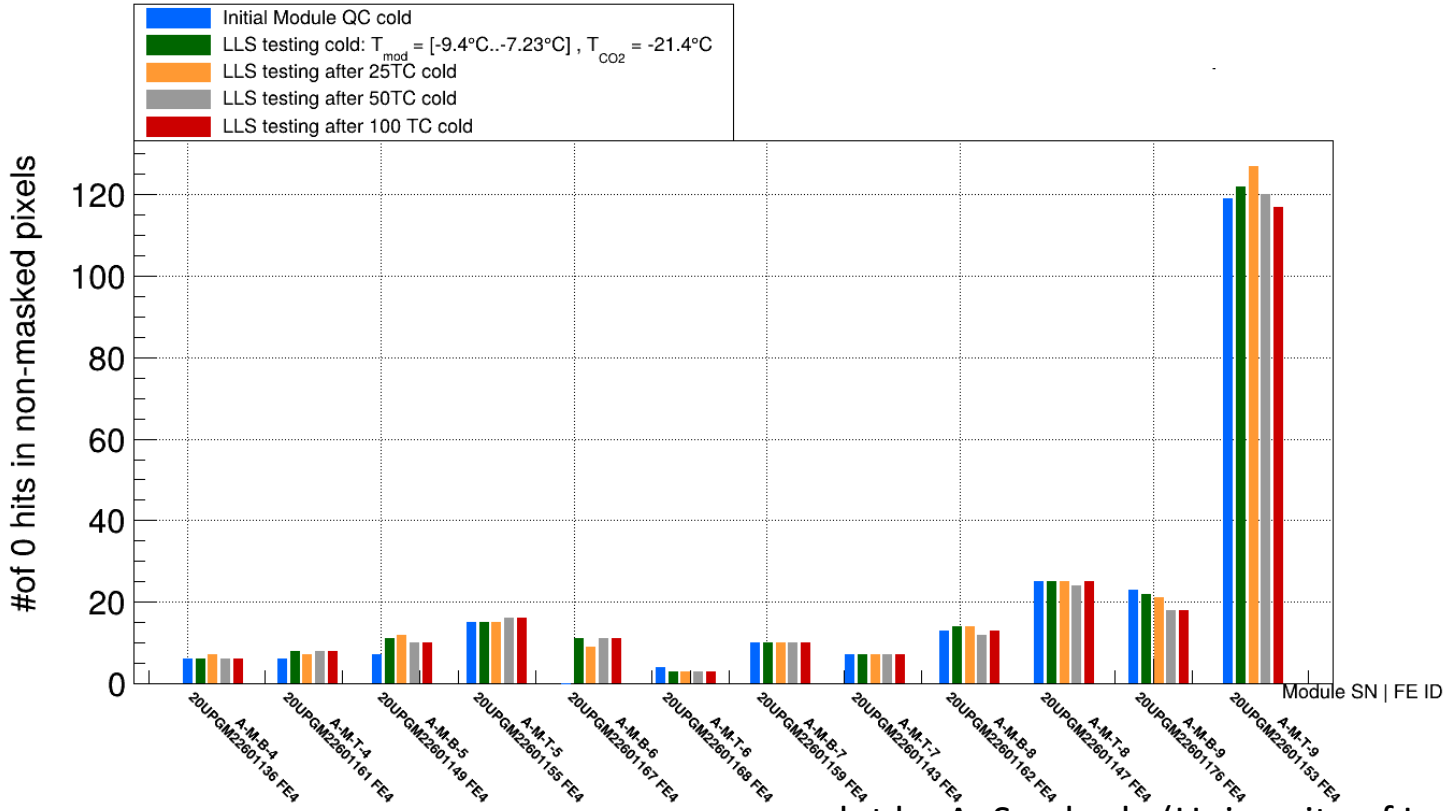
- Thermal Cycle
  - Using temperature forcing system
  - 25 + 25 + 50 = 100 cycles

Testing Close-to-Real Demonstrator

- Readout results after integration
  - No increase in disconnected bump bonds after thermal cycles



Serial Powered
12 Modules



plot by A. Swoboda (University of Innsbruck)

Prospect

- Keep pruduction moving forward!
  - Continue module production for 2 years
  - Launch integration of production modules into large structure
  - Installation of ITk (strips + pixels) in the ATLAS cavern in 01/2029

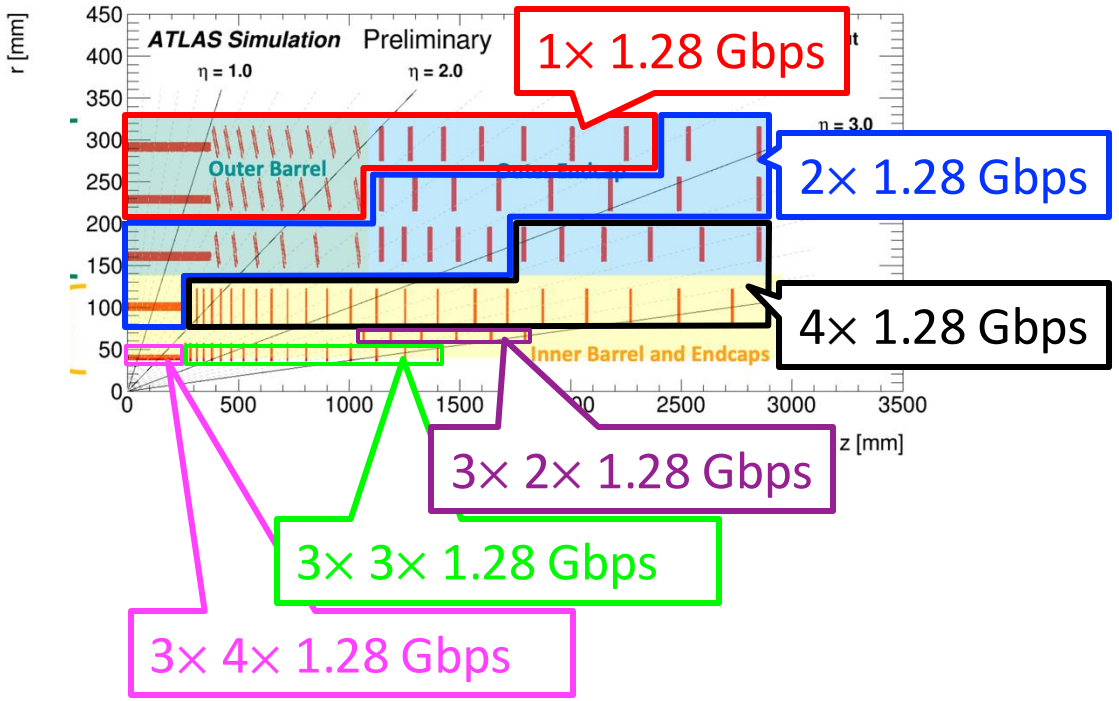
- Study cases where we need to integrate problematic modules
  - Tracking performance with pixel core column masked in simulation (WIP)
  - Large-scale powering and read out test of pixel core column masked modules
- Development of DAQ and DCS towards detector operation

Summary

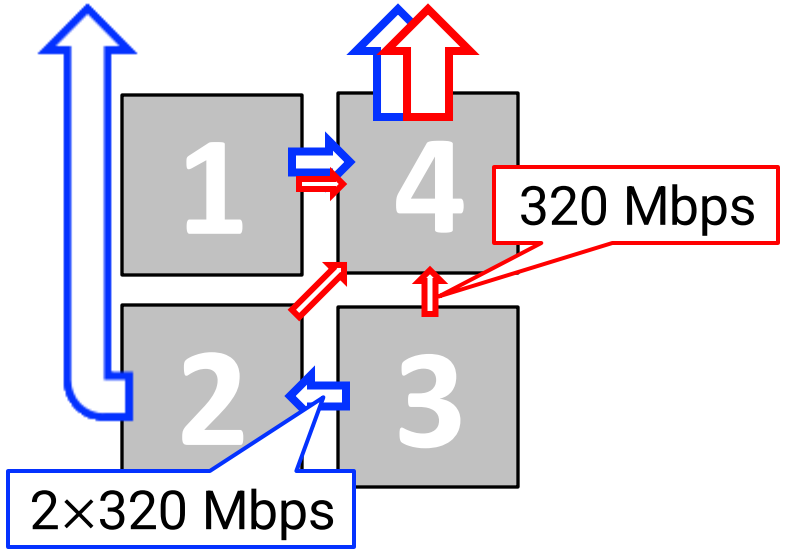
- ATLAS will replace inner detector with 9-layer all silicon detector for HL-LHC
  - Inner 5 layers features hybrid Pixel detector
- Key design
  - Radiation hard sensors/readout chip
  - Data/Power cables optimization
- Module production started; Integration will follow!

Backup

Data Links



- Optimization of data cables
  - Up to 4 1.28Gbps data links per chip
  - Optimize #links depending on the location
  - Shared data link by on-chip merging of data from neighboring chips



Pixel Core Columns Masking

L. Meng, TREDI 2025

- Fraction of affected chips are similar across hybridization vendor
  - = Not associated with a single vendor
- approximately x3 or 4 for fraction of affected modules