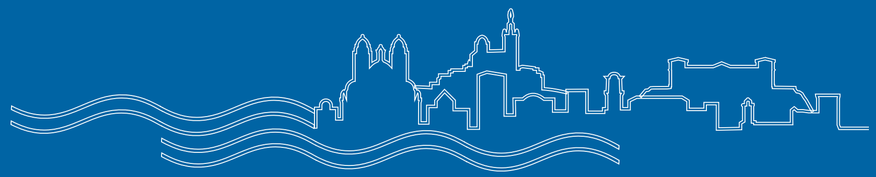
EUROPEAN PHYSICAL SOCIETY
EPS HEP2025 MARSEILLE



Status and testing of the MDT Trigger Processor for the ATLAS L0 Muon Trigger at HL-LHC

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On behalf of the ATLAS collaboration

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ATLAS EXPERIMENT

The Phase-II L0 MDT Trigger Processor

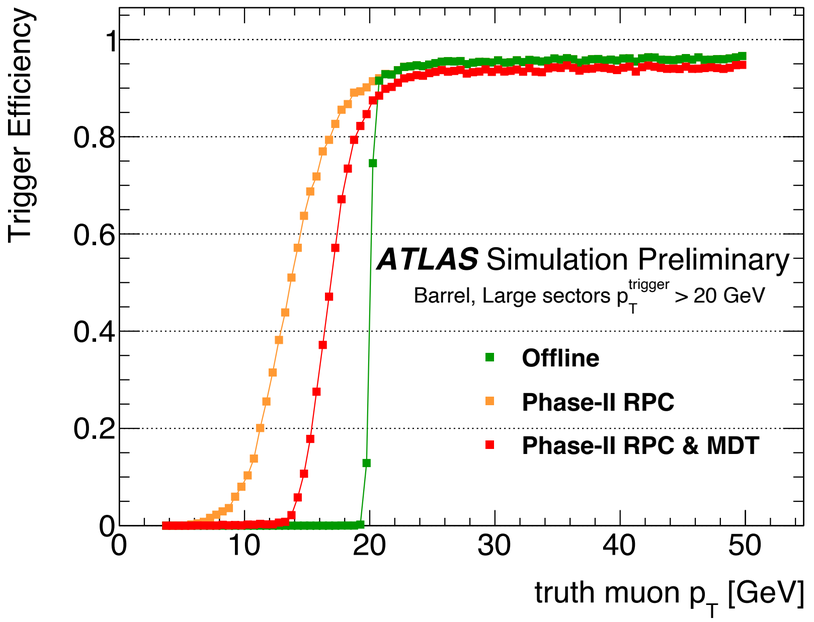
- In order to cope with HL-LHC conditions, several upgrades are foreseen for the ATLAS muon trigger

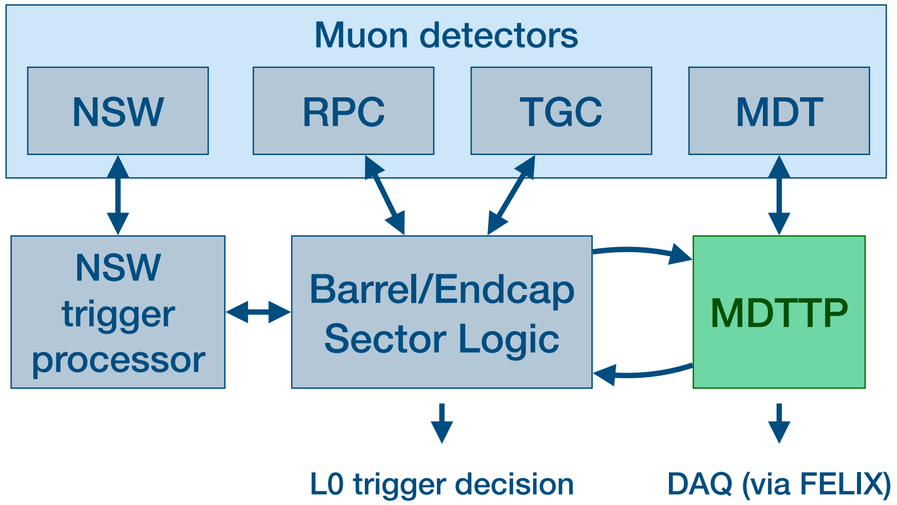
- The Level-0 Muon Trigger brings the precision of the **Monitored Drift Tubes (MDT)** detectors into the trigger algorithm, in order to compensate the limited spatial resolution of Resistive Plate Chambers (RPC) and Thin Gap Chambers (TGC)

- The **L0 MDT Trigger Processor (MDTTP)** combines the Sector Logic (SL) trigger candidate information with the information from the MDT detectors, refining the muon pT measurement and reducing the fake trigger rate

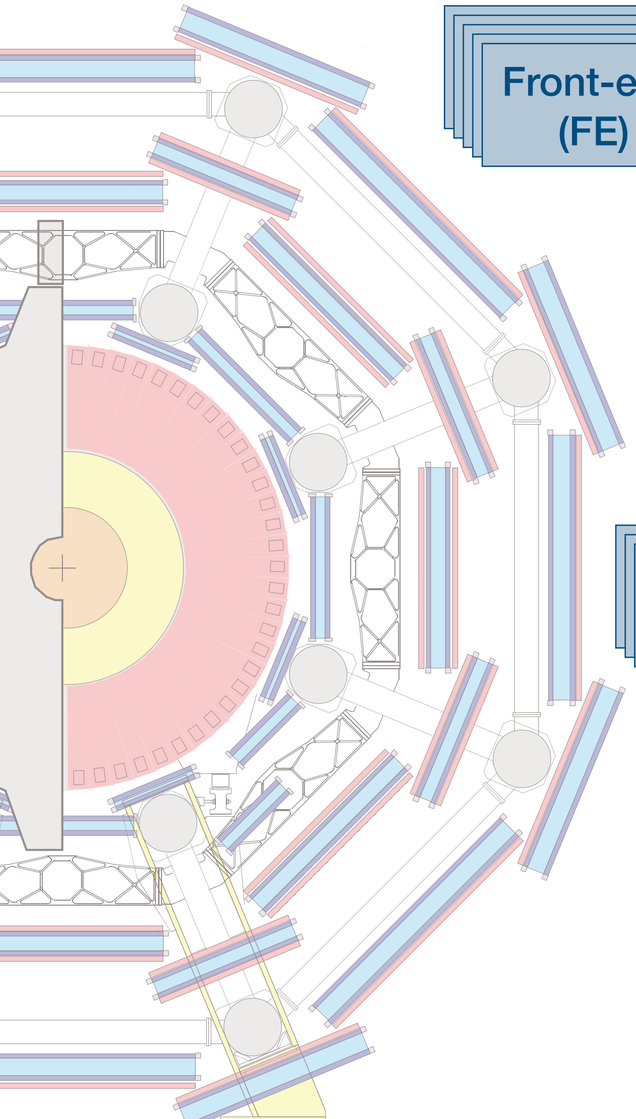
- Configuration, monitoring and readout of the MDT on-detector electronics is also performed via the MDTTP

L0Muon public plots





MDTTP ecosystem



On-detector
UX-15 Cavern

Off-detector
USA-15 counting room

Front-end (FE)

Up to
20 x CSM

Time-to-digital converted (TDC) MDT hits

Chamber Service Module (CSM)

Up to
24 x ATLAS Sector

Barrel/Endcap (SL)

SL Candidates

SL Candidates with improved pT measurement

MDT Trigger Processor

64 boards
One per ATLAS sector

Timing, trigger and control (TTC)

MDT hits readout

Front-End link exchange (FELIX)

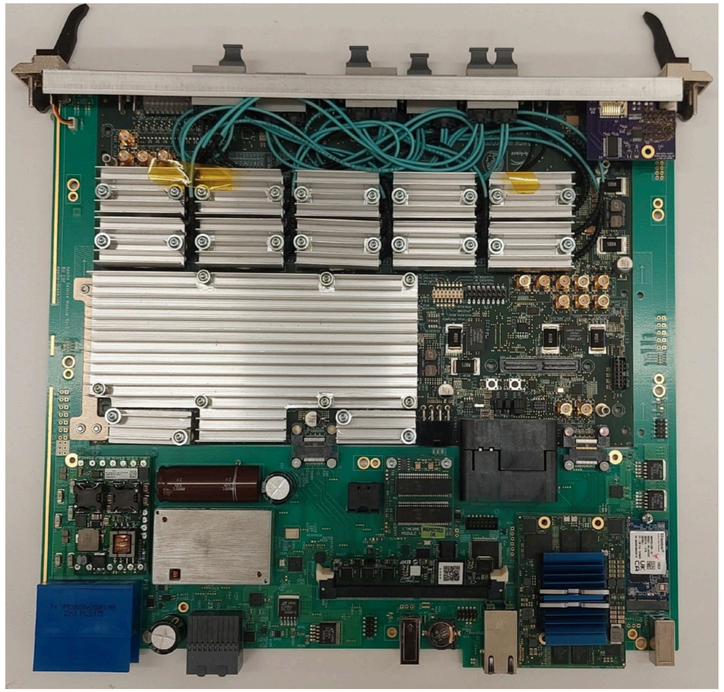
Configuration
Monitoring
Control

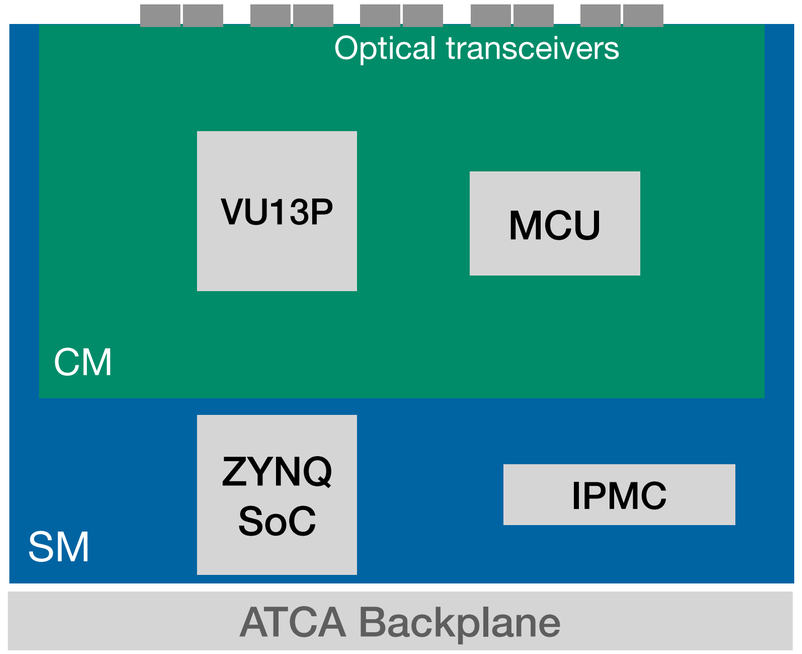
ATLAS Network

MDTTP board

- ATCA blade using the open-source design of the **Apollo-LHC project**

- Each board is composed by a Service Module and a Command Module
  - **Command Module (CM):**
    - Features a **Virtex VU13P FPGA**
    - Optical connectors for on-detector electronics, Barrel/Endcap Sector Logic and **FELIX** for readout and **TTC** (clocks and L0 accept)
    - A microcontroller unit (**MCU**) allows control and monitoring of the hardware on the CM
  - **Service Module (SM):**
    - Implements ATCA standards, requirements and power delivery to the CM
    - Features a **IPMC** controller and a **ZYNQ MPSoC** (Quad-core ARM at 1.2 GHz with 4 GB RAM)
    - AlmaLinux running on the ZYNQ hosts all the services for monitoring, configuration and control



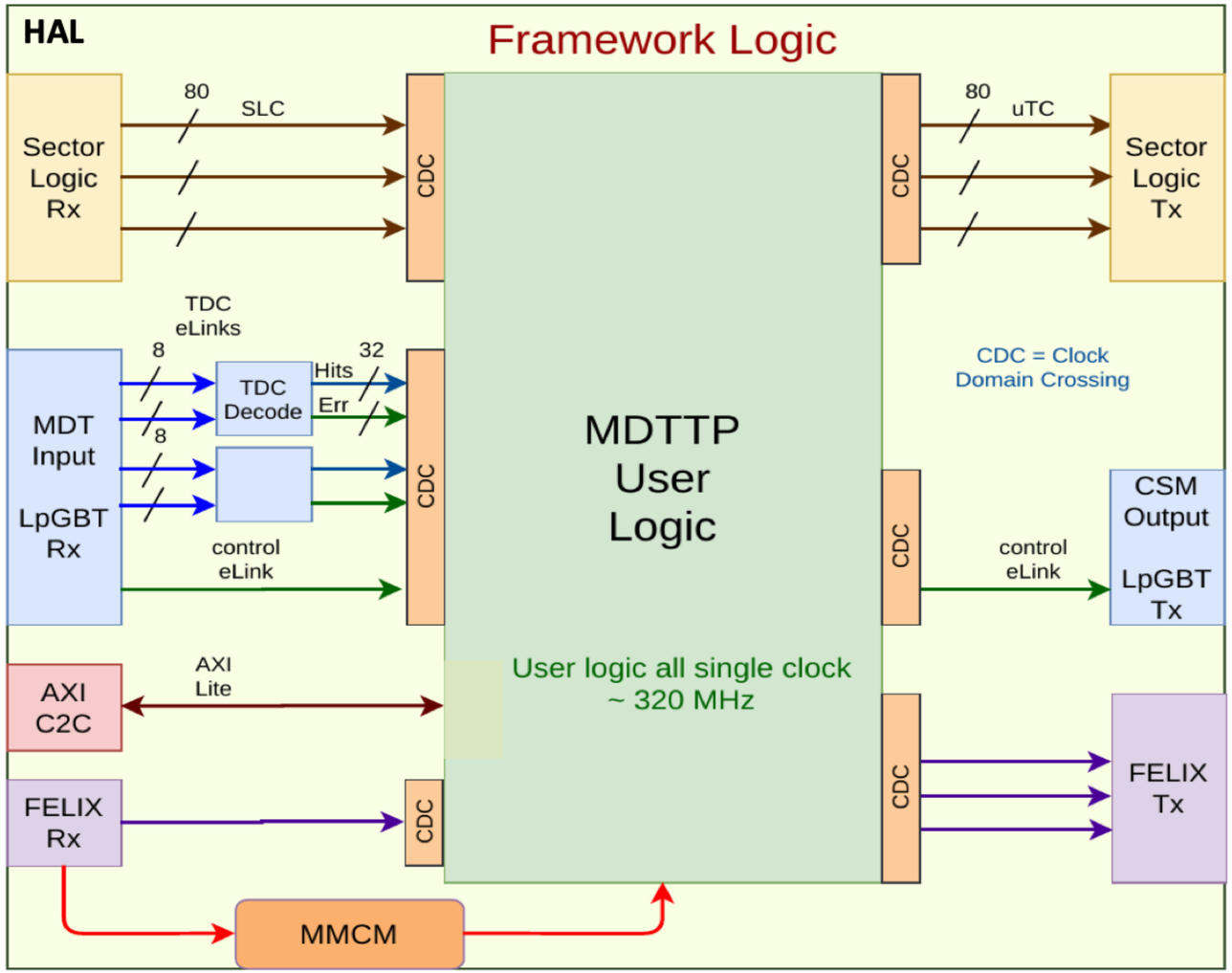


MDTTP firmware overview

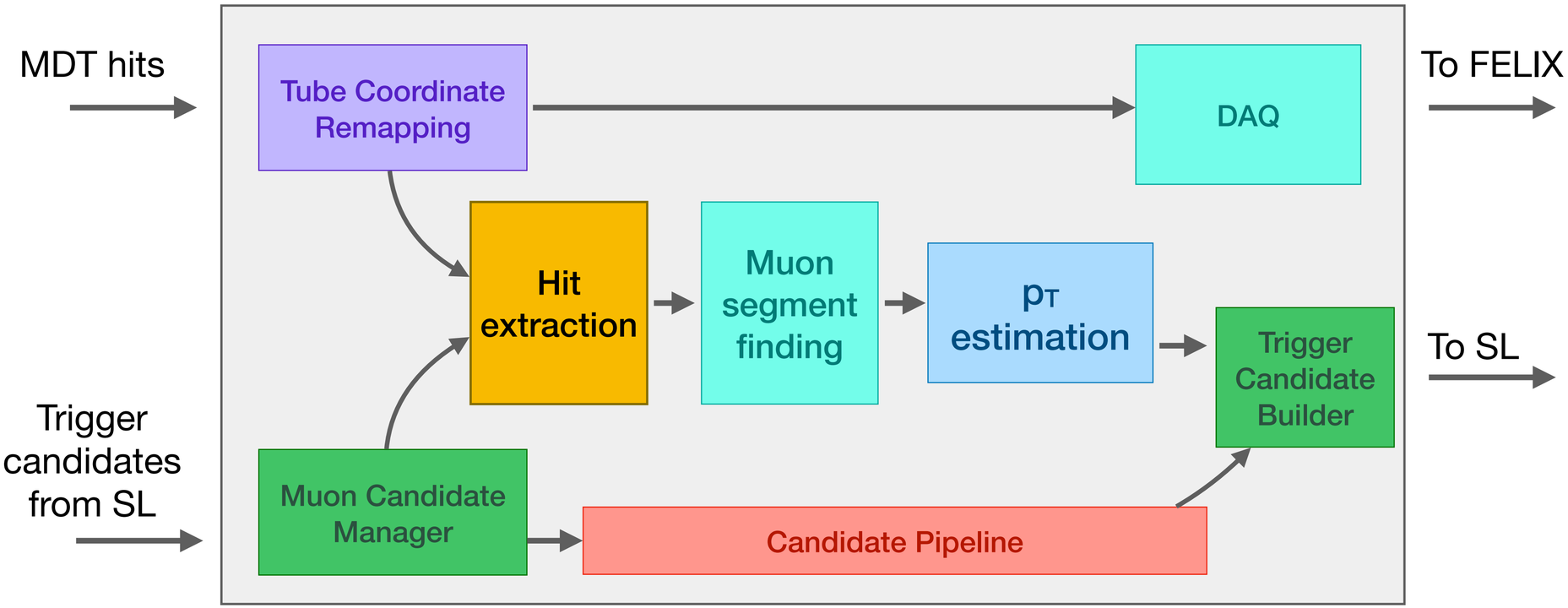
- The VU13P firmware is organised in two macro-blocks

- **Hardware Abstraction Layer** (HAL)
  - I/O interfaces with CSM, SL and FELIX
  - MDT TDC hits preprocessing
  - Clocking
  - AXI Chip2Chip interface with the SM ZYNQ

- The **User Logic** implements the MDT trigger algorithm and DAQ



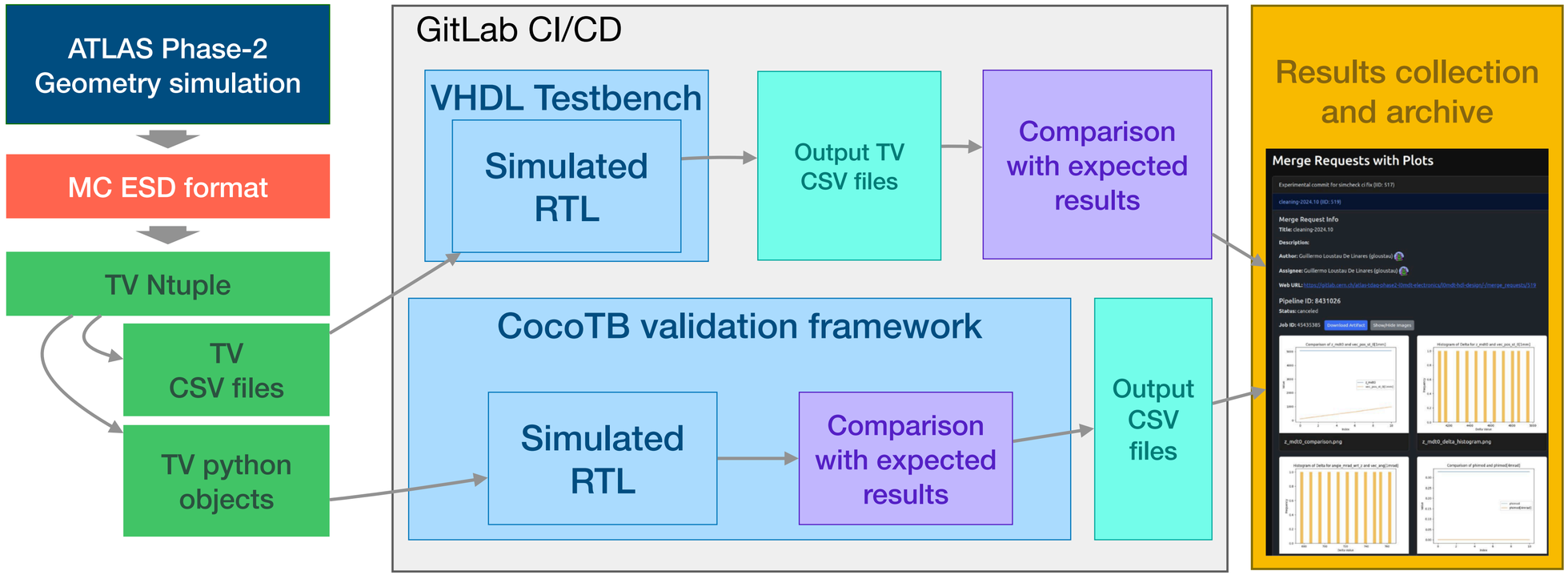
MDTTP trigger logic overview



- Two options for the segment finder: Compact Segment Finder and Legendre Segment Finder (more details here)
- Multi-threaded logic with static routes to process hits and trigger candidates from different stations in different threads
- Work in progress to move from static to dynamic thread assignment in order to improve resource usage and processing time

Firmware validation pipeline

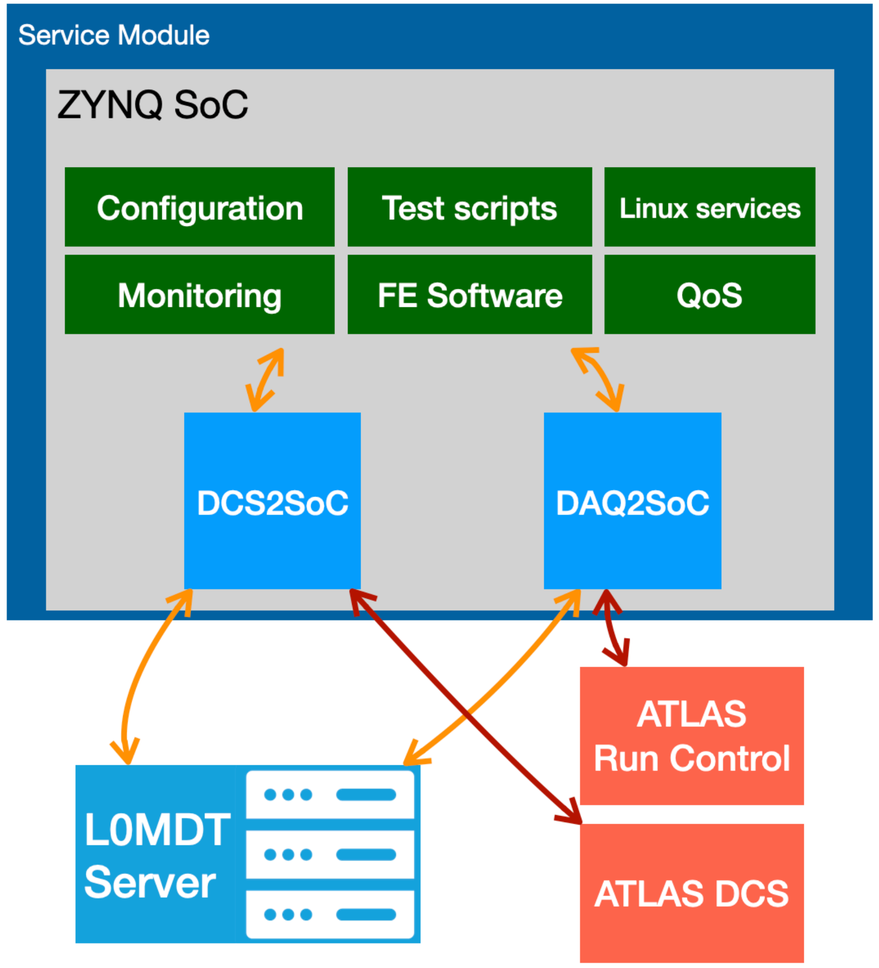
- Inputs are obtained from the Phase-II ATLAS simulation
- Test Vector (TV) Preprocessing pipeline using dedicated format
- Dual-implementation of the Register Transfer Logic (RTL) simulation using a pure VHDL framework and a python-based framework using CocoTB, relying on HDL-on-git (Hog)
  - Possibility of simulating isolated or multiple RTL blocks, up to the complete trigger logic
- Comparison with expected results from simulation and artefacts collection for long-term storage



Control and monitoring - I

- **Remote control and monitoring are needed to ensure reliable and scalable operations of the MDTTP and the on-detector electronics**
  - L0MDT server is employed as a gateway to the MDTTPs during development
  - Control and monitoring already based on services compatible with Phase-II operation systems

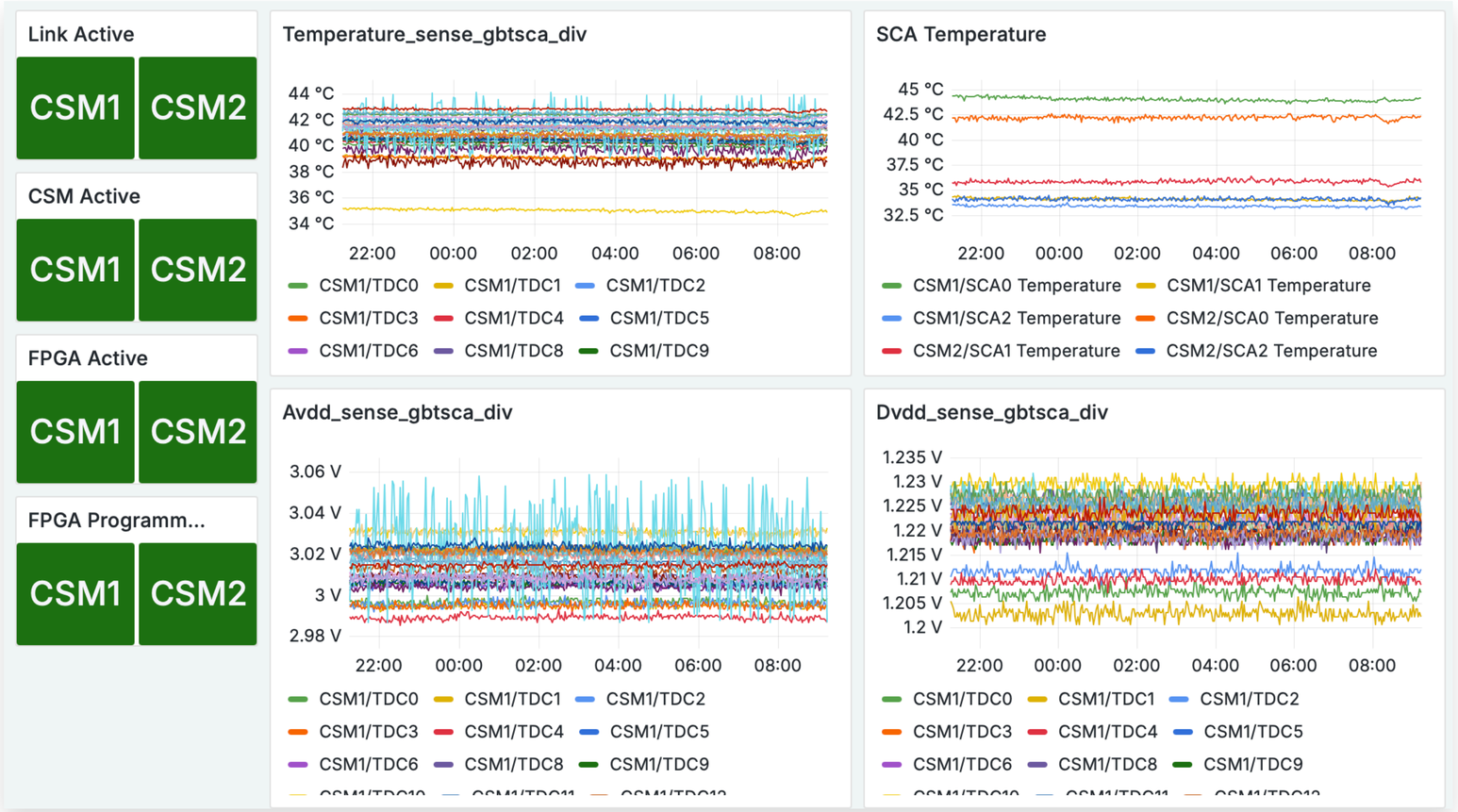
- **DAQ2SoC service:**
  - Implements HTTP API corresponding to specific commands executed by the SoC (Power control of the CM, FPGA programming, initialisation and configuration of the FE)
  - Keeps track of the status of the MDTTP and upstream electronics implementing finite state machine
  - Service shared across ATLAS Phase-2 TDAQ systems relying on SoC



Control and monitoring - II

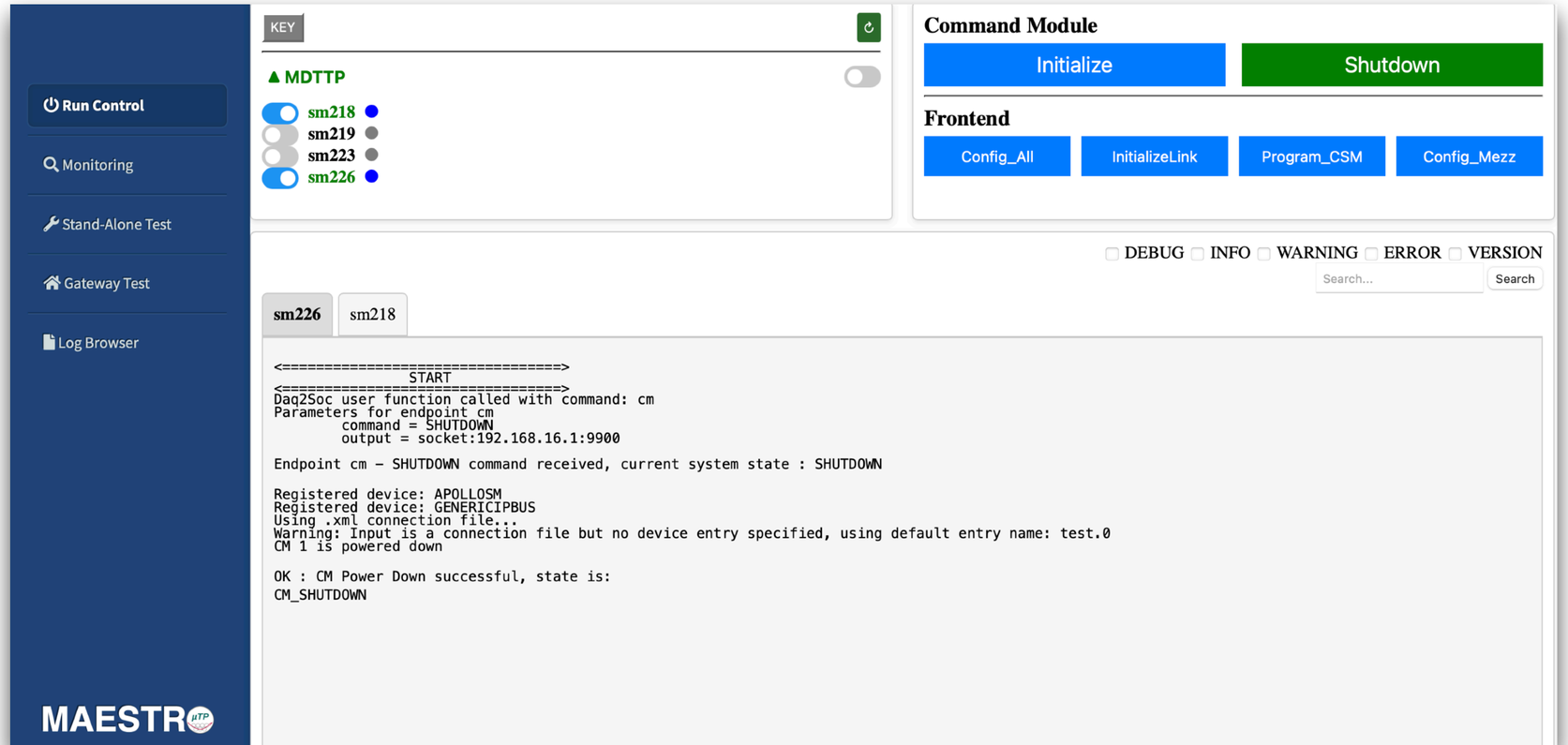
- **DCS2SoC service:**
  - Implements OPC UA server compatible with the ATLAS Detector Control System
  - Publishes monitoring values of the on-detector electronics

- During the development phase, monitoring values are stored in a time-series database enabling visualisation with grafana



Control and monitoring - III

- Dedicated web interface to simplify interaction with the MDTTP and on-detector electronics
- Streamlines initialisation and configuration of the available boards, allowing the remote execution of tests on multiple devices at a time
- Developed for extensive use during the development stage, with the target to migrate it to a tool to support experts during HL-LHC runs

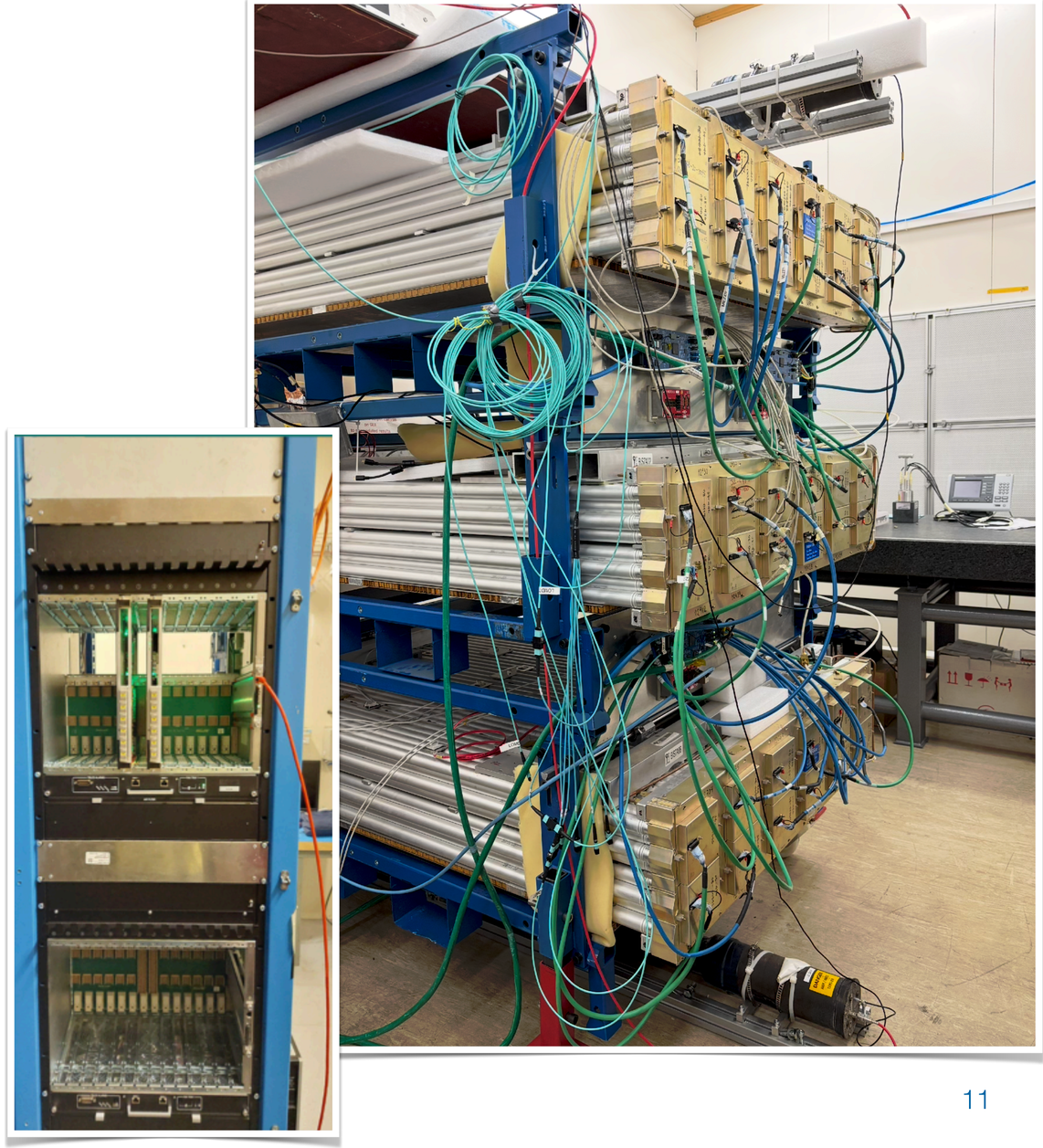


Test stands at CERN

- Several tests are conducted with a MDT Vertical Slice with 3 MDT stations, 3 CSMs and 36 TDC boards
  - On-detector electronics configuration and monitoring
  - Interface with readout via the FLX-182 platform
  - Data acquisition tests using cosmic rays

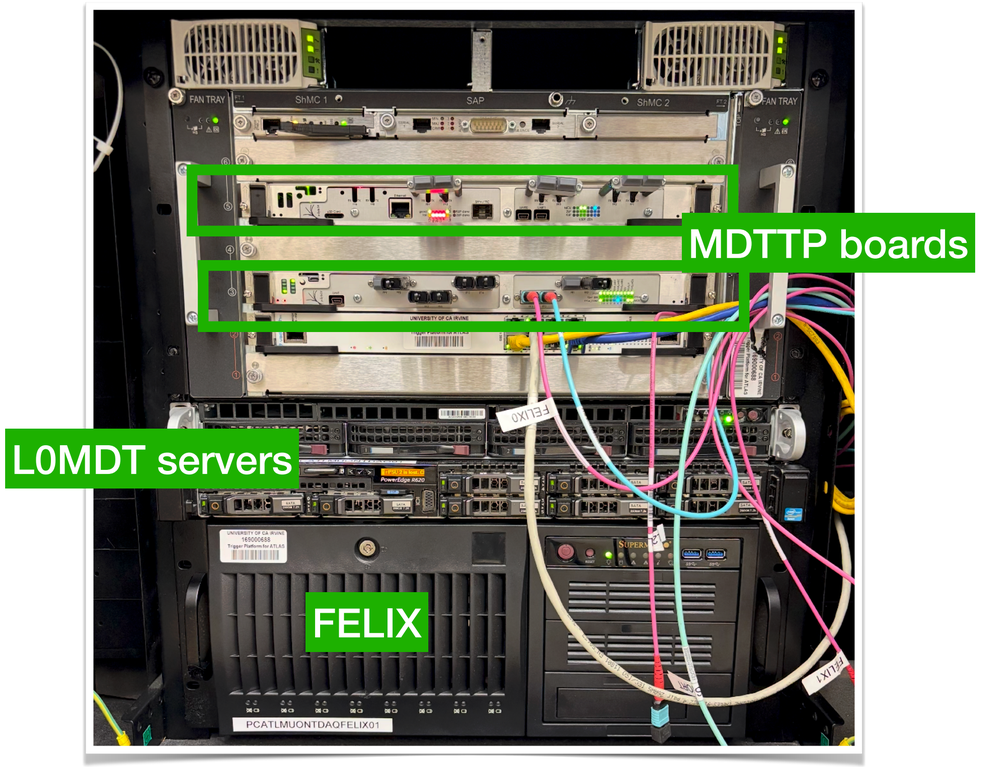
- Separate test-stand shared with other Muon TDAQ systems
  - Integration with the Barrel/Endcap SL
  - Full-crate thermal and airflow tests
    - Currently testing fiberglass-epoxy (FR4) and aluminium covers for the MDTTP blade
  - Network strategy development

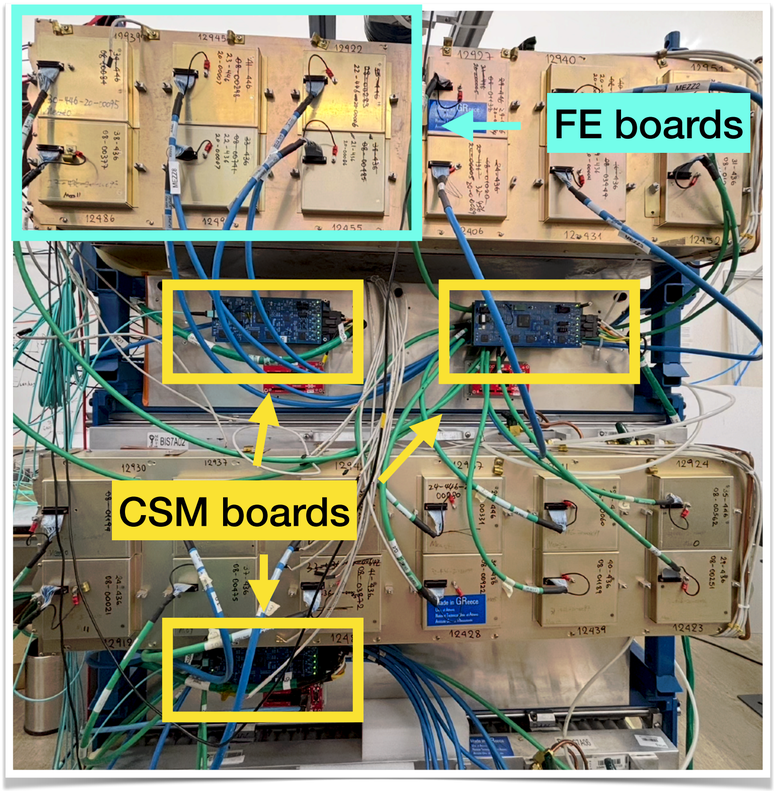
- Additional test stand at research institutes and universities



On-detector electronics configuration

- Exercised connection with CSM boards and configuration of the FE
- Monitoring of the optical link between CSM and MDTTP based on actual data received in the transceiver
- Scaling up to multiple MDT chambers and CSM boards





Communication with FELIX

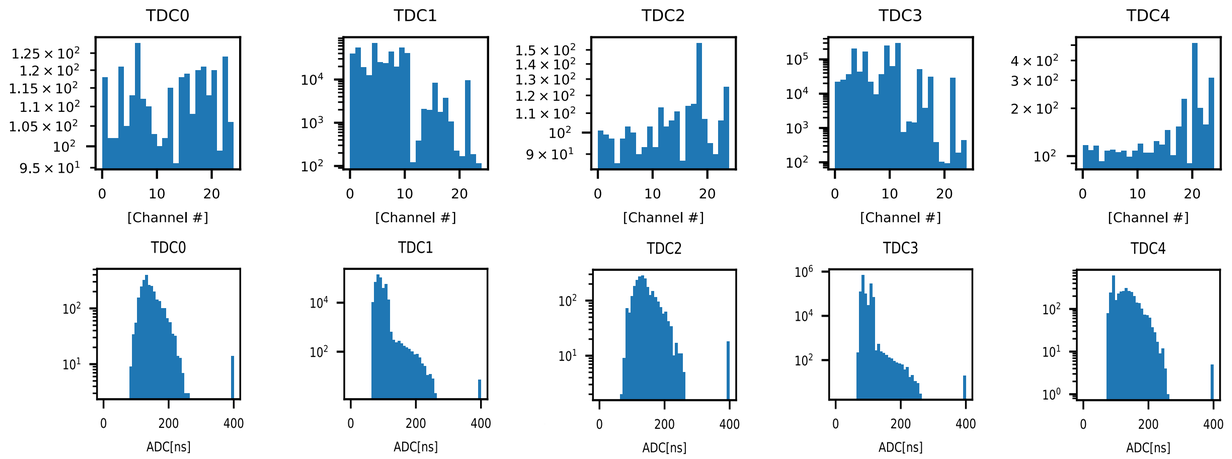
- Interface with FELIX was tested for TTC distribution and data acquisition
  - MDTTP clocks successfully aligned with the one distributed from FELIX
- MDTTP to FELIX links aligned allowing triggerless DAQ

```
Card type : FLX-182
Firmw type: FULL

Link alignment status
-------------------------
Channel |  0    1    2    3    4    5    6    7    8    9   10   11
        ---------------------------------------------------------------
Aligned | NO   NO   NO   NO   NO   NO   NO   NO  YES  YES  YES  YES

Channel | 12   13   14   15   16   17   18   19   20   21   22   23
        ---------------------------------------------------------------
Aligned | NO   NO   NO   NO   NO   NO   NO   NO   NO   NO   NO   NO
```

Active links



Conclusions

- The L0 MDT project is progressing rapidly on all fronts
- Hardware is in the pre-production stage
- Test stands at CERN and Universities are a good environment to exercise the system and validate the interface with other ATLAS subsystems
- Configuration and monitoring software are available and are constantly used across all the test stands
- Firmware is constantly being improved in order to improve processing capabilities and resource usage