Development of the Online System for COMET Phase-I

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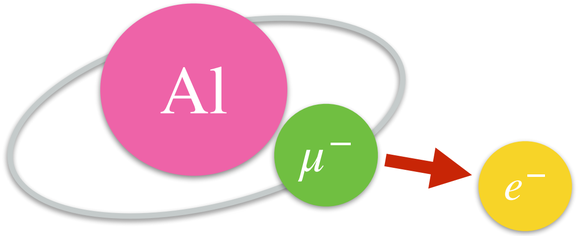
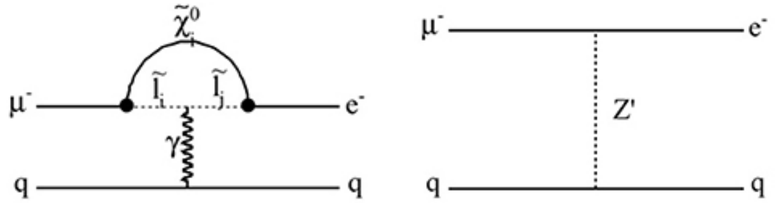
EPS-HEP 2025 @ Marseille

COMET Phase-I @ J-PARC, Japan



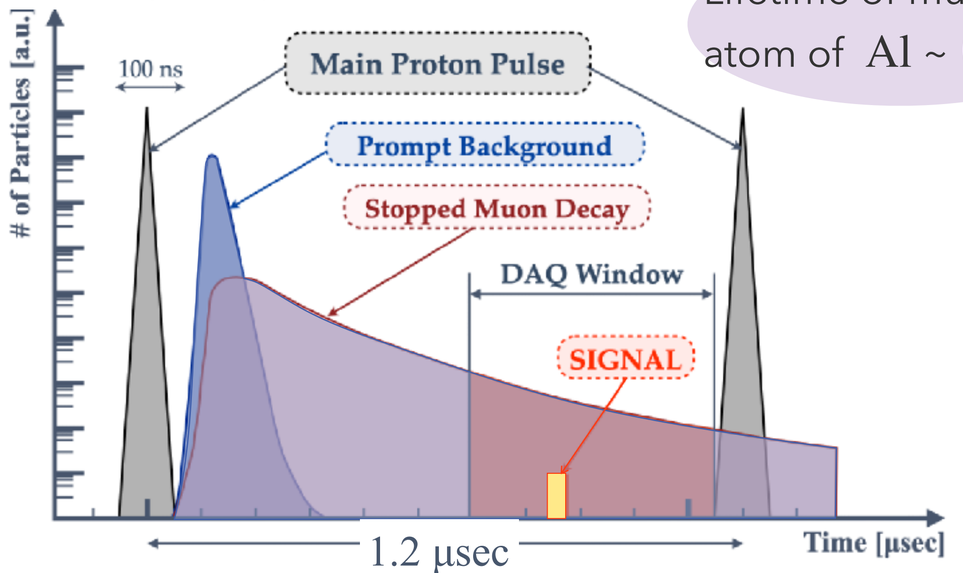
Search for $\mu - e$ conversion in muonic atom (of Al)

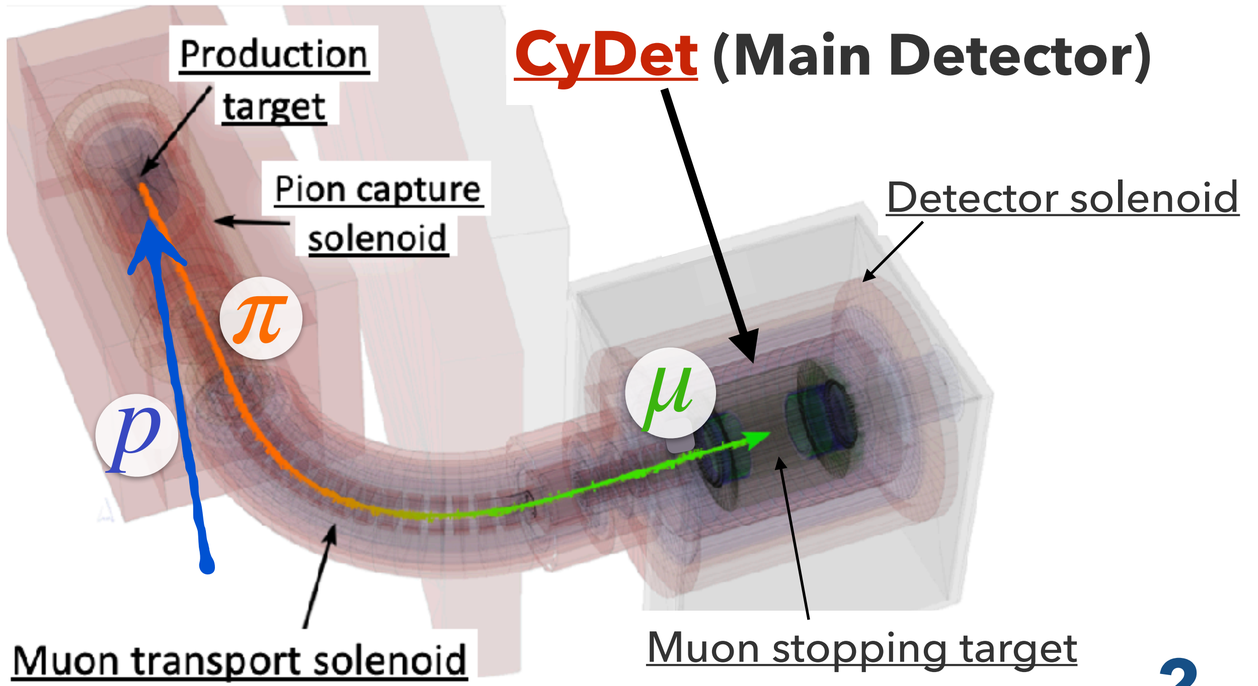
- **One of the <u>charged Lepton Flavour Violation</u> processes**
  - Standard Model w/ neutrino oscillation … $\mathcal{B}(\mu^- N \to e^- N) < O(10^{-57})$
  - New Physics (SUSY-GUT, Z′, etc..) … $\mathcal{B}(\mu^- N \to e^- N) \sim 10^{-15} - 10^{-13}$



- **Target Single Event Sensitivity =** 3×10^{-15}
  - Current upper limit w/ Au $\mathcal{B}(\mu^- \mathrm{Au} \to \mathrm{e}^- \mathrm{Au}) = 7 \times 10^{-13}$ 90% C.L. (SINDRUM II) W. Bertl et al. DOI: <u>10.1140/epjc/s2006-02582-x</u>
- **Beam structure**
  - $\sim 10^{12}$ proton/sec
  - 1.2 μsec pulse time intervals

Lifetime of muonic atom of Al ~ 0.9 μsec



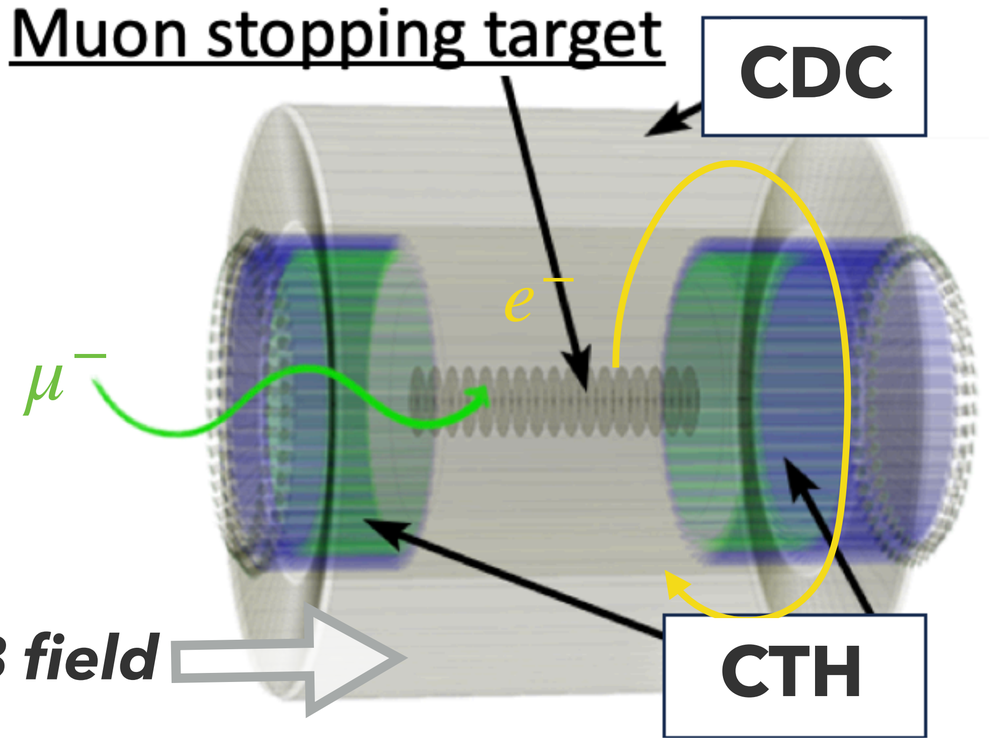


CyDet (Main Detector)

CDC (Cylindrical Drift Chamber)

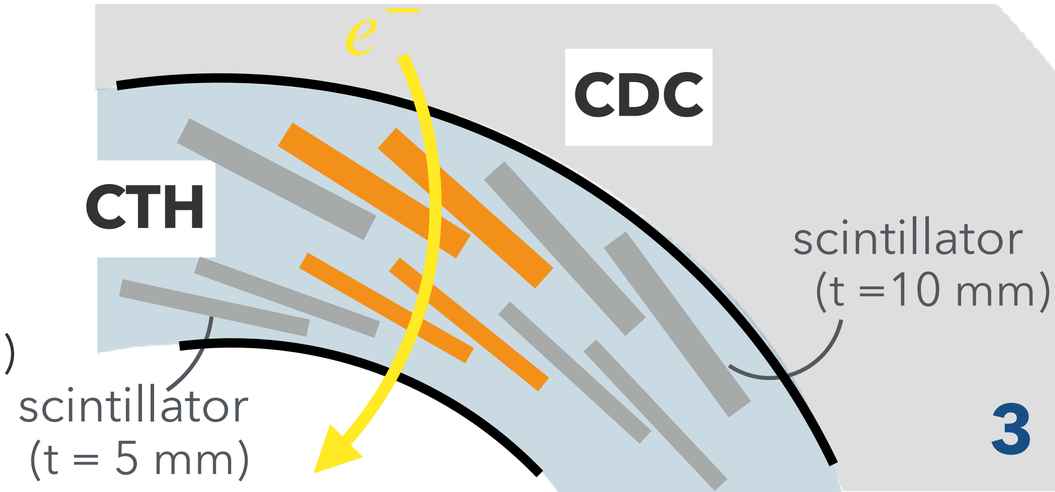
- Tracking, **measuring the e^- momentum**
- He:iC_4H_{10} = 90:10
- ~5000 sense wires (full stereo angle)
- ~250 cell (azimuthal) × 20 layers (radial)
- Momentum resolution 200 keV/c

A.Sato et al : DOI:10.1016/j.nima.2024.169926



CTH (Cylindrical Trigger Hodoscope)

- **Primary trigger** generated by 4-fold coincidence
- Timing measurement with 1 nsec precision
- 64 plastic scintillators × 2 layer × 2 side (upstream & downstream)



COMET Online System Overview & Requirements

Trigger System

Fast, efficient online event decision

- Multi-stage electronics with FPGA

Data Acquisition (DAQ) System

Scalable data handling

- Fully parallel & asynchronous design

Monitoring System

Stable management of the detectors / devices

- **Hardware stability**

  Estimated radiation dose in detector area

  Neutron : 10^{12} $n_{1-MeVeq}/cm^2$

  Gamma : 1 kGy

- **Latency < 8.5 μsec**

  Latency should not be changed

- **Event selection efficiency > 90%**

  To achieve the target S.E.S in 150 days

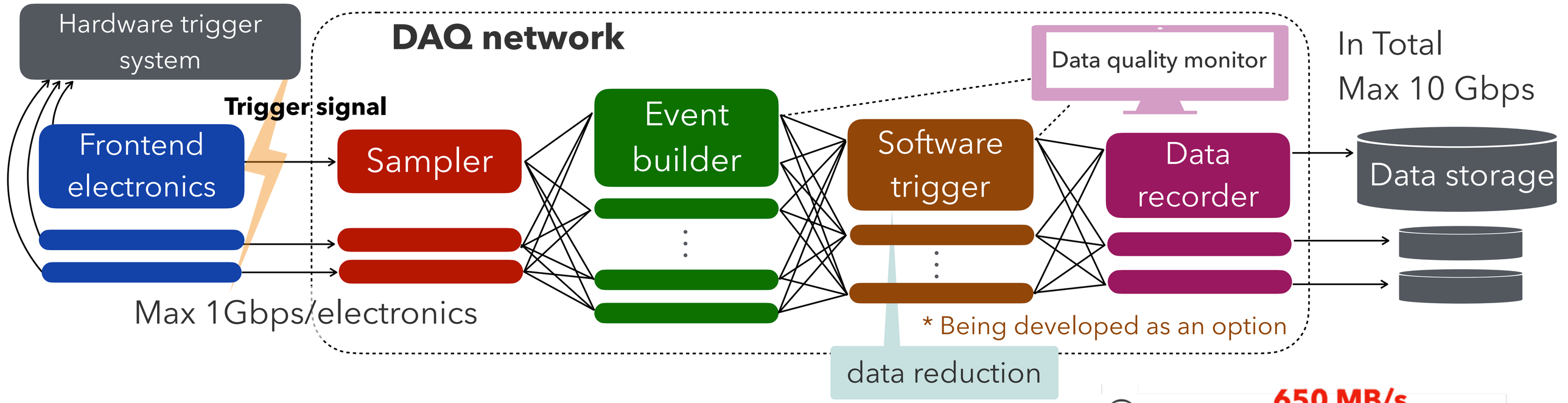
- **High data-rate capability**

  Primary trigger rate of CTH ~ 200 kHz

  → Trigger system reduces some load, but DAQ should still support high rates.

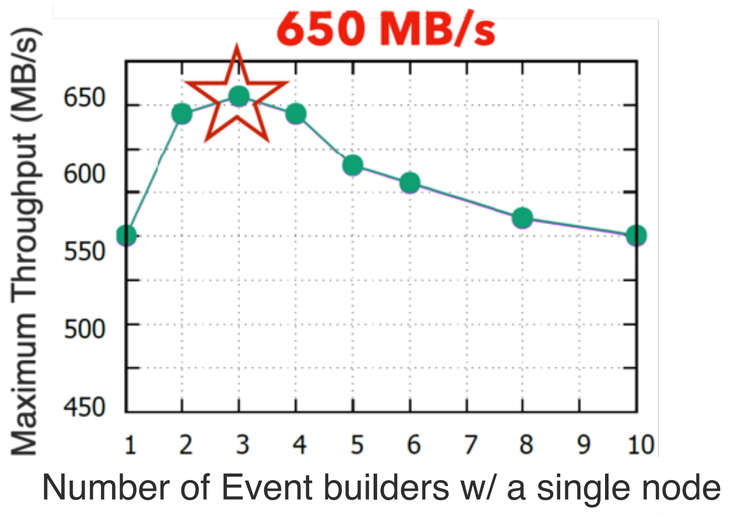
- **Flexible user & developer interface**

Data Acquisition (DAQ) System



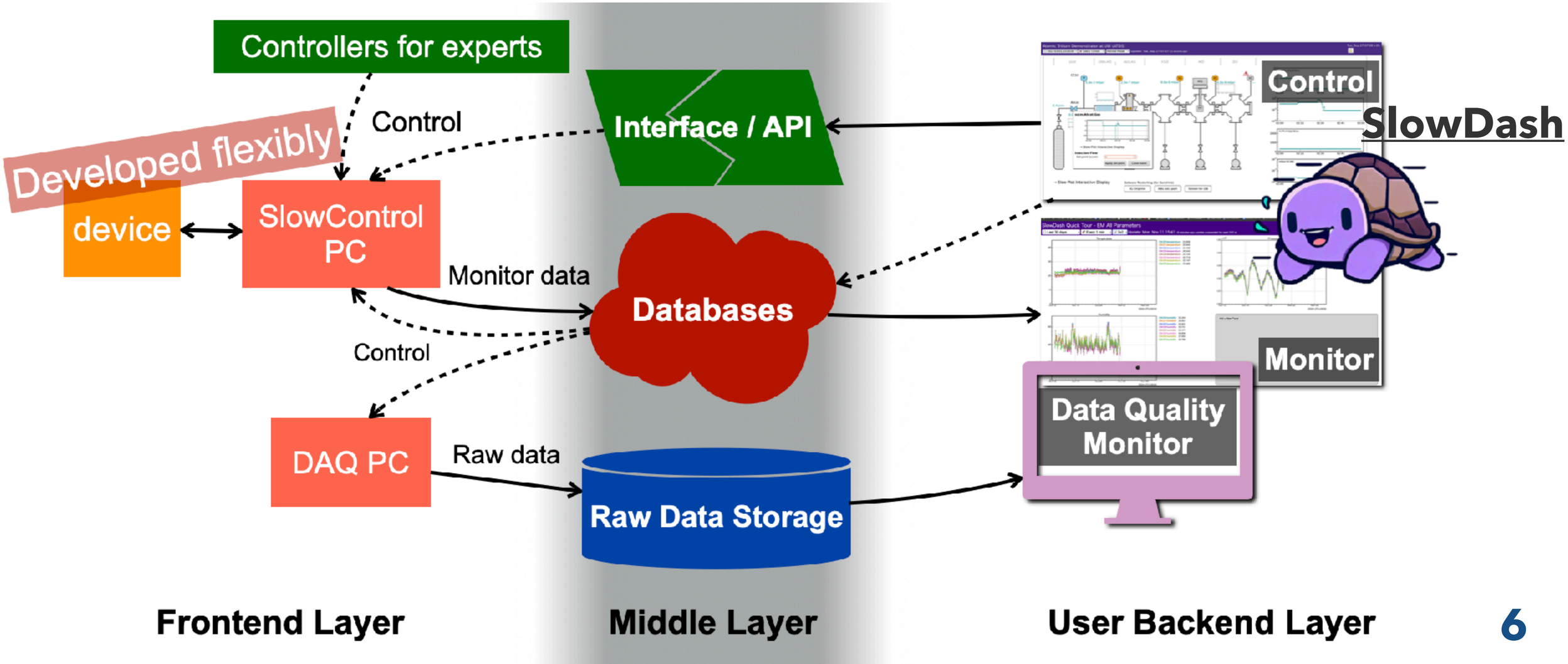
- **Principally fully scalable system**
  - Fully parallel & asynchronous (NestDAQ)
  - Data-recording rate limited by the backend data storage
  - Additional software trigger can ease the requirements for the trigger rate
- **A full CDC DAQ test is performed**
  - With a single node achieved a data-readout rate of 650 MB/s
- **Data Quality Monitor implemented**

T. Takahashi et al., DOI:10.1109/TNS.2023.3262061
Y. Igarashi et al. DOI:10.1109/TNS.2024.3506783



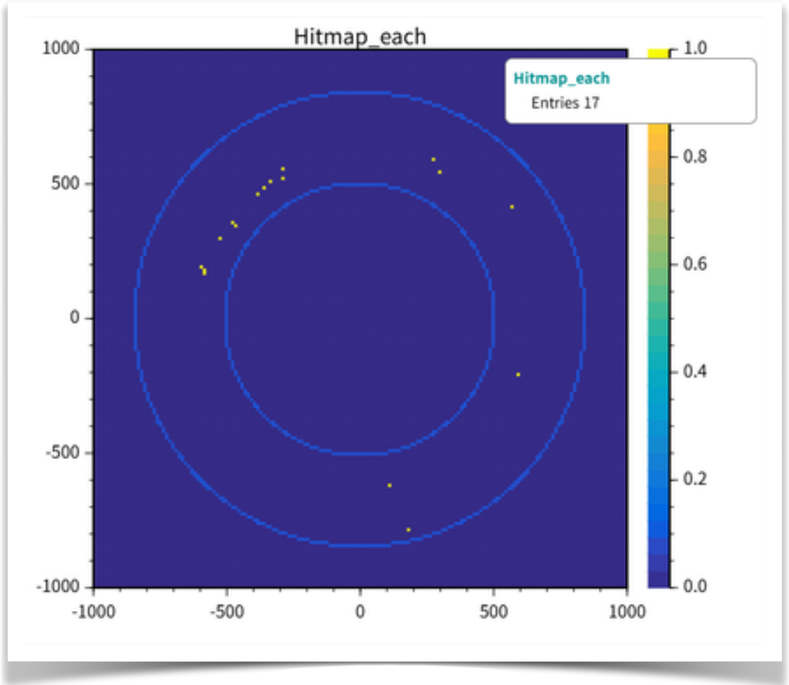
Monitoring System

- The **SlowDash** (developed by S.Enomoto @docs) can handle diverse frontend systems
- **A data quality monitor display has been implemented** →demonstrated with CDC DAQ

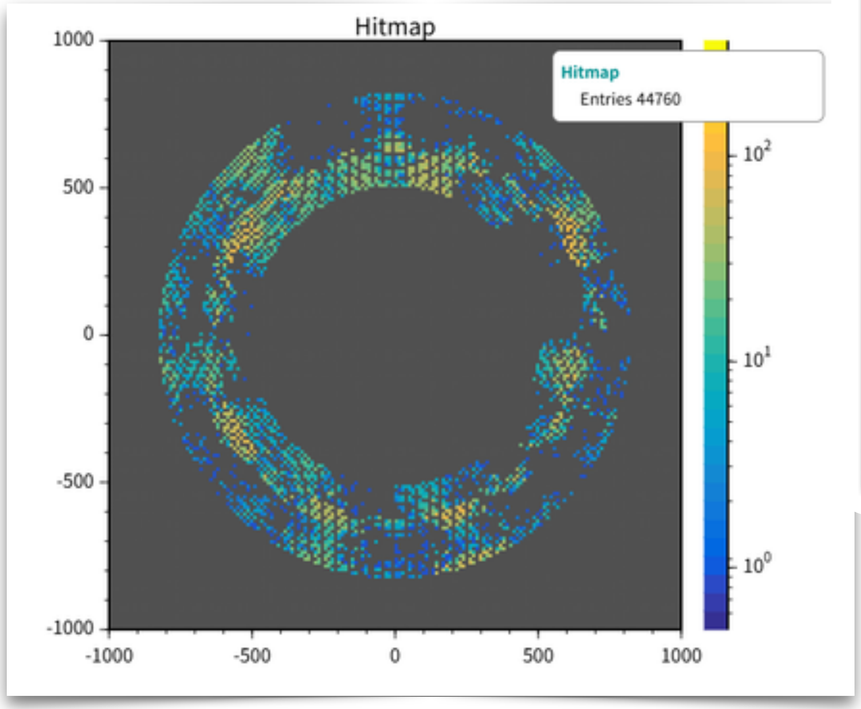


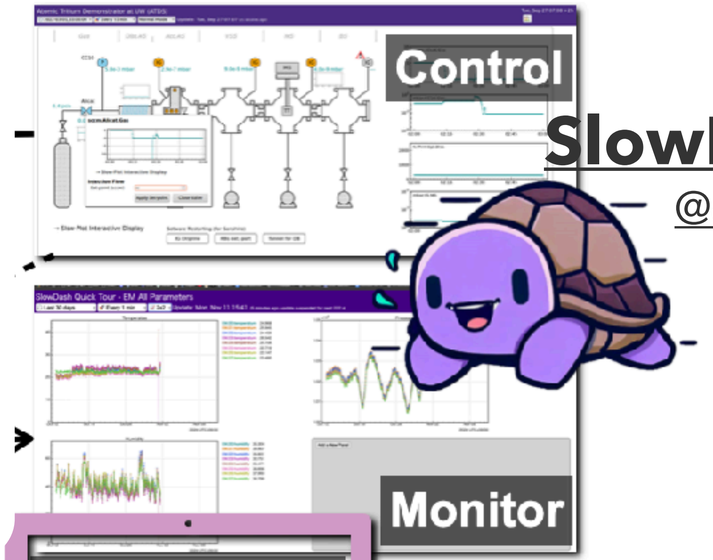
Monitoring System (Display)

CDC hit map (event)



CDC hit map (accumulate)





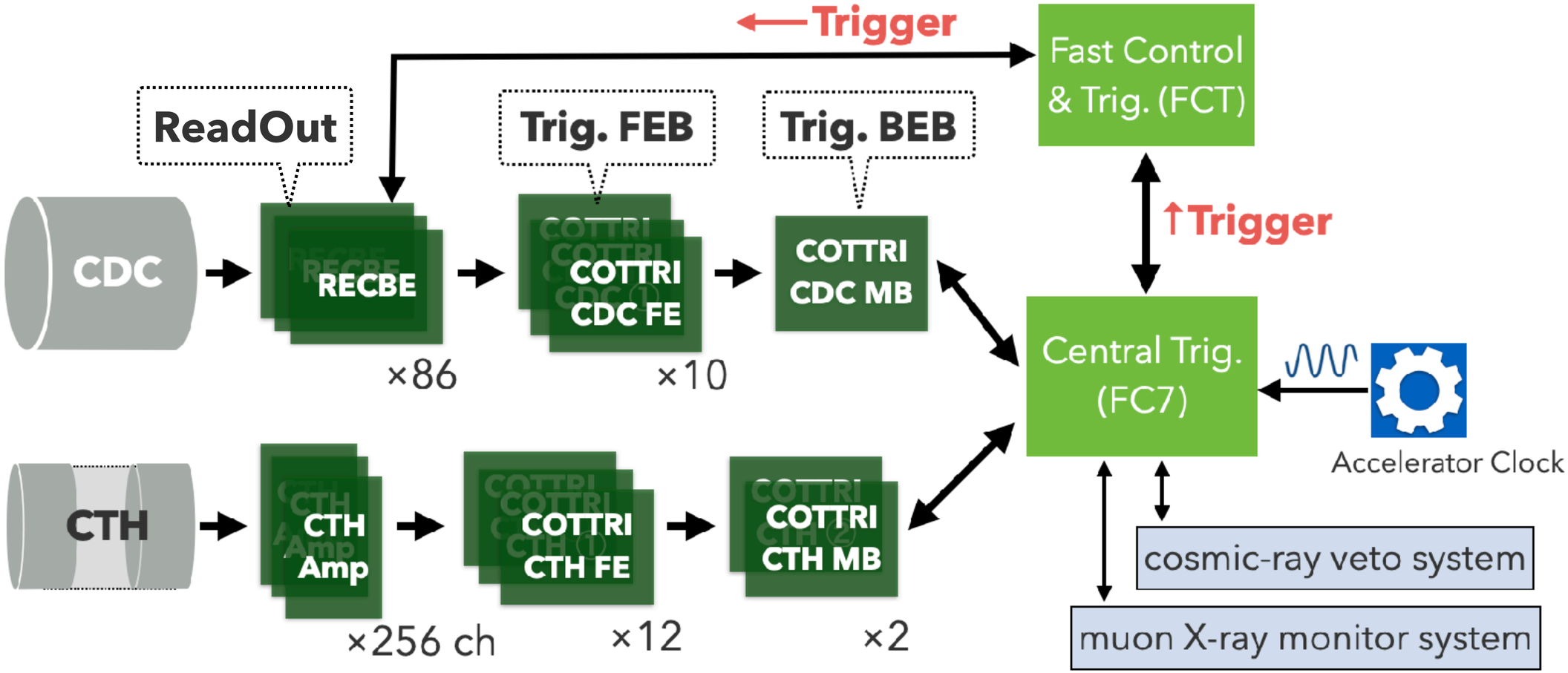
SlowDash

@docs

Frontend Layer **Middle Layer** **User Backend Layer**

Trigger System

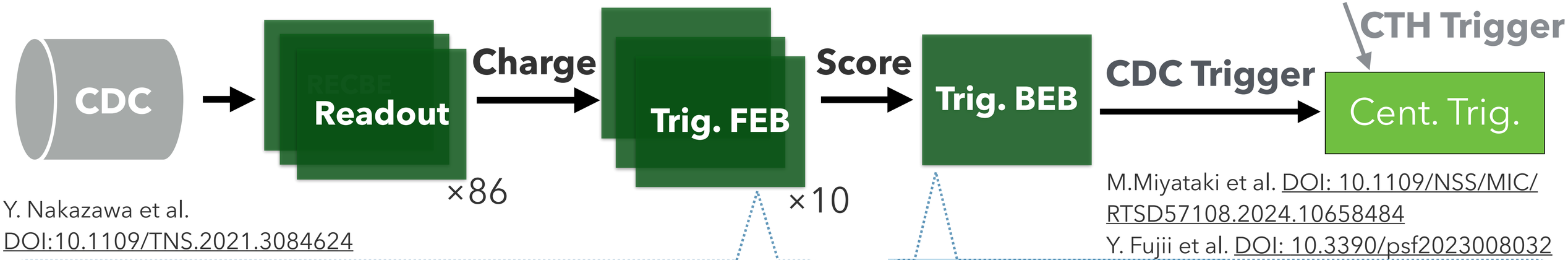
- Multi-stage hardware trigger system (**CO**me**T TRI**gger) with independent CDC/CTH pipelines



Current Status : All CDC trigger hardware has been prepared and connected

This talk : Full hardware integration test of CDC trigger system

CDC Trigger System



Y. Nakazawa et al.
DOI:10.1109/TNS.2021.3084624

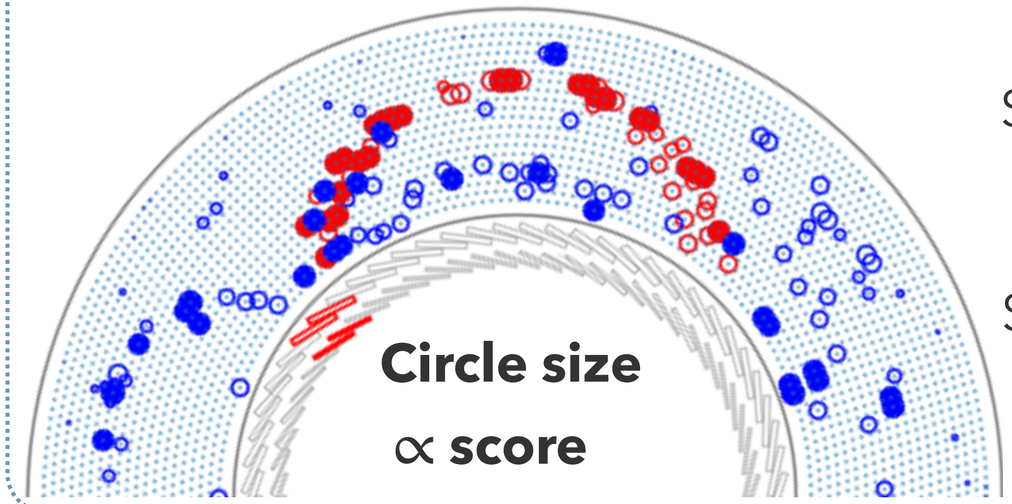
M.Miyataki et al. DOI: 10.1109/NSS/MIC/RTSD57108.2024.10658484

Y. Fujii et al. DOI: 10.3390/psf2023008032

Scoring to each wire by GBDT → Score cut

convert to array

Input : charge on the target wire
charge on the neighboring wires
radial position

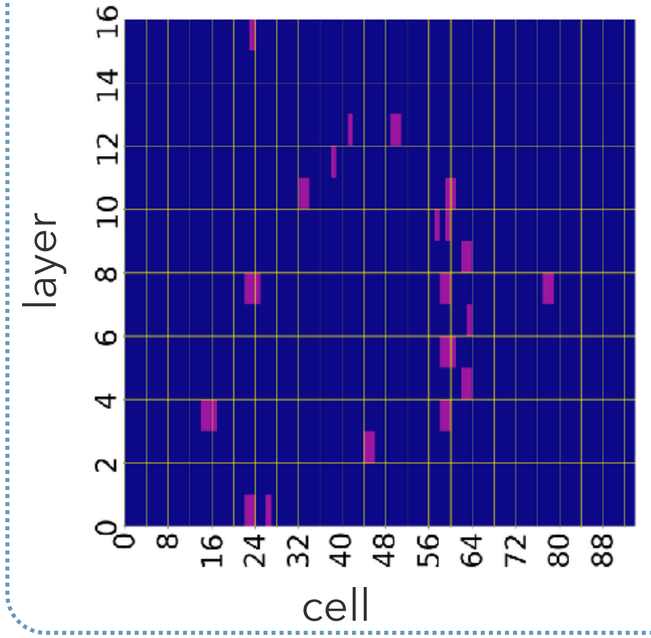


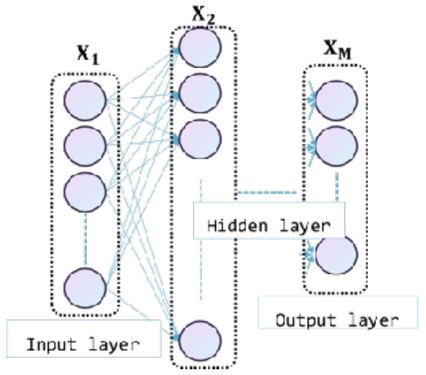
Score ≦ 0.75
Signal
Back ground

Score > 0.75
Signal
Back ground

Classification based on neural network

under development





Communication of CDC Trigger Electronics

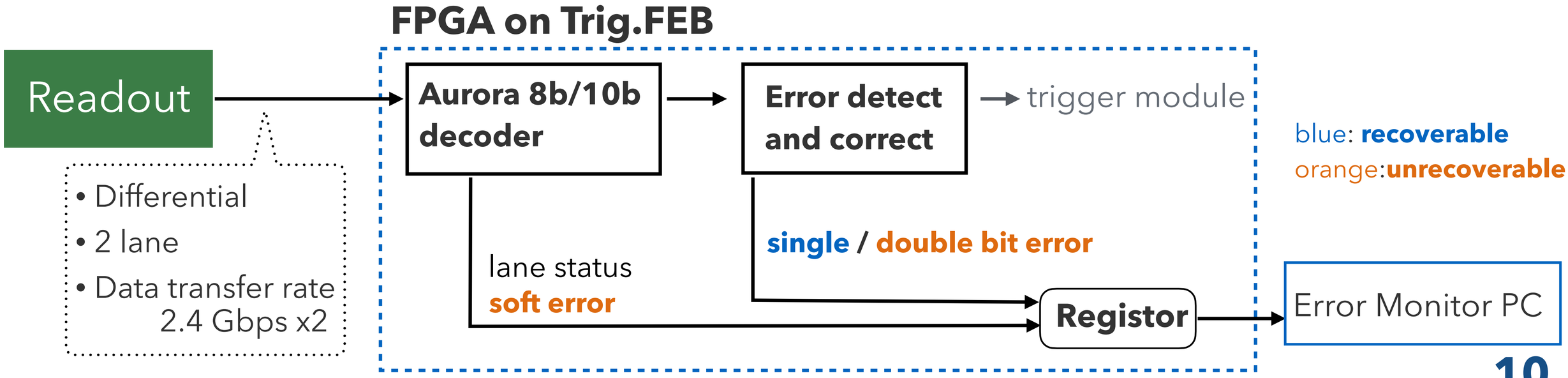
Connection : DisplayPort (DP) cable (capper)

- Length : Readout - Trig. FEB = 5 m (to keep away from high-radiation area)

Communication Protocol : Aurora 8b/10b by AMD

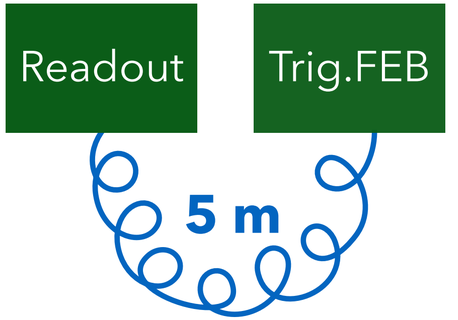
scalable, lightweight, link-layer protocol for high-speed serial communication

Module in FPGA detects communication errors
→ Evaluate communication stability



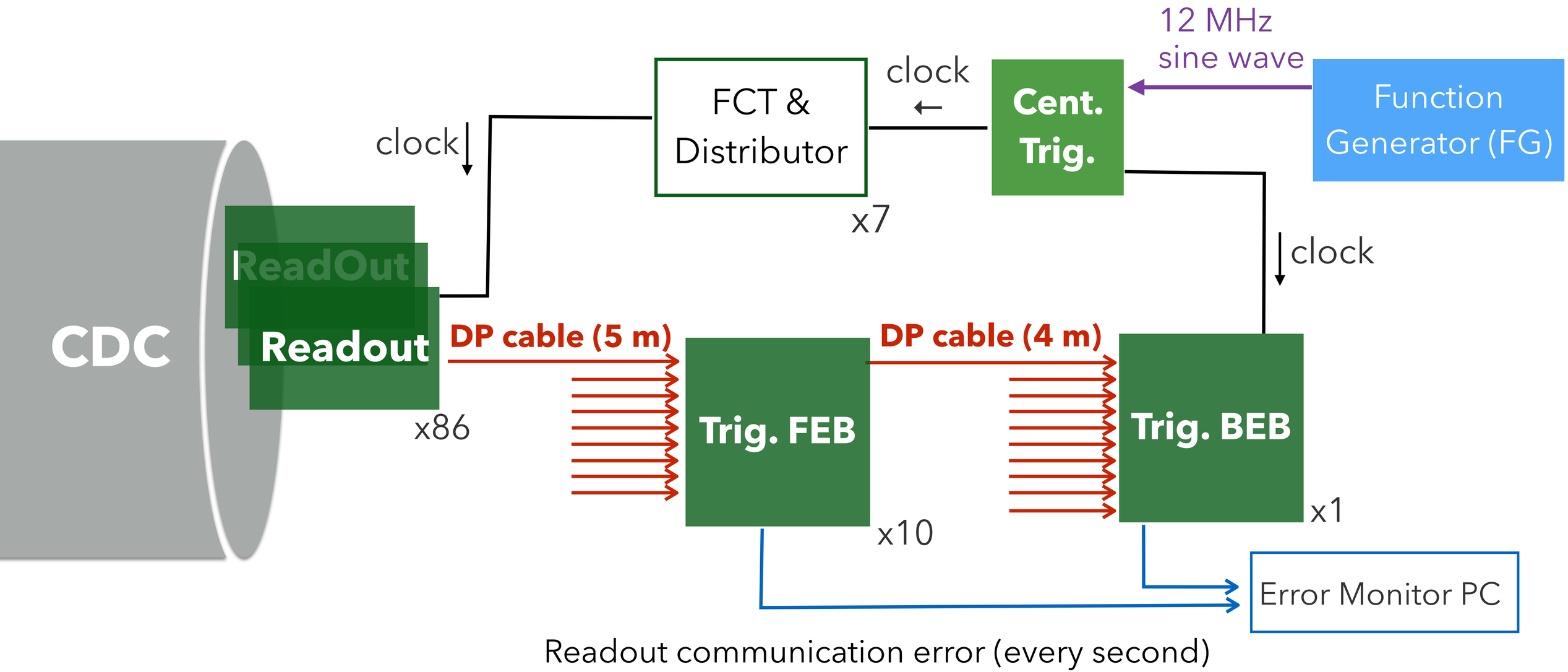
Hardware Performance Test Motivation

- **Communication Stability**
  - Verify stable communication with 5 m DP cables (Readout-Trig.FEB)
  - If lost → reset communication / firmware reprogram
    - Dead time
      - Assuming 3-min dead time/unrecoverable error (for firmware reprogramming)
    - Requirement : **Error rate <** 5.6×10^{-5} **error/sec/system** for <1% dead time



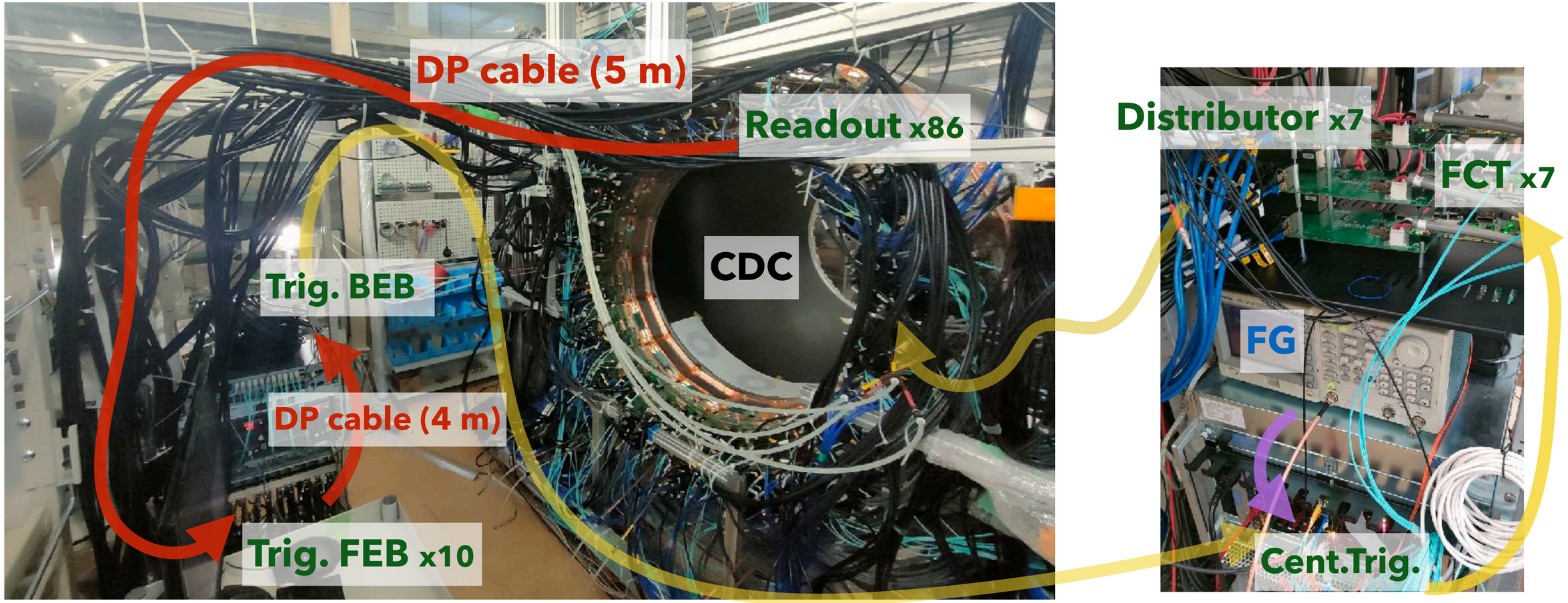
- **Latency Measurement**
  - Determine if CDC trigger alone meets **less 8.5 μsec latency** requirement
    - CTH trigger less critical due to fast response

Communication Stability Test Setup



Readout communication error (every second)

Communication Stability Test Result @ J-PARC

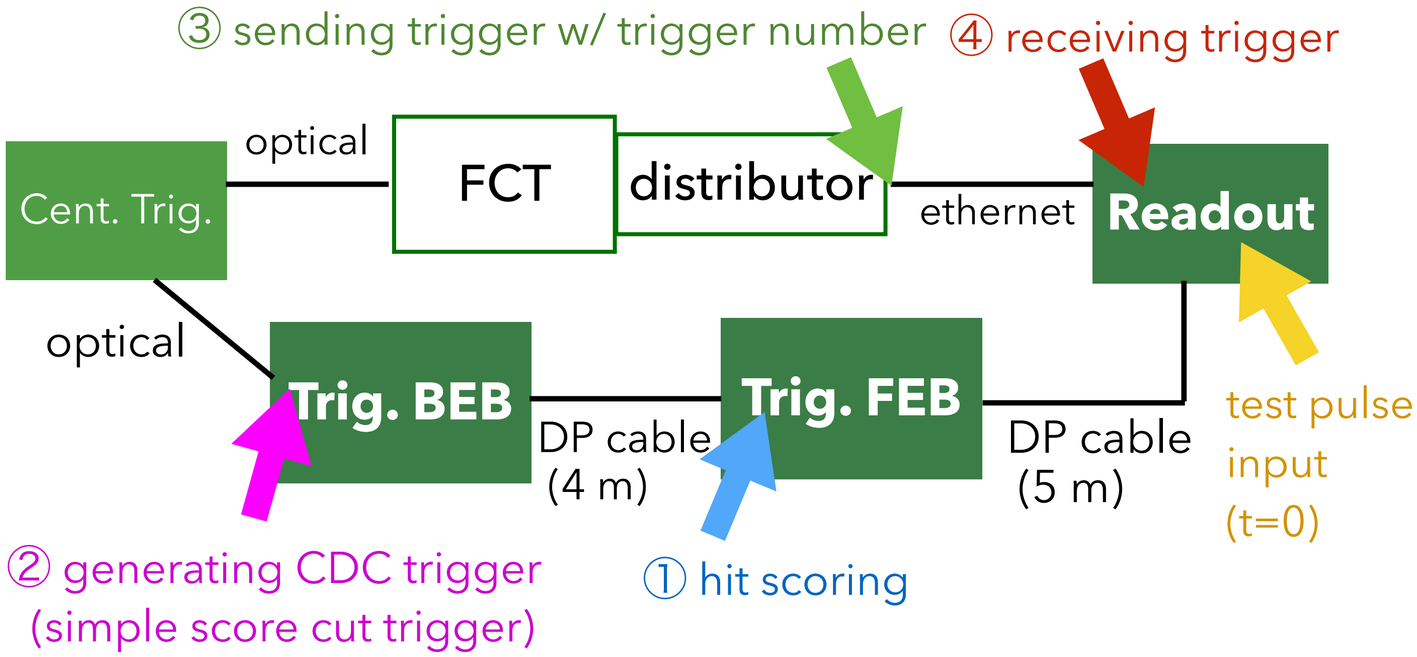


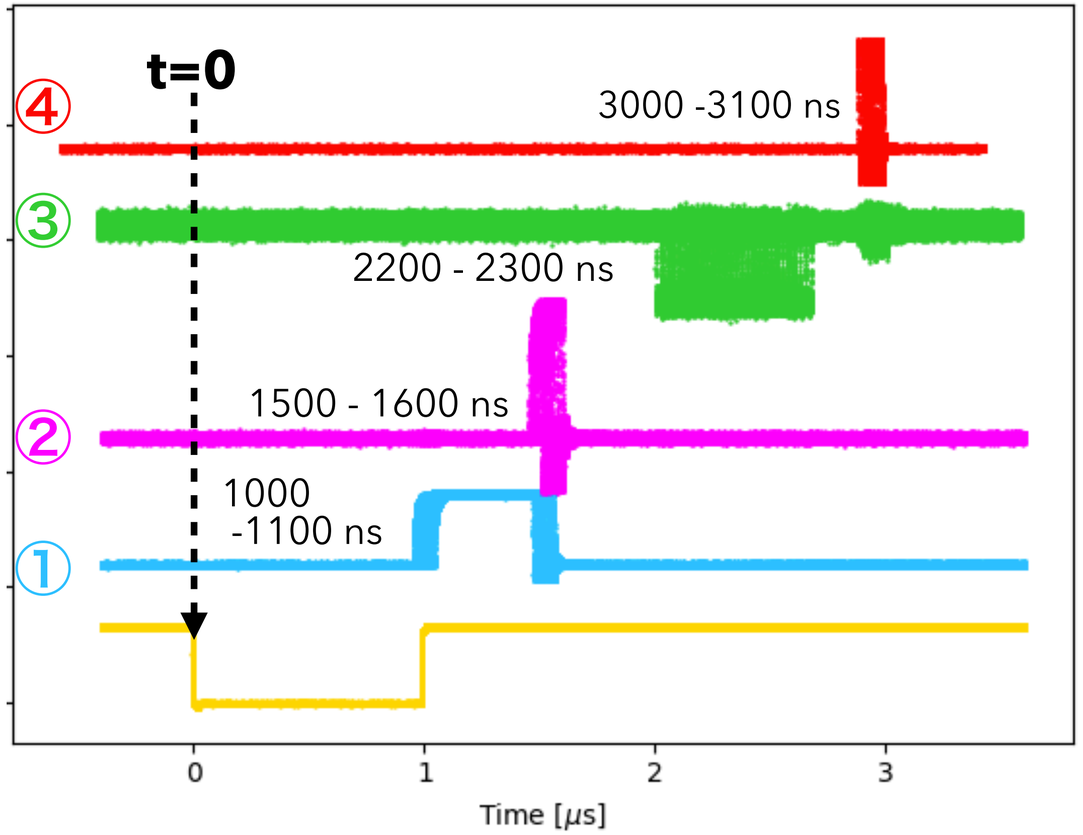
Connected all cables linking CDC trigger system boards

Measurement for 66,880 seconds (~18 hours) → **NO communication errors**

Error rate $< 4.6 \times 10^{-5}$ error/sec/system **(95% C.L.)**

Latency Measurement Setup & Result





	latency [nsec]
measurement latency	3000-3100
drift time	400
Total	**3400-3500**

Satisfy requirement << 8.5 μsec

Summary & Future Plan

- **COMET Phase-I searches $\mu - e$ conversion**
  - Target single event sensitivity : 3×10^{-15} (a factor of 100 improvement of upper limit)
- **Main Detector CyDet**
  - CDC (momentum measurement) & CTH (primary trigger)
- **Online System**
  - DAQ System : parallel and asynchronous data processing (NestDAQ) →High data-rate capability
  - Monitoring System : Web-based modern interface (SlowDash) → developer- & user-friendly
  - Trigger System : Multi-stage hardware system → fast & efficient event selection
- **CDC Trigger System Hardware performance**
  - Communication stability : verified all boards communicated properly with less than 1% dead time
  - Trigger Latency : confirmed within 8.5 μsec of required value
- **Future plan**
  - Implement fixed latency on transceiver
  - Implement NN algorithm on COTTRI CDC MB
  - Integrate with CTH trigger system

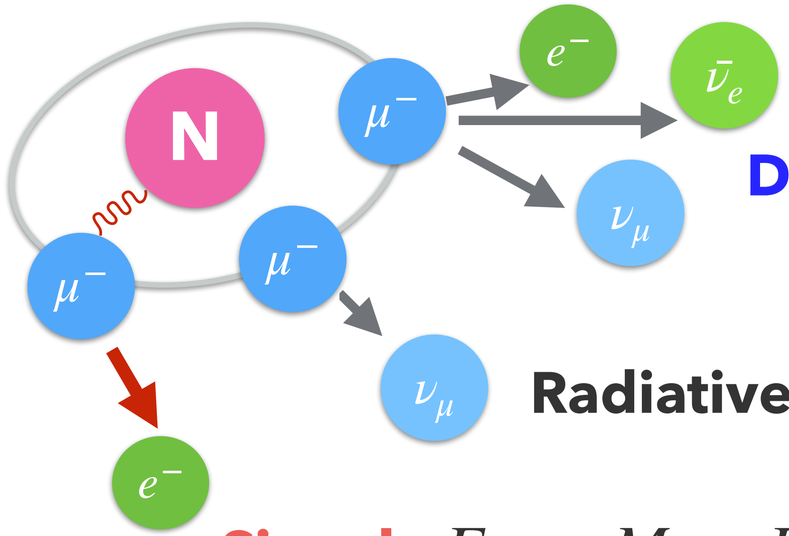
Other COMET presentation :

09/07 17:30 Muon beam monitor by O. Kenya (Poster T11)
10/07 10:00 COMET Overview by C. Cristina (Parallel T09)
11/07 10:00 Straw-Tube Tracker by H. Masaaki (Parallel T11)

backup

COMET (COherent Muon to Electron Transition)

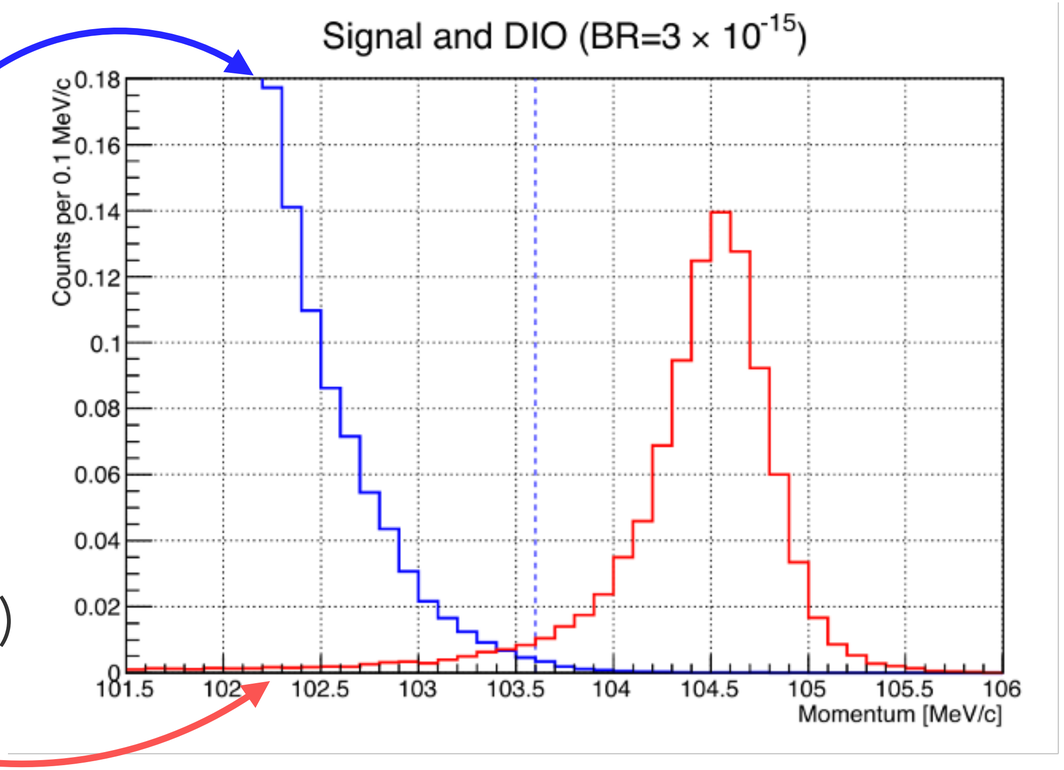
muonic atom



Decay In Orbit (DIO)

Radiative Muon Capture

Signal : $E_{\mu e} \simeq M_\mu - E_B \simeq 105$ MeV (N=Al)



other background

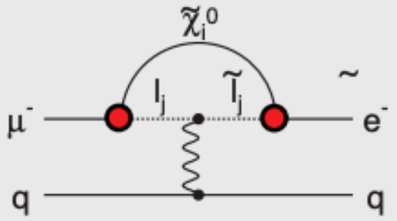
- Cosmic-ray induced background
- Beam related background
  - radiative pion capture

cLFV in BSM

Possible Contributions to CLFV

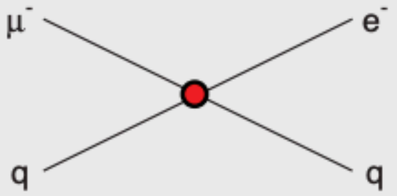
Supersymmetry

rate ~ 10^{-15}



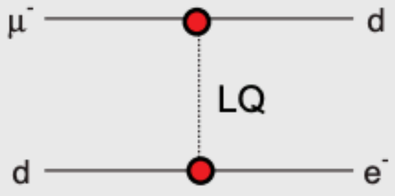
Compositeness

Λ_c ~ 3000 TeV



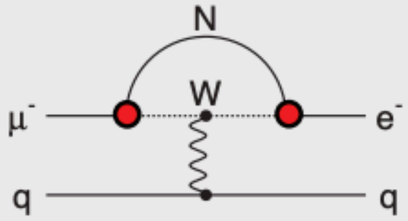
Leptoquark

M_{LQ} = 3000 $(\lambda_{\mu d}\lambda_{ed})^{1/2}$ TeV/c^2



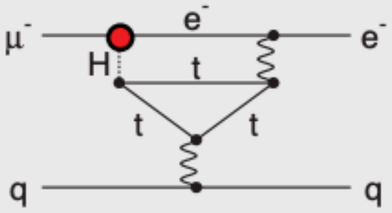
Heavy Neutrinos

$|U_{\mu N}U_{eN}|^2$ ~ 8×10^{-13}



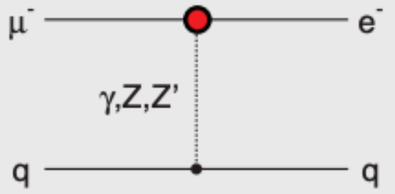
Second Higgs Doublet

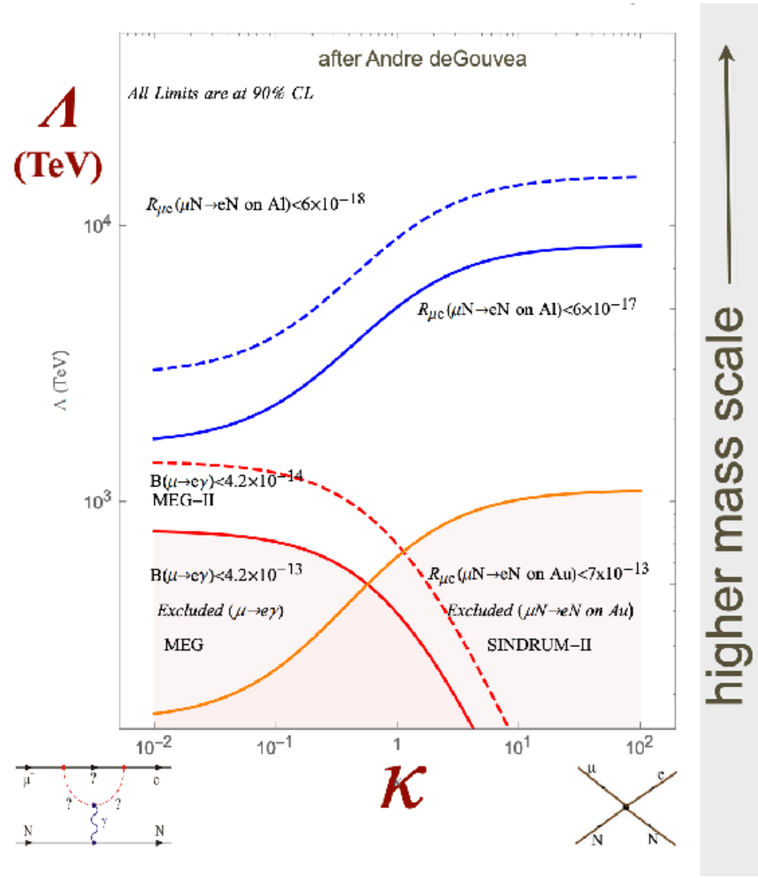
$g(H_{\mu e})$ ~ $10^{-4} g(H_{\mu\mu})$



Heavy Z' Anomal. Z Coupling

$M_{Z'}$ = 3000 TeV/c^2

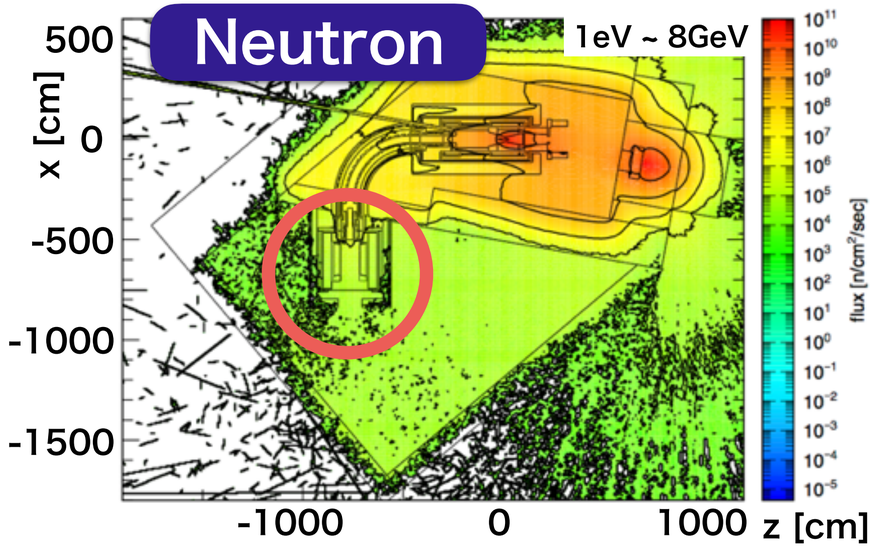


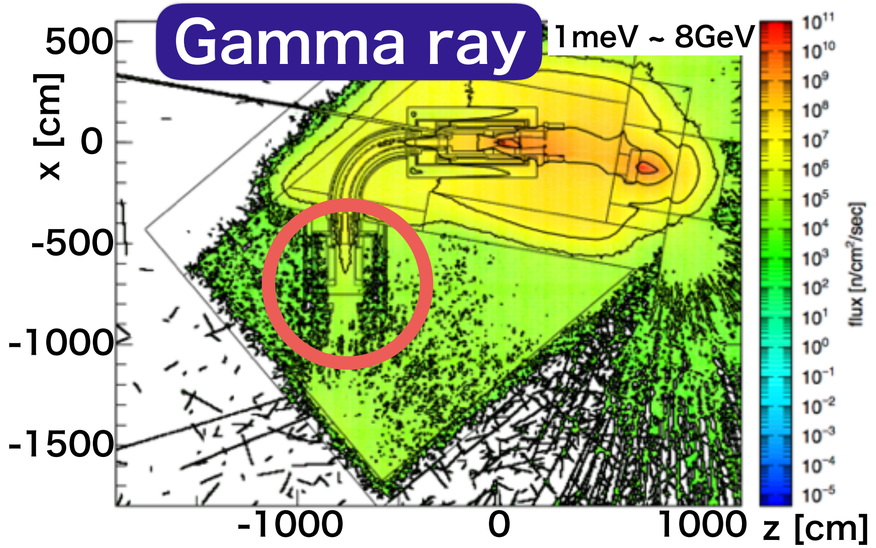


https://indico.cern.ch/event/452998/contributions/2184888/attachments/1306687/1958605/PASCOScLFV_Bernstein.pdf

estimated radiation dose and layout

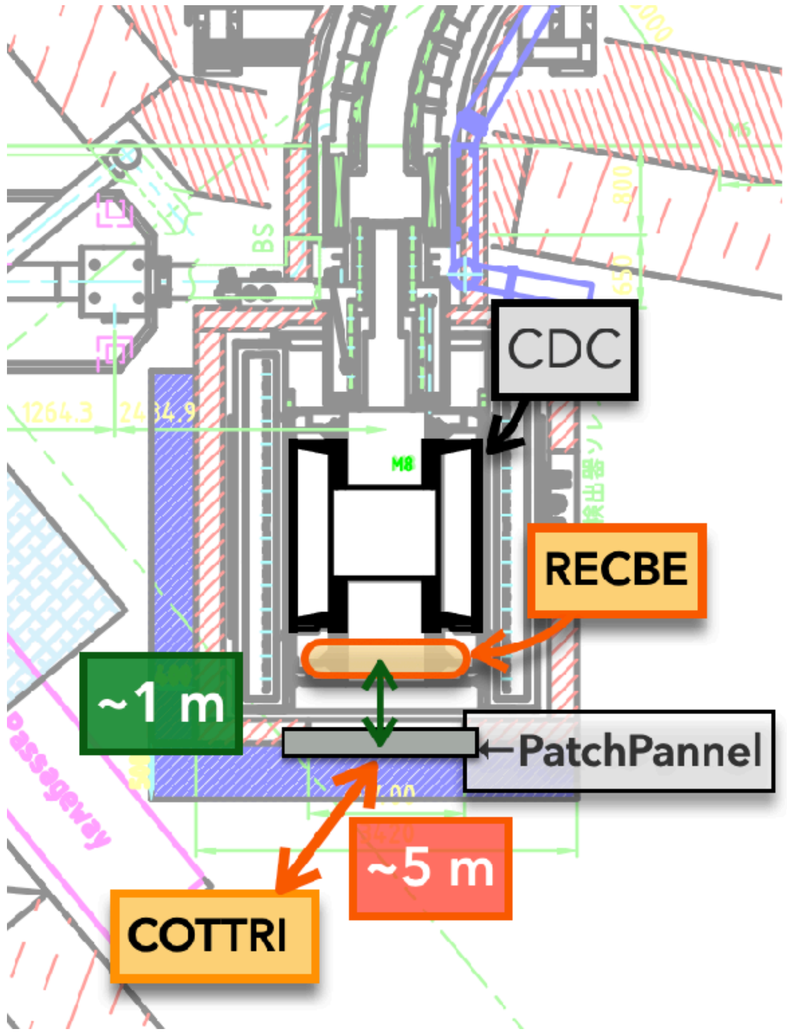
- radiation damage Neutron : 10^{12} $n_{1-MeVeq}/cm^2$ Gamma : 1 kGy



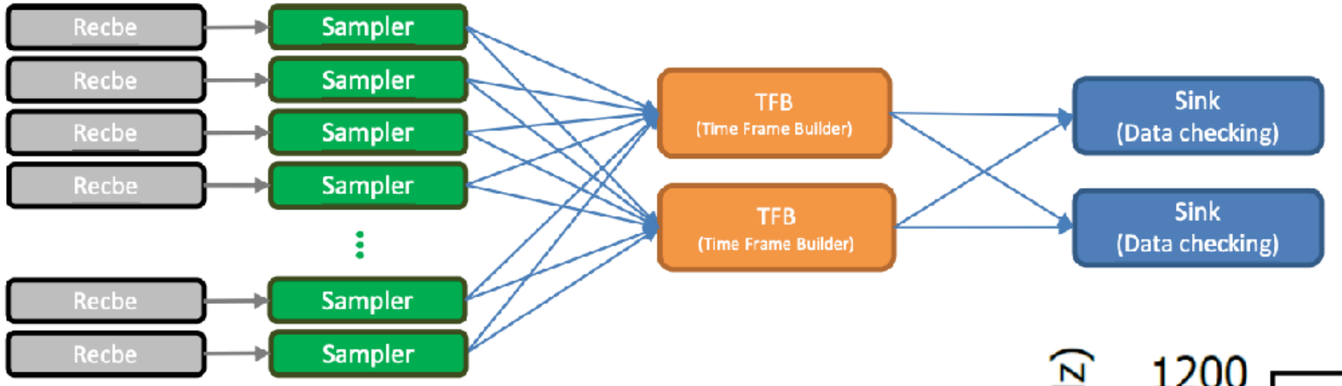


detector region

- layout



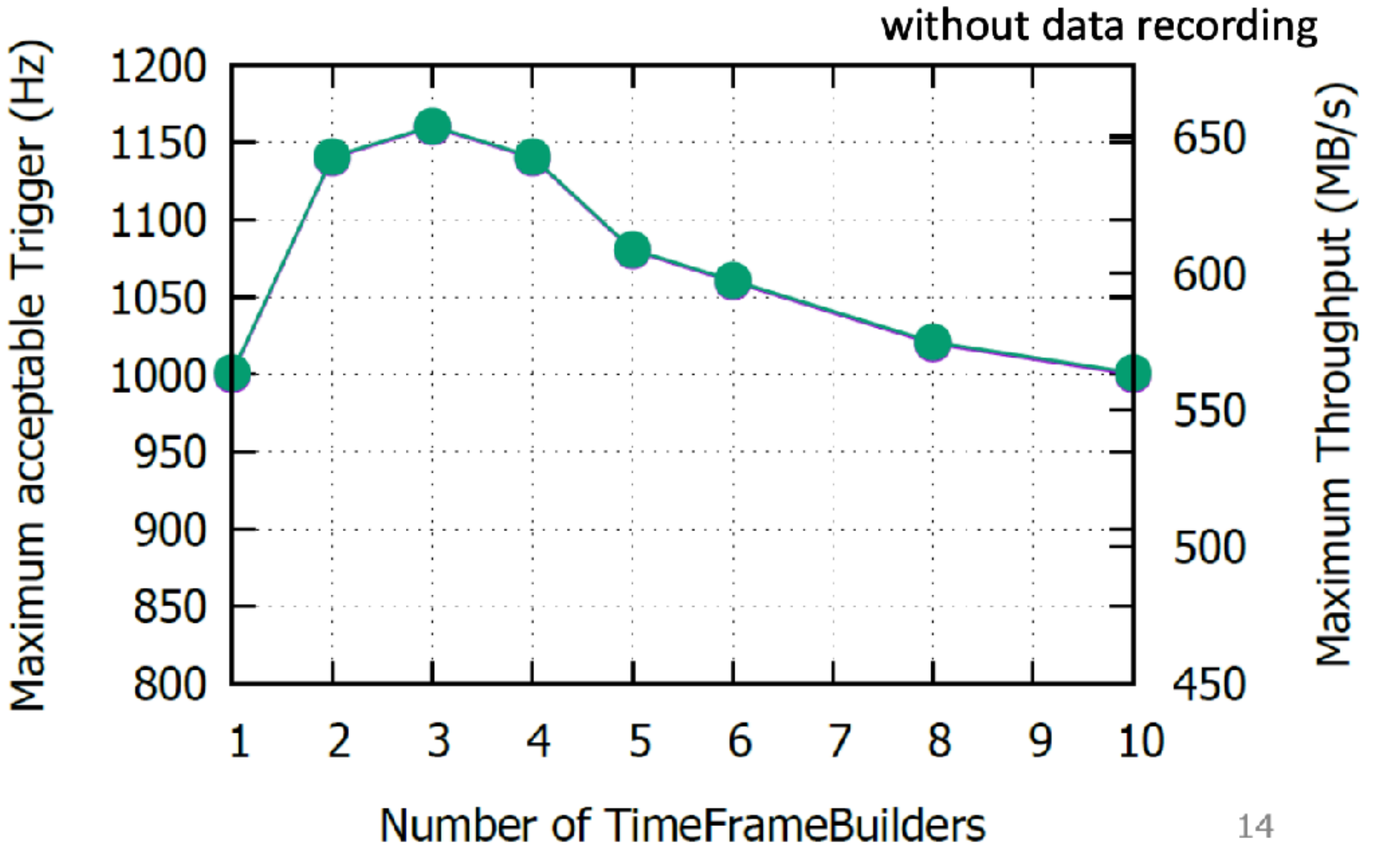
Data flow throughput



The time frame builder works as an event builder using the sampler which reads data from Recbe event by event.

UDS (Unix Domain Socket) was used for internal process communication.

- One DAQ server PC
- Event size: 6156B
- Number of Recbes: 96
- DAQ PC
  - Xeon E-2236 @ 3.40GHz 6 Cores
  - Memory 32 GB
  - NIC: Broadcom NetXtreme II BCM57810
- 1G/10G network switch
  - FS.com S3900 24F4S



Trigger data format

RECBE -> FE

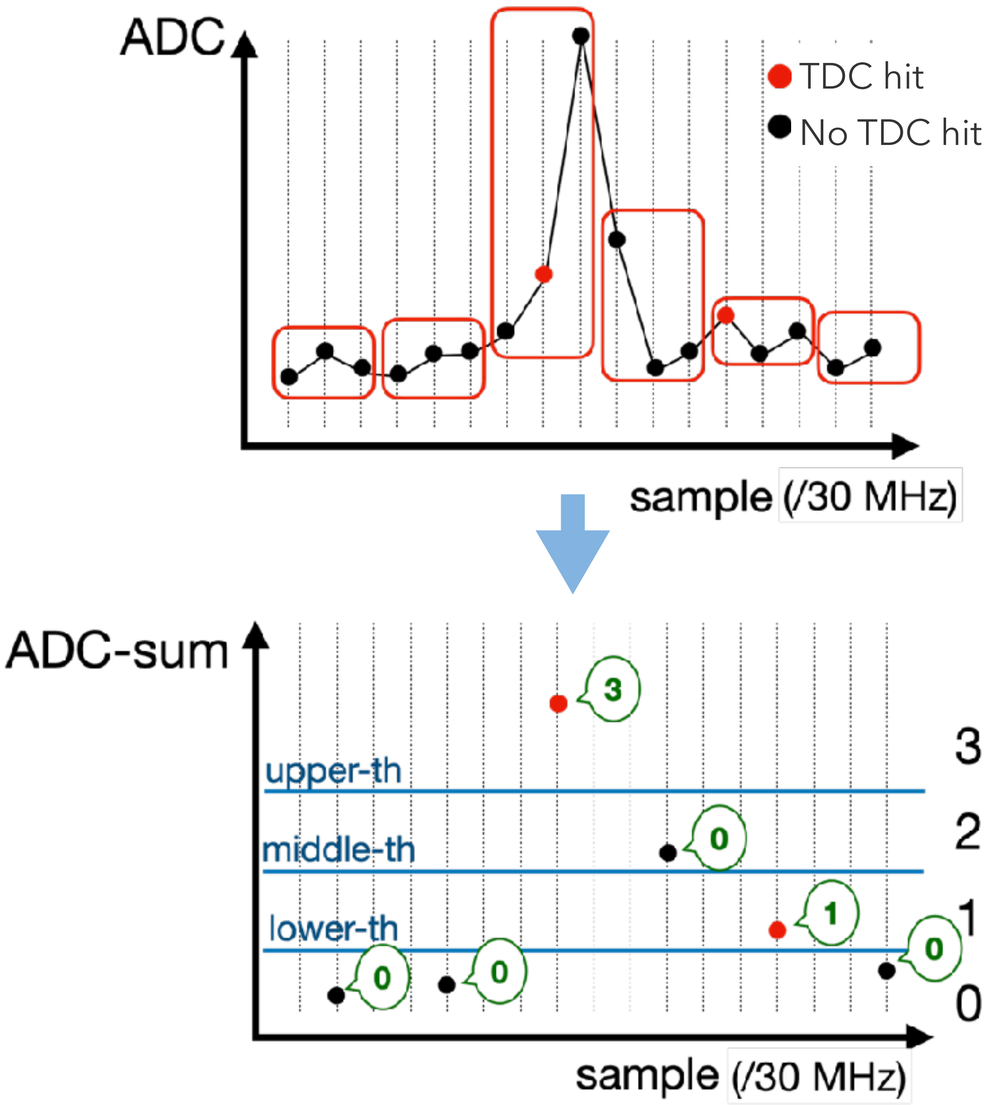
1 frame (10 MHz)
：data transfer rate 1.6 Gbps　(maximum data transfer rate 3.28 Gbps)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	0	Parity bits						1	Sent number																Board ID							
2-bit data	0	Parity bits						0	ch11	←																					0	
	0	Parity bits						0	ch23	←																					12	
	0	Parity bits						0	ch35	←																					24	
	0	Parity bits						0	ch47	←																					36	

FE -> MB

1frame (10 MHz).
：data transfer rate 1.9 Gbps (maximum data transfer rate 3.84 Gbps)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	0	Parity bits						1	Board ID								Sent number															
Integrated score	0	Parity bits						0	RECBE 9								RECBE 8															
	0	Parity bits						0	RECBE 7								RECBE 6															
	0	Parity bits						0	RECBE 5								RECBE 4															
	0	Parity bits						0	RECBE 3								RECBE 2															
	0	Parity bits						0	RECBE 1								RECBE 0															



Event features

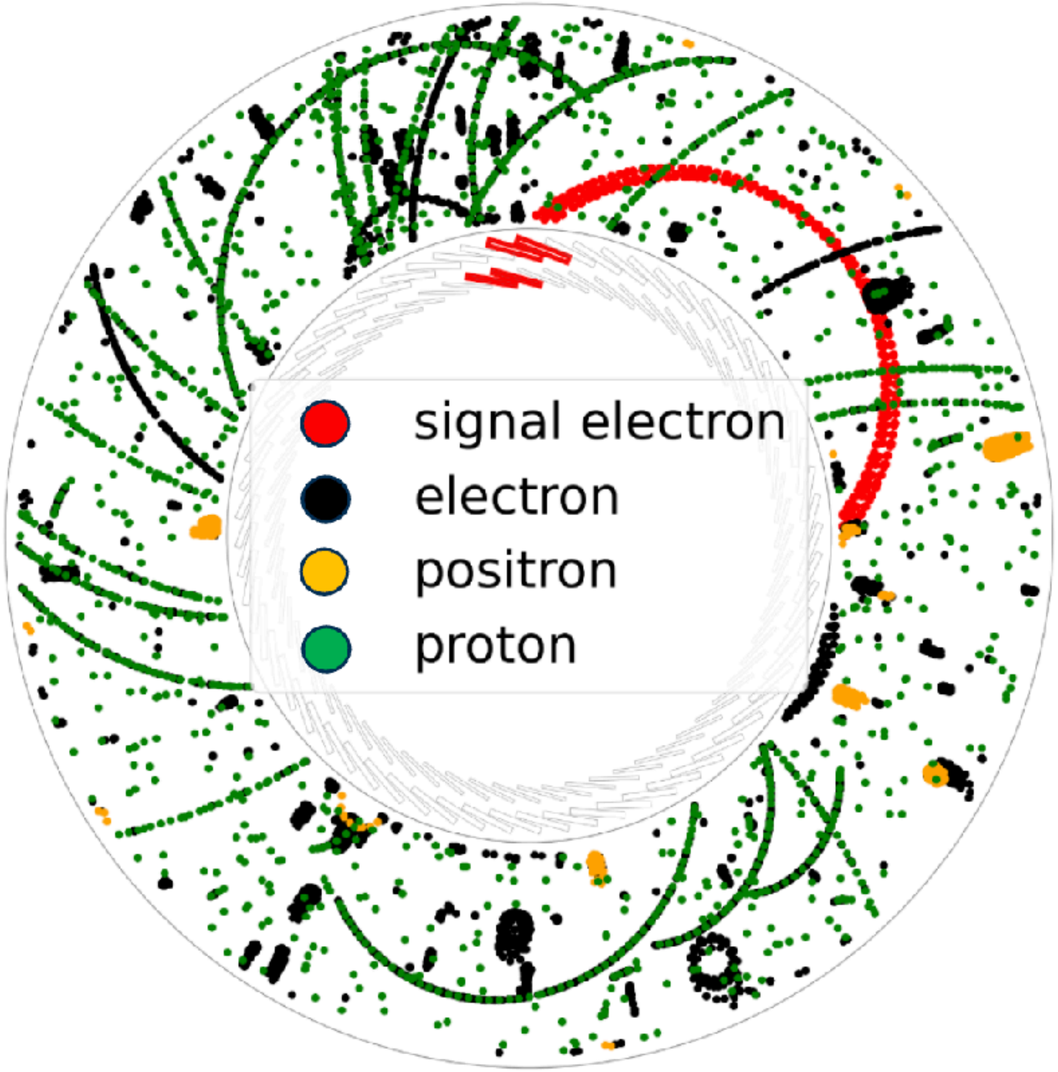
Signal characteristics

- **Helical tracks with a signal-like curvature**
- MIP-level hit in a cell

Background characteristics

- Low energy electrons
  - Long lived in a small region
- Protons
  - Large curvature
  - Large energy deposit

Simulated event display in cross–section view in CyDet
Each dot represents MC hits.



NN algorithm

M.Miyataki et al. DOI: 10.1109/NSS/MIC/RTSD57108.2024.10658484

Training and optimization

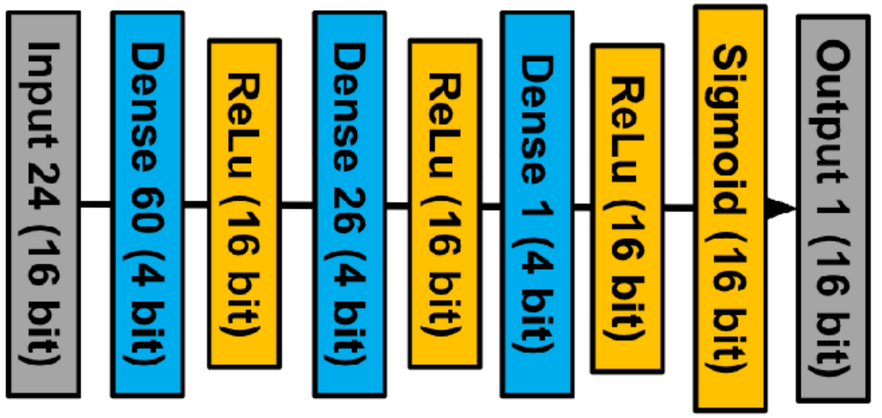
[5] https://doi.org/10.48550/arXiv.2006.10159
[6] https://doi.org/10.1145/3292500.3330701

- Quantized MLP (QMLP) was constructed by using QKeras[5].
  - Quantization (calculation precision reduction) is essential.
    - For our target FPGA, AMD Xilinx Kintex7 xc7k355t-ffg901-1

- Parameters were optimized by using Optuna[6].
  - Hit mapping
    - Score threshold
    - Compression ratio
  - QMLP structures
    - Number of layers
    - Number of neurons
    - Precision

The best QMLP model structure

(GBDT score threshold = 0.75)



Number of parameters 3,113

Dense = Fully connected layer

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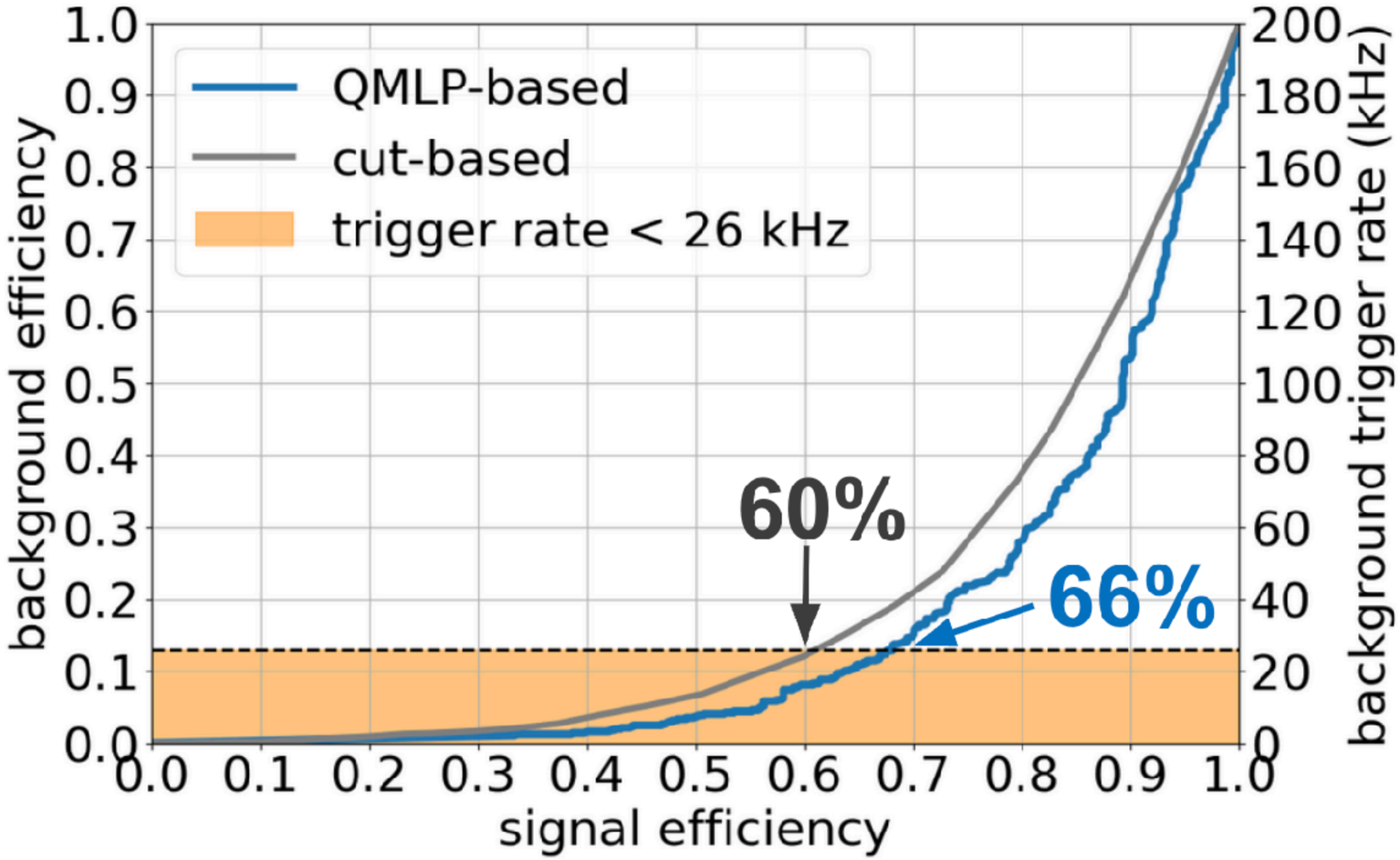
Result

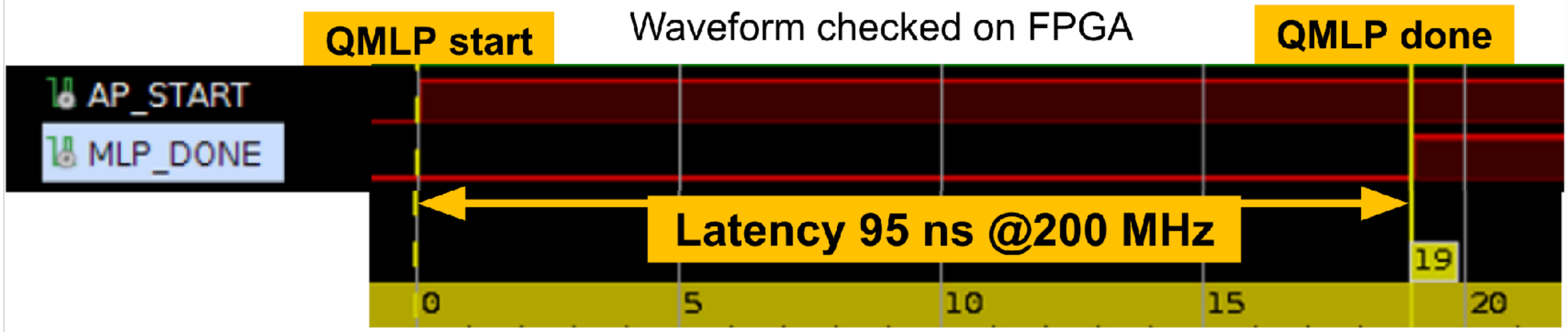


- The signal efficiency is **66% at a trigger rate of 26 kHz**, assuming a CTH trigger rate of 200 kHz.
- **10% better** performance is achieved than the cut-based method.

Latency of neural network logic

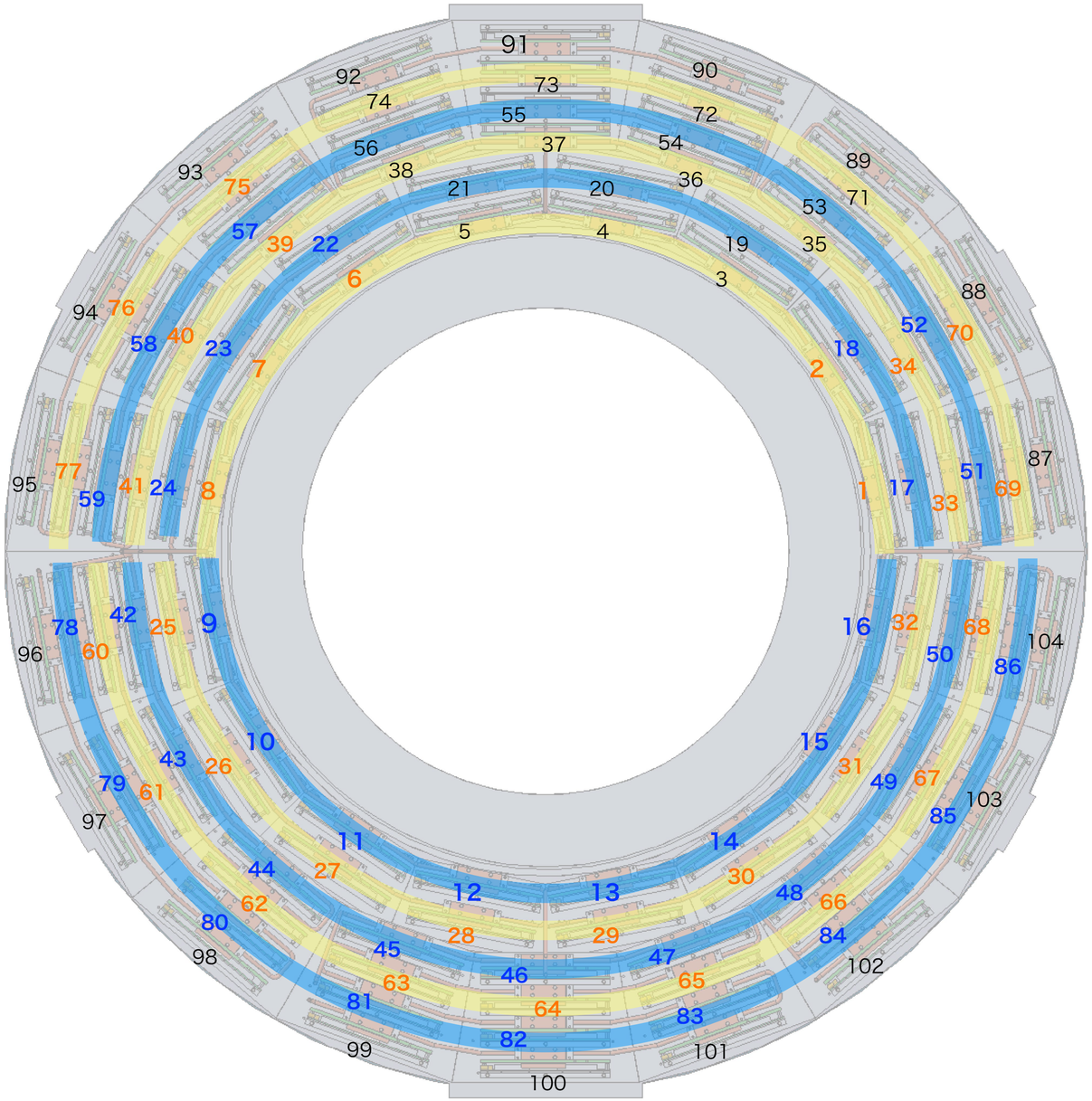
FPGA implementation

The optimized QMLP was converted into FPGA firmware using hls4ml [4].
The firmware worked in the trigger MB.
The latency was measured with the logic analyzer.



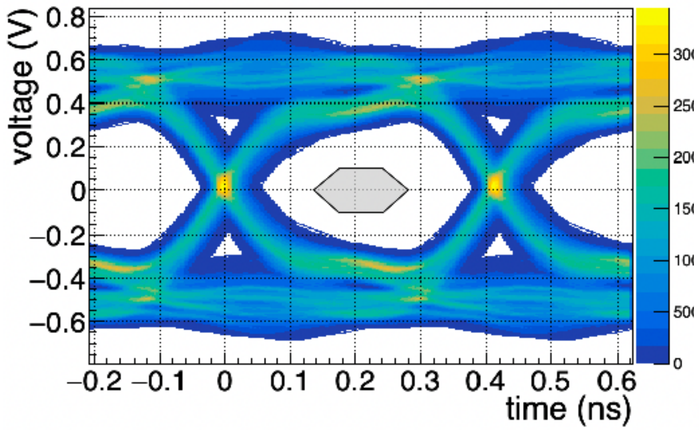
The expected total latency is 3.4 μs.
This satisfies the requirement !!

RECBE position

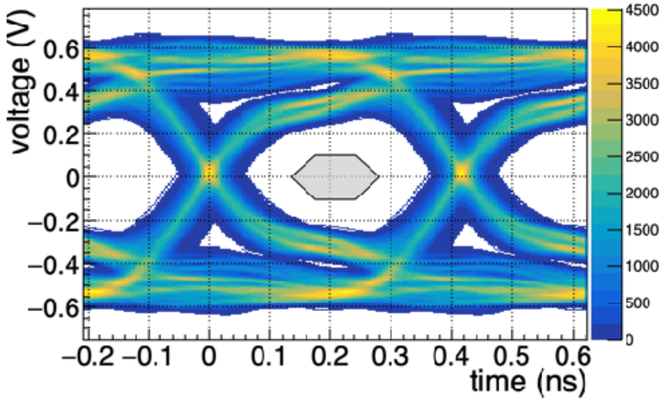


cable selection

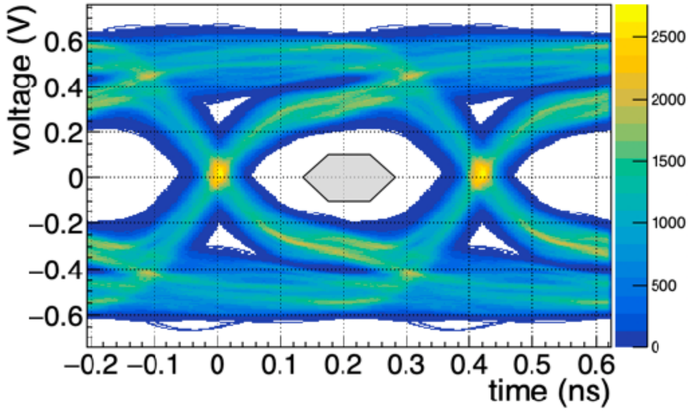
4 m (ver1.4)



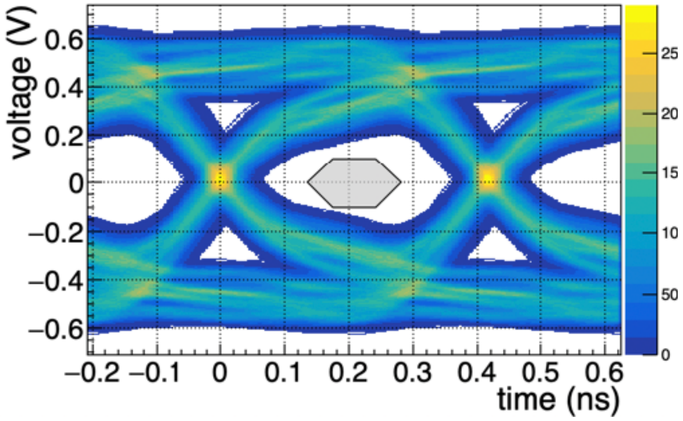
5 m (ver1.4)



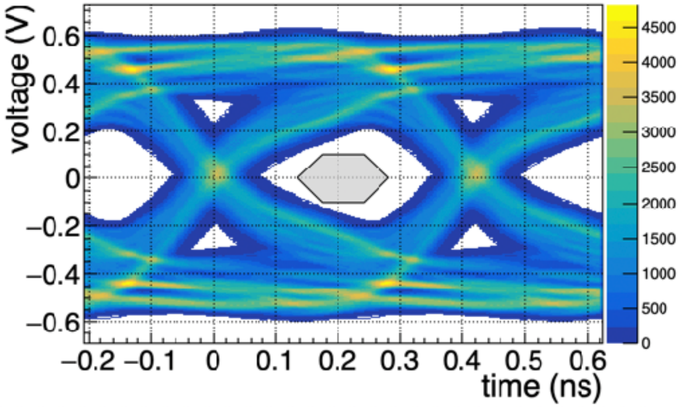
5 m (ver1.2)



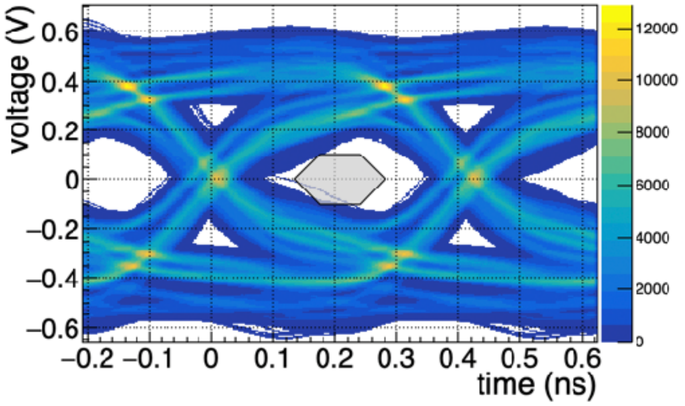
4 (ver1.4) + 0.9 m



5 (ver1.4) + 0.9 m



5 (ver1.2) + 0.9 m



ECC Error Correction Code

- Hamming Code

  6 bits of parity are added to 25 bits of data, and the erroneous bit is identified based on the combination.

  $2^m \geq m + k + 1$ m : # of parity bits k : # of data bits n : code length $n = m + k$

ex.) when D17 flip

… CB1 (01000b), CB2(10000b), CB5(00100)が 1

-> XOR

11100 = D17

↓the address for bit

11	10	01	00	
	D24	D23	D22	111
D21	D20	D19	D18	110
D17	D16	D15	D14	101
D13	D12	D11	CB5	100
D10	D9	D8	D7	011
D6	D5	D4	CB4	010
D3	D2	D1	CB3	001
D0	CB2	CB1	No error	000

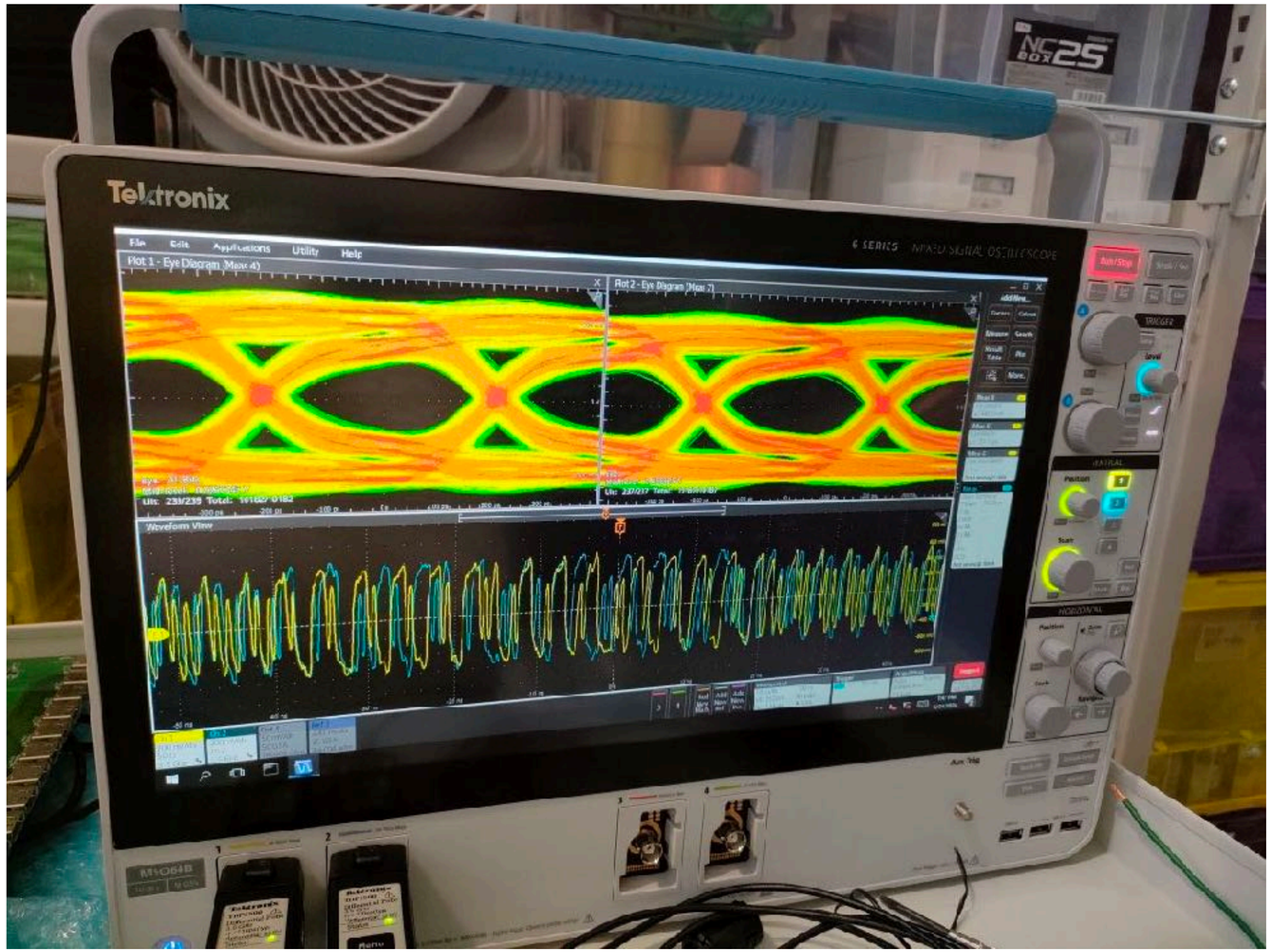
corresponding to data bits and parity bits

Bits	CB1	CB2	CB3	CB4	CB5	CB6
0	✓	✓				✓
1	✓		✓			✓
2		✓	✓			✓
3	✓	✓	✓			✓
4	✓			✓		✓
5		✓		✓		✓
6	✓	✓		✓		✓
7			✓	✓		✓
8	✓		✓	✓		✓
9		✓	✓	✓		✓
10	✓	✓	✓	✓		✓
11	✓				✓	✓

Bits	CB1	CB2	CB3	CB4	CB5	CB6
12		✓			✓	✓
13	✓	✓			✓	✓
14			✓		✓	✓
15	✓		✓		✓	✓
16		✓	✓		✓	✓
17	✓	✓	✓		✓	✓
18				✓	✓	✓
19	✓			✓	✓	✓
20		✓		✓	✓	✓
21	✓	✓		✓	✓	✓
22			✓	✓	✓	✓
23	✓		✓	✓	✓	✓
24		✓	✓	✓	✓	✓

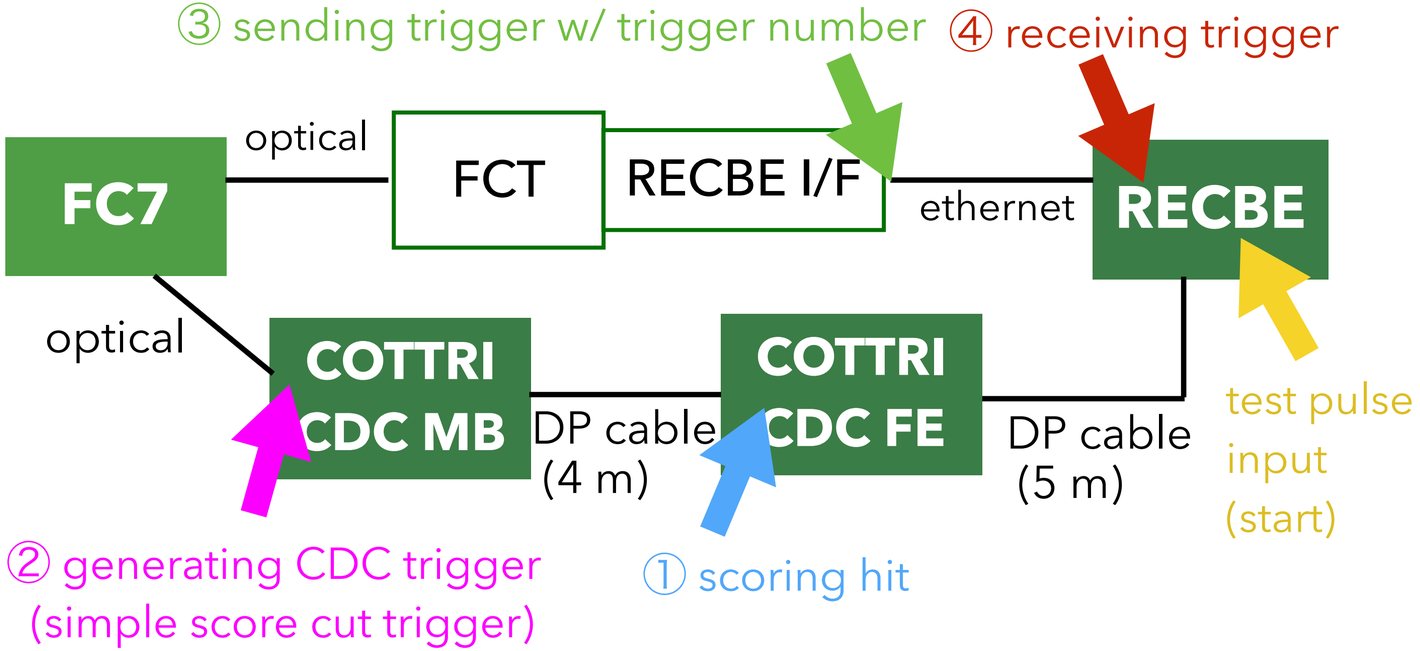
latency measurement

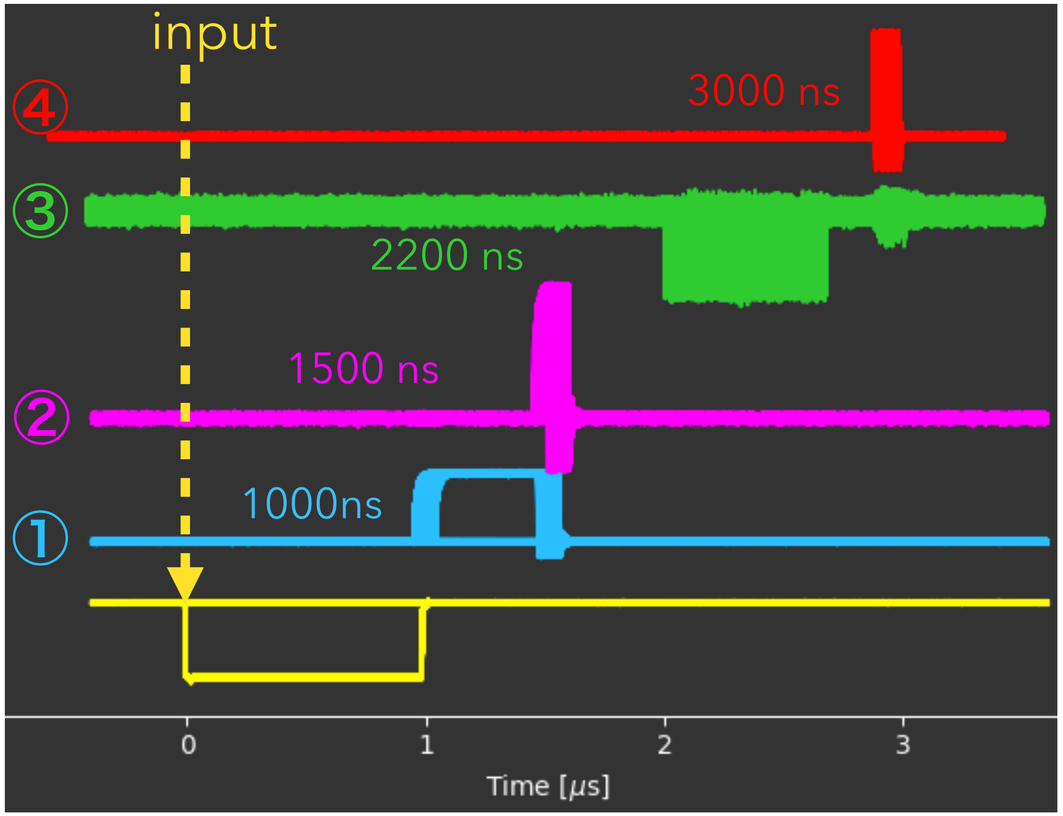
Tektronix MOS64B 10GHz, 50GS/s



Differencial probe

Latency measurement

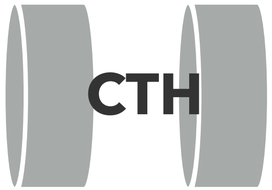




detail process

① 1000-1100 ns : generate compressed ADC “10bit→2bit & 30MHz->10MHz “(RECBE) , scoring (FE)
② 500 ns : calculate simple score cut
③ 700 ns : sending CDC trigger to FC7 (MB), generate DAQ trigger (FC7), distribute trigger (FCT)
④ 800 ns ; receiving trigger (RECBE)

Trigger Timing chart



latency ~ 525 - 550 ns

readout & trigger decision
40 MHz

drift time ~ 400 ns

latency ~ 1500-1600 ns

readout & trigger decision
10 MHz

coincidence
w/ CDC trigger delay

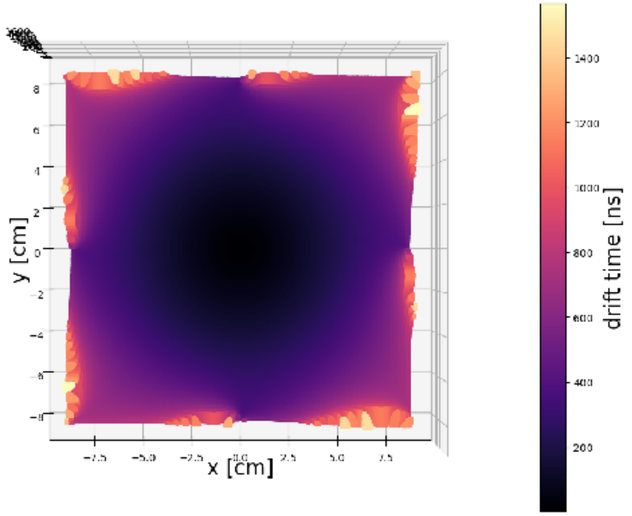
FC7
40 MHz

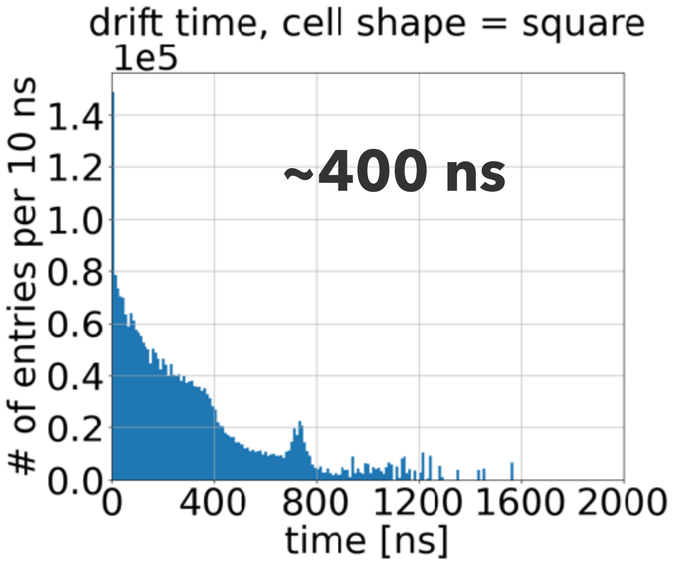
* need fixed latency
(under implementation)

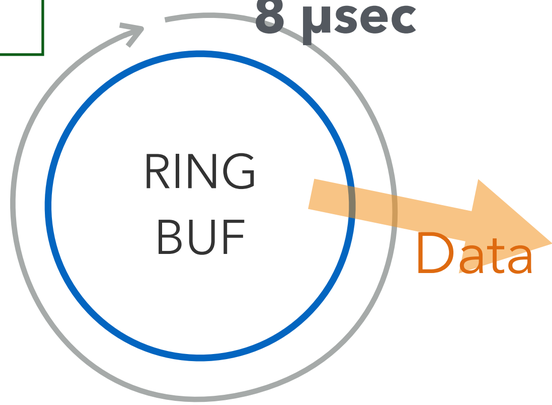
FCT
RECBE I/F

RECBE

2D distribution of the drift time

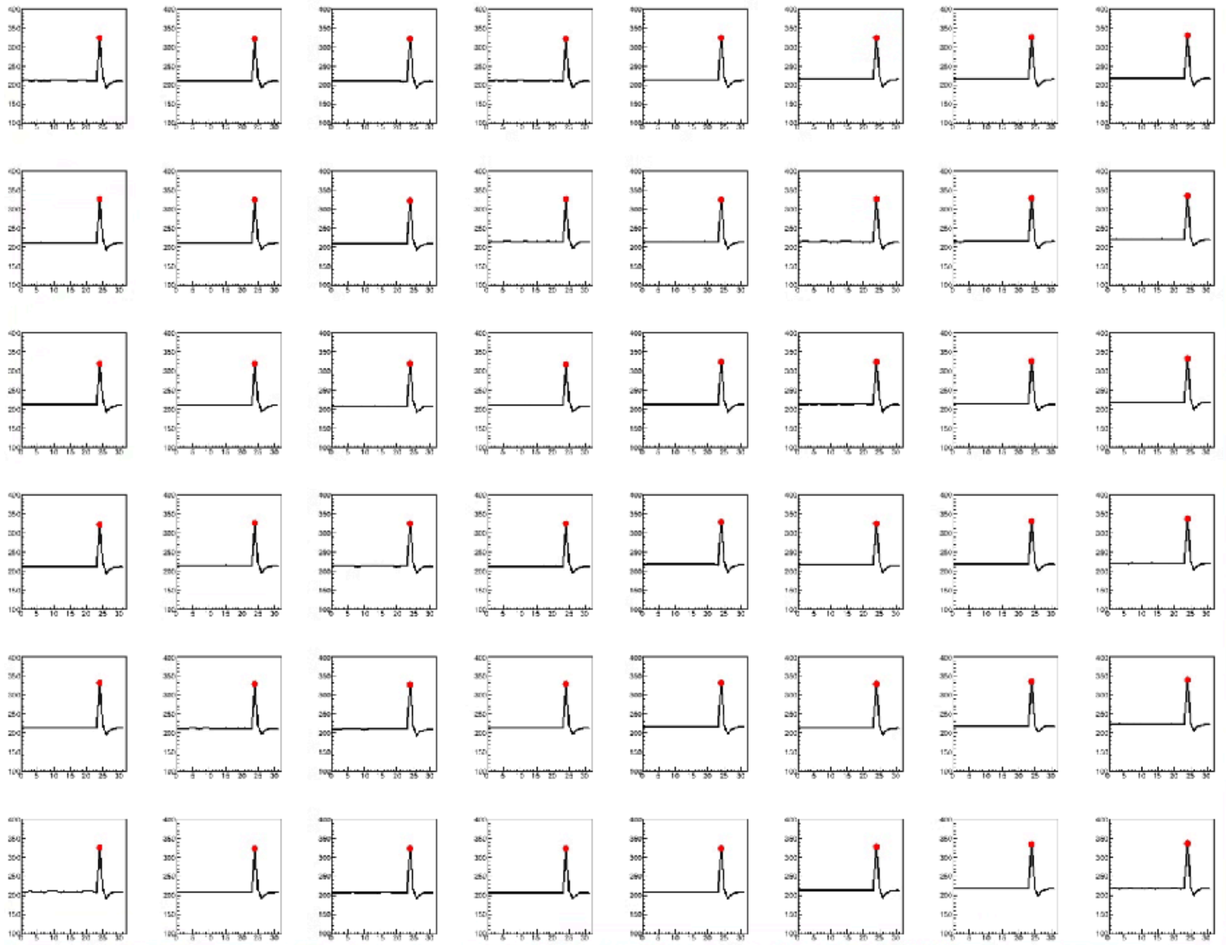






Latency measurement

test pulse 48ch



2 bit ADC