Towards large electrode sensors with intrinsic amplification for ultimate timing performance

CEA/Irfu/DphP and CEA/Irfu/Dedip

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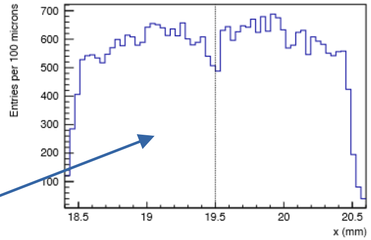
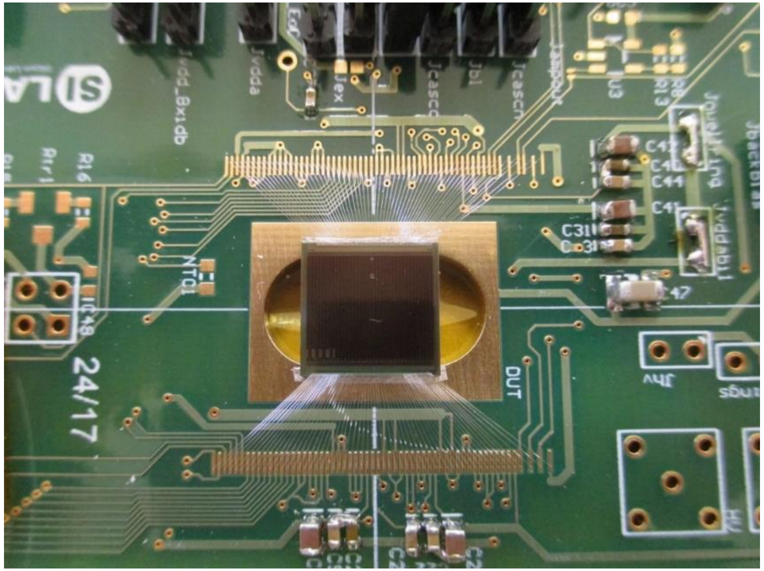
Cactus (Irfu) : Timeline and results

We started around 2017 after being involved into LF-CPIX and MONOPIX strip detector for ATLAS-ITK outer layers (possible backup solution).
CACTUS was designed in parallel, reusing blocks and concepts from LF-CPIX and MONOPIX, adding optimizations towards timing performance



At that time, 2 possible applications for sub-100ps timing detectors:

- ATLAS High η muon tagger (upstream forward calorimeter)
- HGTD in front of ATLAS-LAr



First try with CACTUS:

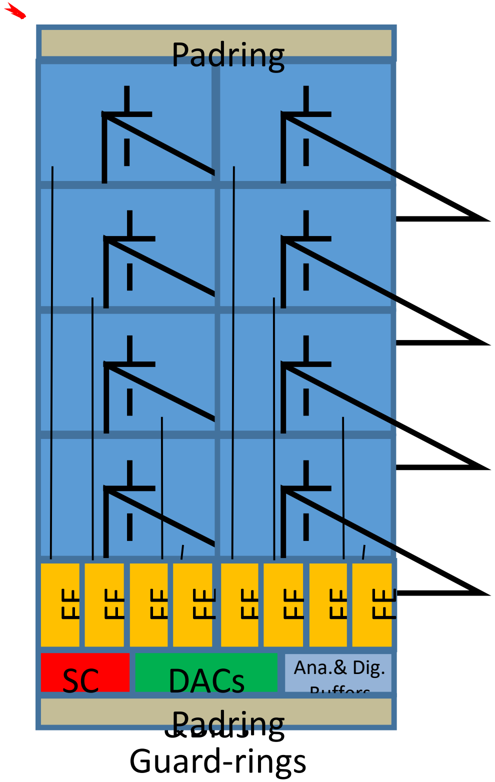
- Yield correct, High break down voltage, homogenous charge collection, deep depletion depth
- Main problem with CACTUS: underestimation of parasitic capacitance → bad S/N
- Also coupling between analogic and digital part → ringing of digital pulse

→ modest timing performance ~500ps

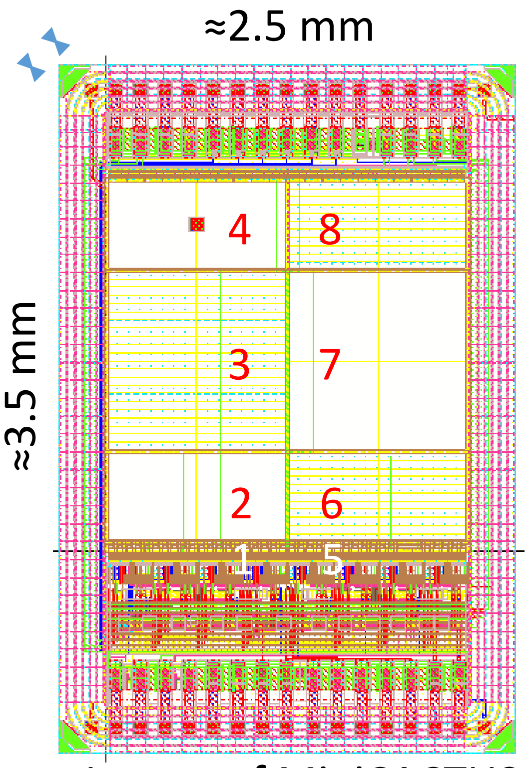
https://arxiv.org/abs/2003.04102

→ Version 2 of CACTUS called Mini-Cactus

MiniCACTUS Sensor Chip



Block diagram of the MiniCACTUS chip (not to scale)

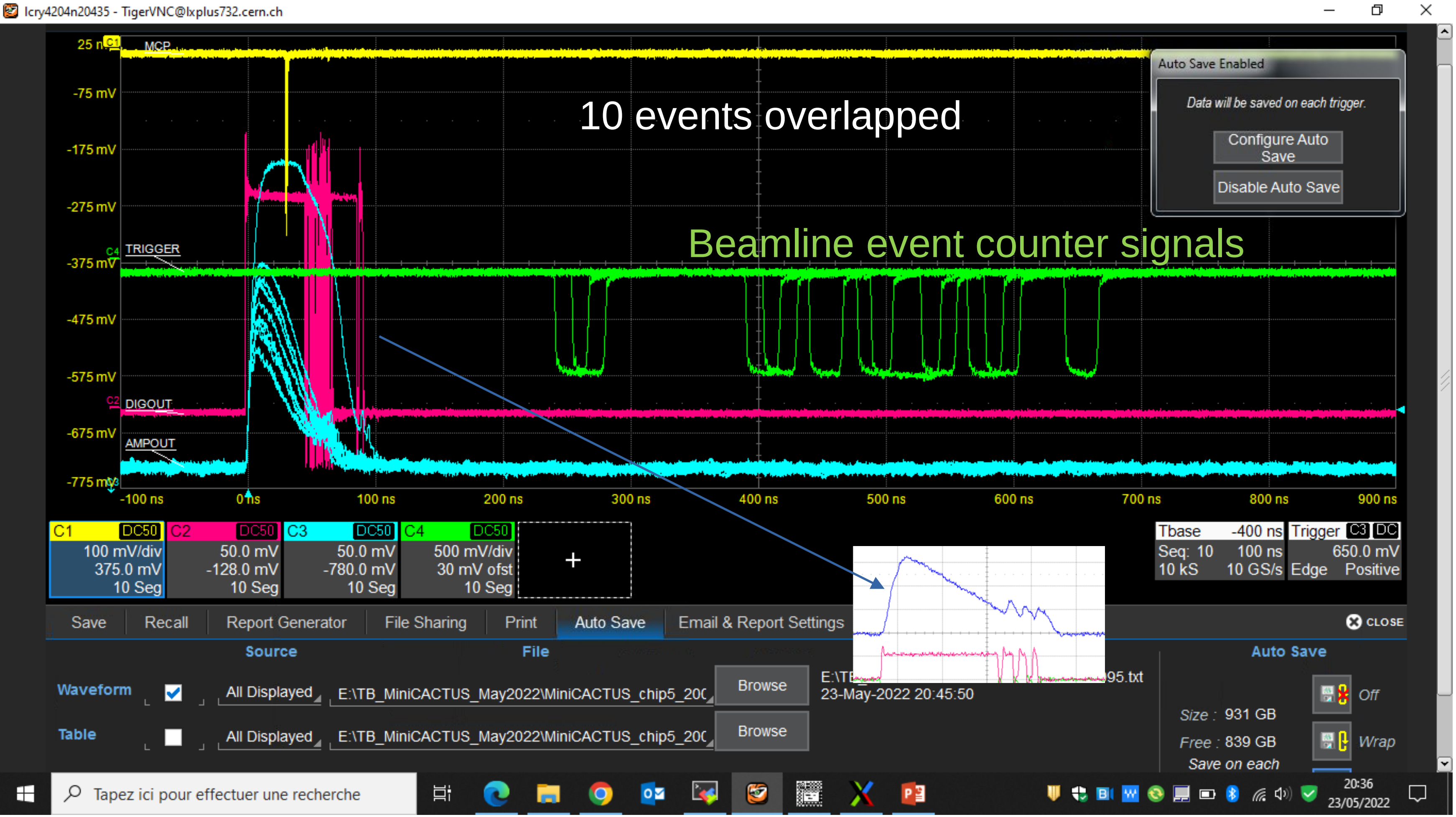


Layout of MiniCACTUS

Pixel Flavors :
Pixels 3 & 7 : 1 mm x 1 mm baseline pixels
Pixels 2, 4, 6 & 8 : 0.5 mm x 1 mm pixels
Pixel 8 : 0.5 mm x 1 mm pixel with in-pixel AC coupling capacitor (20pF)
Pixels 1 : 50 µm x 50 µm test pixel
Pixels 5 : 50 µm x 150 µm test pixel

- **MiniCACTUS** is a smaller detector prototype designed in order to address the *low S/N issue* observed on previous CACTUS large size demonstrator
- Main change in MiniCACTUS: FE integrated at column level, pixels mostly passive
- On-chip **Slow Control**, **DACs**, **bias circuitry**
- 2 discrimated digital (LVDS) and 2 analog monitoring (*slower than CSA output*) outputs for 2 columns
- 2 small pixels implemented as test structures to study charge collection (*FEs not power optimized*)
- Some detectors thinned to 100, 200, 300µm and than post-processed for backside polarization after fabrication

TYPICAL WAVEFORMS OBSERVED DURING TESTBEAM

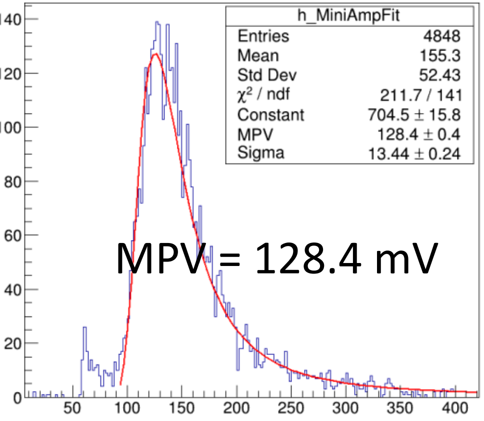


→ Ringing on Digital Output due to coupling from the digital buffers (known problem from in-lab tests, negative impact on TW corrections from digital ToT)

DATA ANALYSIS PROCEDURE

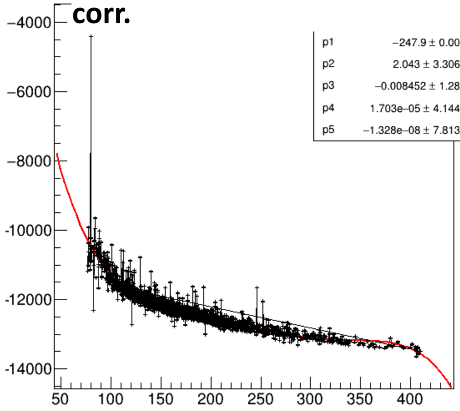
Chip#5, pixel 8**, 0.5 x 1 mm²**, **200 µm**, **-280V** (Back-side pol.)

MiniCACTUS Analog Monitoring Output



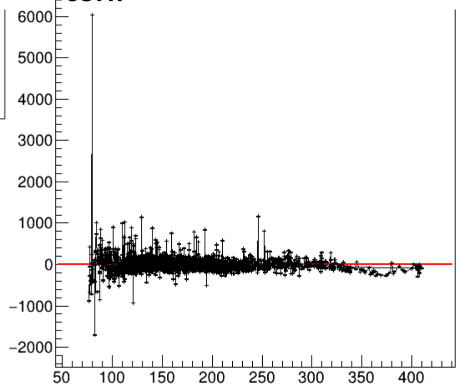
Amplitude (mV)

Fit T_MCP – T_DigOut (ns), no corr.



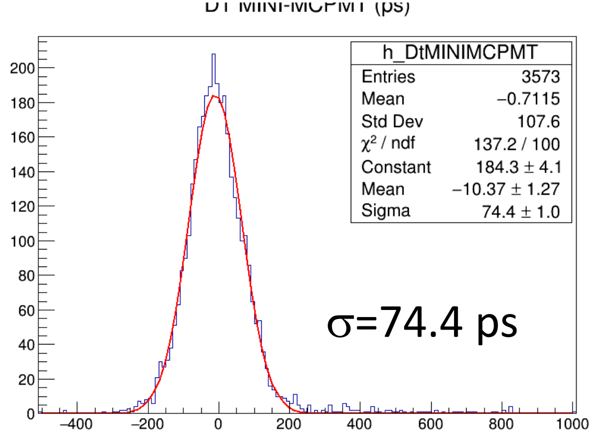
Amplitude (mV)

Fit T_MCP – T_DigOut (ns), TW corr.



Amplitude (mV)

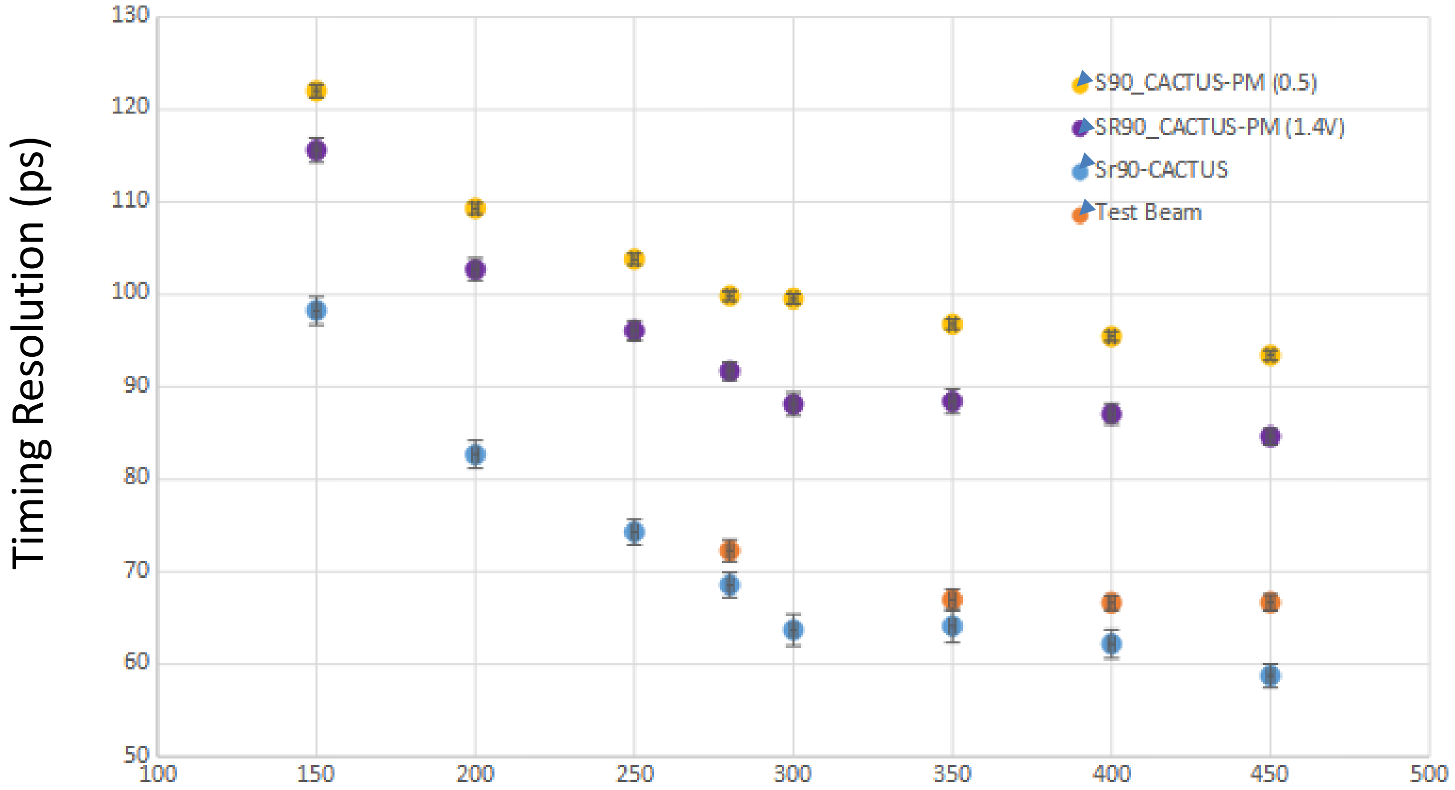
T_MCP – T_DigOut (ps) after TW correction



- Measured timing resolution (-280 V) : **74.4 ps** (MCP resolution negligible), 65 ps at -450 V
- Worse timing resolution measured with 100 µm sensor (*lower S/N* and *ringing from digital*)
- Small pixels have worse performance, probably due to charge sharing effects and field fringe effects

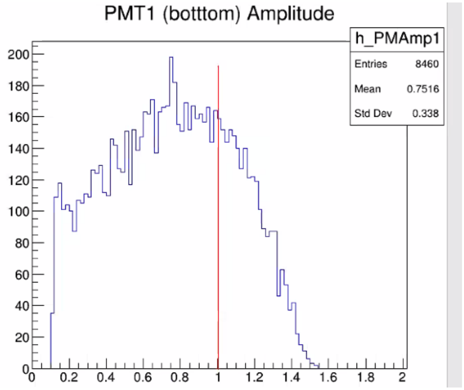
IN-LAB TIMING MEASUREMENTS WITH PMT AND ^{90}Sr SOURCE

Chip#6, pixel 8**, 0.5 x 1 mm², 200 µm**



→ In-lab measurements with 90Sr betas

allowed to predict actual performance with MIPs



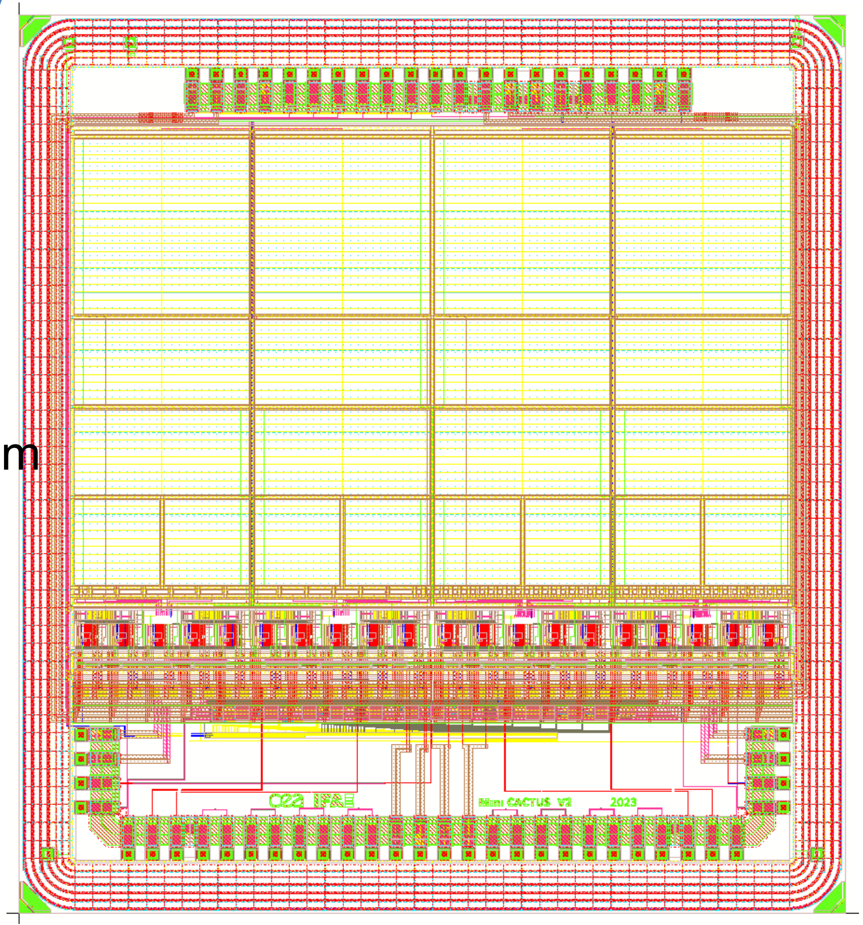
Have to select MIP-like betas by cutting out low energy deposits in PMT

MiniCACTUS_V2 Sensor Chip

Irfu : Yavuz Degerli, Fabrice Guilloux, Jean-Pierre Meyer, Philippe Schwemling
IFAE : Raimon Casanova, Yujin Gan, Sebastian Grinstein

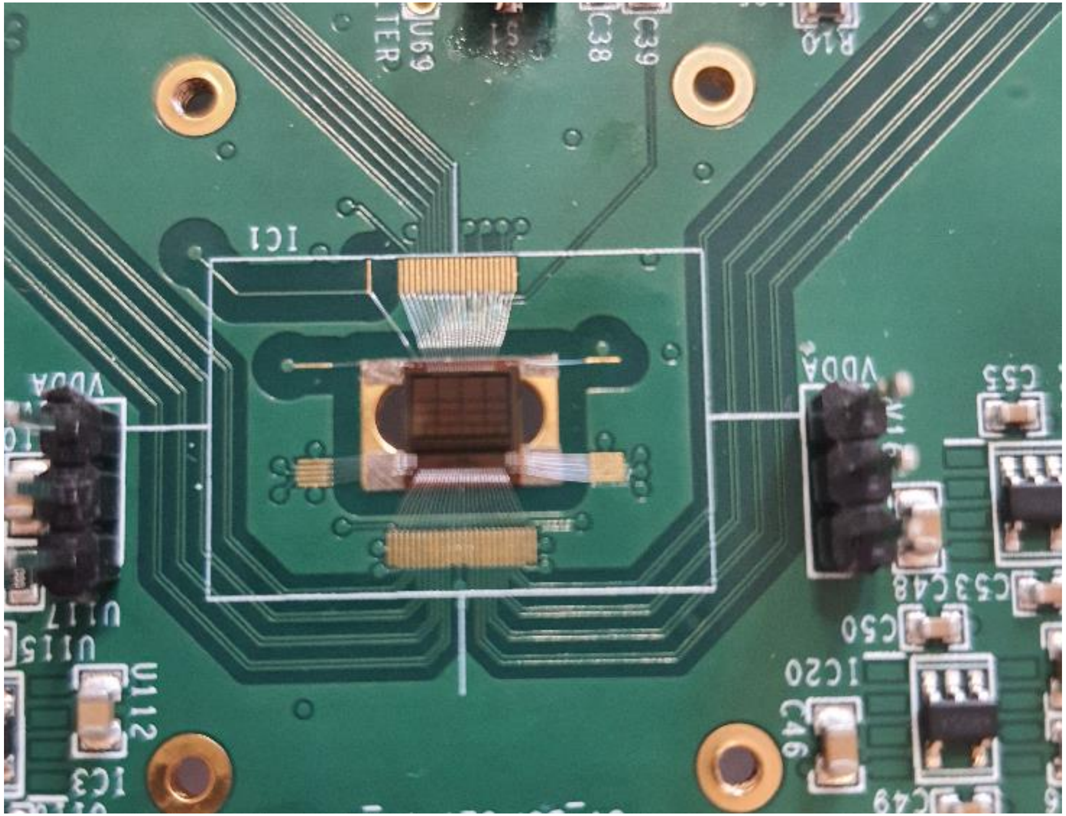
≈4.6 mm

≈ 5 mm



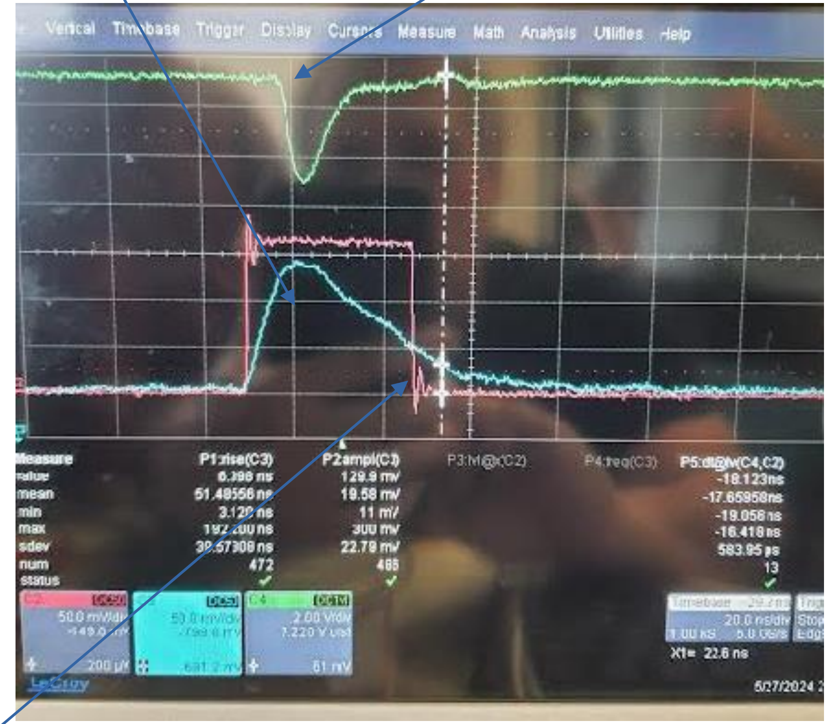
- ~ 2 times larger than MiniCACTUS
- 0.5 mm x 1 mm (baseline), 1 mm x 1 mm and 0.5 mm x 0.5 mm diodes
- 50 µm x 150 µm and 2 50 µm x 50 µm small test diodes
- 3 different preamps
- New multistage discriminator with **programmable hysteresis**
- Improved layout for better mixed-signal coupling rejection
- **CEA-IRFU** & **IFAE-Barcelona** coll.
- Submitted in May 2023, chips came back from post-processing end May 2024

First look at MiniCactus v2



Analog

PMT

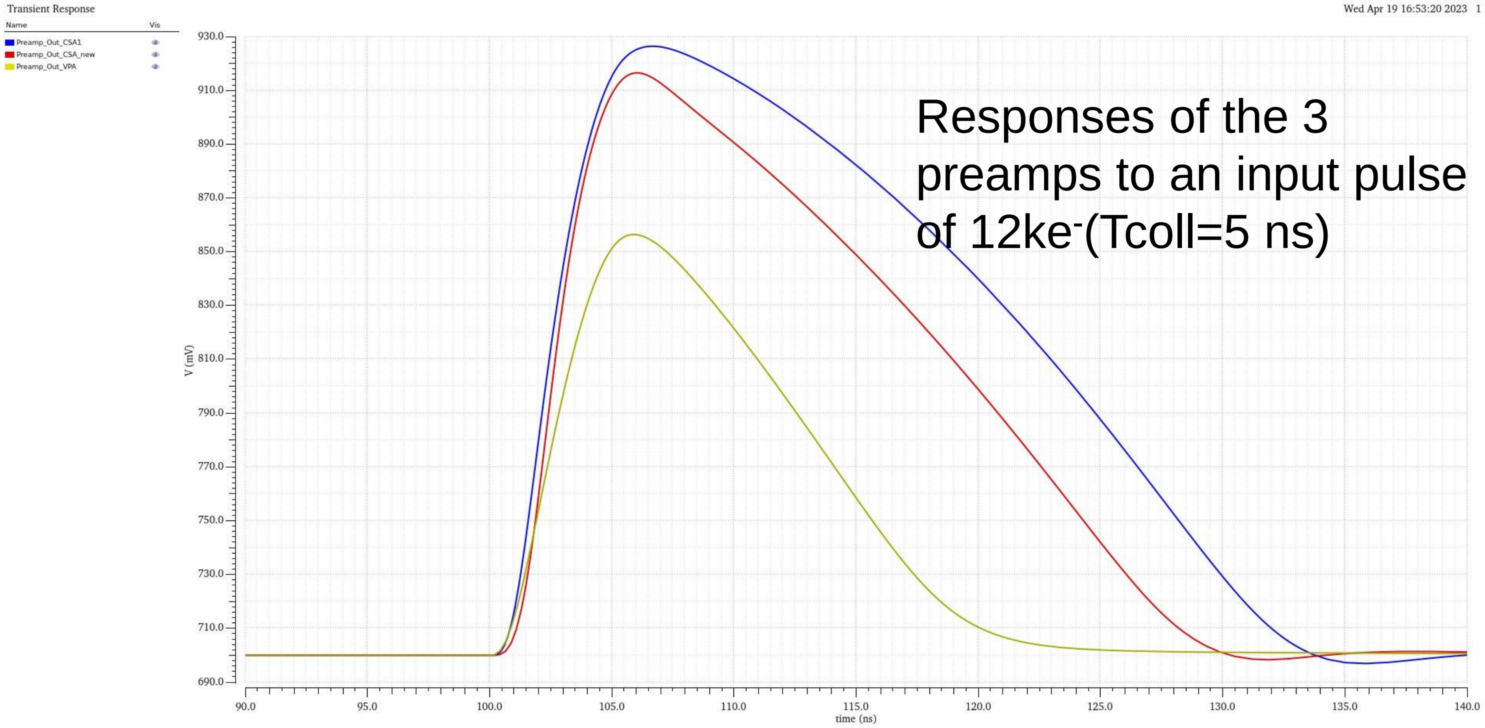


Digital

Analog/Digital couplings are gone !

MiniCACTUS_V2 Sensor Chip

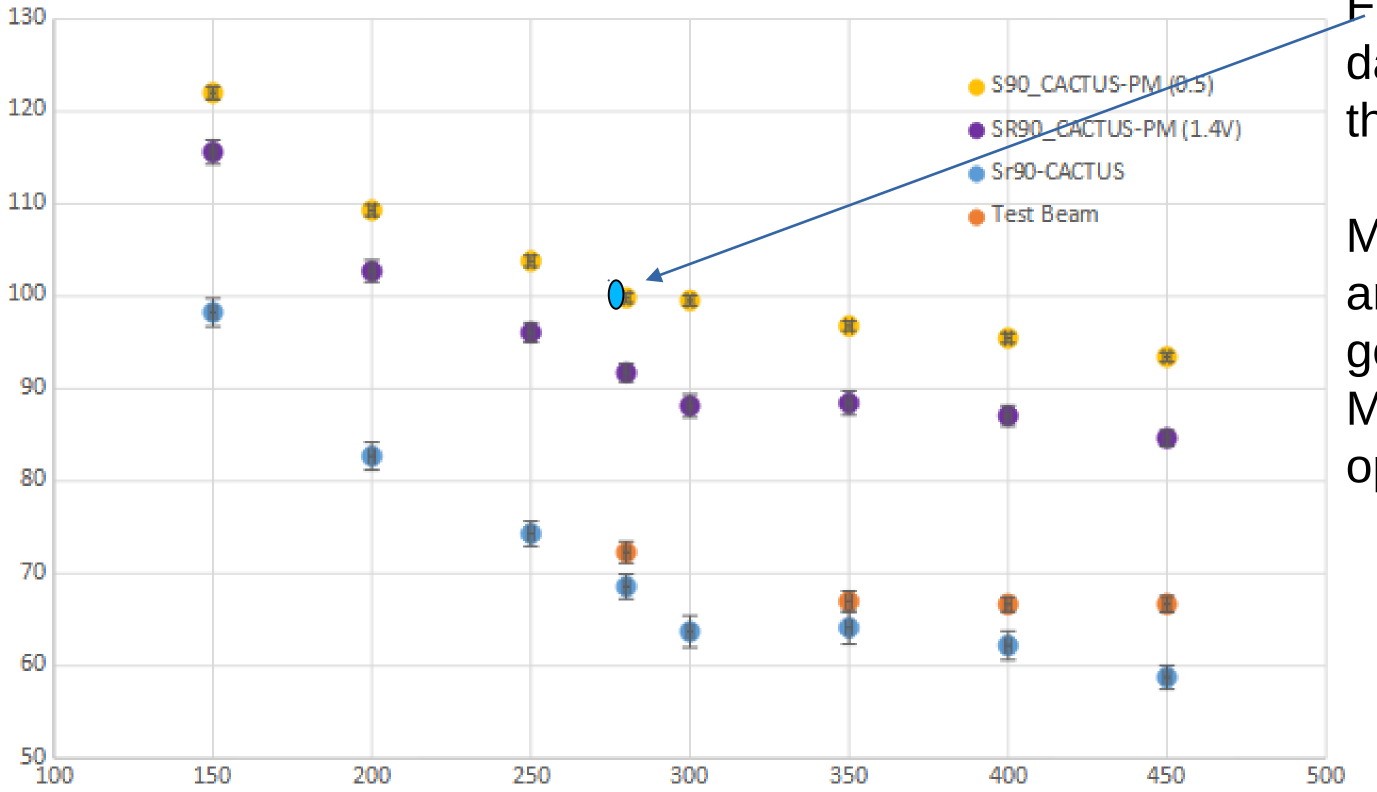
- 3 different preamps implemented in MiniCACTUS_V2
- 2 new preamps (CSA_new and VPA) designed by **IFAE-Barcelona** for better jitter and reduced ToT



Responses of the 3 preamps to an input pulse of 12ke$^-$(Tcoll=5 ns)

- CSA1 : MiniCACTUS_V1 charge sensitive preamp
- CSA_new : new charge sensitive preamp
- VPA : new voltage preamp

First comparison MiniCactus v1 and v2



First MiniCactus 90Sr v2 data (500 x 1000 u pixel, thickness 200 u)

MiniCactus v2 before any FE optimization has as good performance as MiniCactus v1 after optimization

MiniCactus v2 next steps

- Study and optimize all pixels, especially the new Altiroc inspired Front-Ends
- Testbeam period (RD-51/DRD1 parasitic) just ended → perf similar to v1, but cleaner signals
- Hope to get improvements from sensors with thicknesses < 200 u, i.e. less Landau fluctuations (we have 175 u and 150 u)

How to improve further ?

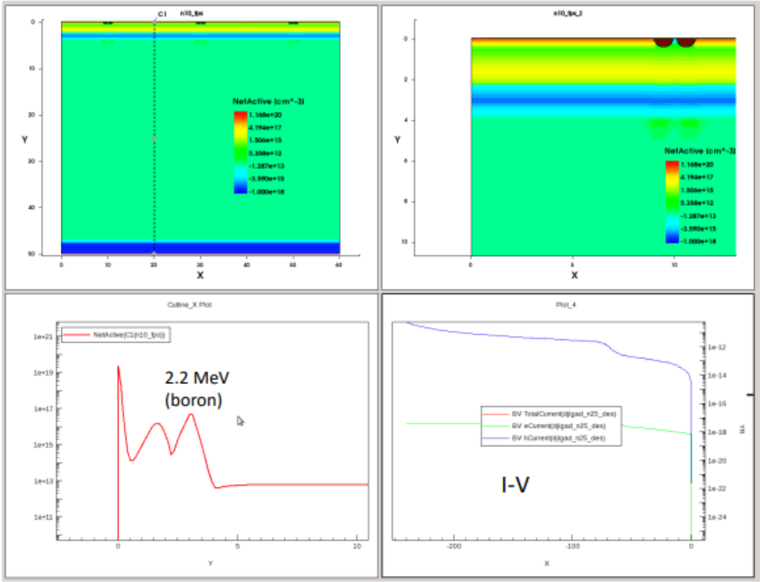
- Intrinsic gain allows to :
  - Improve S/N → Improve on time resolution
  - Reduce FE power consumption
  - Reduce pixel pitch
- Ultimate goal is reaching 20 ps resolution

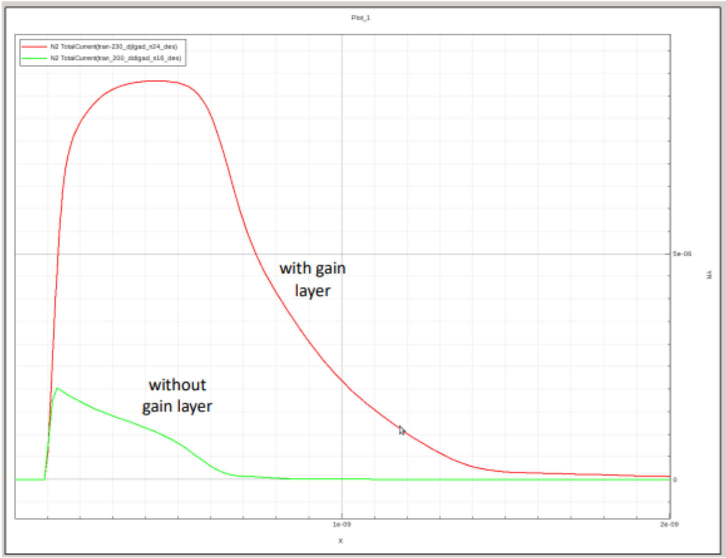
First test structures in LF15A technology

species	max allowed Energy	max dose (ions/cm^2)	expected concentration at peak.	
Phosphorus	4.0MeV	1E13 /cm^2	~1E17 atoms/cm^3	N
Boron	2.2MeV	1.5E13 /cm^2	~3E17 atoms/cm^3	P
In both cases we strongly suggest to make angled implantations (7 Deg tilt) in order to avoid second order effects like channeling that may generate uneven depth of the peaks within the wafer.				will limit implant depth: ~3µm according to simulations

Gain layer can only be implanted very close to the surface

First simulation attempts (Sentaurus)

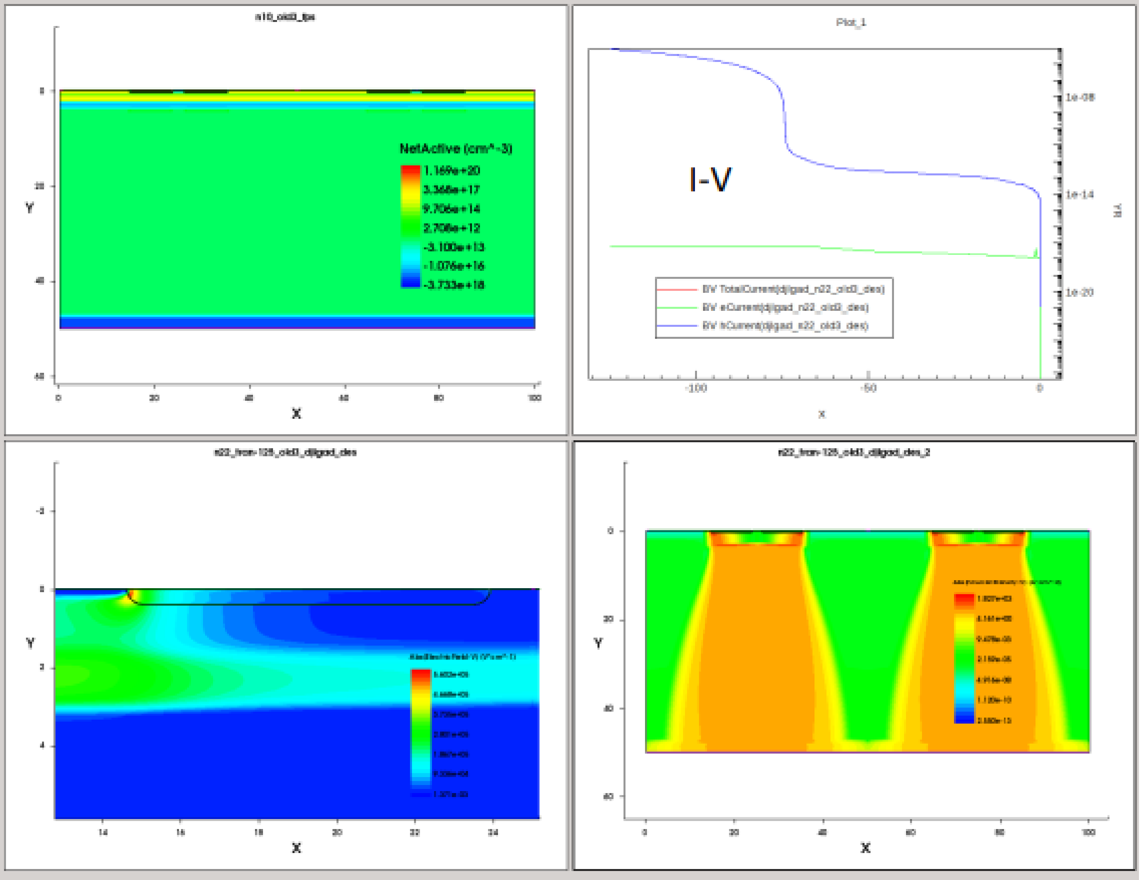




Initial structure and simulation files received from T. Hemperek
N+ collection electrode **with** STI and P-Stop, small distance between n-wells (~2 µm)
BV > 230V can be obtained in these conditions

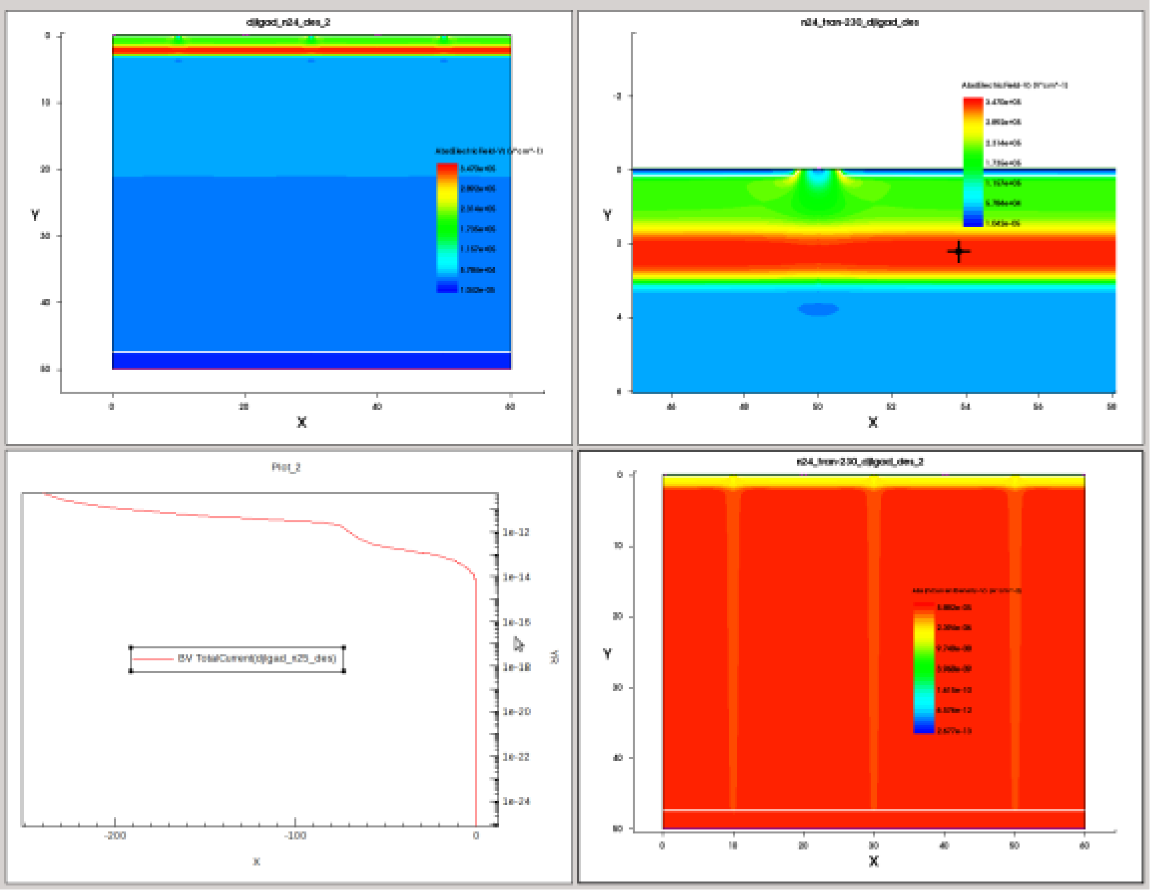
- Gain > 10 possible after optimization of deep P & N doses and energies (limited by BV)

What happens with present (MiniCactus) sensor diodes ?



- **CACTUS/MONOPIX-like (N+) diode** with 50µm pitch including STI and P-Stop (“large” distance between n-wells)
- Early breakdown occurs → No possibility to obtain gain

Optimization of inter pixel region



- Homogenous electric field
- **The distance between the collection electrodes seems to be very critical**

Submission status

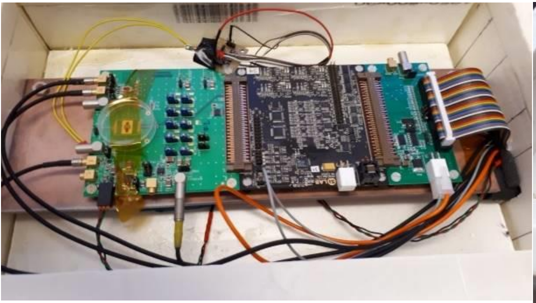
- Test structures (passive sensors) have been submitted in May 2024 LF15A MPW
- Six different layouts, identified as promising by TCAD
- Production implies only minimal modifications to LF15A standard process
  - Changes of implant energies for two layers
  - Addition of one Customer Reserved Layer
- HR wafers (same as MiniCactus) → will need postprocessing
- 30 u epi wafers → hope is to get rid of postprocessing
- Expect to have chips back from foundry by end of 2024

Conclusions and perspectives

- Short term : In-lab and test-beam tests of MiniCactus v2
- Medium term : investigate test structures with integrated gain layer.
- If test structures work, integrate front-end, and submit a MiniCactus like design in LF15A (2025?)
- Investigate more advanced technologies (TJ 65, 2025-2026 ?)
- Interested groups : IFAE-Barcelona, Irfu-Saclay, University of Liverpool
- Publications :
    - MiniCACTUS: A 65 ps Time Resolution Depleted Monolithic CMOS Sensor (arXiv:2309.08439, NSS 2022 conference)
    - MiniCACTUS: Sub-100 ps timing with depleted MAPS, Nucl.Instrum.Meth.A 1039 (2022) 167022, VCI 2022 conference)
    - CACTUS: A depleted monolithic active timing sensor using a CMOS radiation hard technology (arXiv:2003.04102, JINST 15 (2020) 06, P06011)

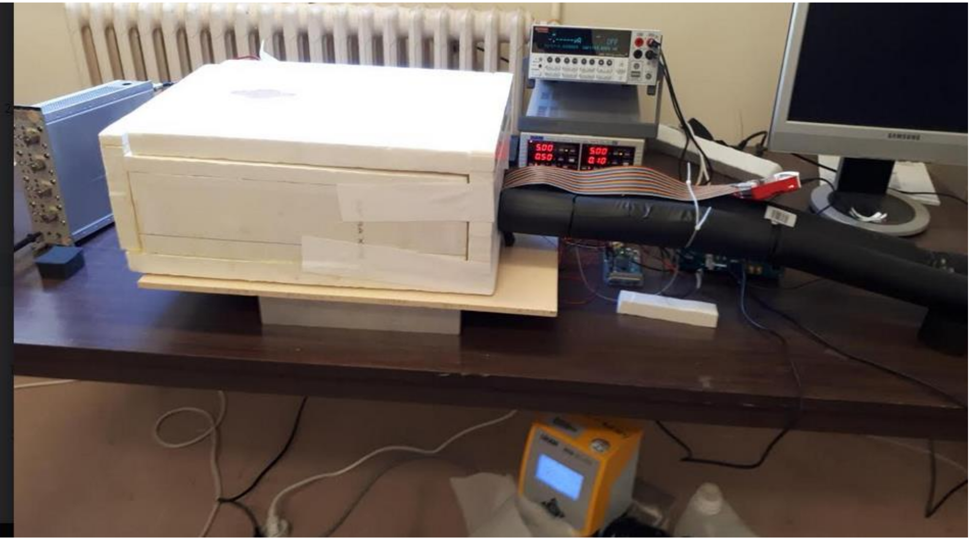
Backup

Development of cold box setup



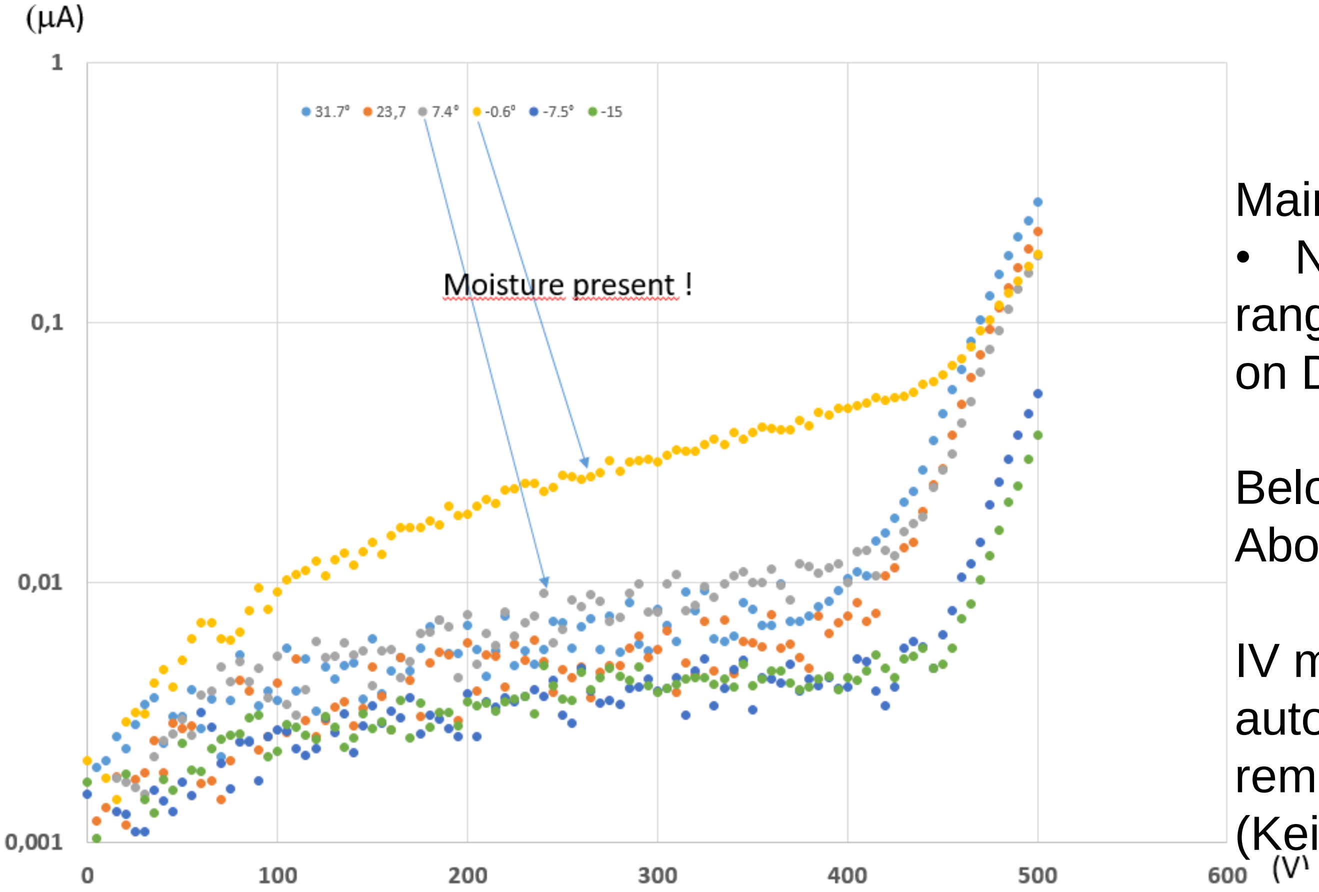
Initial status

After one month of continuous operation at -15°C



- Mostly intended to test irradiated samples
  - We have 100 µ and 300 µ irradiated at 10^{14}, 10^{15}, 10^{16} 1 MeV neq/cm^2
- MiniCactus testbench (DUT board, GPAC, Raspio) in insulating foam box (plus feedthroughs for power and cooling)
- Copper plate with a cooling pipe welded to it plus copper fingers bring cold surface as close as possible to DUT
- Monitoring of temperature and moisture level at various places in cold box
- No moisture control, we just try to minimise water input
- LAUDA chiller, min temp -30°C at chiller output
- Kapton windows allow use of 90Sr beta source (has to stay outside of cold box for safety/regulatory reasons)

IV curves vs temperature (Unirradiated DUT. 300 µ thick)



Main conclusion :

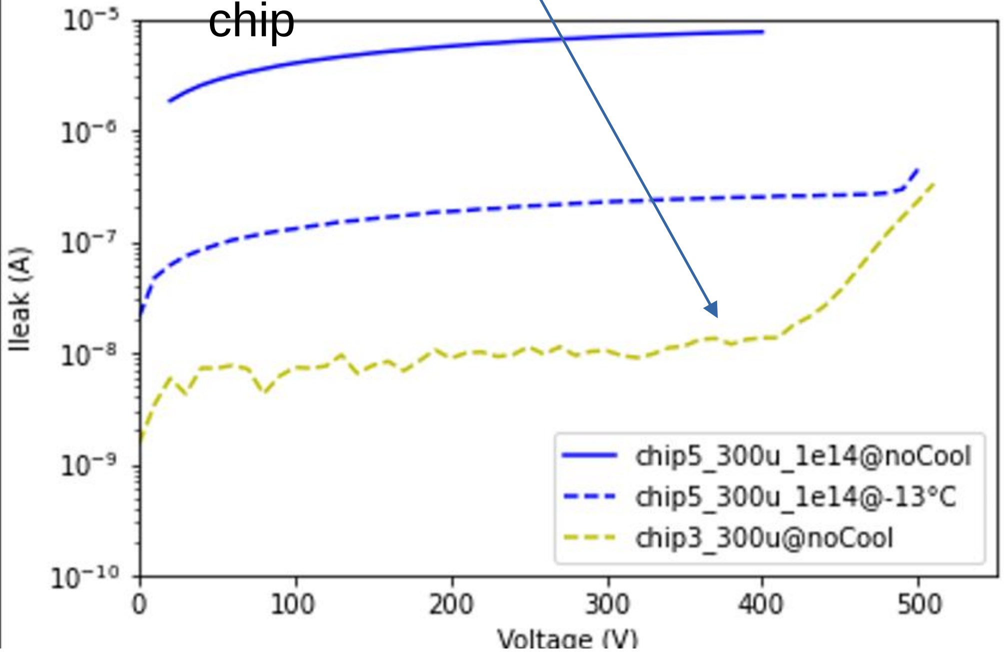
- Need to run avoiding temperature range between 7.5°C and -1°C measured on DUT

Below -1°C all water is frozen → OK
Above 7.5°C all water is vapour → OK

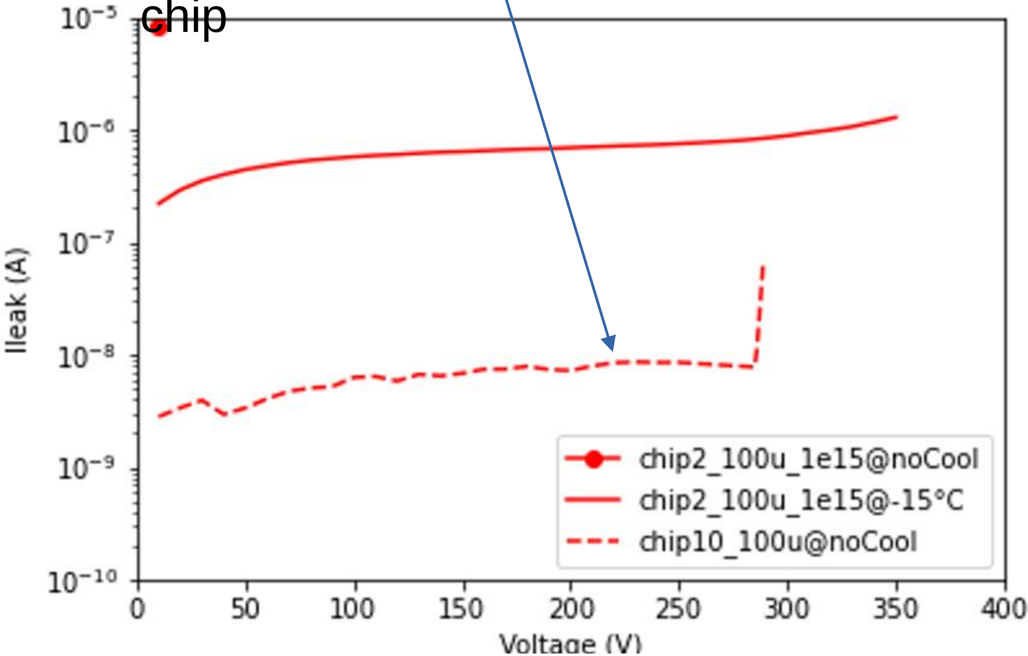
IV measurement done routinely and automatically through
remote control and monitoring of HV PS
(Keithley sourcemeter)

IV curves of irradiated MiniCactus v1

Reference 300 µ unirradiated chip

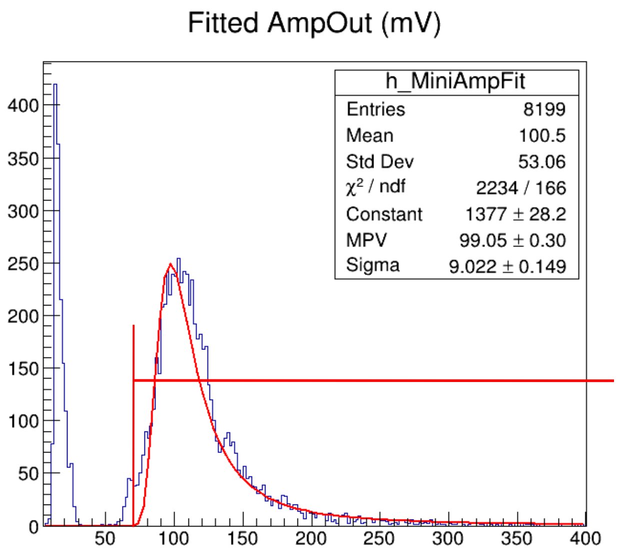


Reference 100 µ unirradiated chip

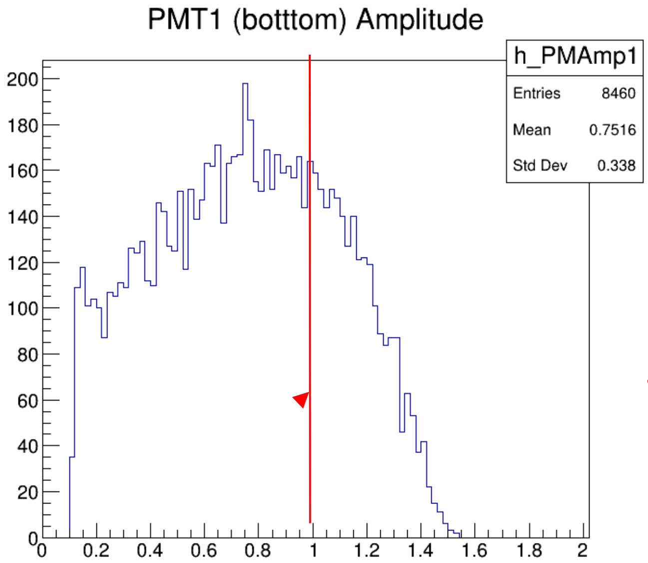


As expected, BV increases with total dose
Cooling is essential to bring leakage current to manageable

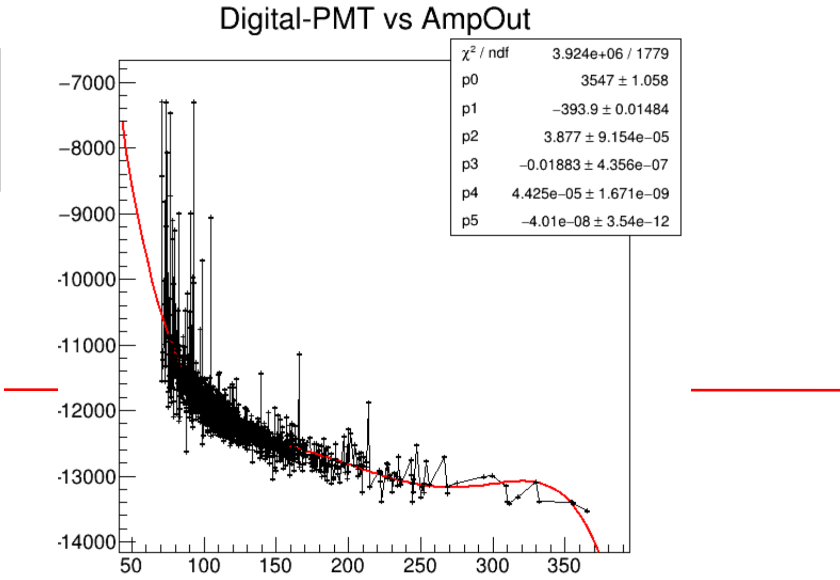
PMT and MiniCactus data
10^{14} 1 MeV neq irradiated DUT, 300 µ thick, 200V



Amplitude (mV)



Amplitude (V)



TW correction
As a fct of analog amplitude

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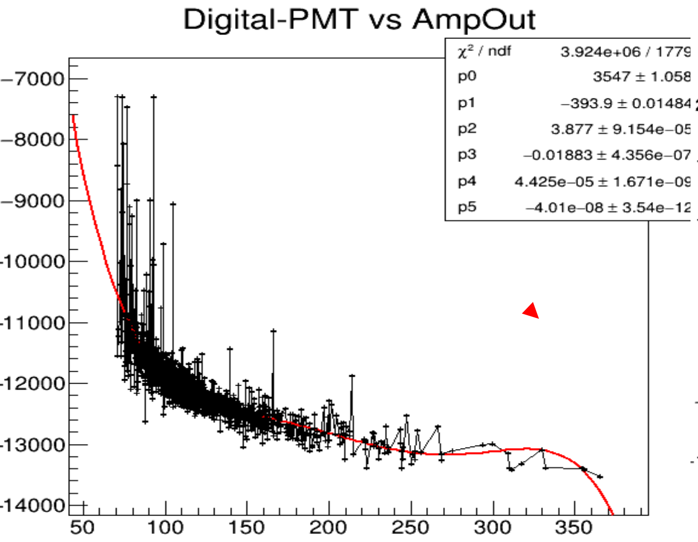
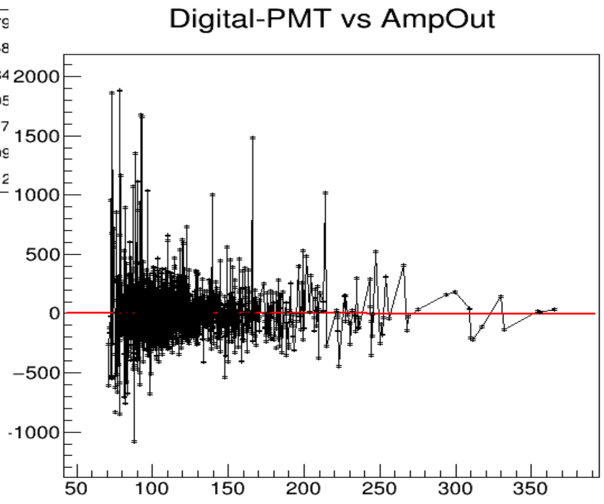
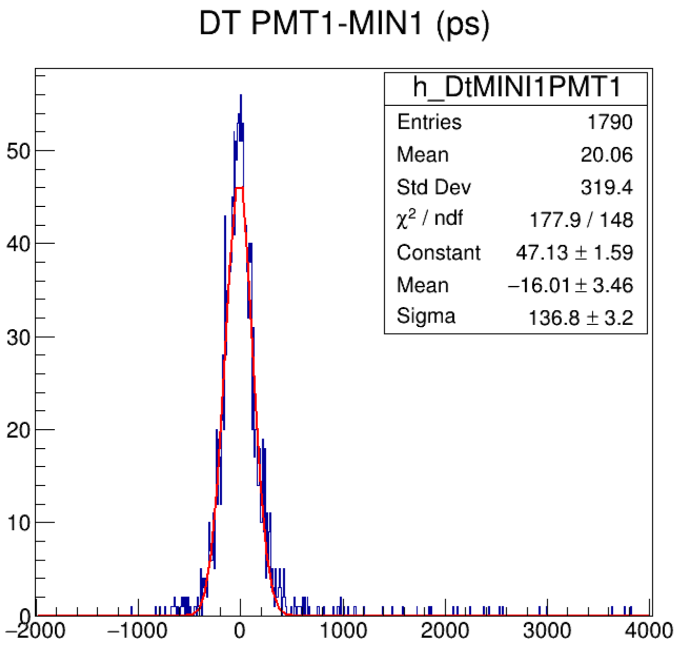
PMT and MiniCactus data
10^{14} 1 MeV neq irradiated DUT, 300 µ thick, 200 V







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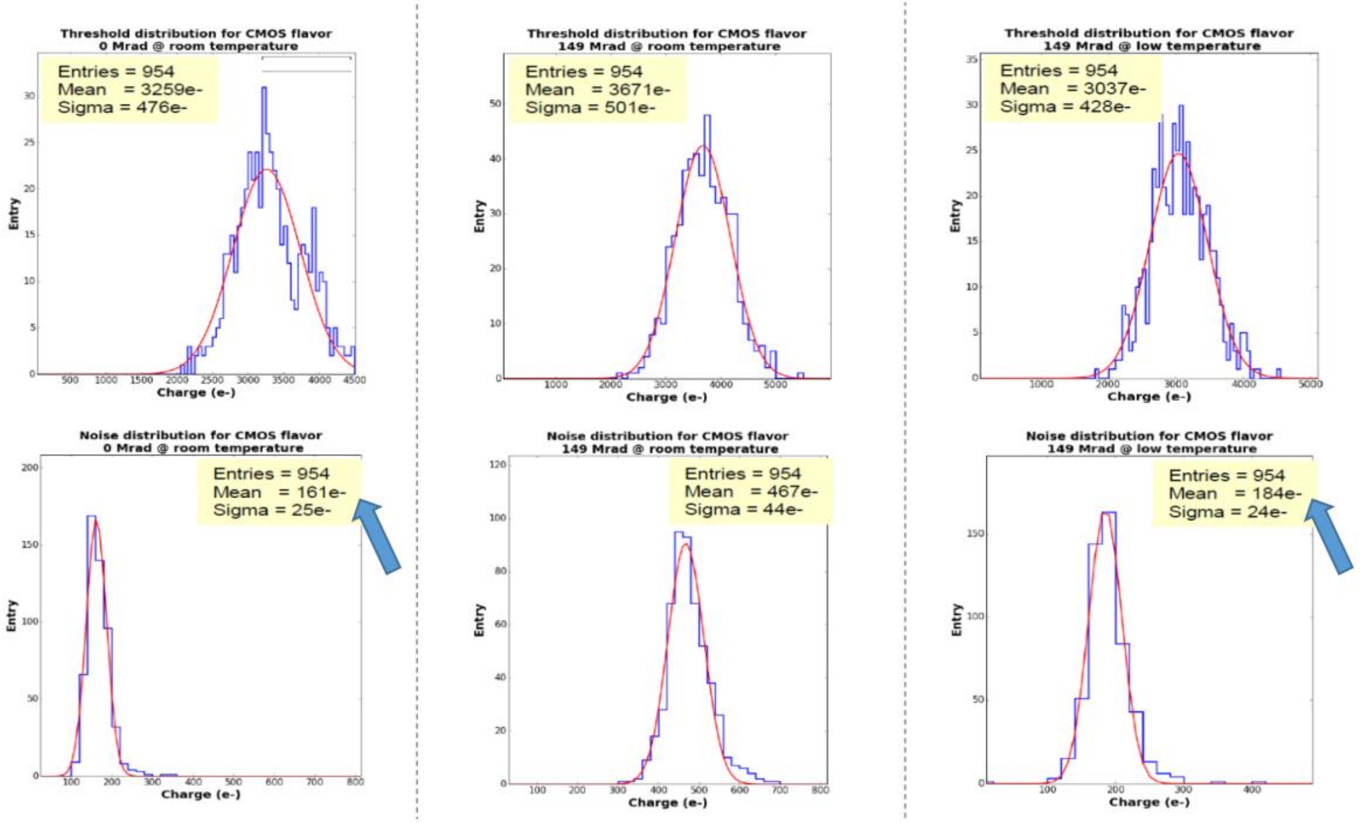
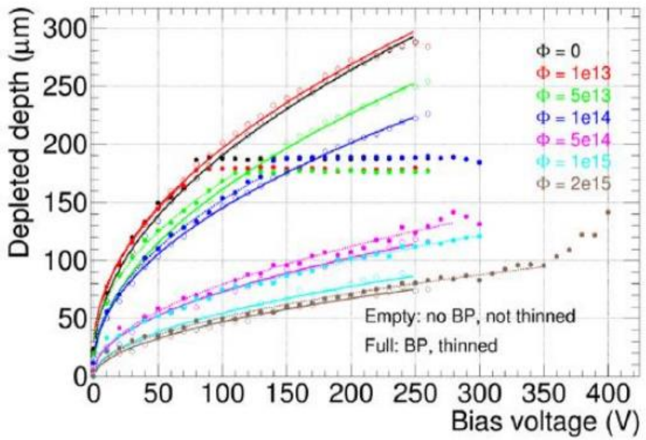
LF15A radiation hardness

0 Mrad @Room Temp   149 Mrad @Room Temp   149 Mrad @Low Temp -15°C





[I. Mandic et al. NIM A 903, 2018]

→ Radiation tests at CERN-SPS with **proton** beam on **LF-CPIX** chip (**CPPM**)
→ 14% increase of noise after irradiation with cooling

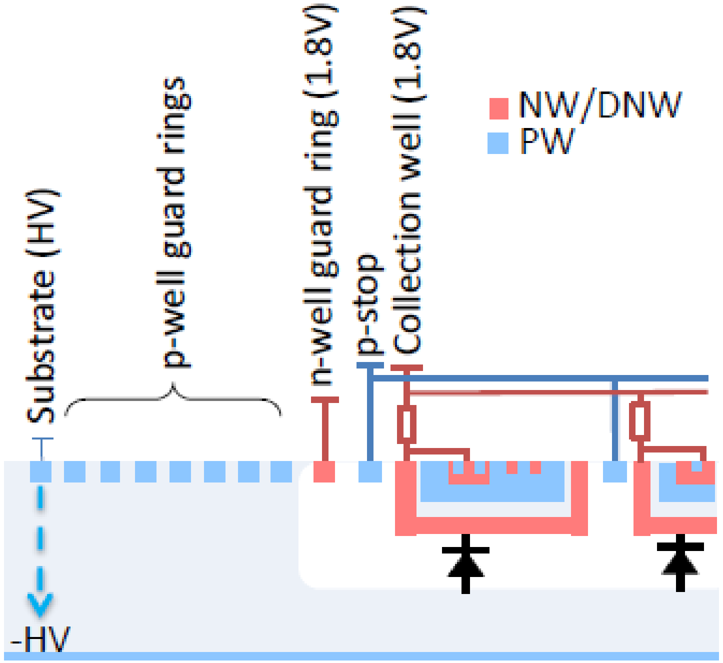
Comparison of time resolution of unirradiated and 10^{14} 1 MeV neq chips

Sensor	HV bias (V)	Conditions	Temp. (°C)	Time res. (ps)	MPV (mV)
Unirradiated 300 u	400	testbeam, MCPMT time reference	room	78.97 ± 1.36	201.9 ± 0.5
Unirradiated 300 u	400	90Sr, PMT time reference*	room	104.5 ± 2.30	195.7 ± 2.3
Unirradiated 300 u	280	testbeam, MCPMT time reference	room	89.11 ± 1.56	200.9 ± 0.5
Irradiated 300 u	280	90 Sr, PMT time reference	20	108.2 ± 3.2 (PMT subt.)	108.2 ± 3.2
Irradiated 300 u	320	90 Sr, PMT time reference	20	132.9 ± 5.0 (PMT subt.)	113.5 ± 0.8
Irradiated 300 u	320	90 Sr, PMT time reference	-15	87.9 ± 4.7 (PMT subt.)	132.7 ± 0.6

Irradiation at 10^{14} n_{eq} worsens time resolution by 18 % w.r.t. unirradiated at 20 °C
Cooling at -15°C brings time resolution more or less back to unirradiated performance (less dark current fluctuations)

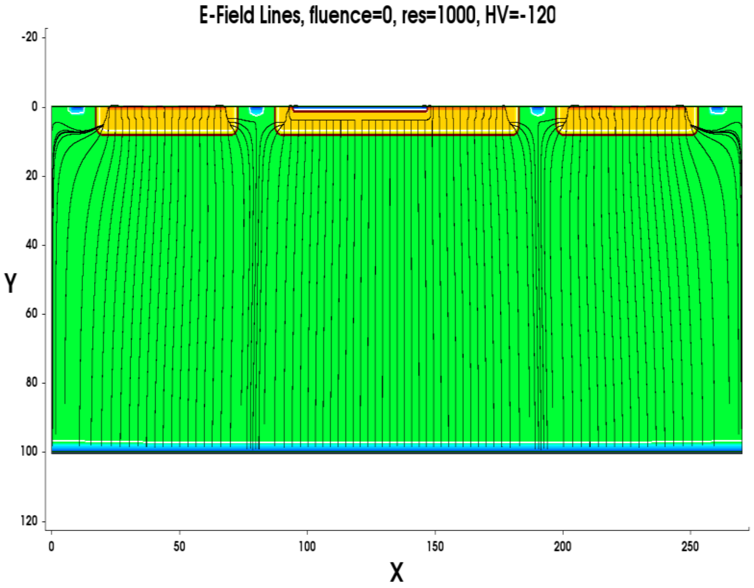
*PMT resolution for 90 Sr betas estimated to be 71.3 ps ± 1.7 ps

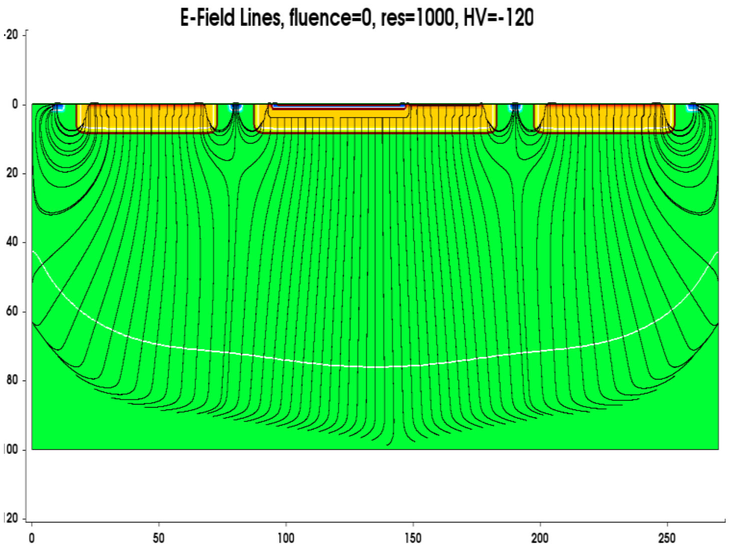
GUARD-RINGS OF LF-MONOPIX1



[M. Barbero et al. JINST 15, 2020]

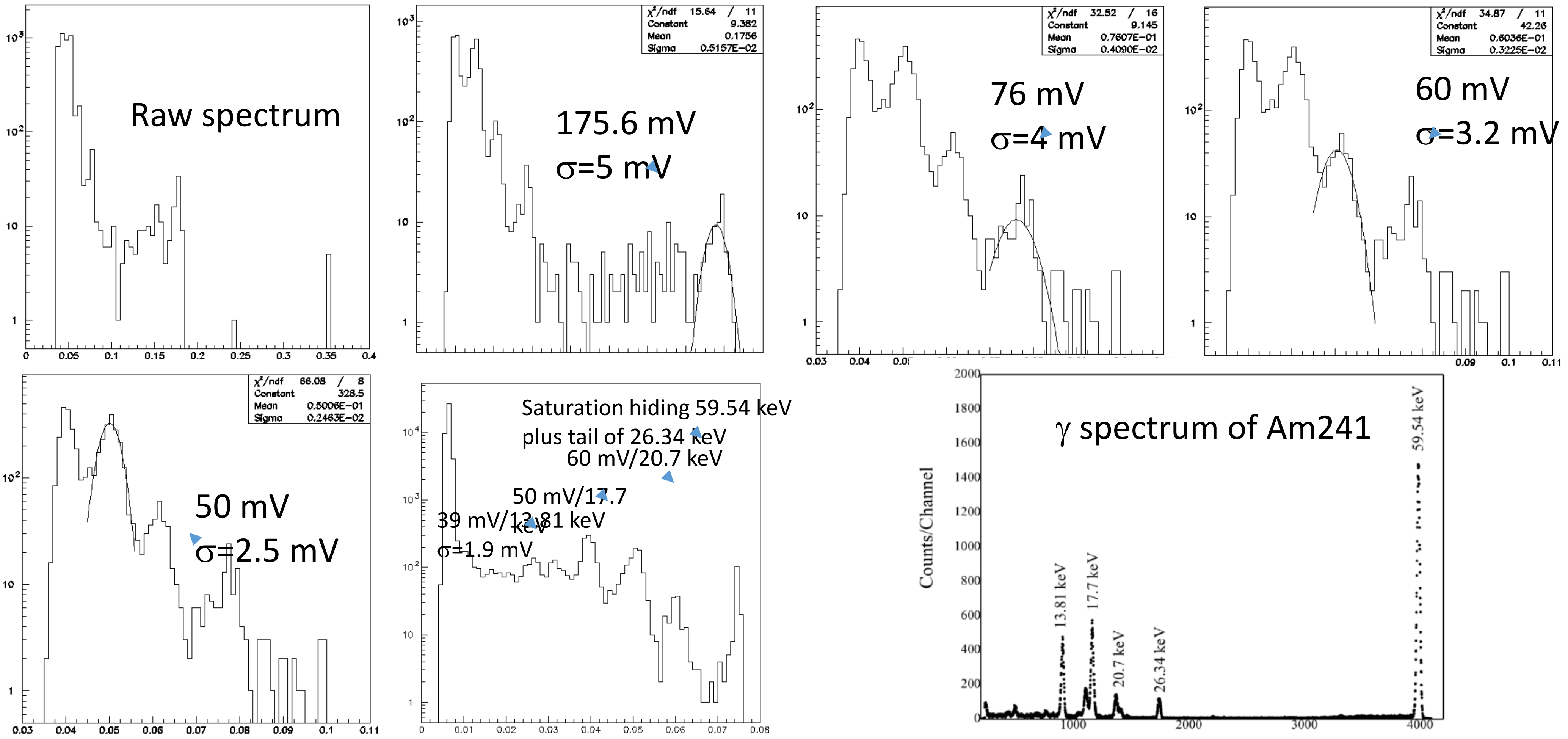
ELECTRIC FIELDS





Backside versus top biasing → Need backside polarization to ensure best charge collection and signal shape uniformity!

241Am Amplitude Spectrum (pixel 5, 50 µm x 150 µm)



Test-beam at Synchrotron Soleil
June 2022

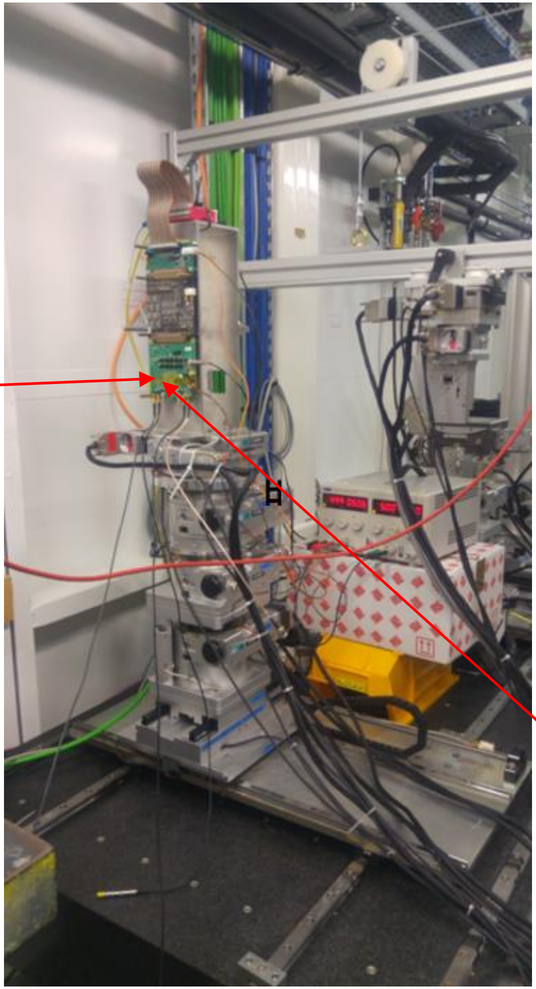
Many thanks to Fabienne Orsini and Arkadiusz Dawiec
(Synchrotron Soleil)
for the beam time and the technical support !

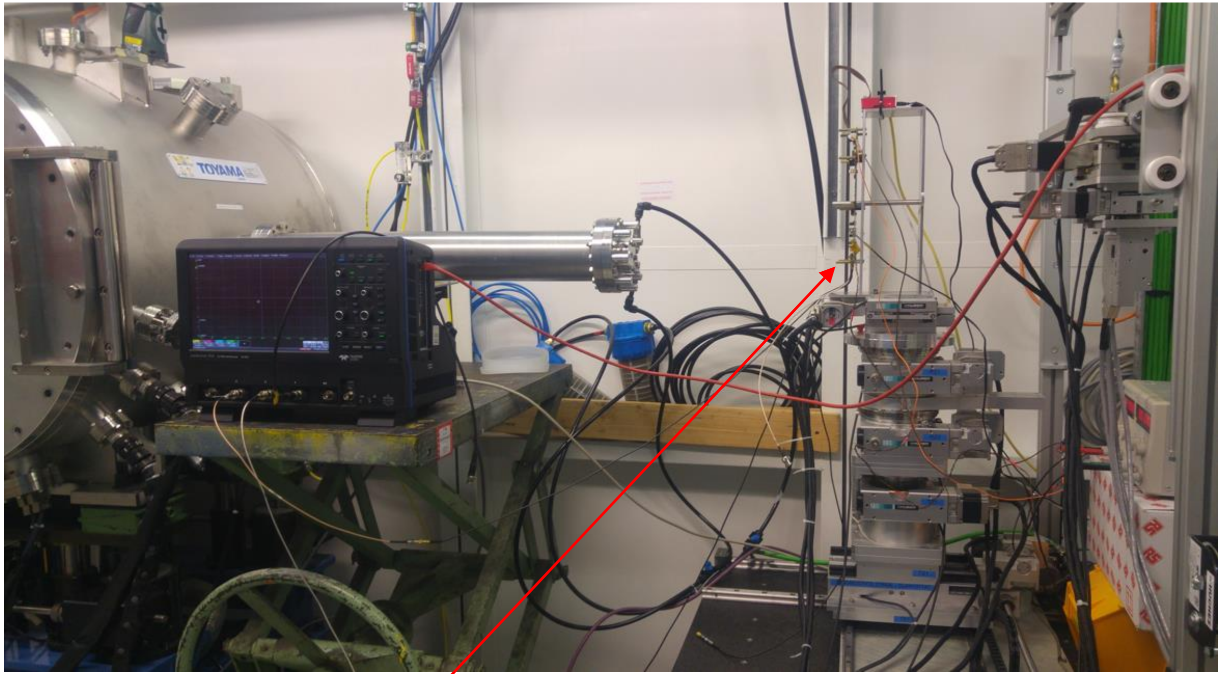
Photon beam is bunched : 90 ps pulse length
Every 2.6 ns

Allows to study energy and time response
Beams of 10 keV, 20 keV, 30 keV, 40 keV
Available, attenuated to have ≈ 1 photon/bunch

With X/γ radioactive sources, only energy response can be studied

Setup pictures



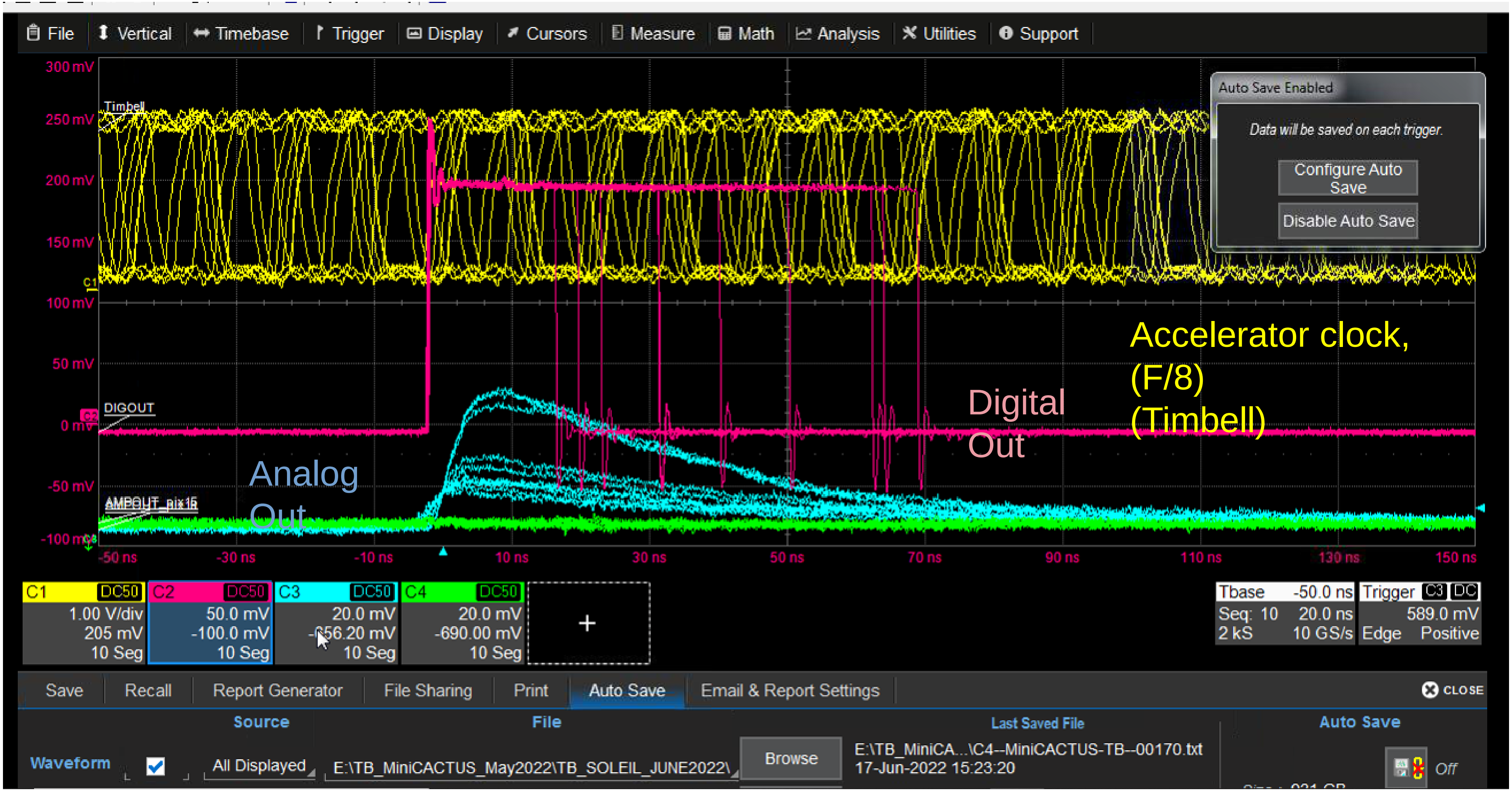


Beam direction

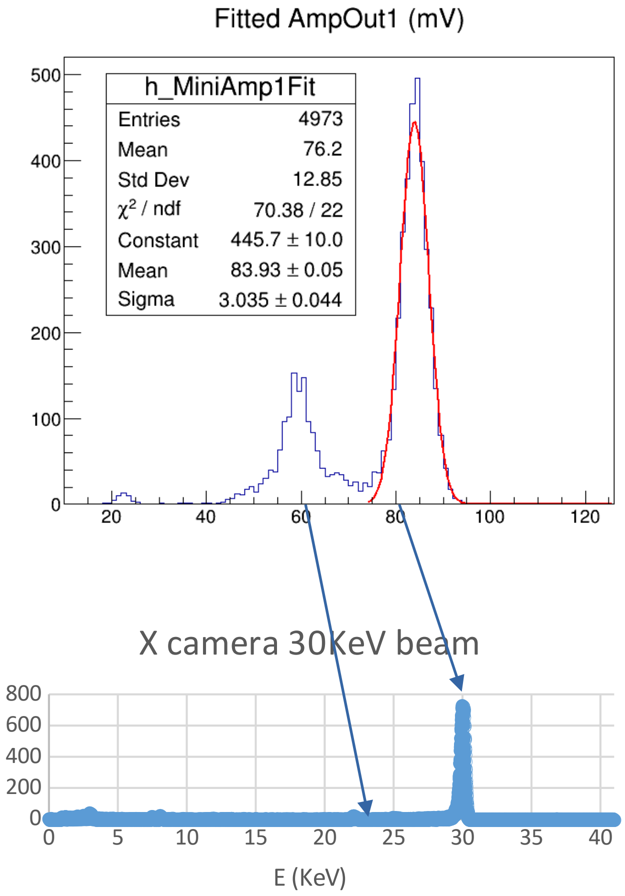
MiniCactus chip

Data acquired with LeCroy oscilloscope,
at 10 GSPS, 8 bits

Typical waveforms



Energy spectra at Soleil

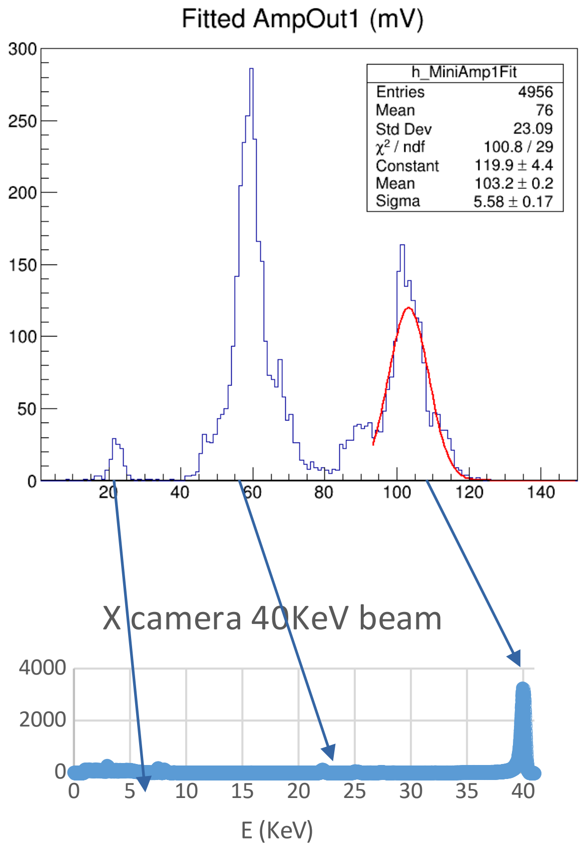


Parasitic energy peaks observed in MiniCactus

Their existence is confirmed by a dedicated camera installed
on the beam line

Most probably due to fluorescence
of PCB material (close to MiniCactus)

Camera sees different amplitude due
to solid angle effect

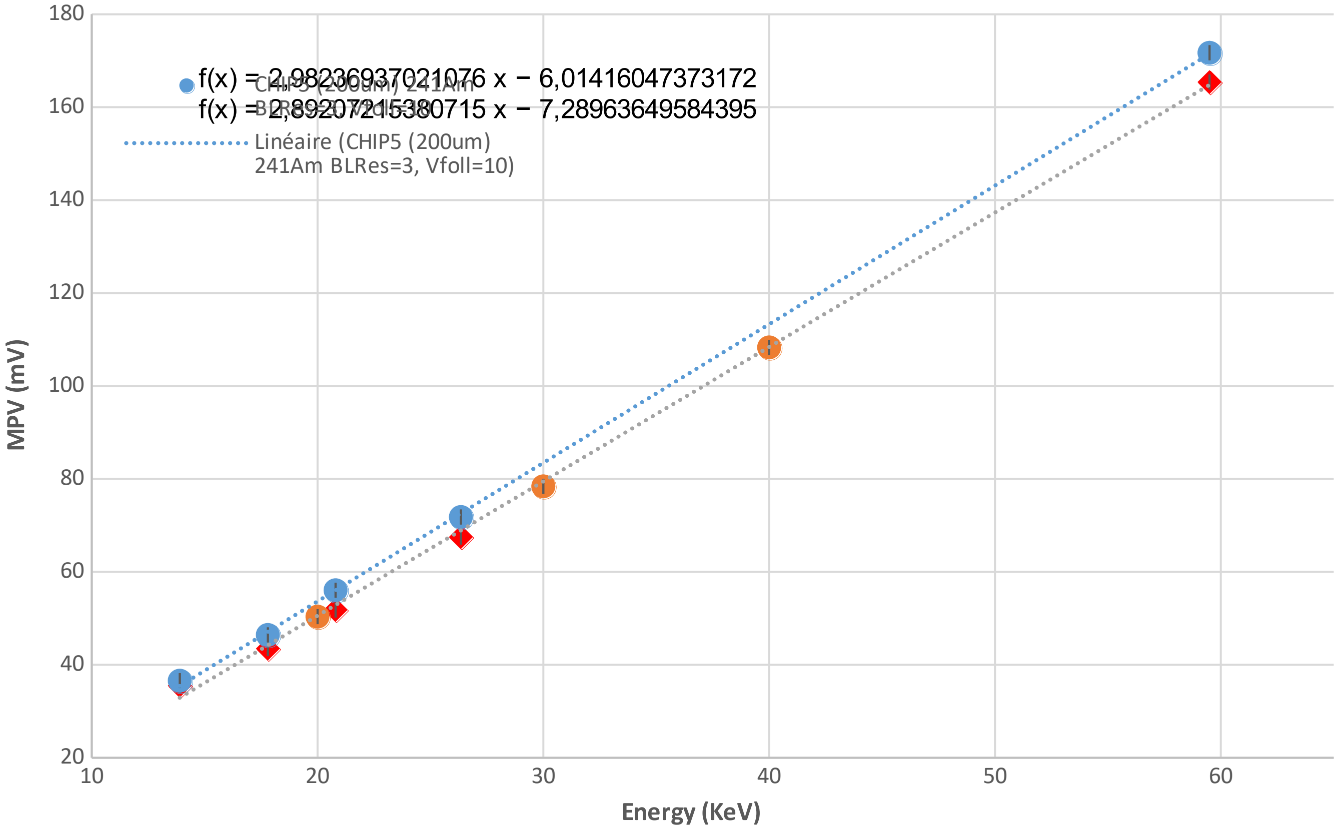


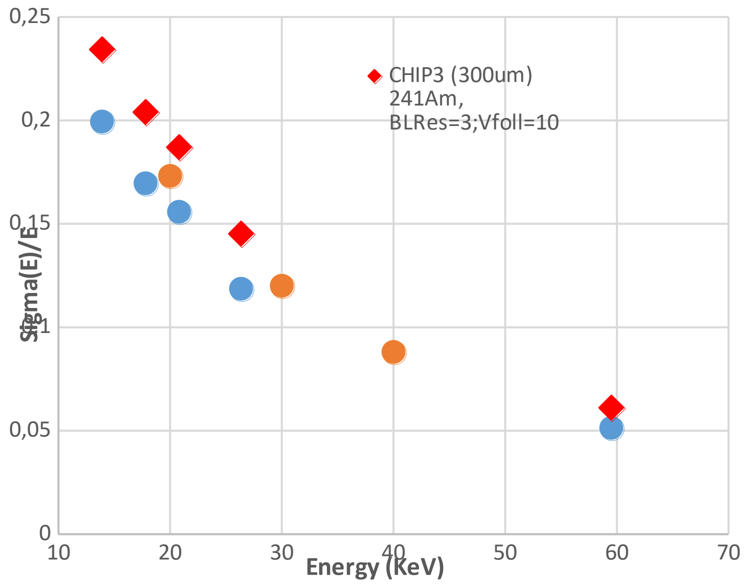
Calibration comparison between Soleil data and 241Am X-ray lines

200 μ chip, 241Am data (200 V), px 8

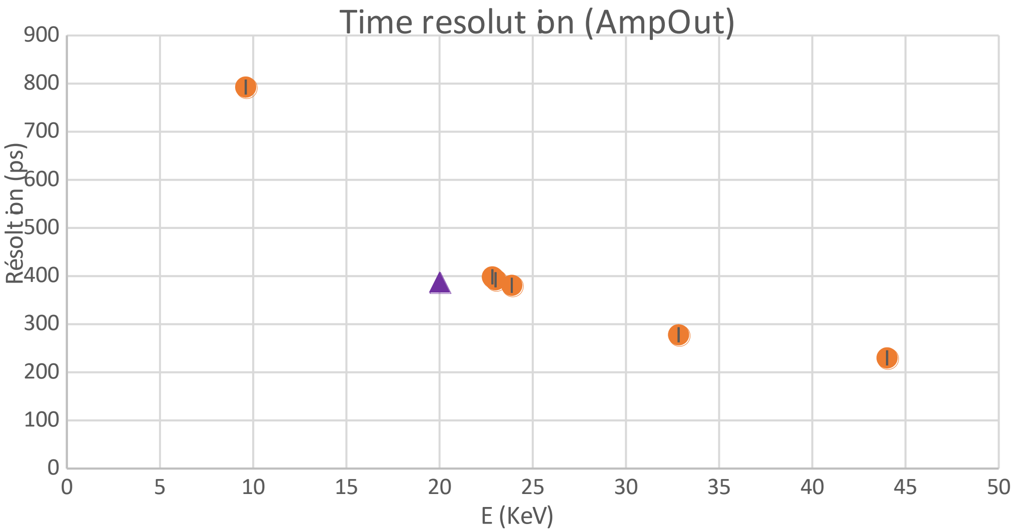
300 μ chip, Soleil data (400 V), px 8

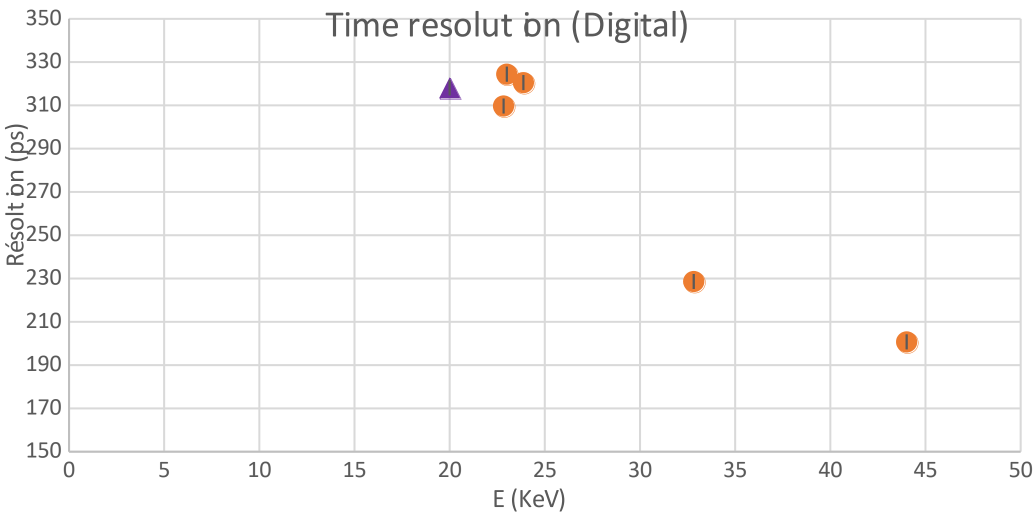
300 μ chip, 241Am (300 V)





Time resolution with photons





Time resolution worse for photons than for MIPs, at similar S/N

40 keV photon (≈200 ps) releases similar charge as a MIP (≈65 ps)

Interpreted as due to the different structure of energy deposits :

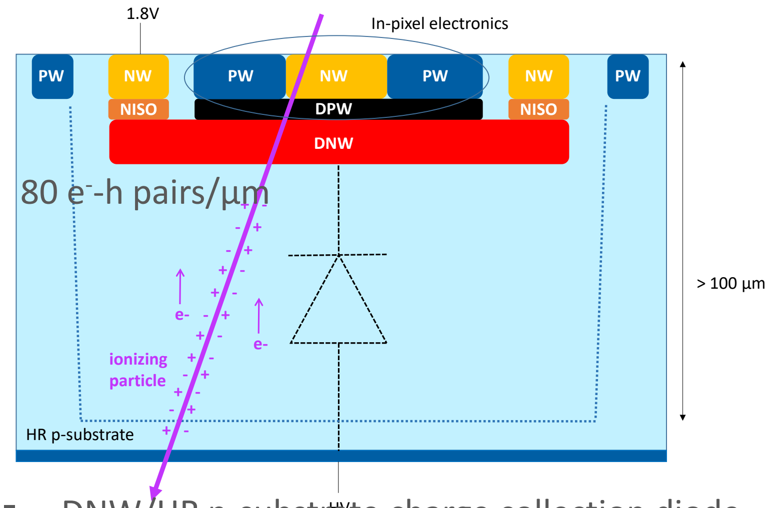
Pointlike for photons, along a line for MIPs

TIMING WITH HV-CMOS/DMAPS*

*Depleted MAPS

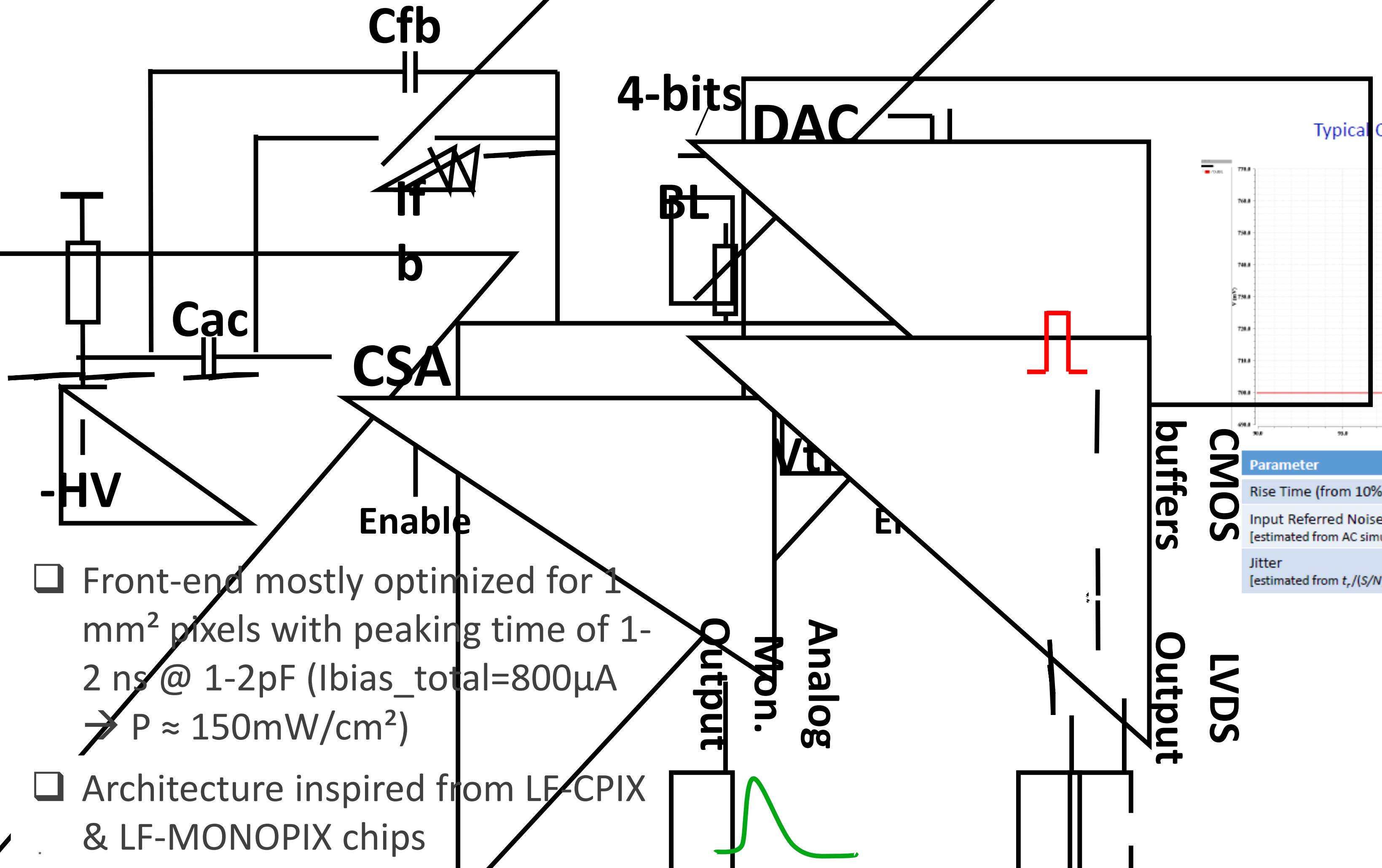
- The objective of our R&D is the development of a **monolithic timing sensor** in a **commercial HV-CMOS process** for future high energy physics experiments or for LHC upgrades (timing detectors, after phase 2 upgrades)
- **LFoundry 150 nm** HV-CMOS is one of the CMOS processes studied extensively for the CMOS option of the ATLAS Inner Tracker Upgrade
- Several large size demonstrators already designed and tested for tracking applications (**LF-CPIX**, **LF-MONOPIX1**, **LF-MONOPIX2**) in this process with proven **radiation hardness** (Bonn, IRFU and CPPM coll.)

HV-CMOS Sensor Pixel

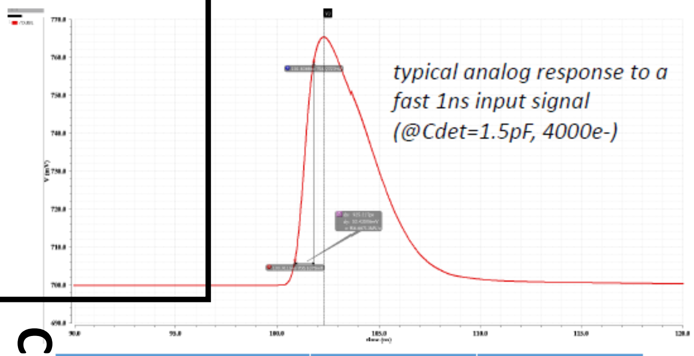


- DNW/HR p-substrate charge collection diode
- HV (≥ 300 V) applied on the substrate (from top or back)
- Large depletion depth (≥ 300 µm)
- **Charge collection by drift (fast)**
- **No internal amplification**
- Electronics can be integrated inside charge collection diode

ON-CHIP FRONT-END



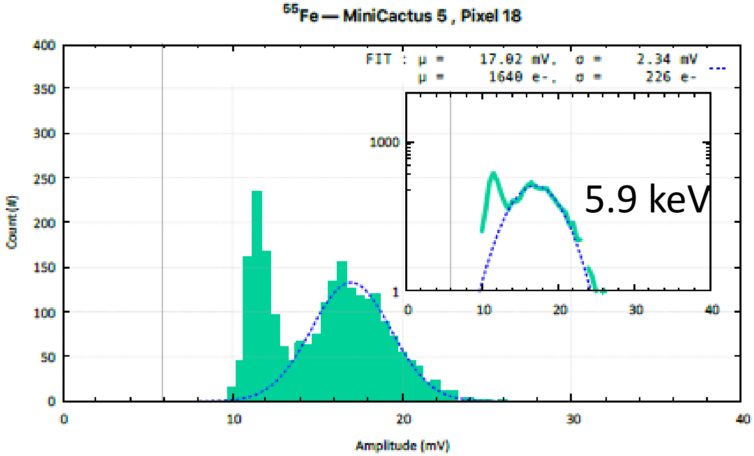
Typical CSA transient simulation result

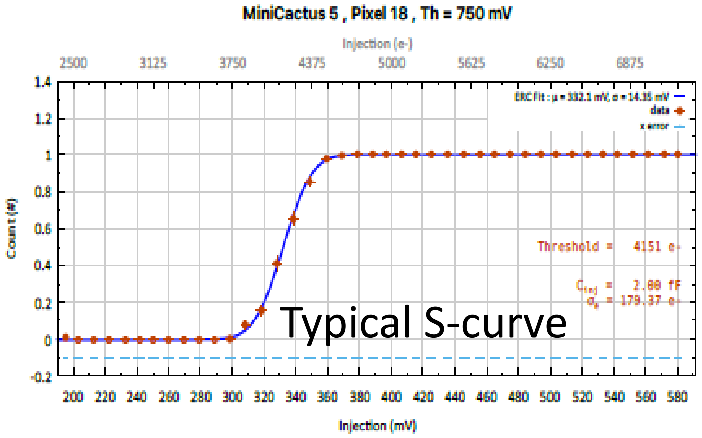


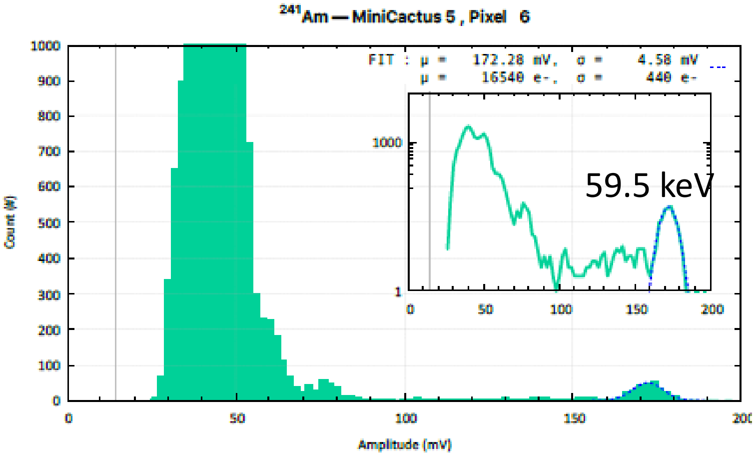
Parameter	1.5 pF	1 pF
Rise Time (from 10% to 90%)	~ 0.9 ns	~ 0.8 ns
Input Referred Noise [estimated from AC simulations]	~ 290 e-	~ 220 e-
Jitter [estimated from t_r/(S/N)]	~ 67 ps	~ 44 ps

- Front-end mostly optimized for 1 mm² pixels with peaking time of 1-2 ns @ 1-2pF (Ibias_total=800µA → P ≈ 150mW/cm²)
- Architecture inspired from LF-CPIX & LF-MONOPIX chips

IN-LAB TESTS (injection pulse, Gamma-ray sources)

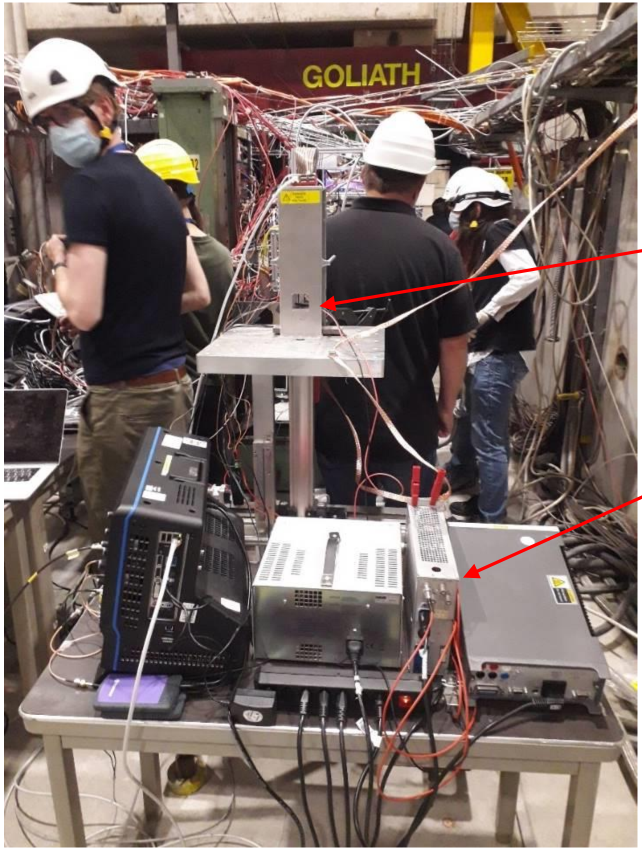






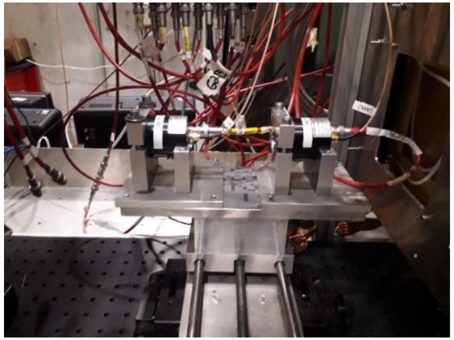
- → Best S/N observed on pixel 8 (0.5mm²) among large pixels
- → Noise$_t$:
  179.4e- (chip#5_200µm)
  155.9e- (chip#8_100µm)

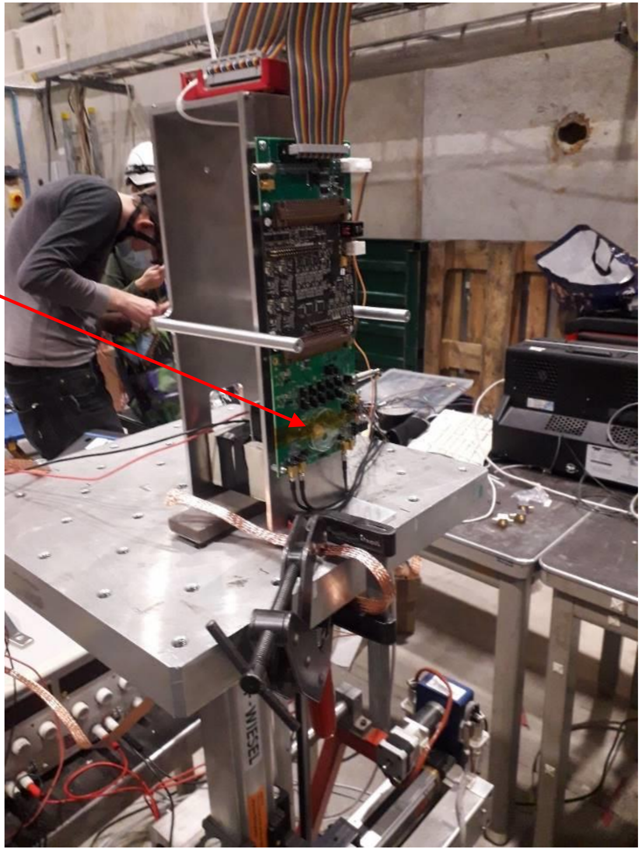
TESTBENCH OF MINICACTUS IN TESTBEAM



MiniCACTUS

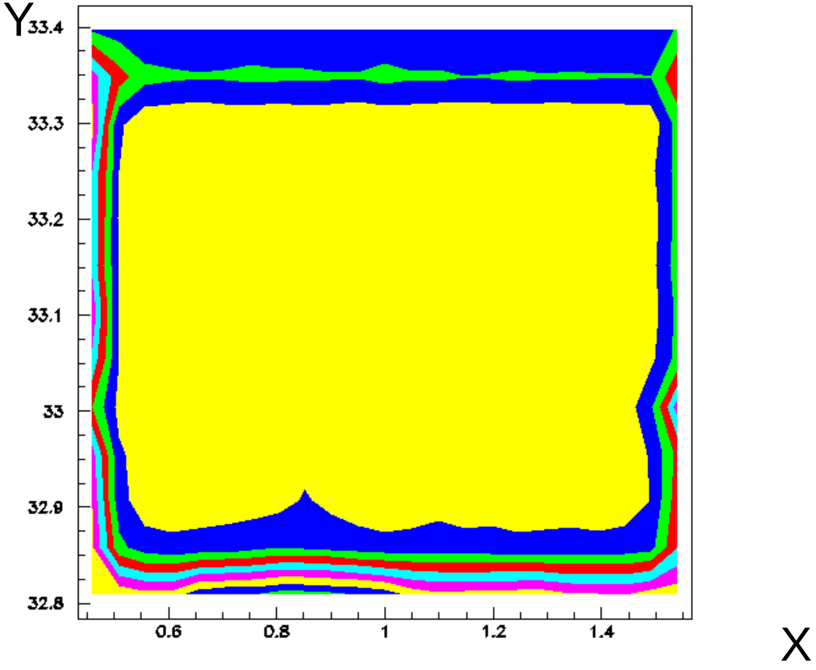
Power Supplies
(LV and HV)



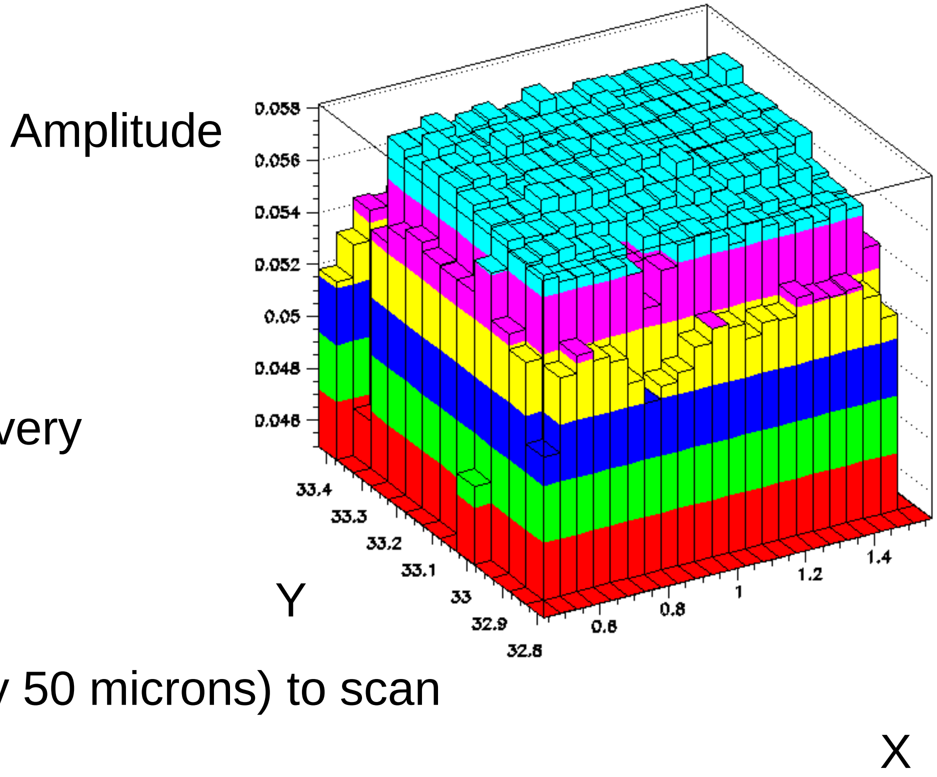


Time reference
RD-51 MCPs (resolution < 10 ps)

Pixel position scan at 20 keV with photons (data taken at Synchrotron Soleil)



Pixel has very good uniformity



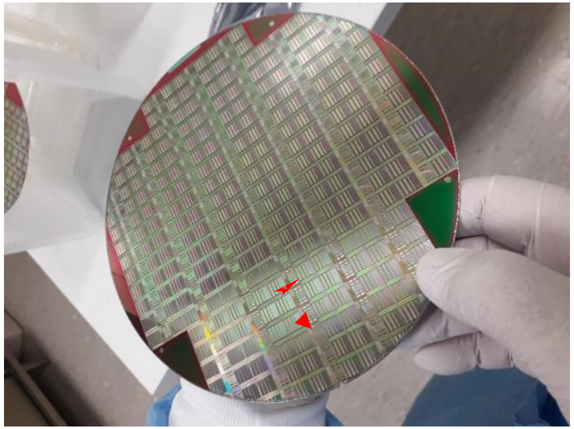
Used a pencil beam (50 microns by 50 microns) to scan pixel surface

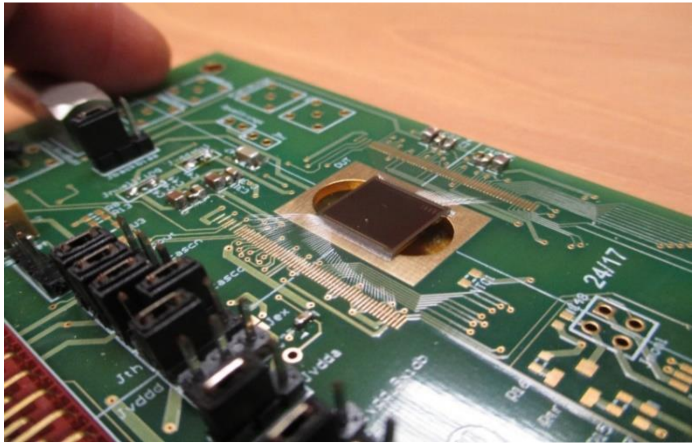
No non-uniformity found

CACTUS* DEVELOPMENT

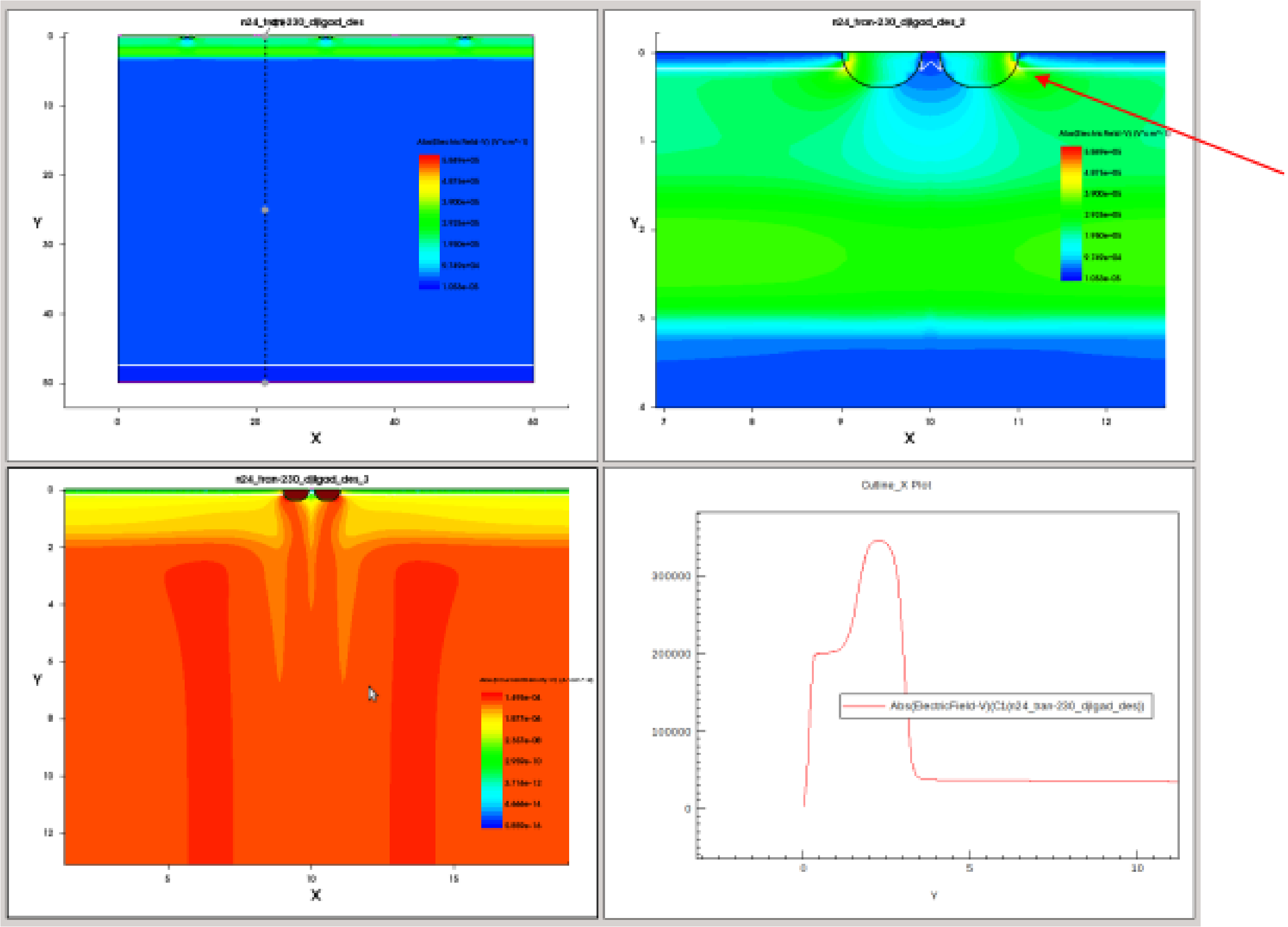
*__CMOS AC__tive __T__iming __µS__ensor

- The first demonstrator called **CACTUS** for timing in LF 150 nm process designed in 2019
- The front-end in CACTUS is based on an **in-pixel fast preamplifier** followed by a **leading edge discriminator**
- Time walk corrections done off-line by **ToT measurement**
- Expected timing resolution from Cadence & TCAD simulations: 50-100 ps





The CACTUS demonstrator on PCB
(chip size : 1 cm x 1 cm)



- But heterogeneous electric field in amplification/drift region with “hot” areas at pixel perimeters → issue