EICROC and HGCROC/CALOROC status and plans

Scientific Council IN2P3
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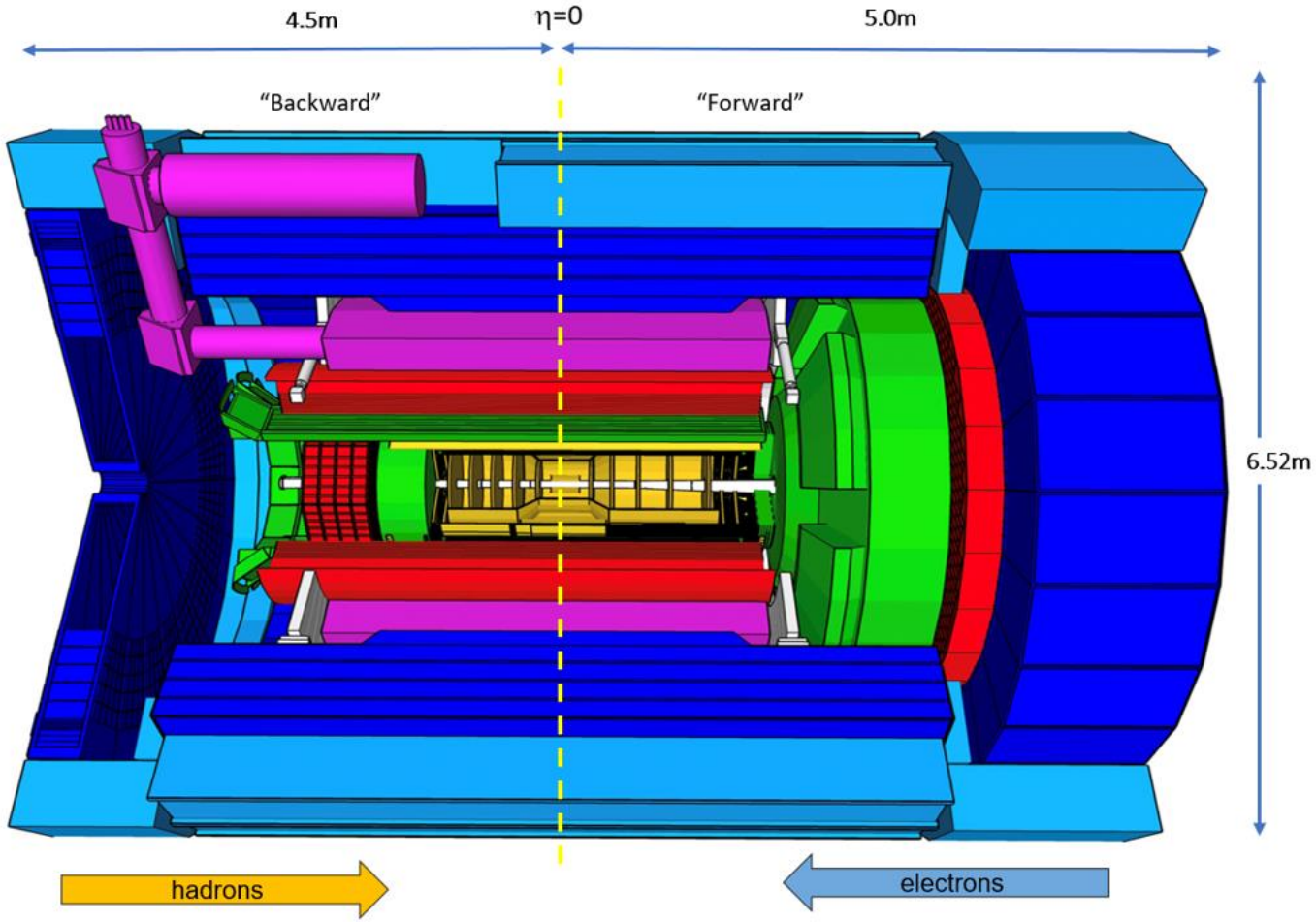
Organization for Micro-Electronics desiGn and Applications

OMEGA chips for EIC

- HGCROC and EICROC considered for EIC calorimetry and AC-LGAD readout
  - Officially IN2P3 groups participate to Backward ECAL and roman pots but other detectors are also interested in theses chips

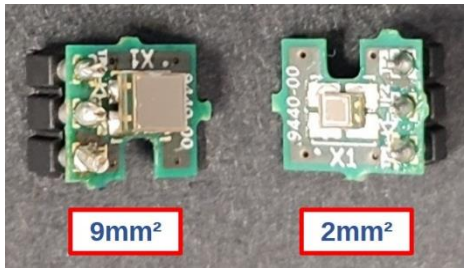


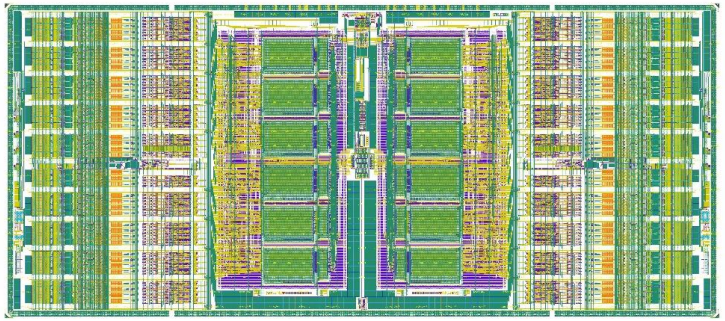
Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
racking	32 B			100k
alorimeters	50M		67k	
ar Forward	300M	2.3M	500	
ar Backward		1.8M	700	
ID		3M-50M	600k	
OTAL	32 B	7.1M-54M	670k	100k
SIC	ITS-3	EICROC FCFD HPsOC ASROC FAST	Discrete/COTS HGCROC3 ALCOR-EIC	SALSA

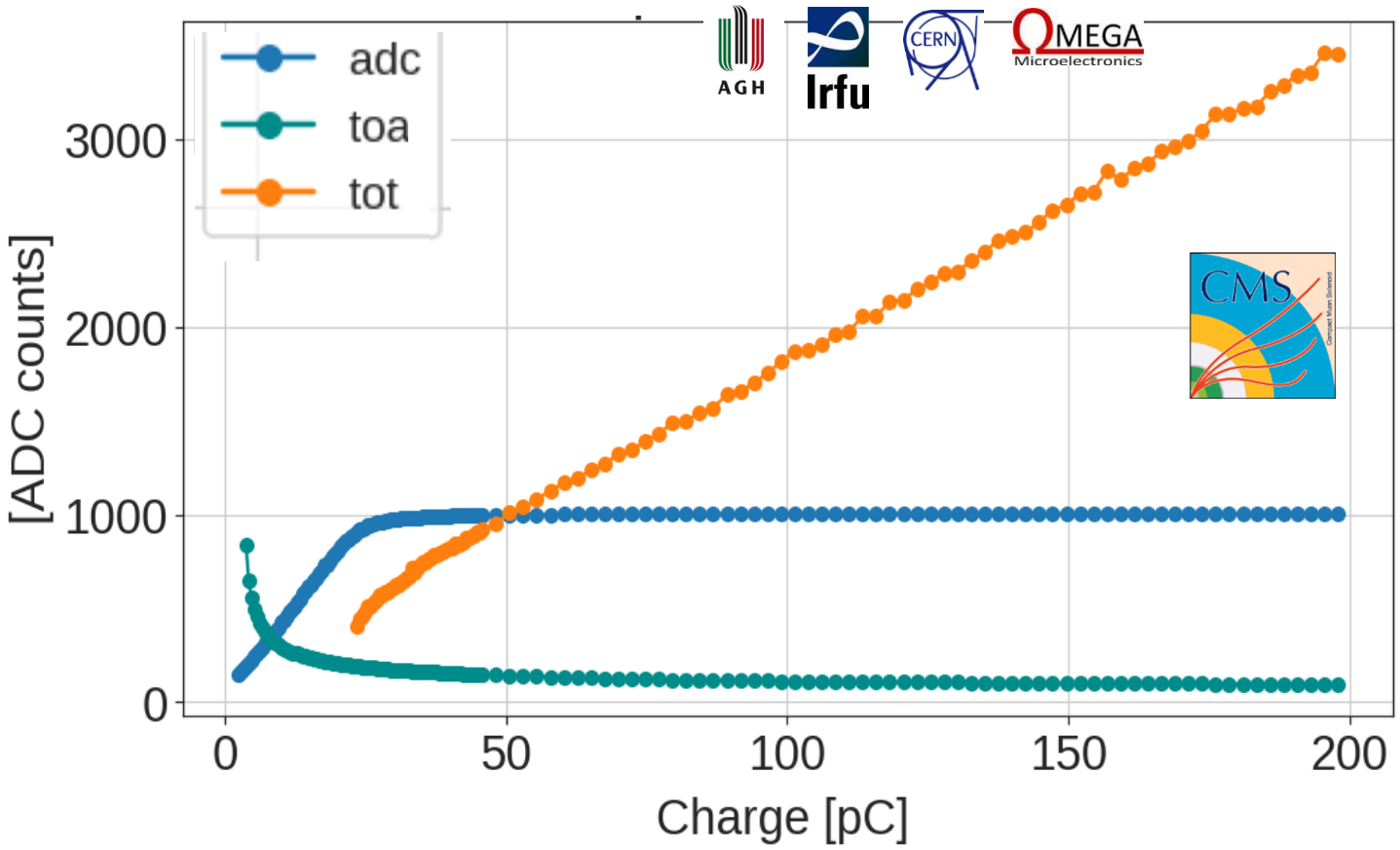
Calorimetry : SiPM readout experience from CMS (H2GCROC)

- H2GCROC developed for CMS HGCAL is a good candidate to provide charge and time on a large dynamic range

- H2GCROC provides 72 channels with (see backup)
  - Charge measurement from 30 fC (noise) to 300 pC (MIP ~0.5 pC)
  - ToA measurement down to 15 ps
  - Optimized for Cd=500 pF
  - 15 mW/ch. Radiation hard, TMR.

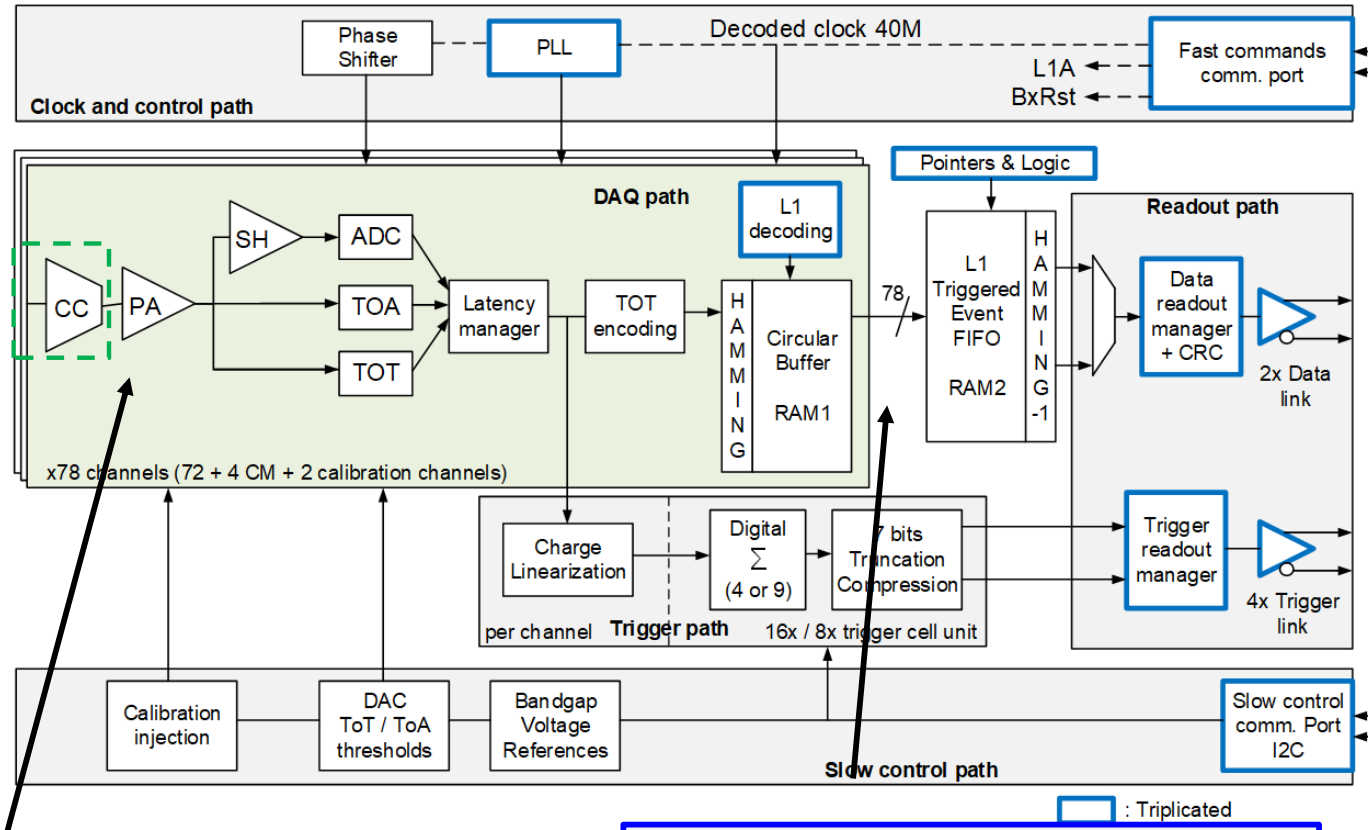






H(2)GCROC : LHC specific

- HGCROC is designed for LHC : needs a LVL1 trigger



Dedicated fast command interface : calibration pulses, external L1 trigger.

Data and trigger serial links with CLPS signaling (LpGBT @ 1,28 Gbps)

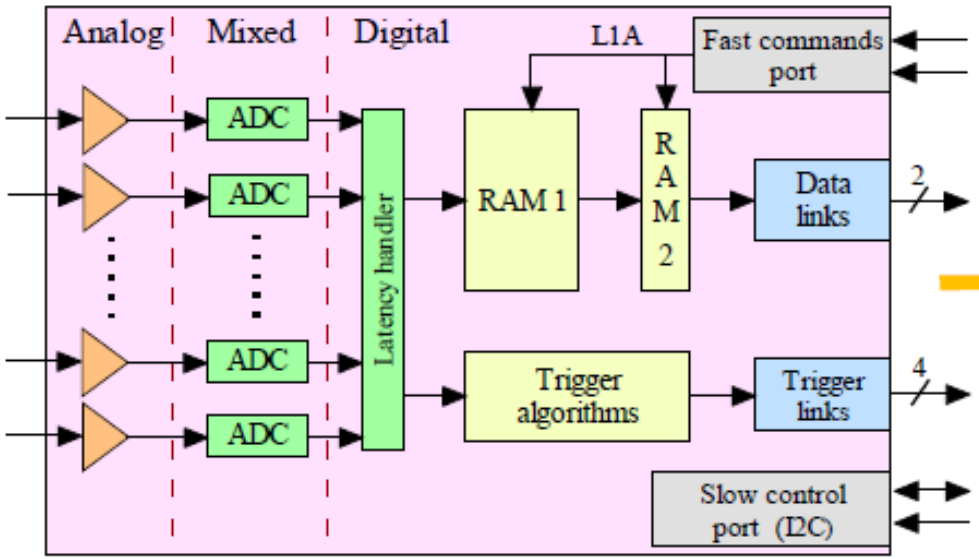
I2C interface to load the ASIC parameters (slow control interface)

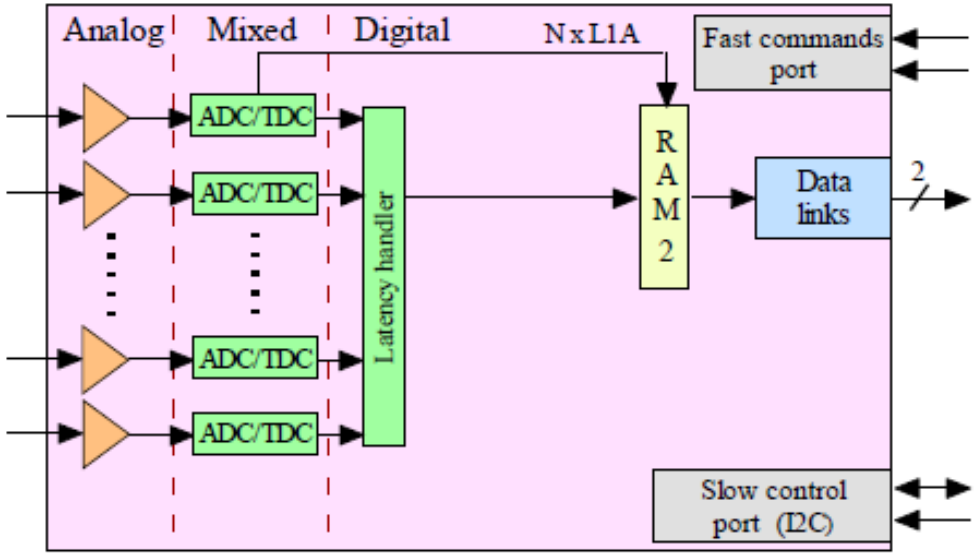
Analog front-end specific to sensor

LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

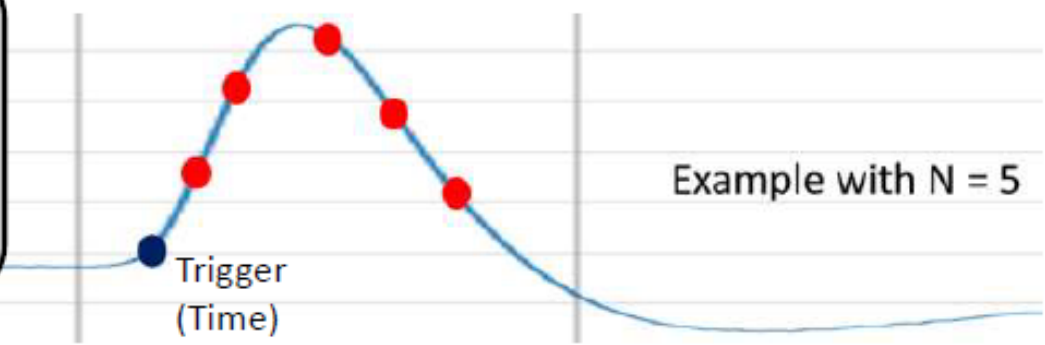
Evolution for EIC readout : CALOROC

- No more LVL1 : data streaming => auto-trigger and zero-suppress
  - Also very interesting for future DRD6 readout ASICs !



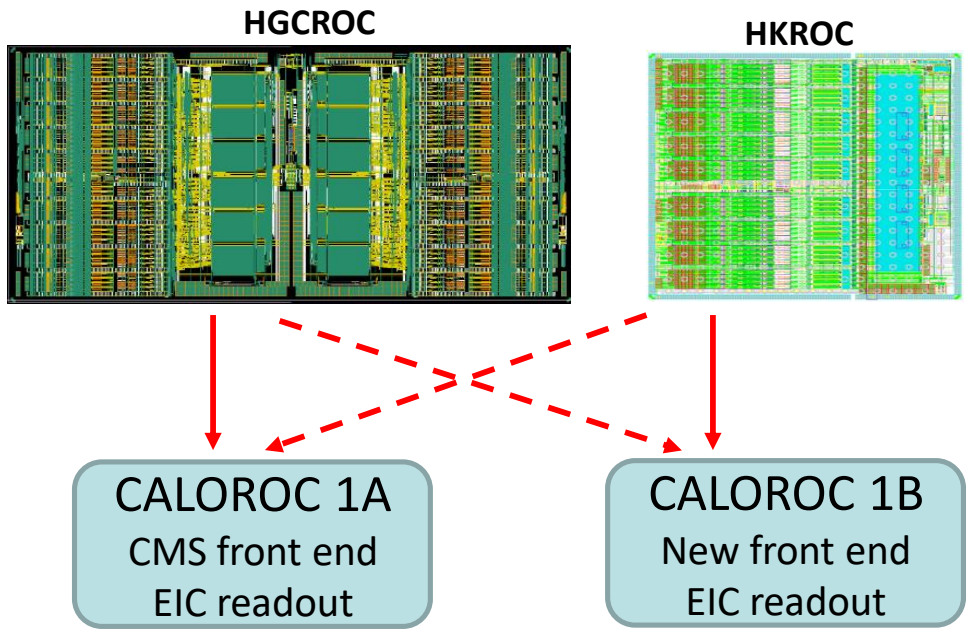


- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)



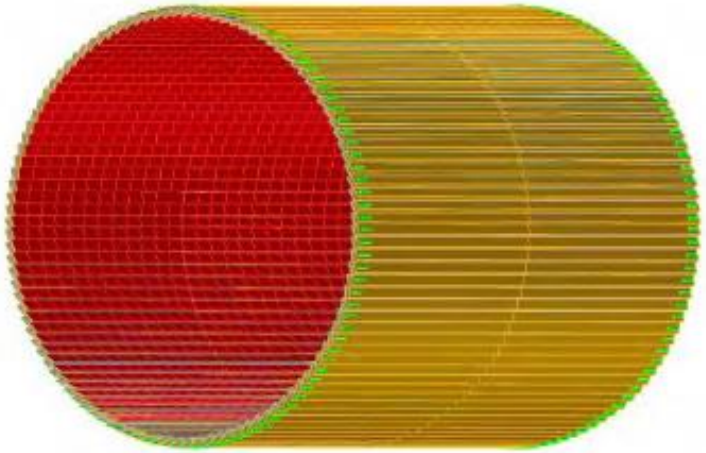
CALOROC1A/1B development plan

- CALOROC1A is H2GCROC with EIC readout (conservative)
  - Same analog front-end but new digital backend
  - Auto-trigger/zero-suppress : already exercised in HKROC (see backup)
  - ~~New 100 MHz EIC clock and fast commands~~ : moved to DAQ, remains 40 MHz chip
- CALOROC1B is CALOROC1A with a new analog front end (innovative see backup)
  - Better signal to noise ratio (no current conveyor)
  - No ToT : dynamic gain switching
  - Pin-to-pin compatible
- Both chips also provide useful R&D for DRD6

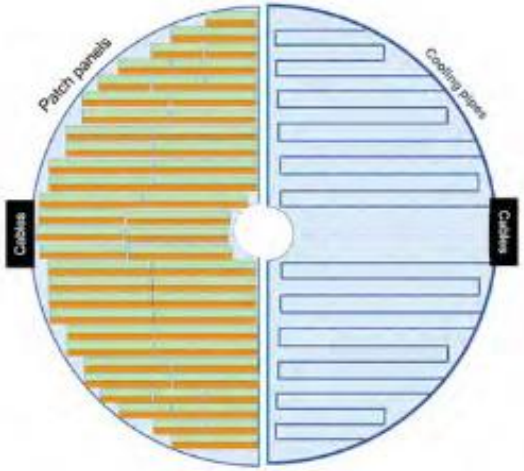


Specifications of ePIC AC-LGAD detectors:

BToF



FToF



Roman Pots

4D Trackers

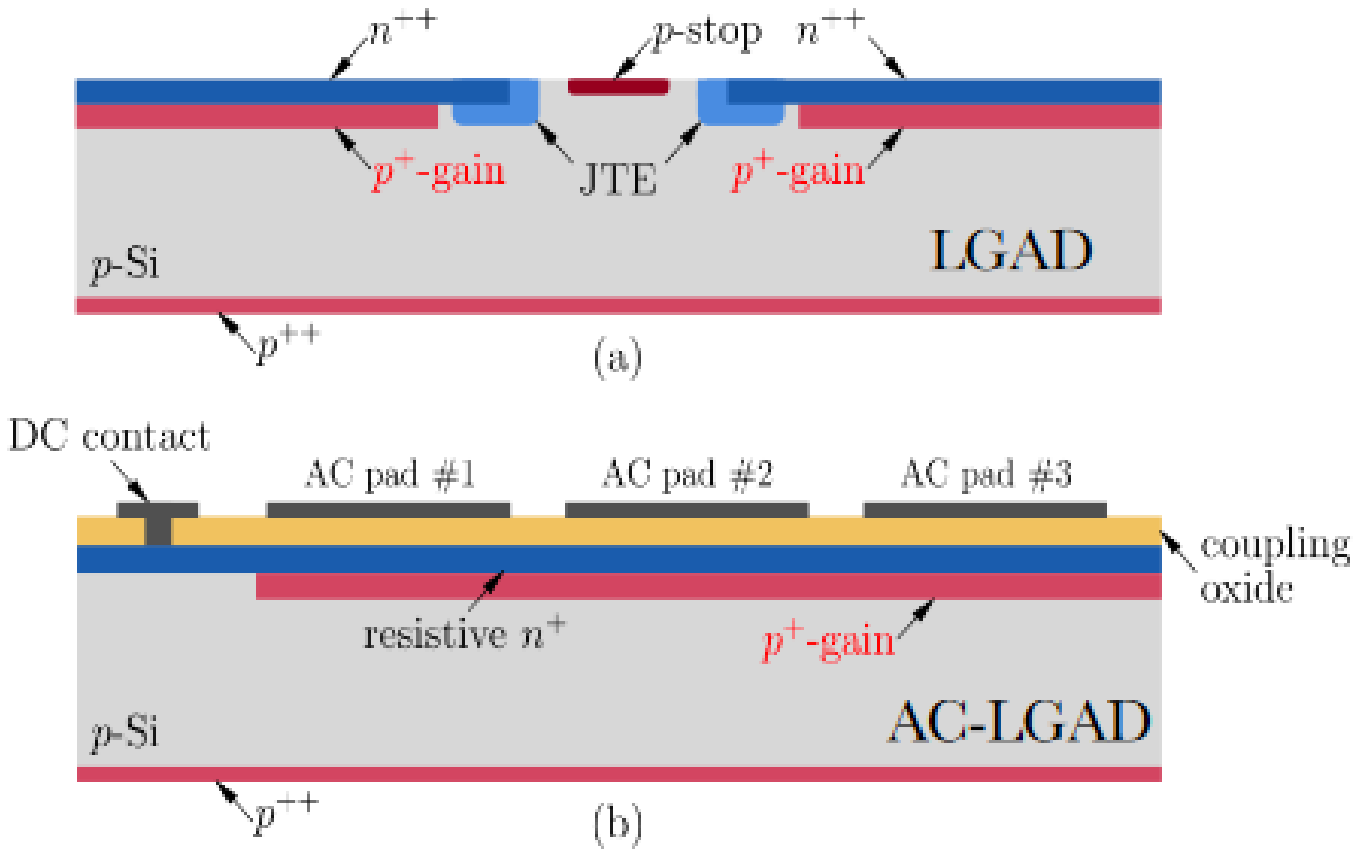
	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10.9	0.5*10 (strips)	2.4M	30 ps	30 μm in φ	0.01 X0
Forward TOF	2.22	0.5*0.5 (pixels)	8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5 (pixels)	0.28M	30 ps	20 μm in x and y	0.05 X0
RPs/OMD	0.14/0.08	0.5*0.5 (pixels)	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

DC LGAD and AC LGAD

From S. Nanda : https://indico.cern.ch/event/1232761/contributions/5321425/

- MIP timing detectors (HGTD, ETL) use DC LGAD sensors
  - ~10 fC/MIP
  - Area : (1.3 mm)²
  - Good timing resolution : 30-50 ps
  - Poor position resolution : ~400 µm
  - « dead zone » between pixels

- AC LGADs for EIC
  - Resistive layer to get signal sharing
  - Area (500 µm)²
  - Good position resolution : < 50 µm
  - No dead area
  - Good timing resolution (as DC LGAD)

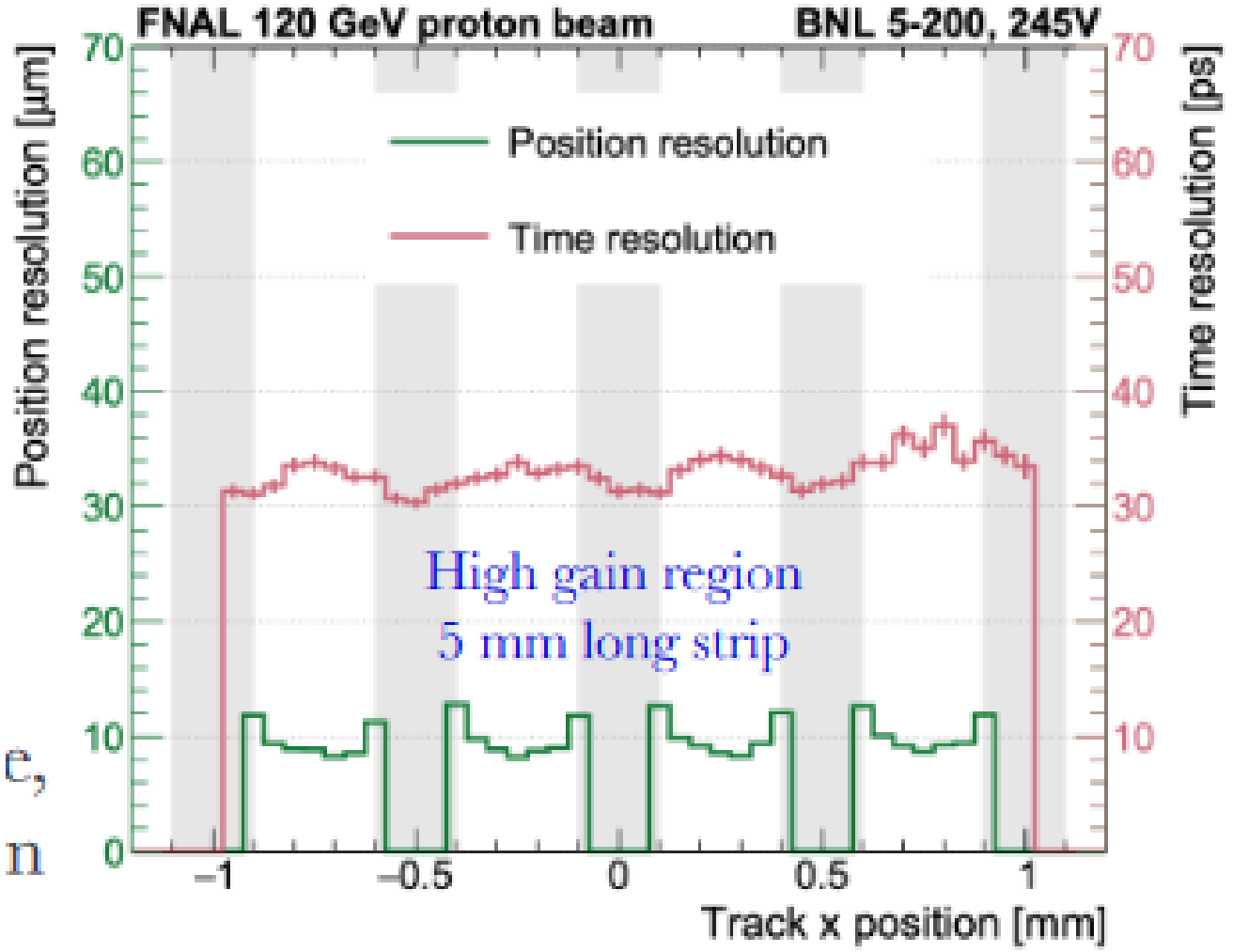


AC LGAD performance *[FNAL]*

From S. Nanda : https://indico.cern.ch/event/1232761/contributions/5321425/

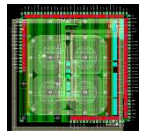
- Here for strips : 500 µm x 5 mm
  - ~30-35 ps timing resolution
  - ~10 µm position resolution
  - Oscilloscope readout
  - Still preliminary results and improvements underway on gain uniformity
  - Chosen as baseline for several EIC detectors

- New and promising detector



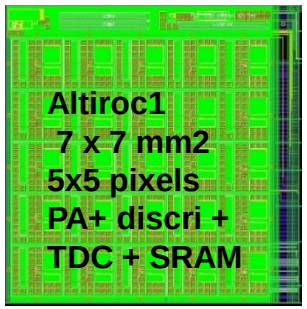
DC-LGAD readout : experience from ATLAS : ALTIROC

2016



Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

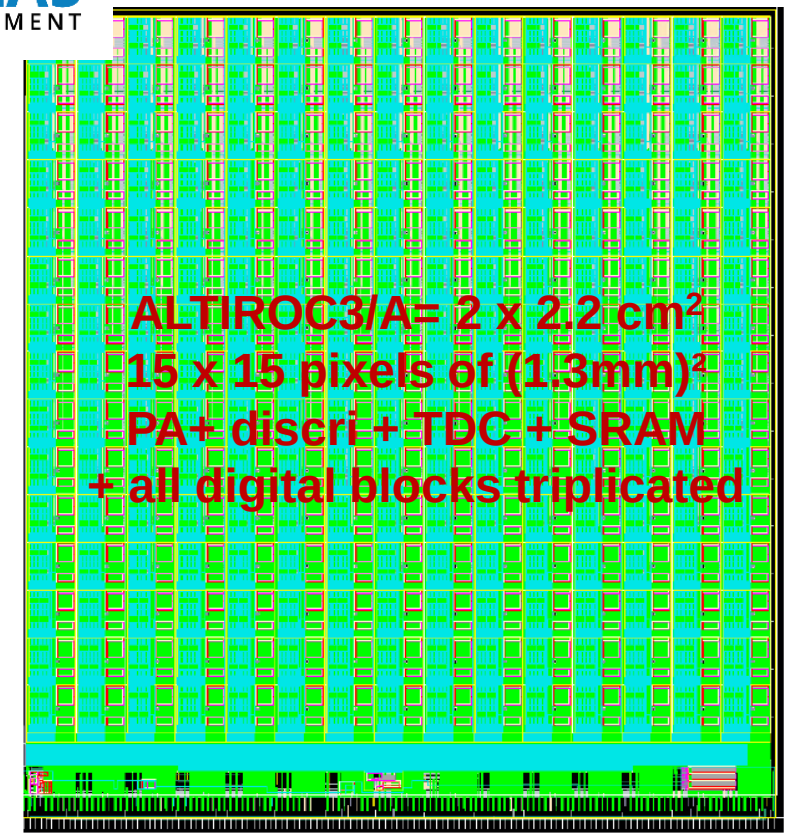
2017



Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

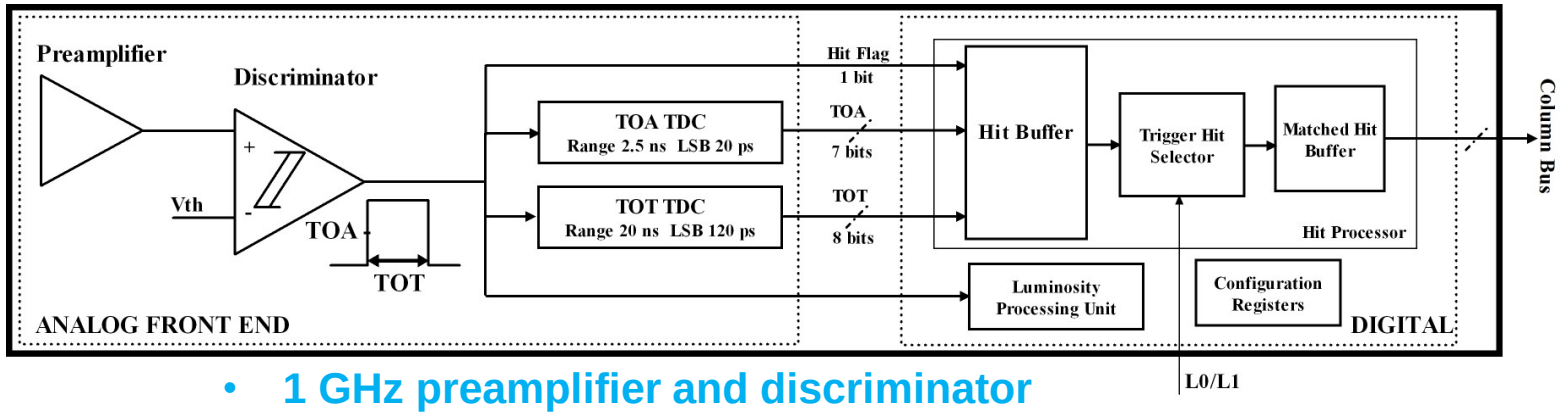
2019

2022

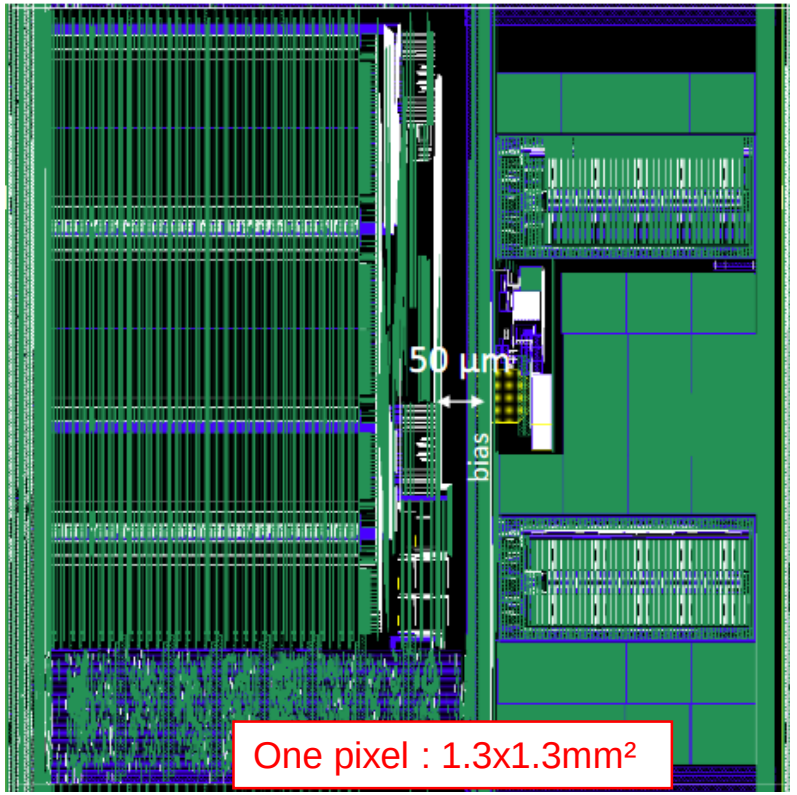


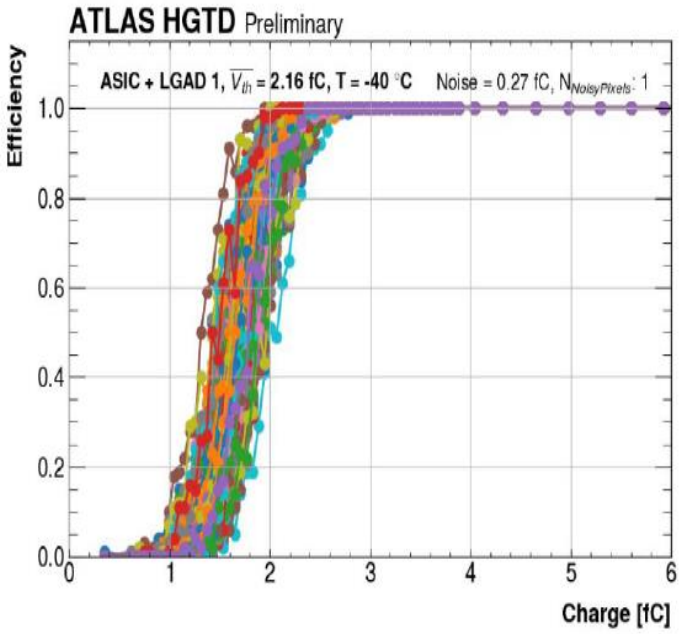
ALTIROC2/3/A: Digital on Top design

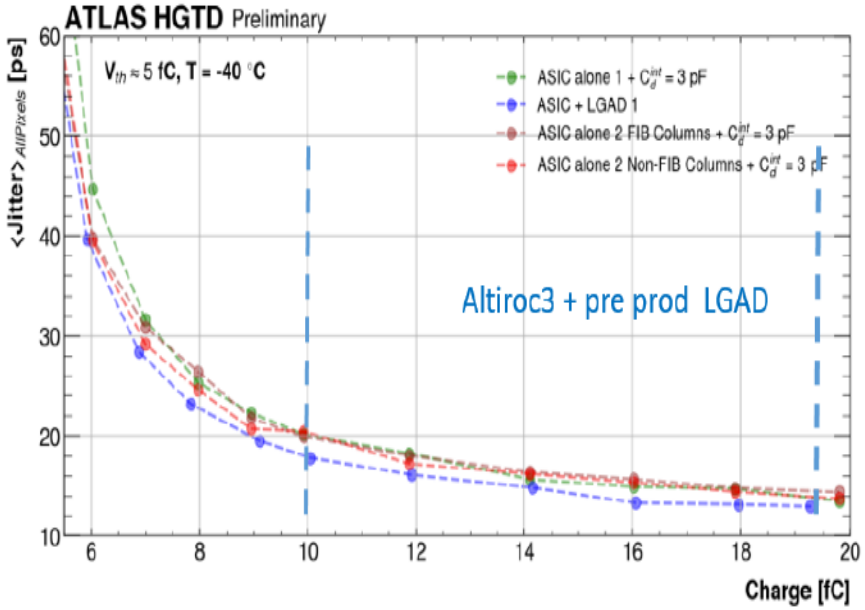
ALTIROC pixel scheme and layout



- **1 GHz preamplifier and discriminator**
- **2 vernier TDCs for ToA and ToT**
- **Hit buffer:** SRAM 1536 x 19 bit (38 µs latenccy)

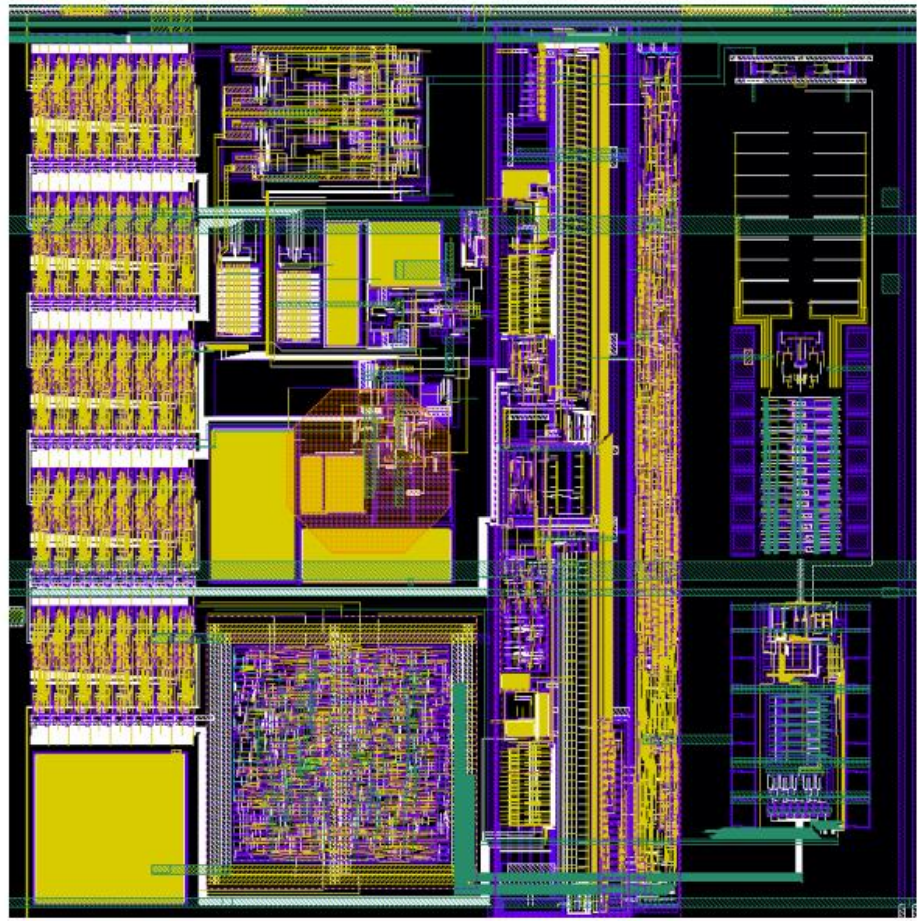


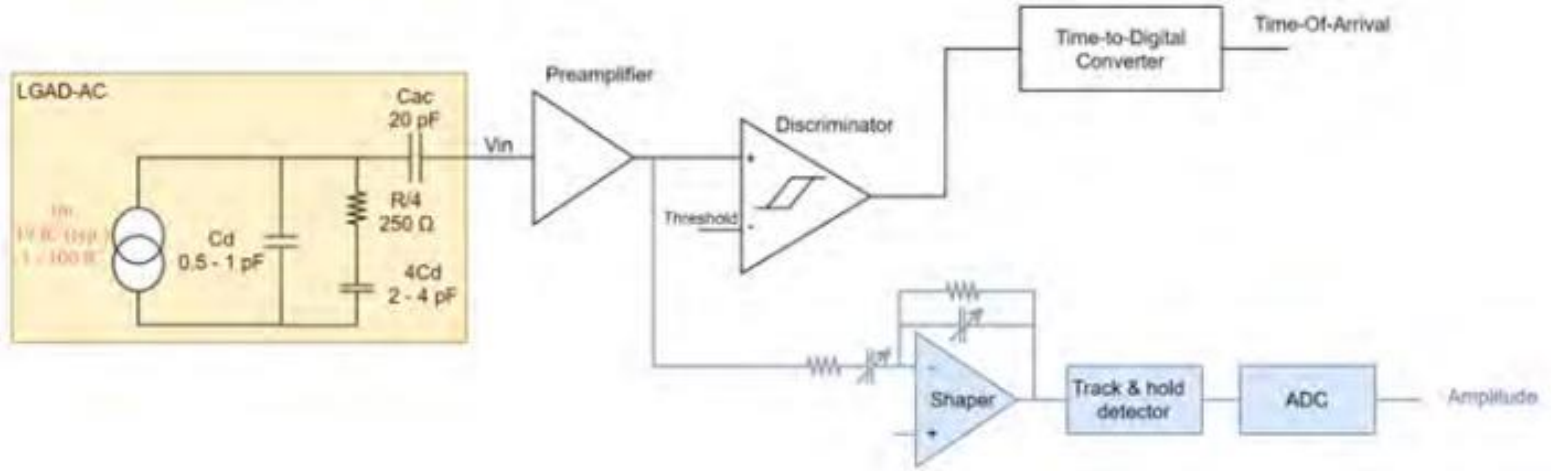




Adaptation to EIC : EICROC

- Shrink into 500x500 µm
- Analog frontend similar to ALTIROC
- Need ADC instead of ToT for charge measurement 8bit 40 MHz from AGH Krakow
- TDC taken from HGCROC by CEA Saclay
- I²C configuration
- Simple digital readout



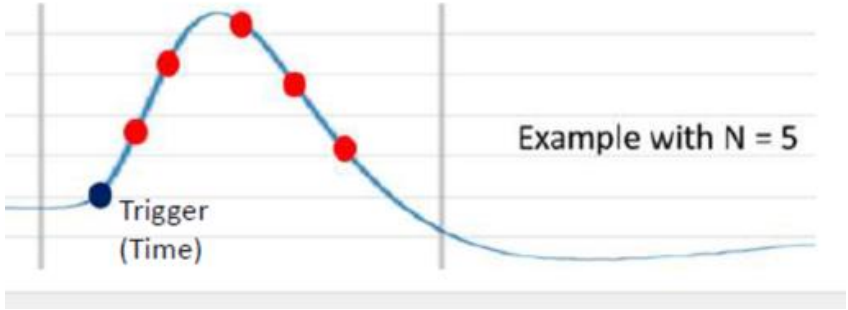


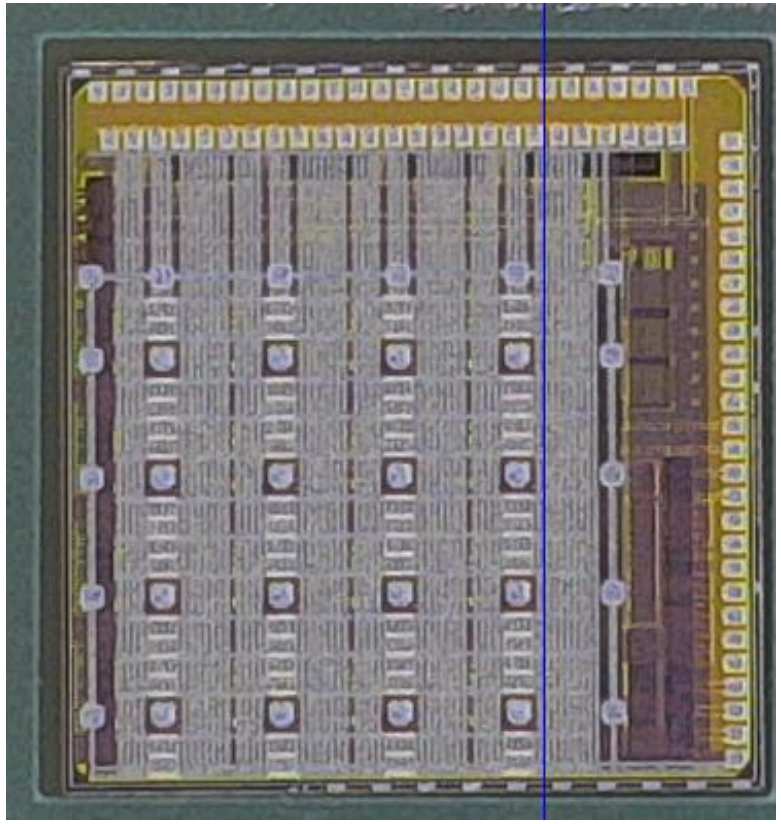
Slow control | PA +discri | TOA TDC | 8b 40M ADC

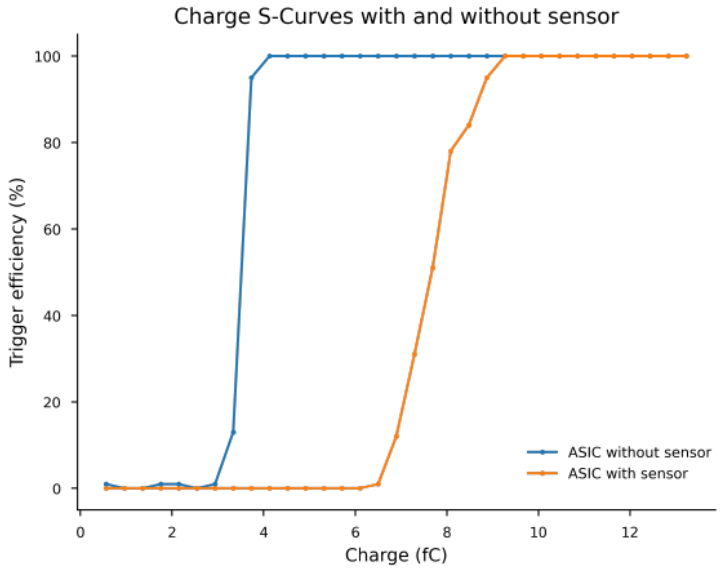
OMEGA Microelectronics | Irfu | AGH

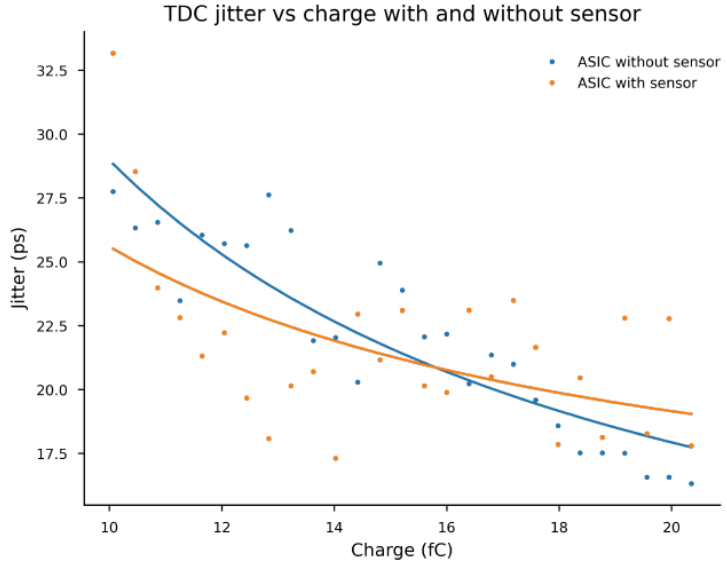
EICROC0 : 4x4 pixels

- EICROC0 : 4x4 test chip for (500µm)² pixels
  - Readout : TDC data and 8 ADC values
  - Performance : a few examples, more in backup







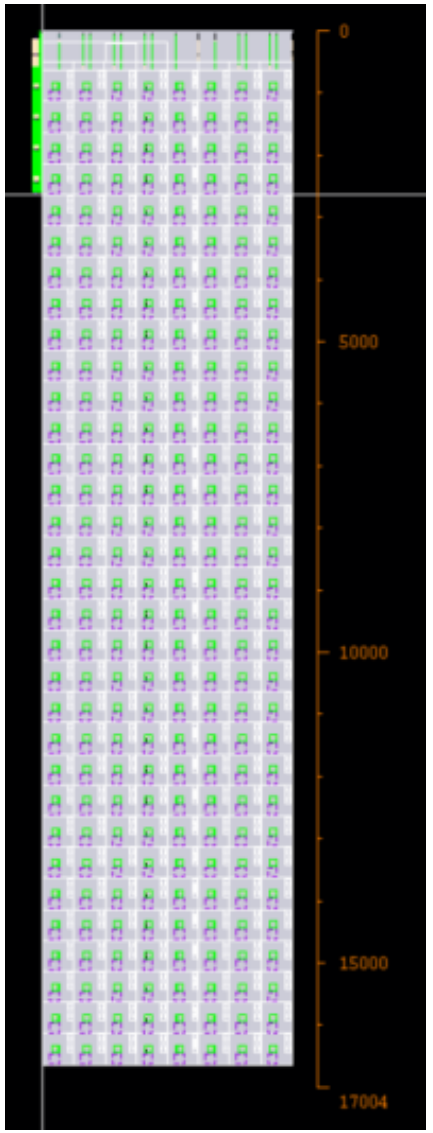


Next steps : EICROC1 8x32 or 32x32

- EICROC1 : 8x32 = 256 pixels or 32x32 = 1024
  - Layout complete. DRC/LVS OK
  - Still EICROC0 digital architecture and Readout
  - 2/8 data outputs : 1 for 128 pixels (4x32)
  - Looking to increase R/O speed. Possibility to skip pixels by SC
  - Looking to improve testability.
  - Verifications in progress (~2 months)
  - 32x32 would allow tests with final sensor

- EICROC1 addresses floorplan issues
  - Power drops along column, threshold uniformity
  - TDC uniformity and dependance on number of channels triggering

- Variants of EICROC0 will also be submitted
  - Lower power in the ADC branch (100 µW)

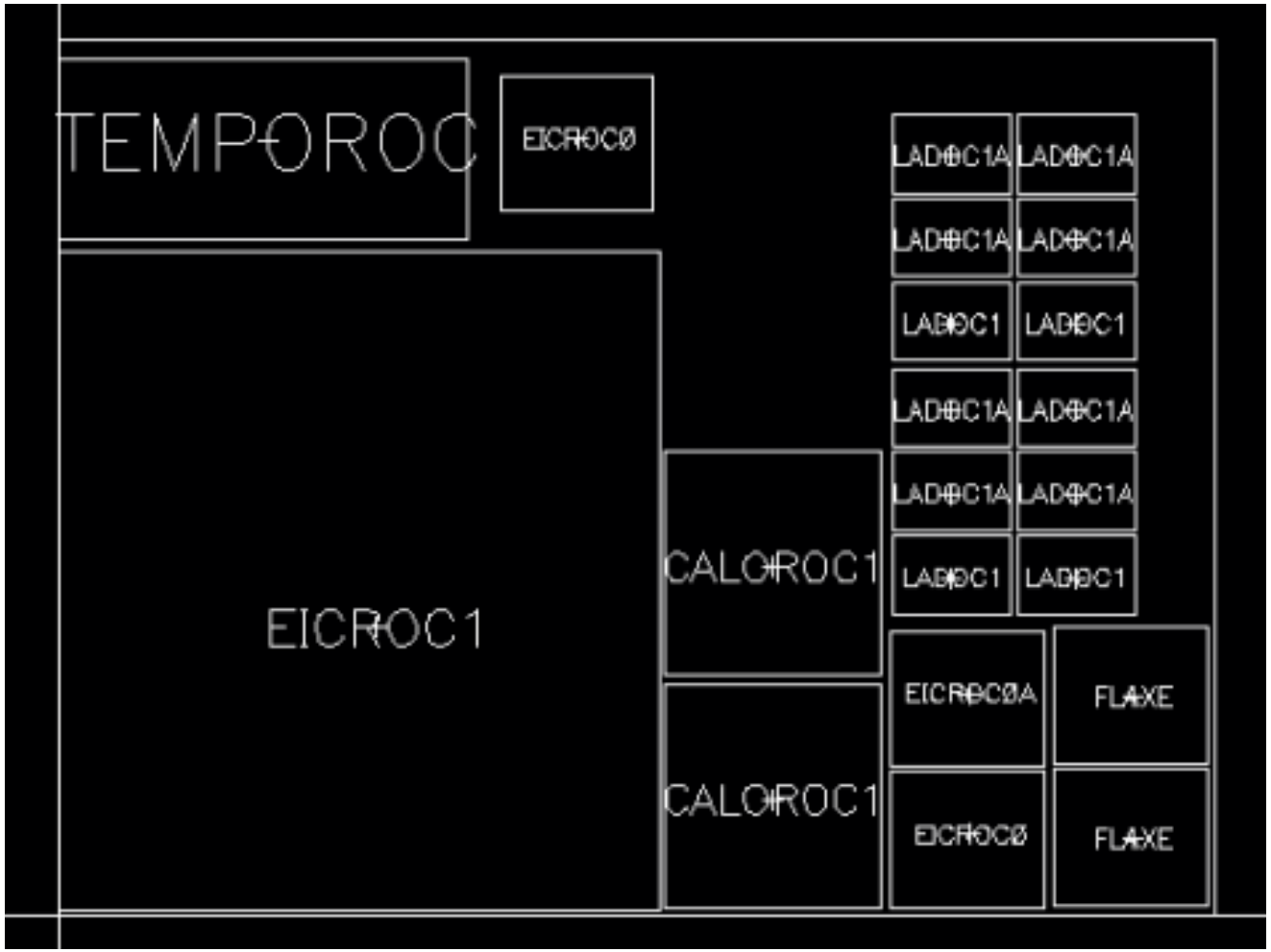


EIC reticle 2024

- TSMC now requires to fully populate the reticle of 24x32
  - Cost ~300 k€

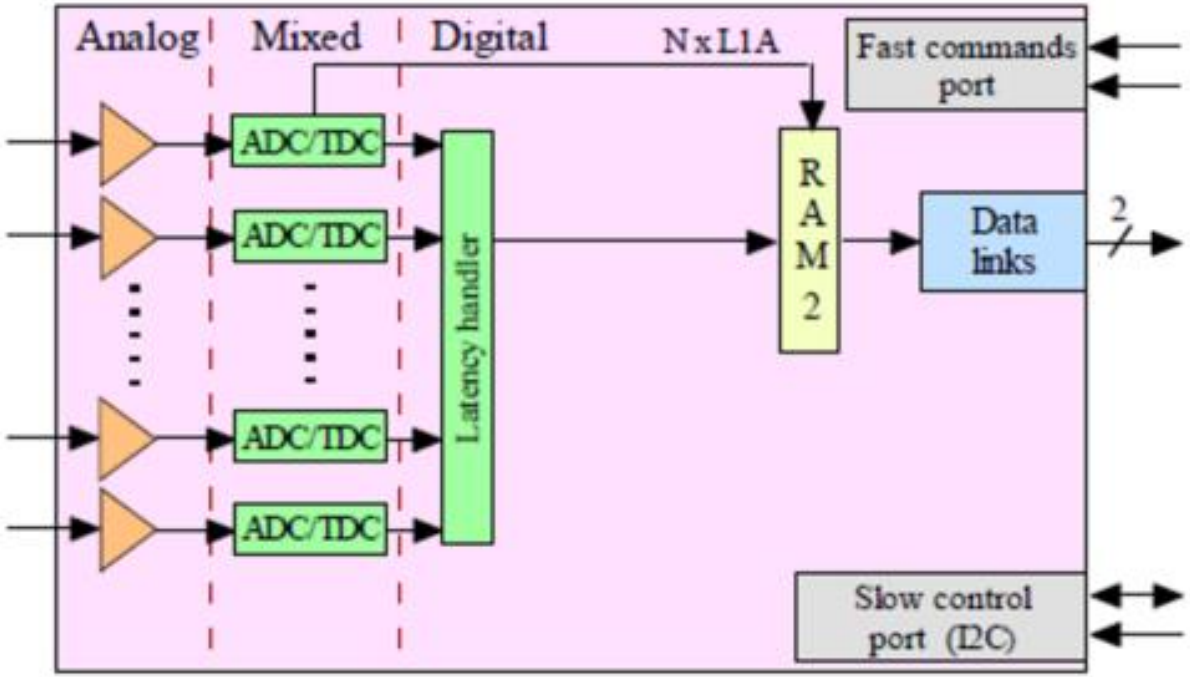
- For EIC we would have
  - EICROC1
  - 2 or 3 EICROC0/A/B
  - 2 CALOROC1A/1B
  - ~60% of reticle area

- Possible additionnal partners
  - ~20% of reticle area
  - Still space available (if ready in time !)



EICROC2 : 32x32 with EIC backend

- EICROC2 needs to address EIC digital architecture
  - Auto-trigger
  - Data driven zero-suppressed readout
  - Only readout hit channels and neighbours
  - Will depend a lot on the (low?) occupancy
  - Triplication and SEE tolerance
  - ~~200 MHz clock and fast commands~~



- Several EIC functions will be tested in CALOROC
  - Sparsified readout
  - Output links 160-1280 Mb/s

- Possible submission mid-2026

Comparison EICROC / HGCROC

EICROC

- « 2D chip » 16 -> 1024 channels
- Input capacitance : Cd = 1-5 pF
- Dynamic range : 1 fC – 50 fC
- ToA and ADC
- Target power : 1 mW/ch
- Area 10 mm² (300 mm² final)

- Target DoT

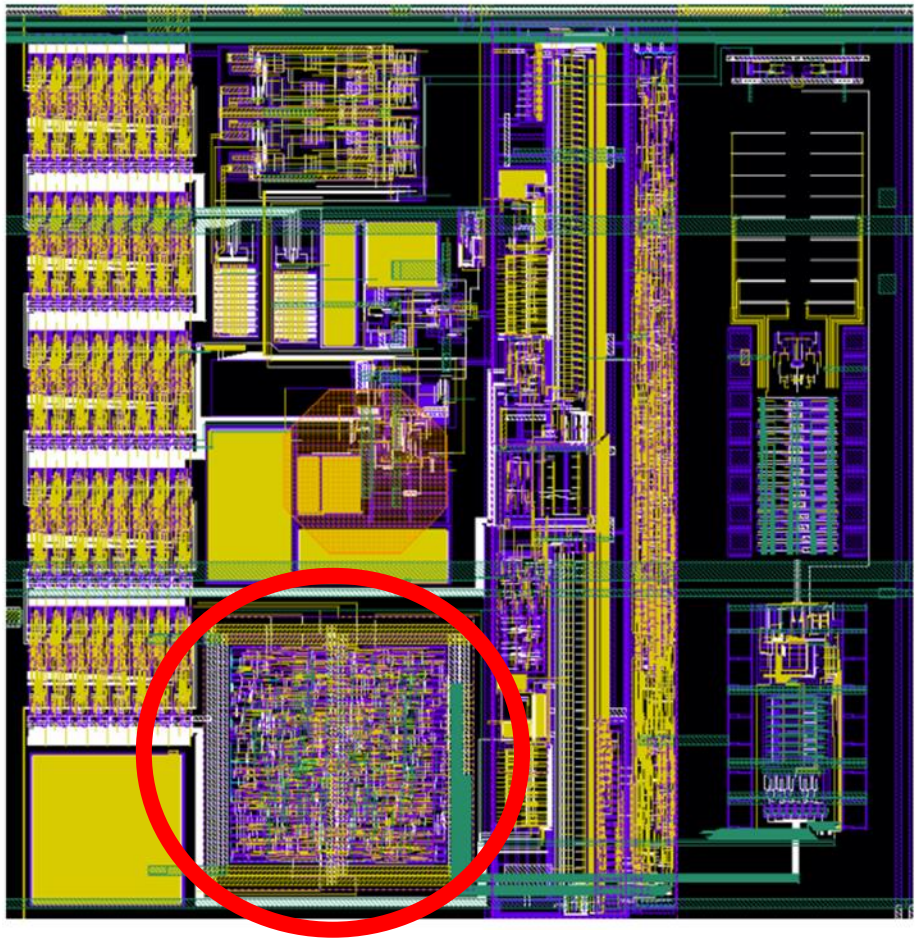
H2GCROC

- « 1D chip » 36/72 channels
- Input capacitance : Cd = 100-1000 pF
- Dynamic range : 30 fC – 300 pC
- ToA and ToT
- Target power : 5-10 mW/ch (now 15)
- Area 100 mm²

- AoT

Technology choice 65/130n

- Little impact on analog/digital performance
  - Analog similar in 65/130
  - Possibly more significant on TDC
  - Digital much simpler than LHC chips
- Update of digital part
  - Little space available => main reason for 65 !
- sizeable cost impact : ER 700 k$ vs 300 k$
  - But possibly more partners (but EICROC 50% of reticle)
- Prepare for design in 65 nm
  - Make an EICROC0/65n to test analog part and TDC



AoT vs DoT

- HGCROC/CALOROC designed Analog on Top (1D chip)
  - Analog inputs on one side / digital output on the other side
  - All digital data resynchronized when transefered to digital block

- ALTIROC designed Digital on Top (2D chip)
  - Powerful tools to verify digital part functionnality/timings in all corners on all the chip area
  - But needs more manpower for digital design (RTL, P&R, IRD, TB, UVM…)
  - Possible help from colleagues at Clermont

- Choice will depend on complexity (occupancy) and manpower availability

Manpower and schedule

- Names in backup. Manpower availability assuming HGCAL&HGTD ASICs completed

	Q4 2024	Q1 2025	Q2 2025	Q3 2025	Q4 2025	Q1 2026	Q2 2026	Q3 2026	Q4 2026
CALOROC1 A	design	fabrication	packaging	test	test	testbeam			
CALOROC1B	design	fabrication	packaging	test	test	testbeam			
CALOROC2 (final)				design	design	design	fabrication	packaging	test
FTE analog	2	1	1	1	2	2	1	1	1
FTE digital	3	1	1	2	2	2	1	1	1
FTE test		1	1	2	2	3	3	3	3

	Q4 2024	Q1 2025	Q2 2025	Q3 2025	Q4 2025	Q1 2026	Q2 2026	Q3 2026	Q4 2026
EICROC0A	design	fabrication	test	test	test	testbeam			
EICROC1	design	fabrication	test	test	test	testbeam			
EICROC2					design	design	desgin	verification	fabrication
EICROC3 (final)									
FTE analog	2	1	1	1	1	2	2	1	1
FTE digital	0	0	0	1	2	3	4	4	4
FTE test		1	1	2	2	3	3	3	3

Conclusion

- CALOROC is a 36-72 channel chip to readout SiPMs for calorimetry

- EICROC is a 1k-channels ASIC to readout AC-LGAD pixels
  - Very promising new family of detectors
  - Combines both good timing and position resolution (30 ps 10 µm)
  - Targeting 1 mW/ch
  - Reuses many blocks from ATLAS HGTD and CMS HGCAL

- Still several choices lying ahead
  - Technology choice 65n/130n
  - Analog on Top / Digital on Top

- Interest of these chips for future detectors (DRD4/6)

backup

Manpower on ASIC design

- CALOROC : AGH, IRFU, OMEGA
  - Analog : F. Bouyjou, P. Dumas-Zielhman, M. Firlej, T. Fiutowski,, F. Guilloux, M. Idzik, A. Laffite, C. de La Taille, J. Moron, K. Swientek, D. Thienpont
  - Digital : F. Dulucq, M. El Berni, S. Extier
  - Tests : LLR, ORNL

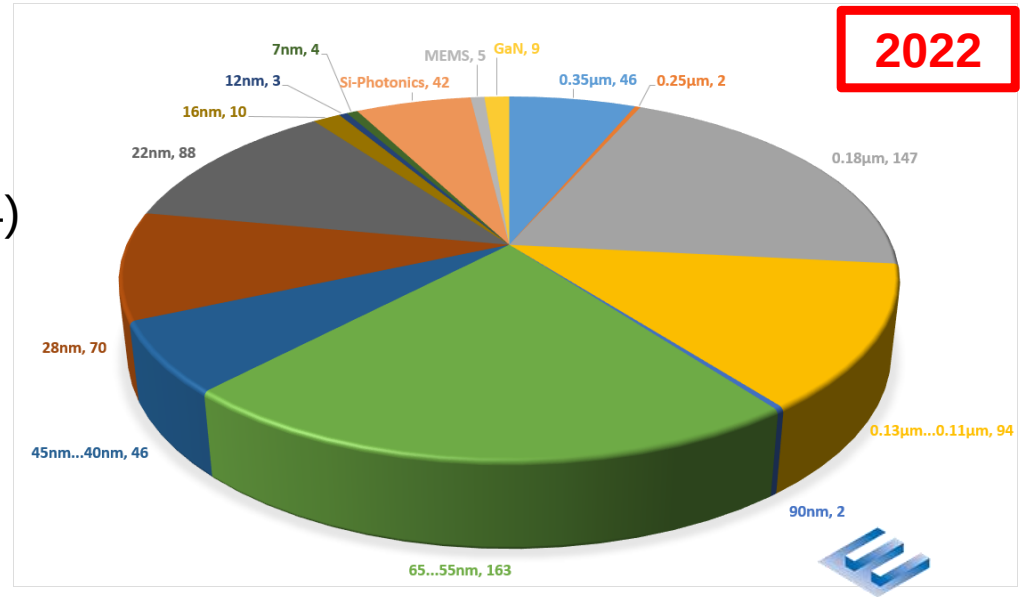
- EICROC : AGH, IRFU, (LPCF ?), OMEGA
  - Analog : F. Bouyjou, S. Conforti, E. Delagnes, JJ Dormard, M. Firlej, T. Fiutowski, F. Guilloux, M. Idzik, B.-Y. Ki, C. de La Taille, J. Moron, D. Marchand, A. Verplanck
  - Digital : F. Dulucq, M. El Berni, S. Extier,, F. Guilloux, (A. Soulier + …)
  - Tests : IJCLAB, BNL,

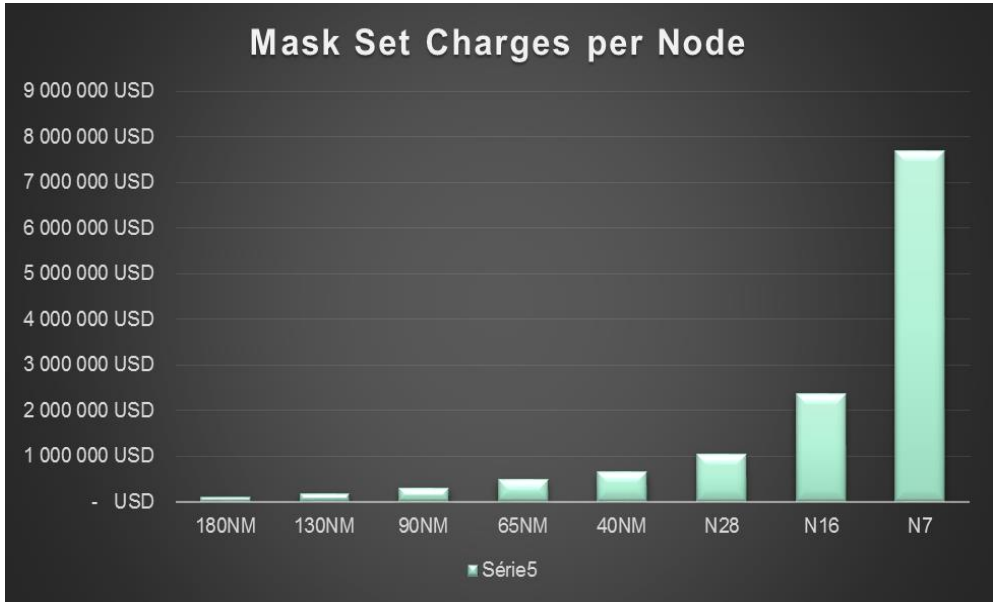
Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

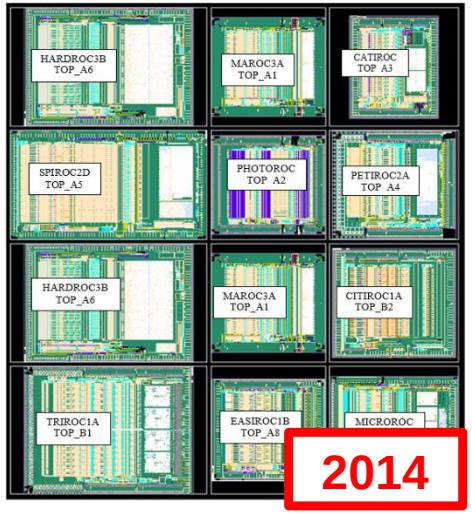
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run

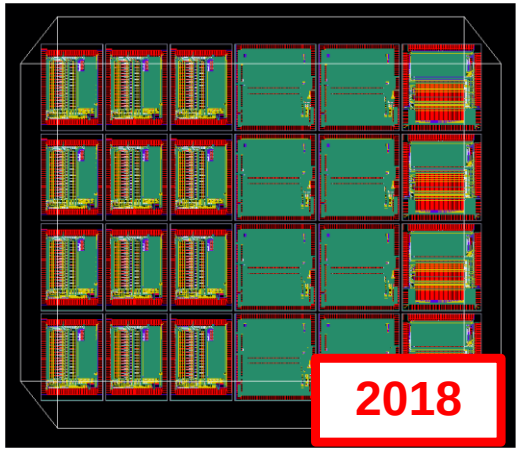


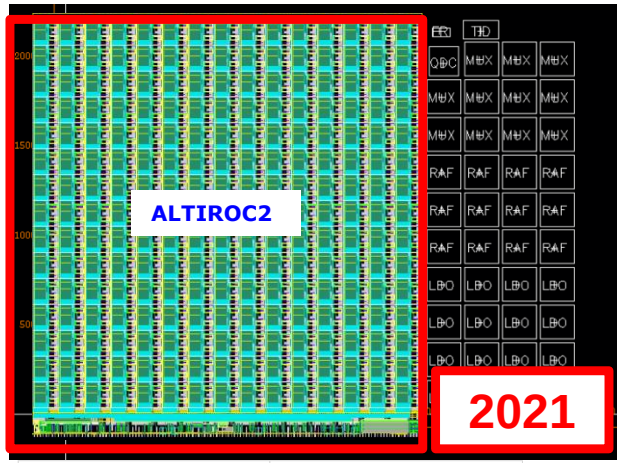


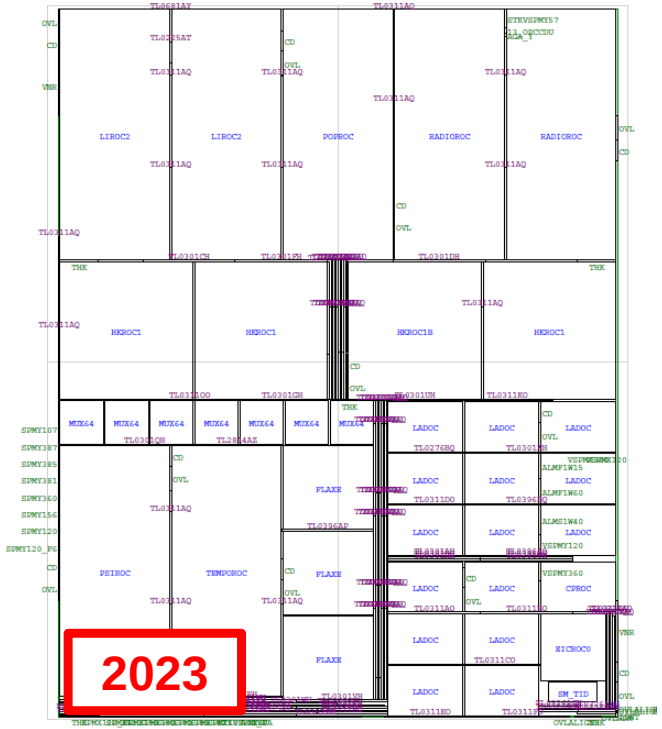
OMEGA Engineering runs

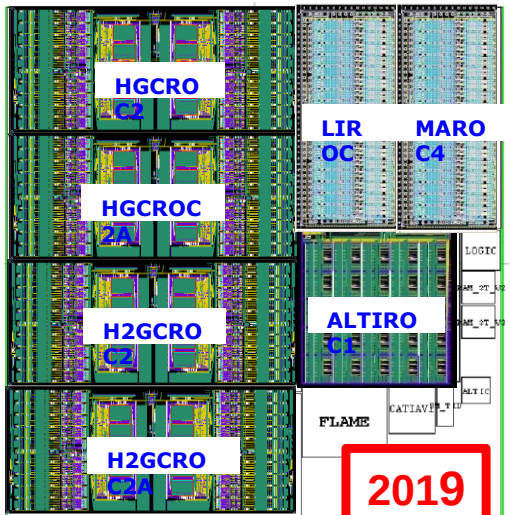
- 8 engineering runs in 9 years !
  - AMS SiGe 0,35um 2014, 2016, 2018
  - TSMc 130nm : 2019, 2020, 2021, 2x2023
  - Cost : 200-300 k€, shared between projects

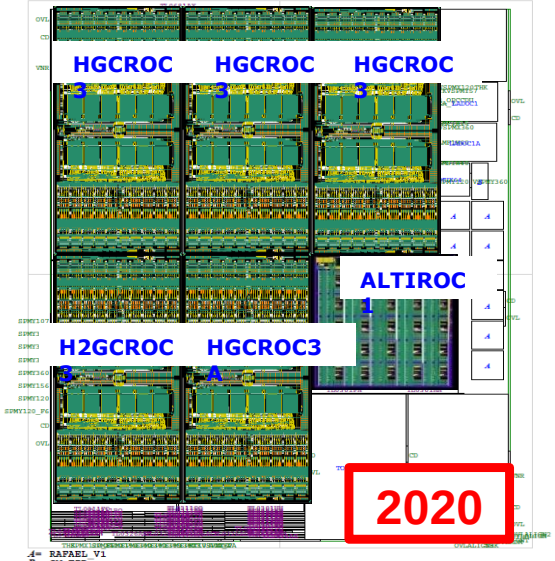


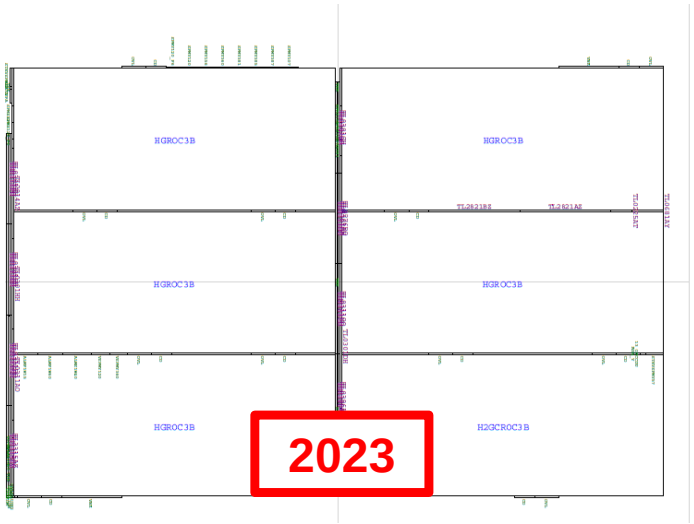




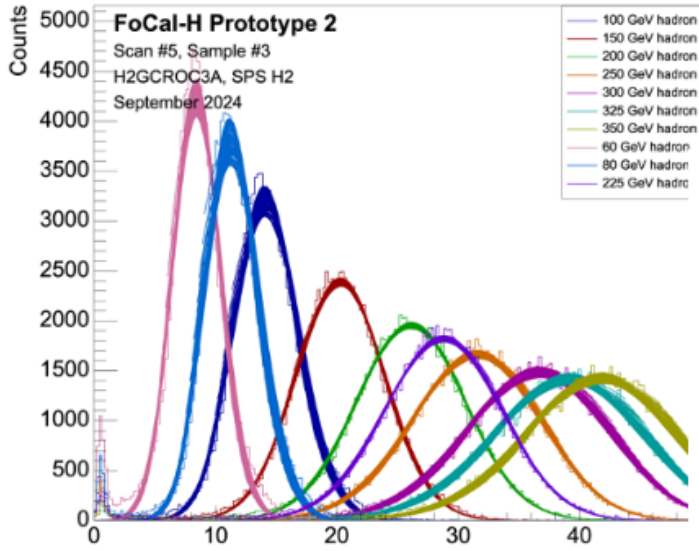


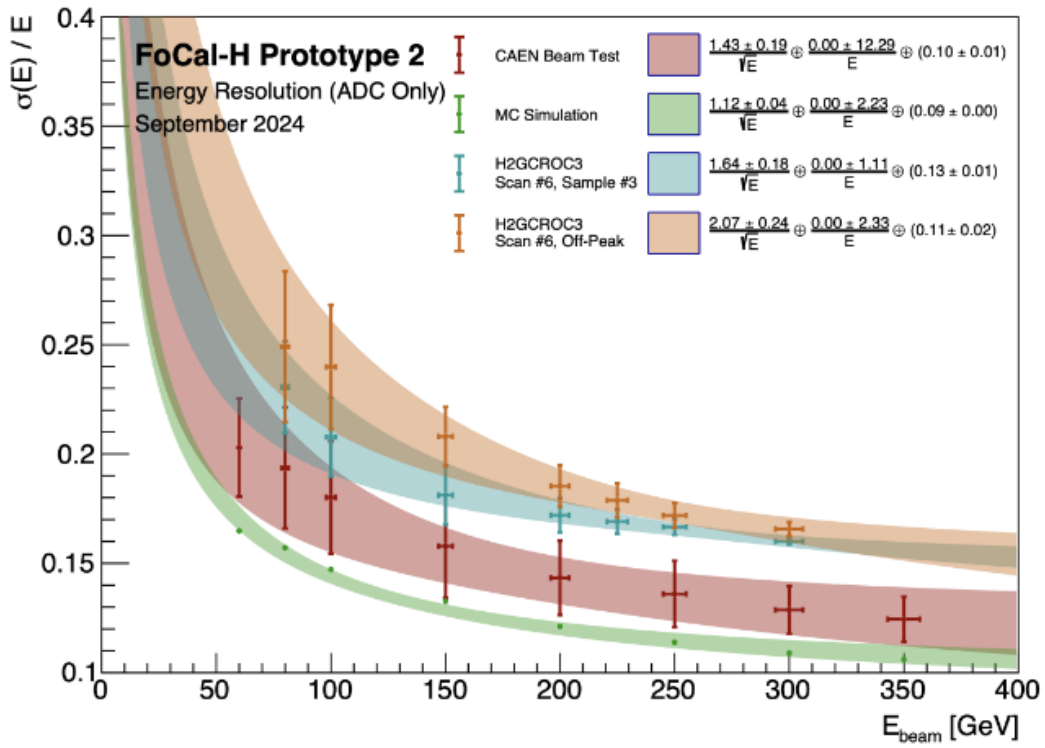


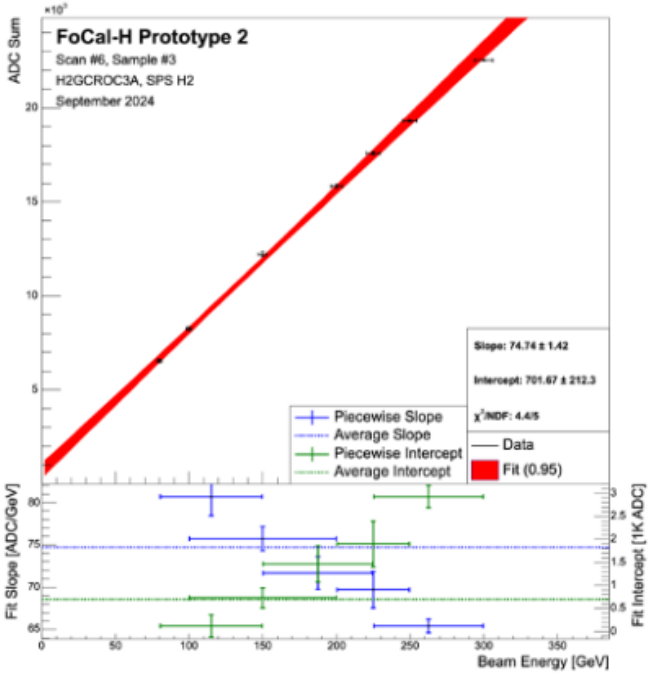




Some very early resolution figures







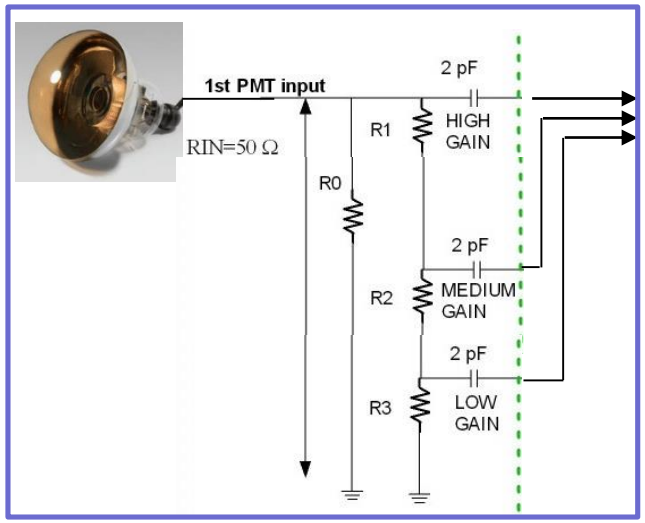
These are just teaser plots, the analysis is still ongoing and we are working on combining the TOT into the analysis

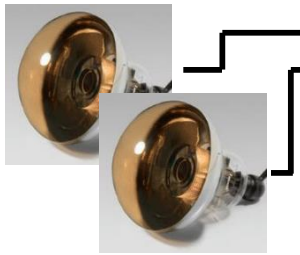
FCFD design status

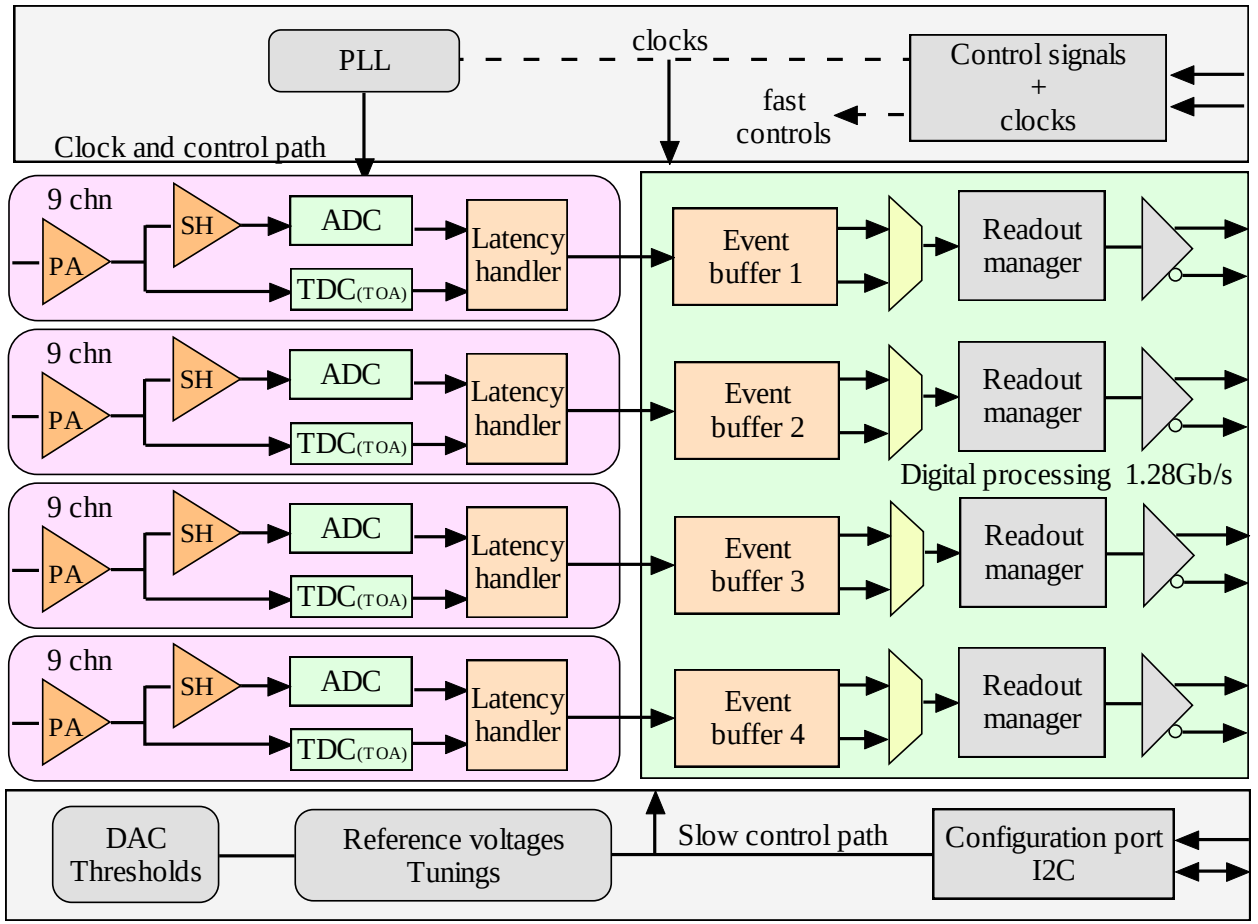
- Currently working on the redesigned front-end
  - In order to achieve the desired performance with the 1-cm long sensors, a redesign of the front-end is required
  - A three-stage amplifier is being implemented now, results look promising
    - After this, implement a comparator with tunable threshold, and the neighbor readout (more on this in the following slides)
- The chip is designed in TSMC 65 nm process
  - We usually submit through CERN to IMEC, have done that for the past two versions, all agreements are in place
- Once the chip is received, during production, the chip should be wafer-tested to define good dies for modules assembly
  - During the R&D phase the plan is to perform the testing upon reception by the chip designers, which is followed by distribution to collaborators for further testing

HKROC main features

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain





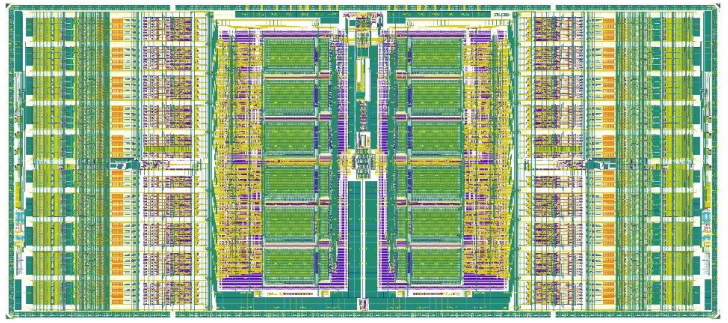


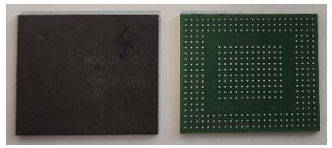
- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger

H2GCROC: SiPM version. Requirements

Requirements for H2GCROC (The SiPM version of the ASIC):

- Charge dynamic range : **160 fC to 320 pC**
- Timing accuracy **< 100ps for pulses above 3 MIPs (4.5pC)** for a $C_{det} = 100pF$
- Compensation of the leakage current up to **1mA**
- Radiation resistance up to **300 kRad**
- **Input DAC** to tune the overvoltage

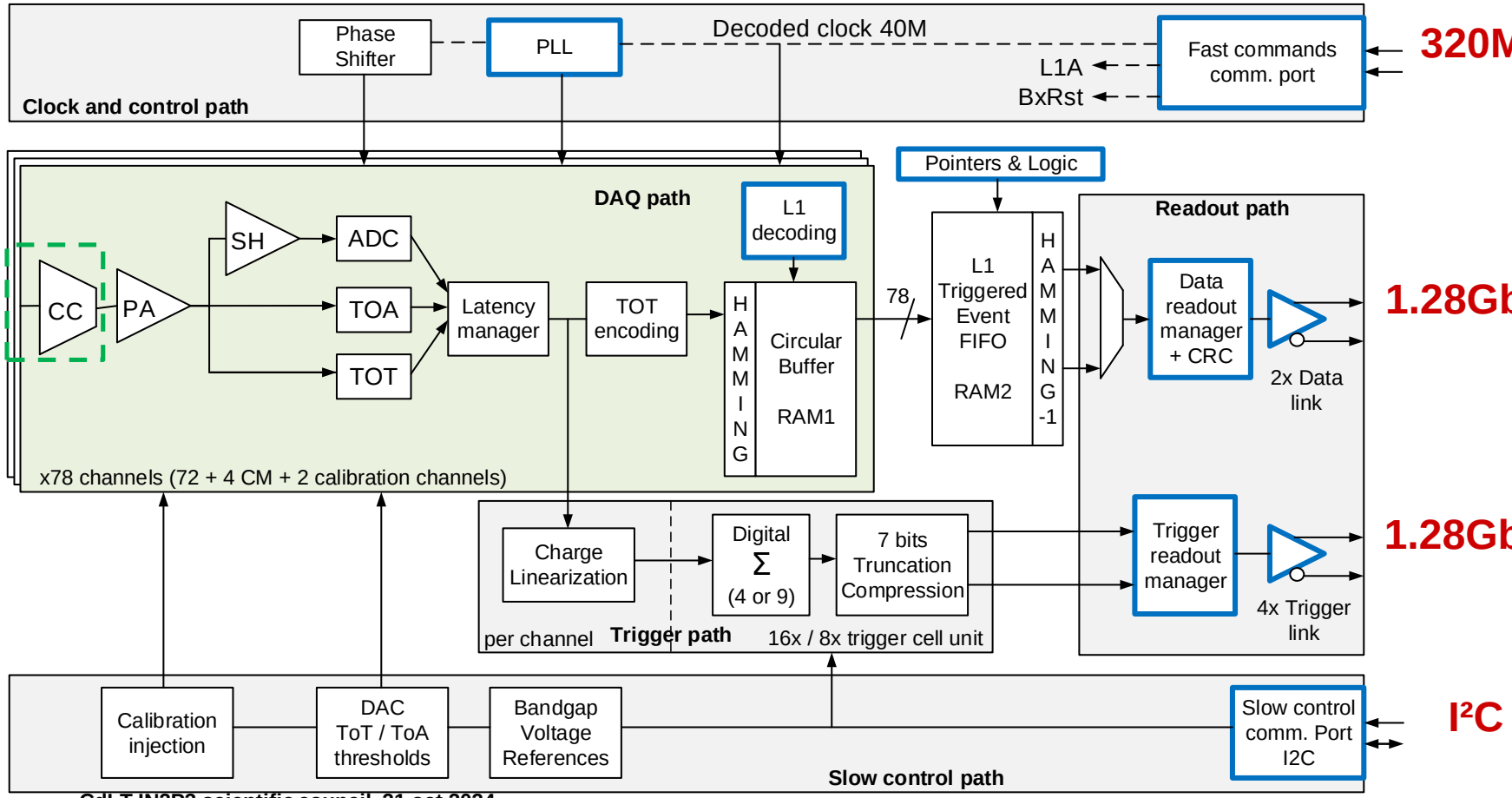




Current Conveyor based on KLAUS chip from Heidelberg UNI.

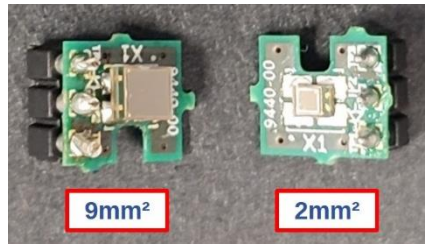
Attenuates the current at the input with 4 bits.

CC gain:
0.025 to 0.375
(step 0.025)

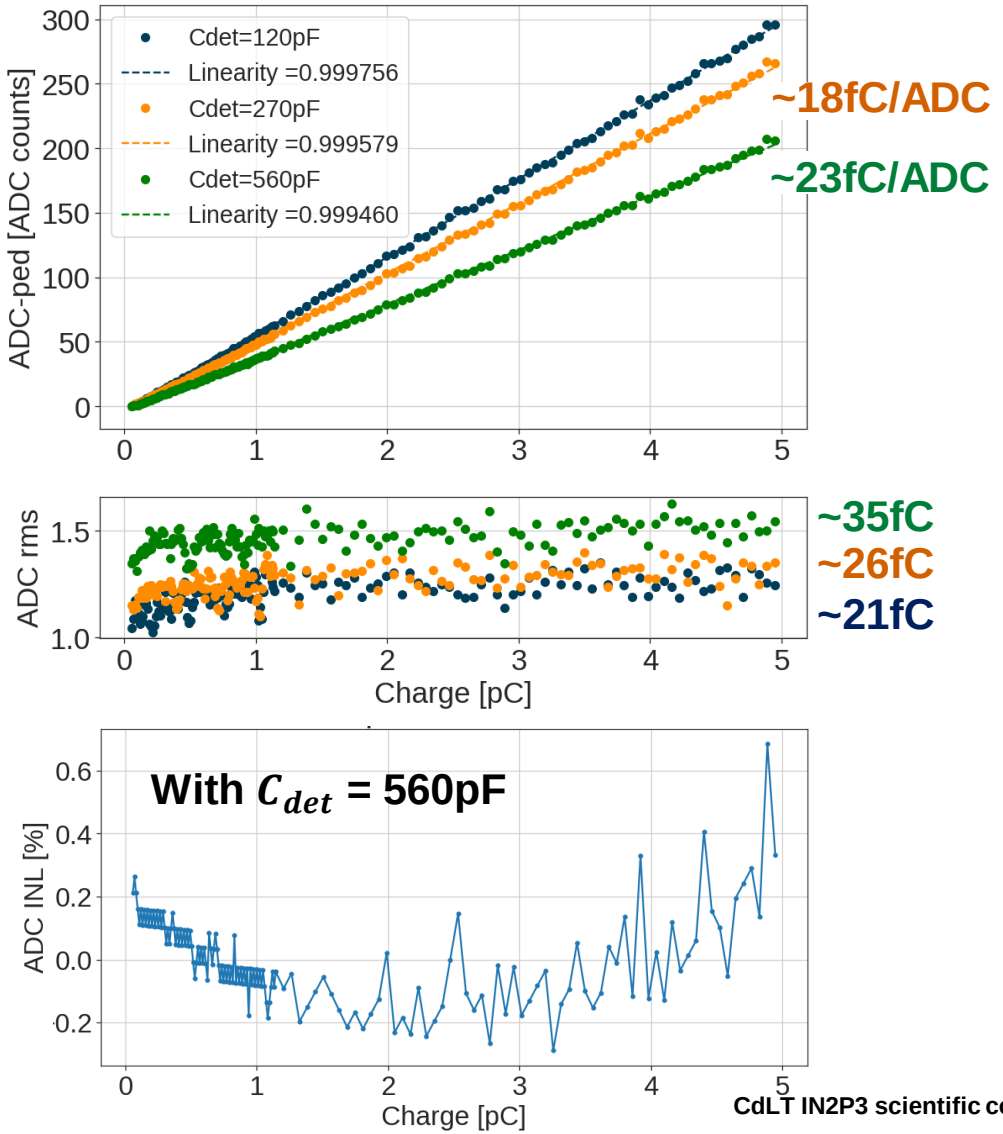


Physics mode : test pulse injection

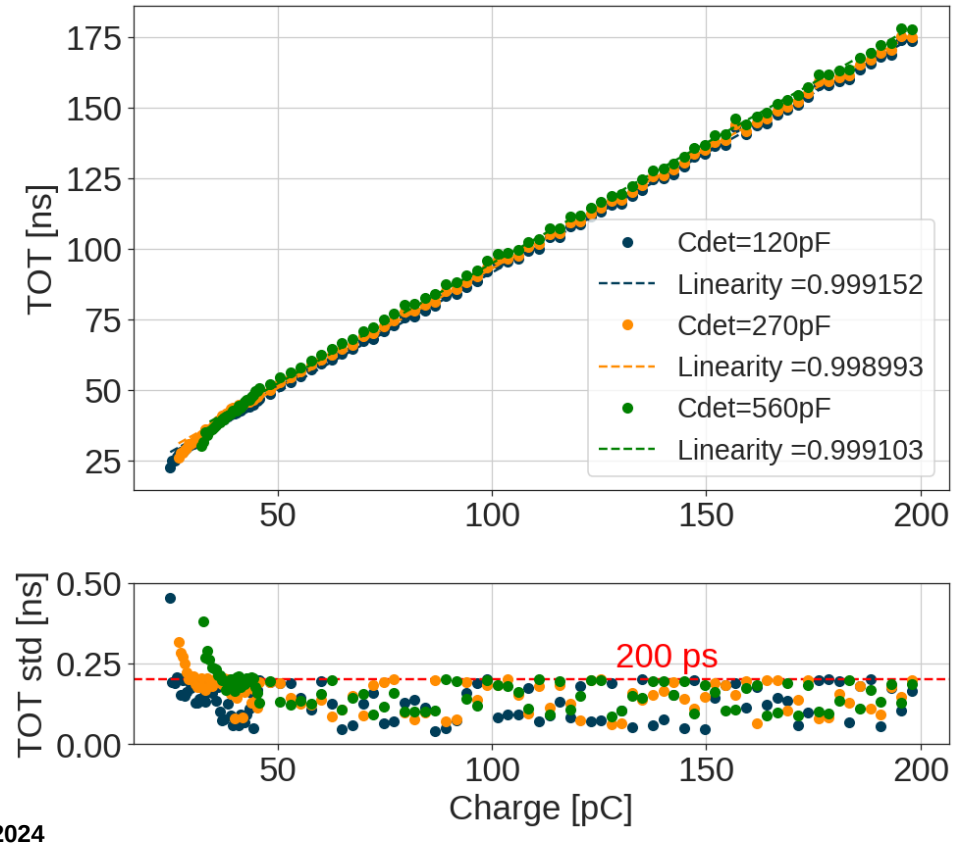
- ~ 60 fC minimum detectable charge efficiently, up to 320pC



Low range injection (ADC):

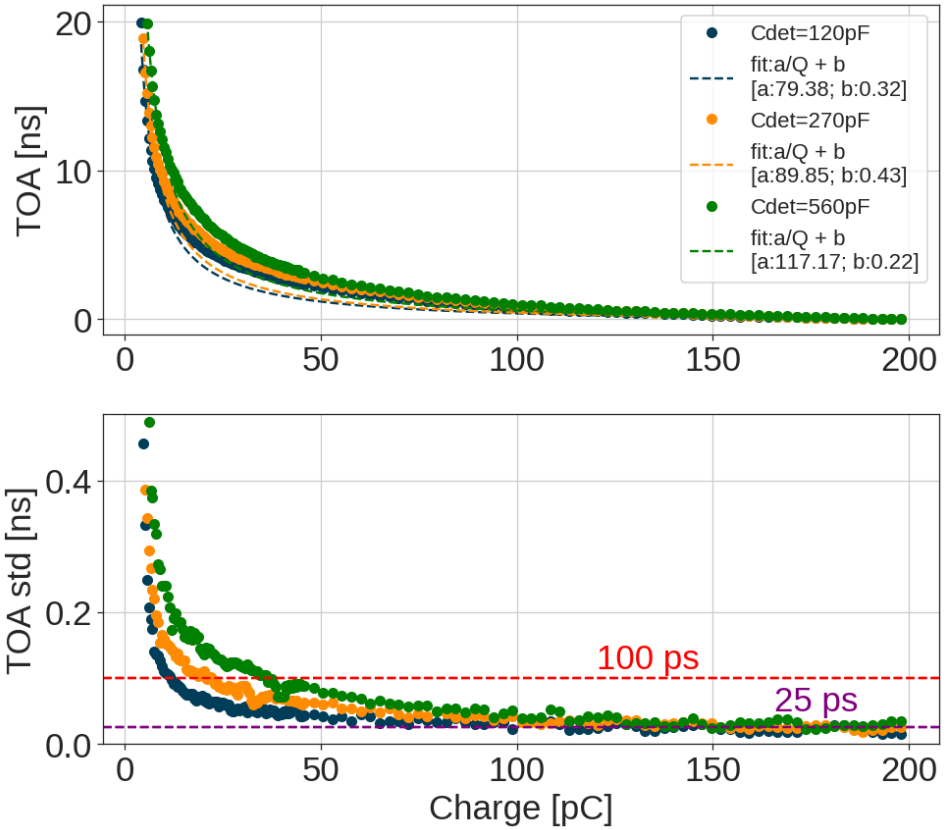


High range injection (TOT):



Physics mode : ToA

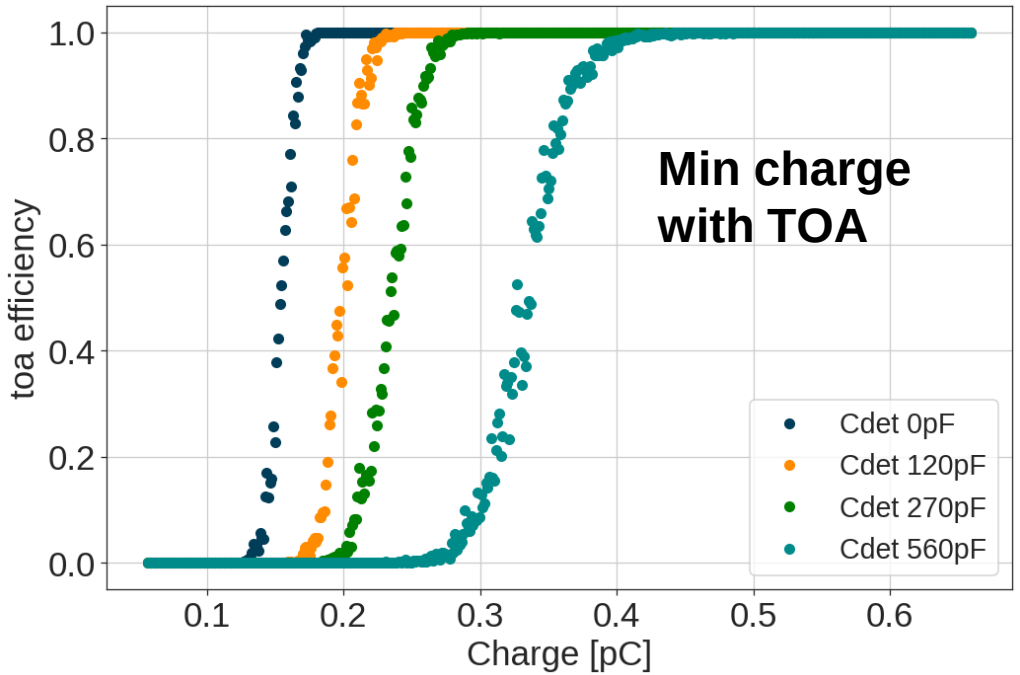
Time of Arrival (TOA) :



- The increase in noise due to larger C_{det} shifts the minimum charge associated with TOA data.
- The thresholds can be adjusted channel-wise for a uniform performance.

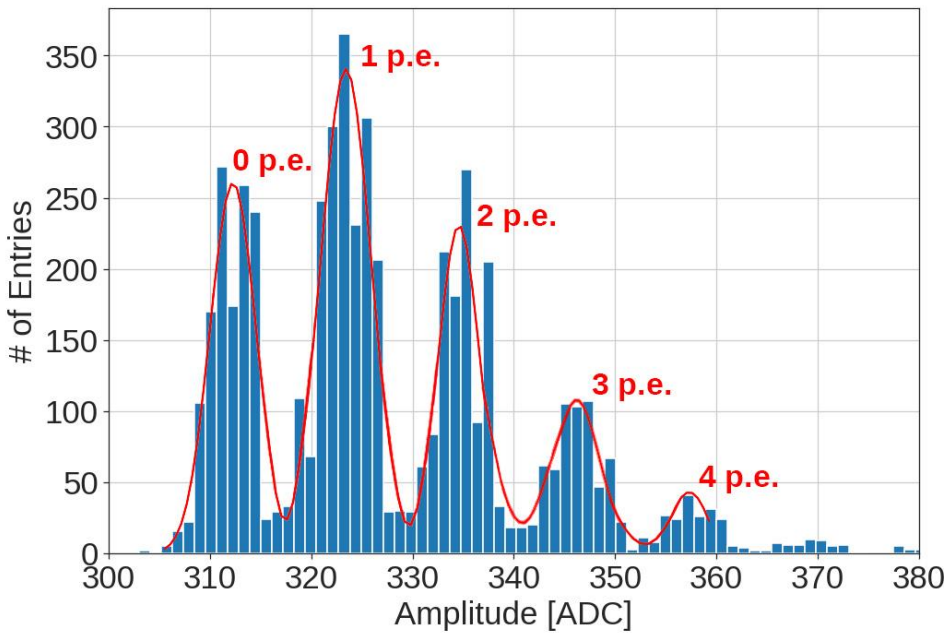
Effect of C_{det} on TOA:

- Larger C_{det} produce larger time walk due to the duration of the signal.
- Increasing C_{det} delayed the achievement of a 100ps resolution in charge injection.

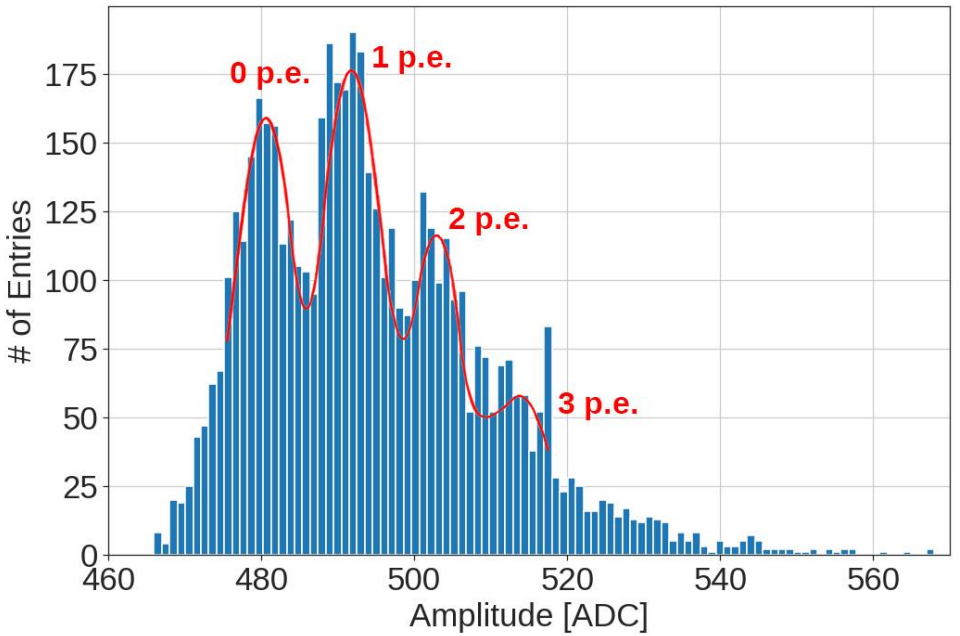


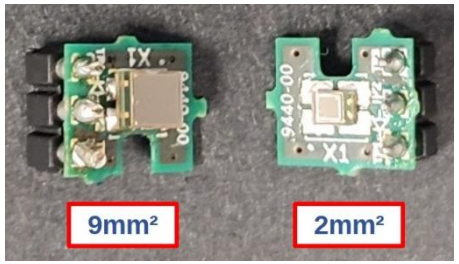
Calibration mode: Single-photon-spectrum

- **2mm²:**



- **9mm²:**



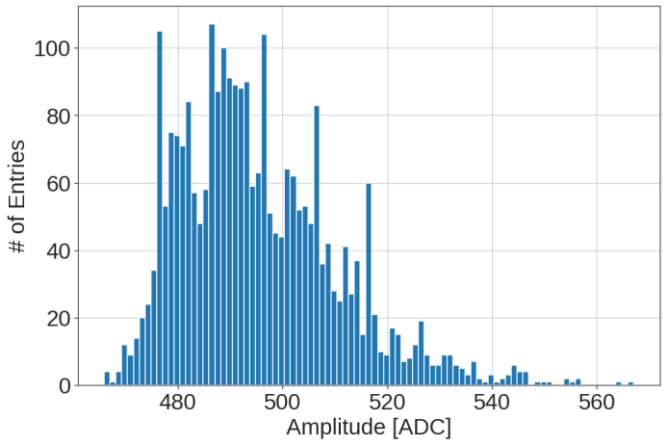


***Extra step for 9mm² SiPM calibration:**

The large C_{det} of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

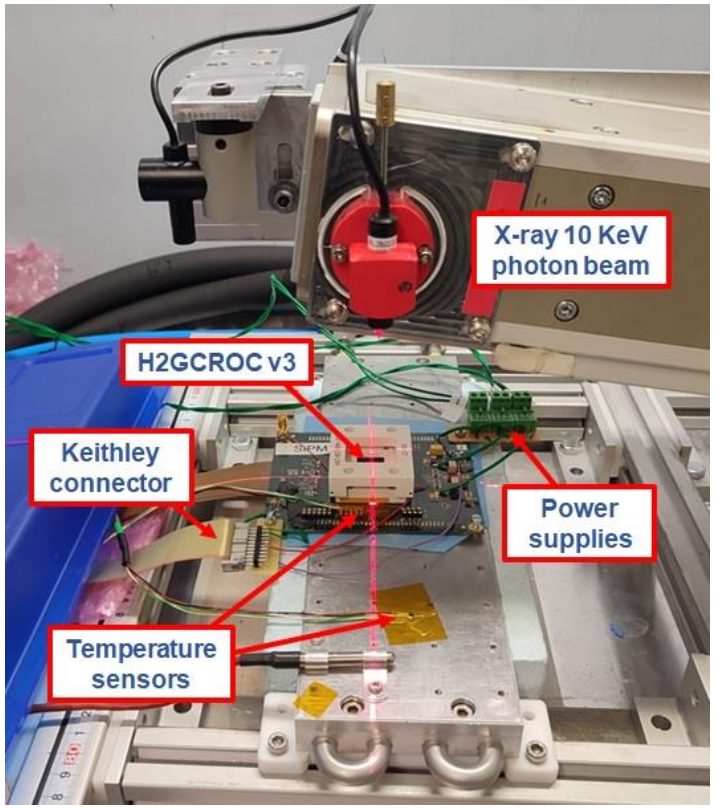
The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

Without DNL correction:

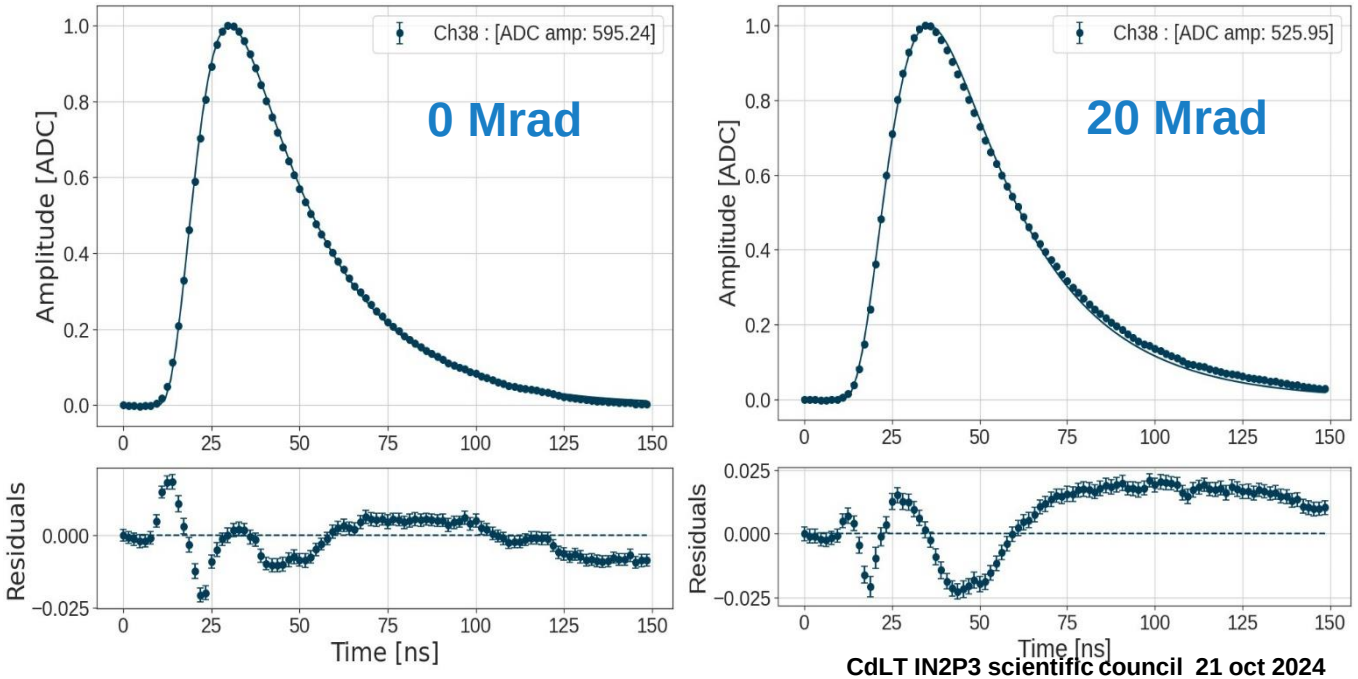


Irradiation campaigns

- Power consumption, ADC & TDC performance, noise, links stability, etc. tested during irradiation
- **TID irradiation tests in both ASIC versions.**
- **Heavy ion and Proton irradiation in the Si version of the ASIC**
  - Increase on triplicated parts for HGCROC3b



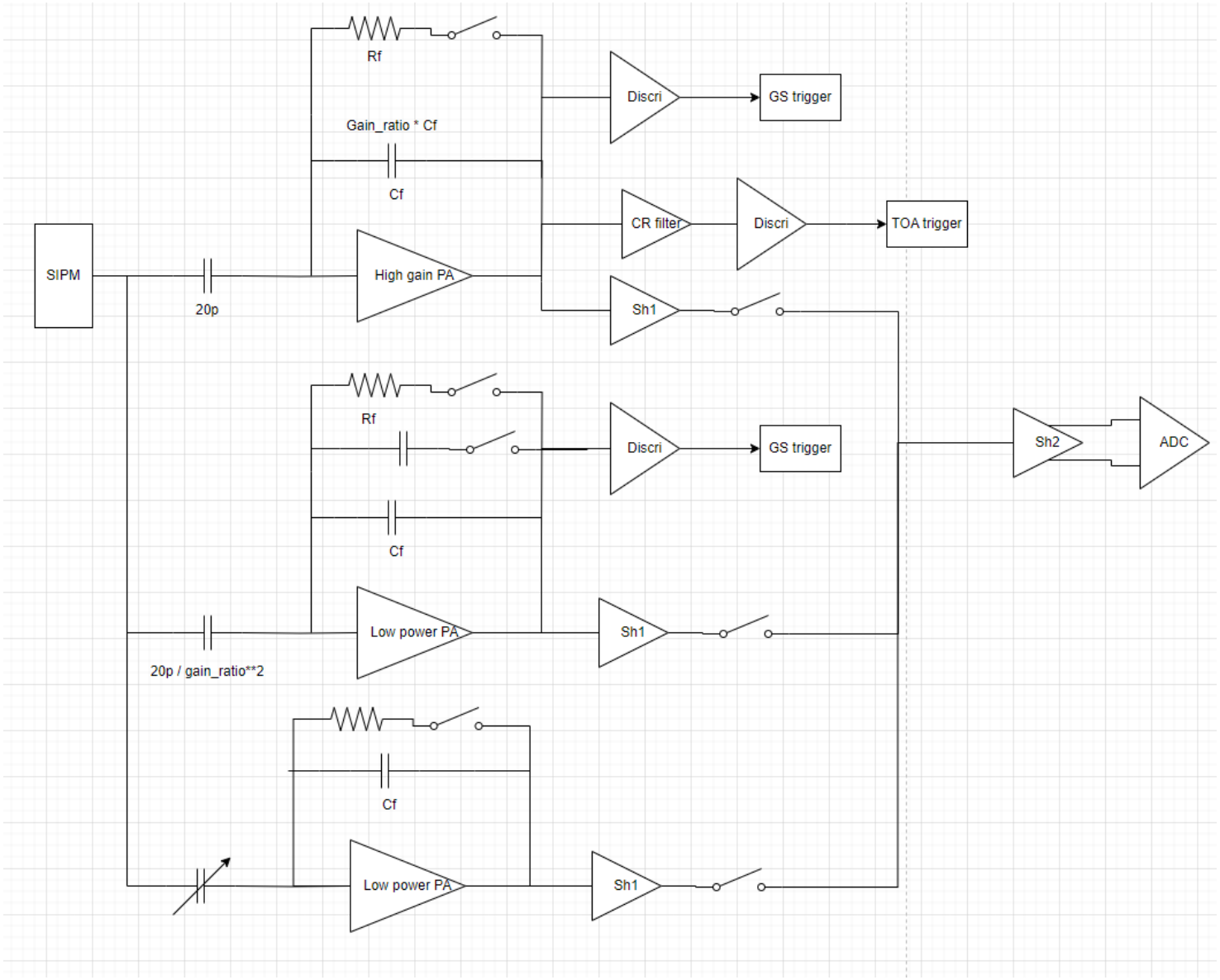
Stability of ADC measurements after 20Mrad:



- **H2GCROCv3** has proven to be **radiation tolerant up to 20 Mrad** at room and -5°C with good ADC, TDC and PLL measurements.

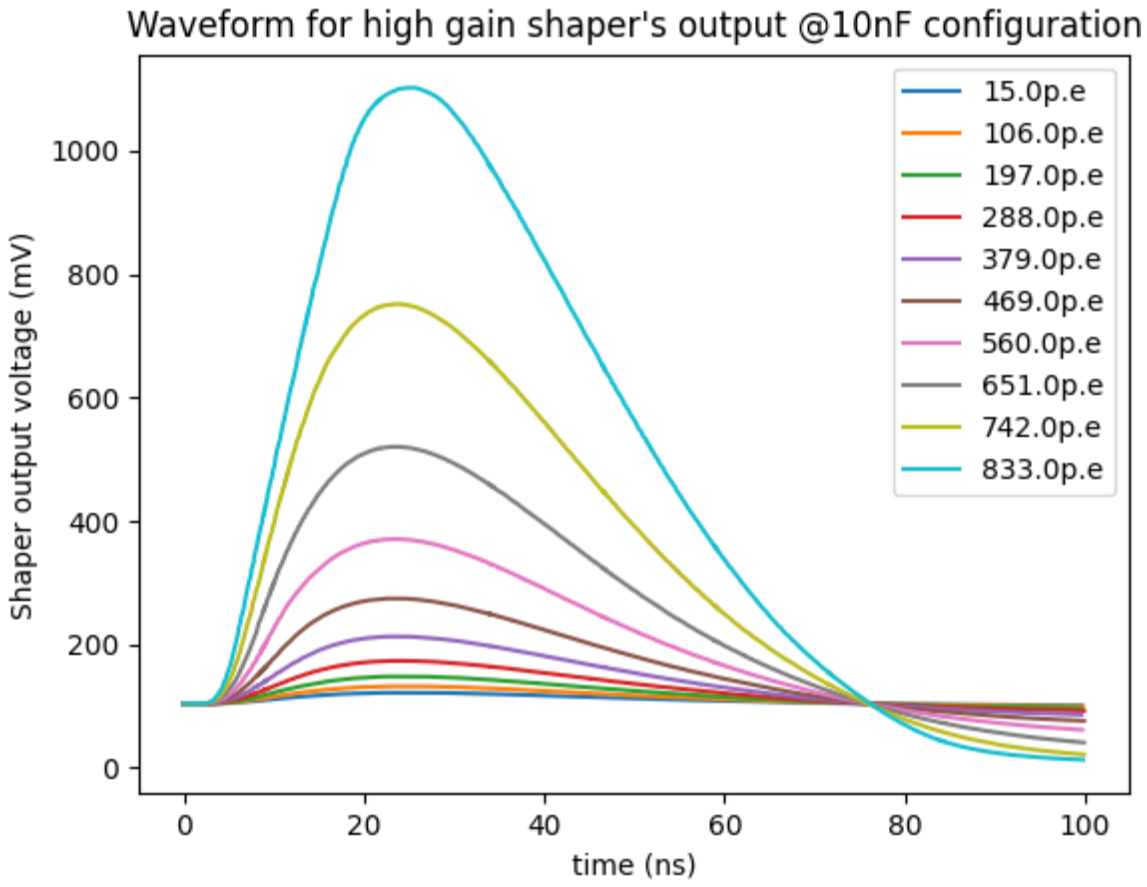
CALOROC1B: Chosen architecture [P. Dumas]

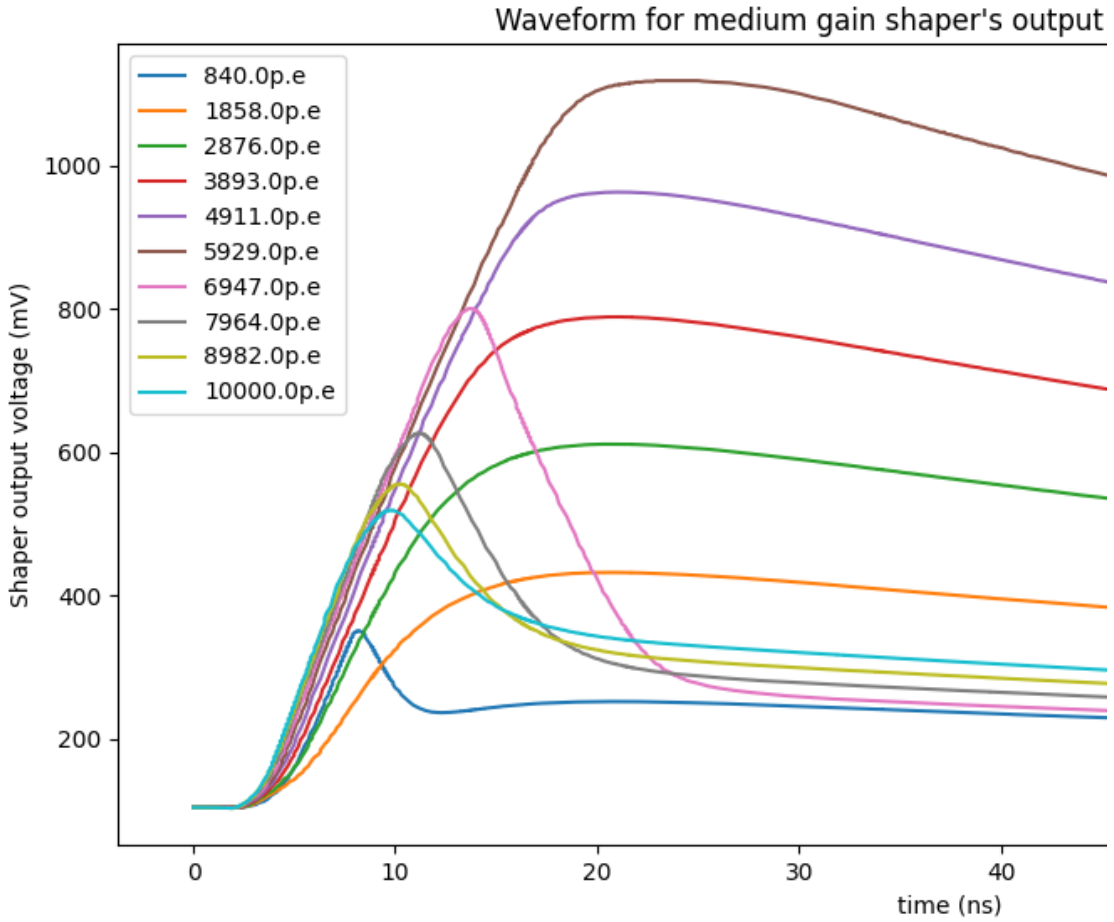
- New dynamic frontend with switched gain:
  - High gain
  - 2x medium gain
  - Low Gain
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 500 pF to 2.5 - 10 nF
  - ~ 10 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



CALOROC1B: Charge and time simulations

- Waveform for HG on the left + gain switching on the right:
  - Example with Cd of 10 nF

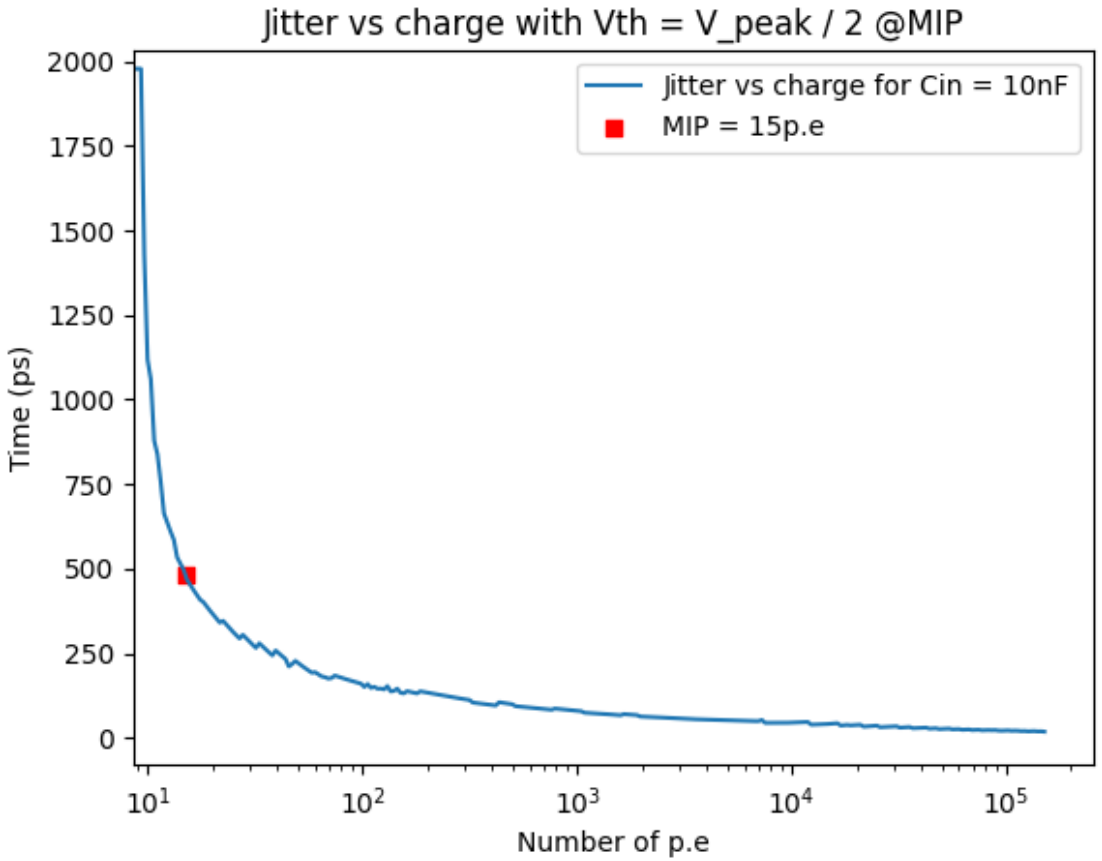


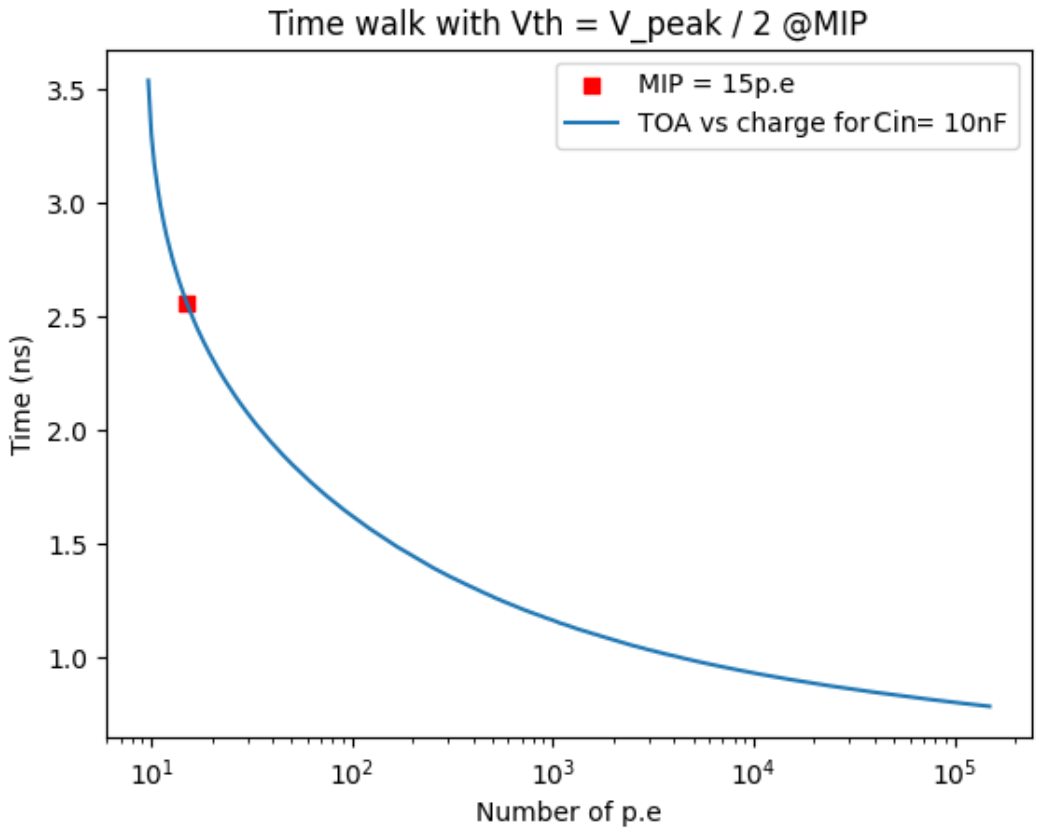


CALOROC1B: Timing precision

- Simulated time jitter goes down to 20 ps with < 500 ps for the MIP

- Time walk is below ~2,5 ns (equivalent to the value of CMS H2GCROC)





CALOROC1B: SiPM vs SNR

- The SiPM configuration has a direct impact on the SNR
  - SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
  - Gain of 1.8e5 electrons per p.e (table below)

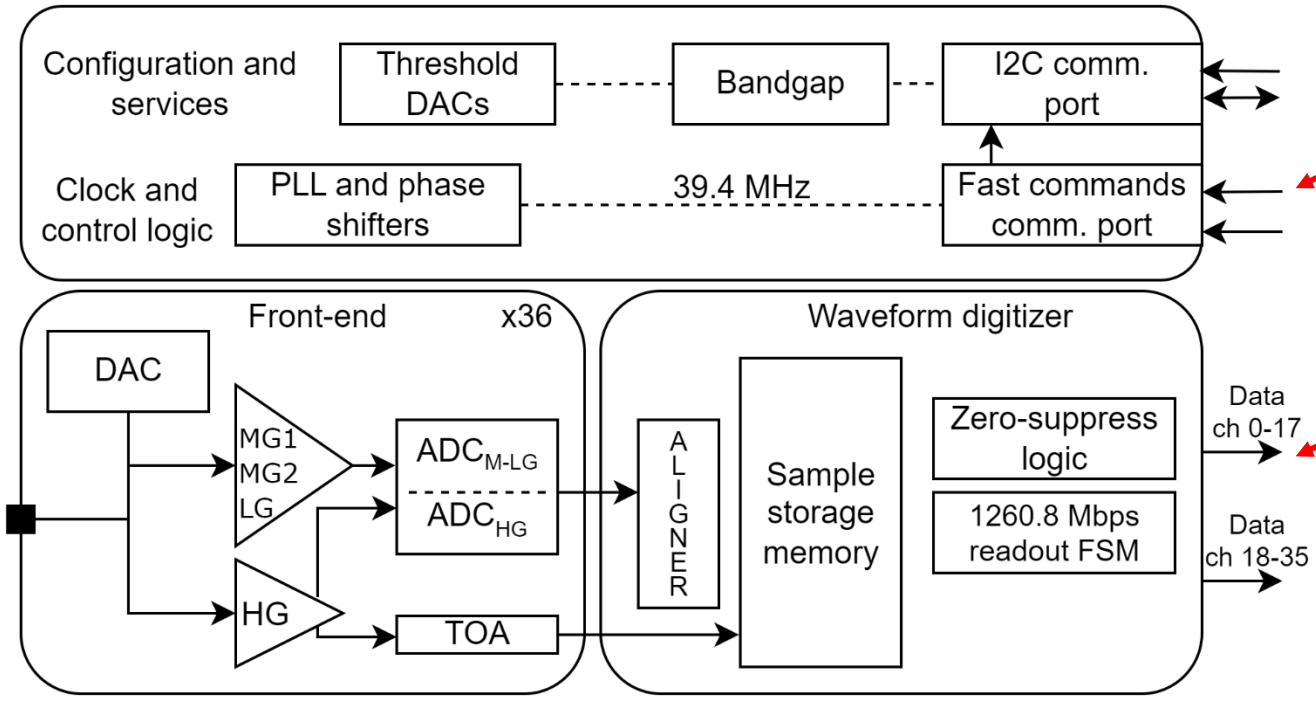
- CALOROC1b will be able to readout SiPM in the range ~ 500 pF to 10 nF
  - Timing measurements will focus on the MIP (~15pe)

Operation modes	1 SiPM of 530pF	1 SiPM of 2.5nF	4 SiPM of 2.5nF
Cin	530pF	2.5nF	10nF
SiPM config gain (μV/p.e or Q/C)	13.58μV	11.52μV	2.88μV
Dynamic range (in p.e)	22.79k	107.5k	430k
Dynamic range (Charge)	656pC	3.1 nC	12.3nC
Jitter @ 1p.e	390ps	Not measurable	Not measurable
SNR @ 1p.e	10	2.13	0.53

SiPM: S14160-3010PS 3x3mm (530pF) / S14160-6010PS 6x6mm (2.5nF)

CALOROCs: block diagram and interfaces

- CALOROCs will have the same interfaces (comparable to CMS H2GCROC *):
  - Fast command to dynamically control the ASIC
  - I2C to set the parameters
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)



Fast commands	Value
Idle	00011
External trigger	01101
ChipSync	01110
BCR	10101
EBR	11001
Link-sync-ROC or Link-reset-ROC	10110
Calibration int or ext	11010

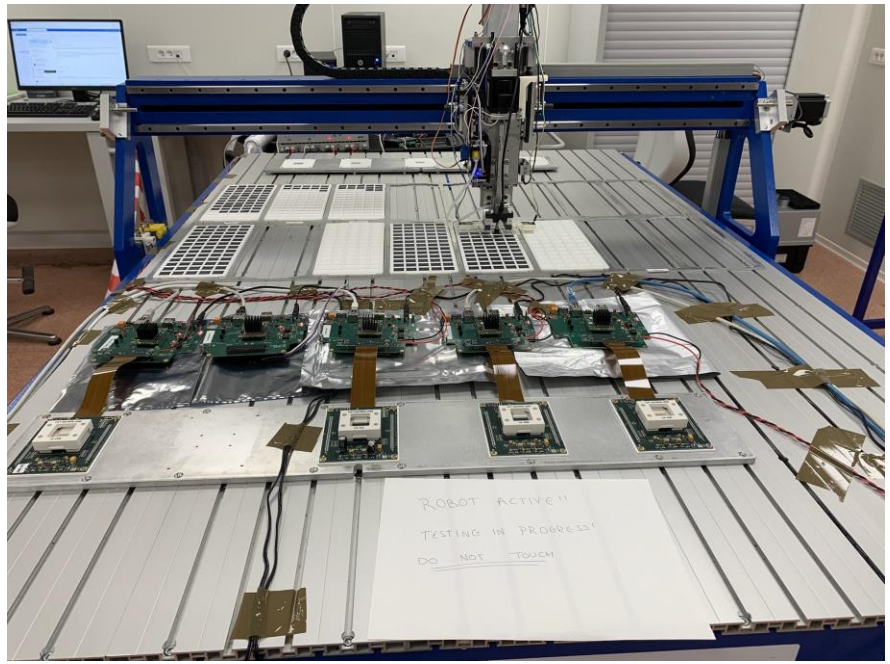
CALOROC1A or 1B

4b-data Header	2b Mode	Dh	24b Timestamp	1
4b-data Header	8b 0	Dh -d	Dh -h	18 channels Hit map
2b Gain	10b ADC$_{-1}$ - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
2b Gain	10b ADC$_{-1}$ - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
⋮				
2b Gain	10b ADC$_{-1}$ - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
CRC				
Idle/Sync Header	28b default IDLE Pattern			

* CERN EDMS ➔ https://edms.cern.ch/document/2954073/1

Quality assurance and timeline

- Expertise in radiation-hardened front-end ASICs for HEP
  - HL-LHC ASICs: ATLAS HGTD and CMS HGCAL (10^5 ASICs)
- Expertise in irradiation testing (dose and displacement)
  - HL-LHC levels 200 Mrad and 10^{16} n_{eq} / cm² (1 MeV equivalent neutrons)
- Standard interfaces ensures a full compatibility with our robot
  - 2x 50 ASICs tested per hour (H2GCROC) with QR code scan
- CALOROC timeline – 2024 to 2027
  - End 2024, CALOROC1A **and** B submission (Eng. Run)
  - 2025, packaging, performance tests and DAQ validation
  - 2025-2026, irradiation tests and CALOROC2A **or** B preproduction (final ASIC/package)
  - (If chosen, possible CALOROC3B extra submission end 2026)
  - Q1 (Roc1A) or Q3 (Roc1B) 2027 production and robot tests

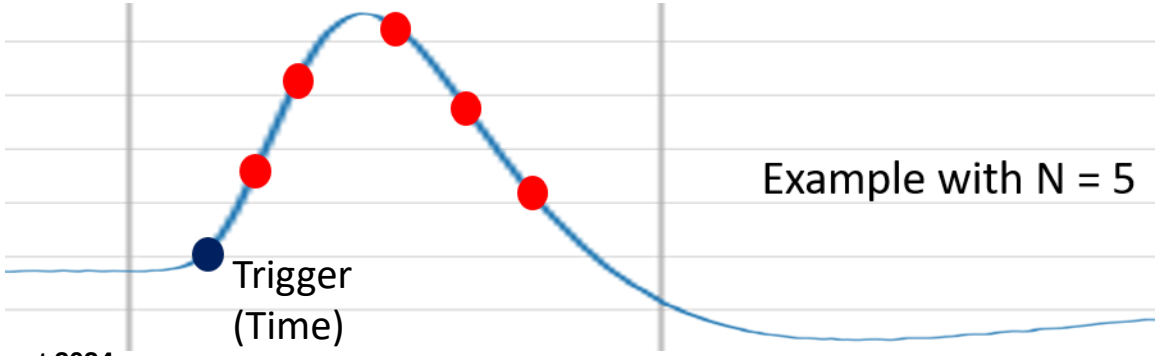


Common: Rates per channel

- Present HGCROC rate calculation: 1 serial link for 36 (+2) channels (HGCROC is arranged by 36 channels)

Version	Number of points (N)	Max rate	Remarks	
Present HGCROC-36ch	1	976 khz / ASIC	LHC is 1 snapshot	Present HGCROC
Per channel (1 link/36 ch)	4 or 3	7-9 kHz / chn	Divide by N and by 36 (could be exercised)	
Caloroc (1 link/18 ch)	4 or 3	24-32 kHz / chn		CALOROC
Caloroc with zero suppress	4	55 kHz / chn	With 6 channels triggered (over 18)	

Conclusion: ZS with 2 serial links mandatory

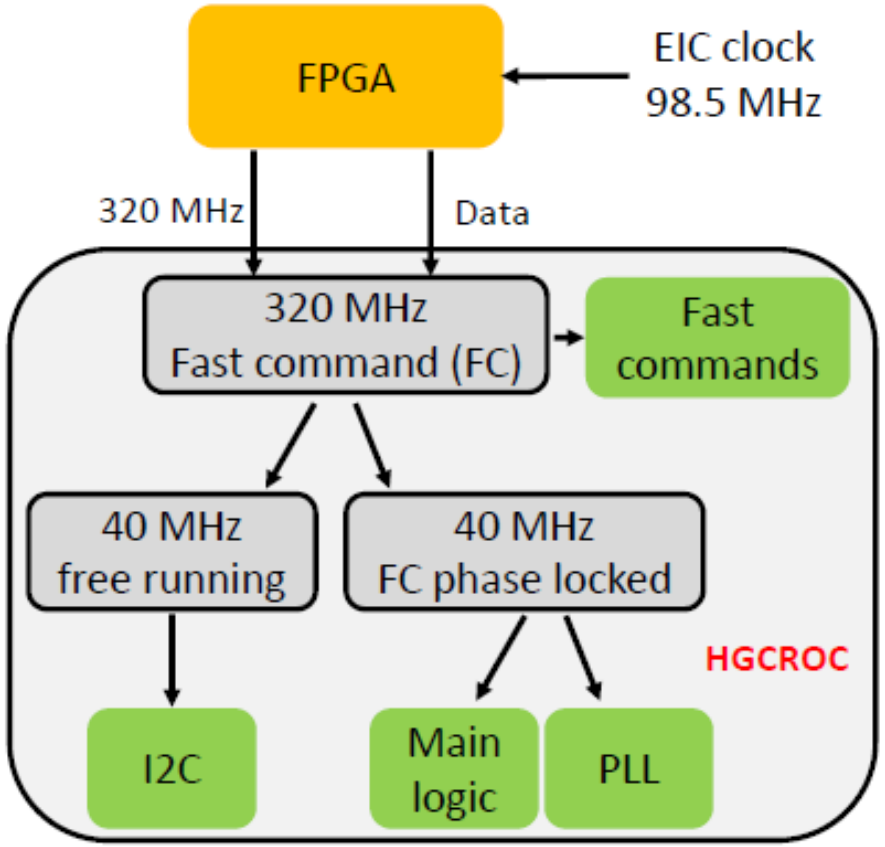


Evolution for EIC readout [F. Dulucq]

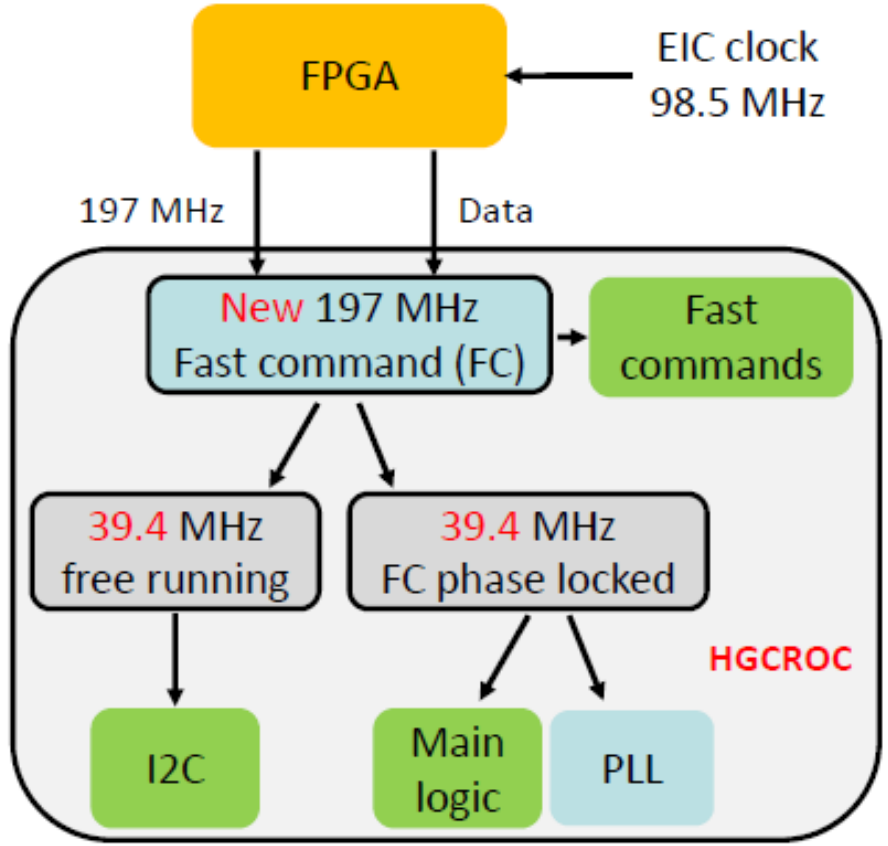
- Clocking scheme : 40 MHz -> 98.5 MHz

❑ Adapt LHC-like 40 MHz to EIC clock ➔ done within the FPGA with 2 possible solutions

❑ 40 MHz / 1280 Mbps or 39.4 MHz / 1260.8 Mbps



Baseline (no change)



This could be tested with actual HGCROC (PLL)
With 315.2 MHz instead of 320 MHz

ALTIROC performance with sensor : test pulse injection