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SALSA: a new versatile readout chip for MPGD

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Context

SALSA specifications

Development plans

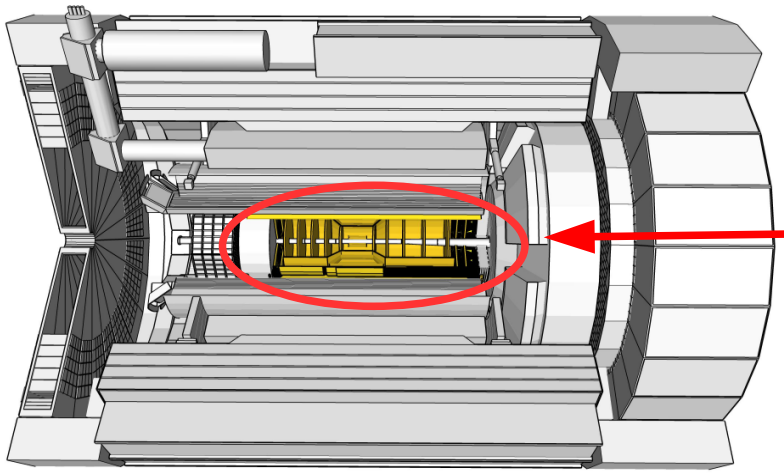
Present status

THE MPGD TRACKERS OF EPIC EXPERIMENT

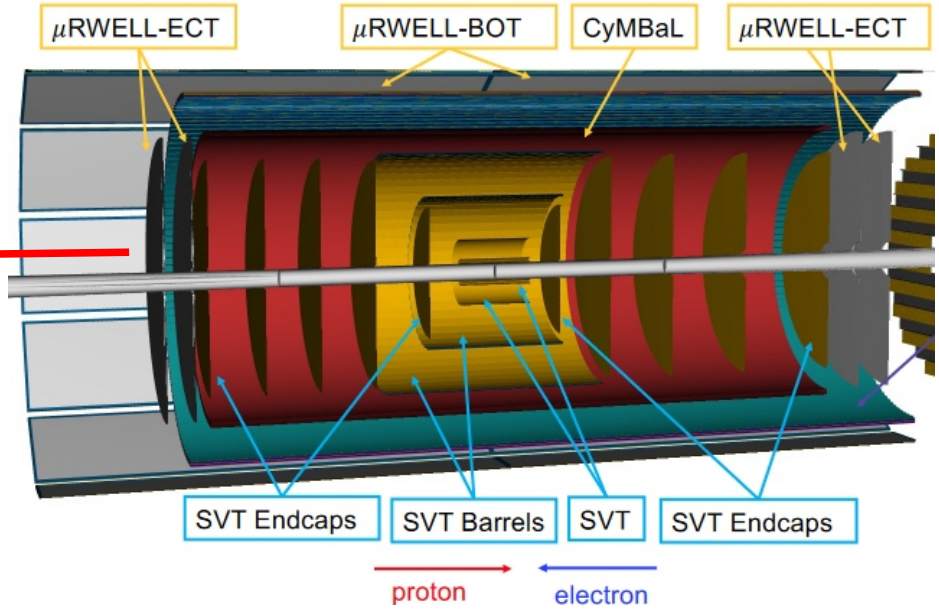
MPGD detectors foreseen in EPIC

- Cylindrical Micromegas barrel layer (CyMBaL) → ~30 k.channels
- μRWell barrel outer tracker (μRWell-BOT) → ~100 k.channels
- μRWell end cap tracker (μRWell-ECT) → ~30 k.channels
- Same readout ASIC to read all MPGD trackers → **SALSA**

EPIC detector



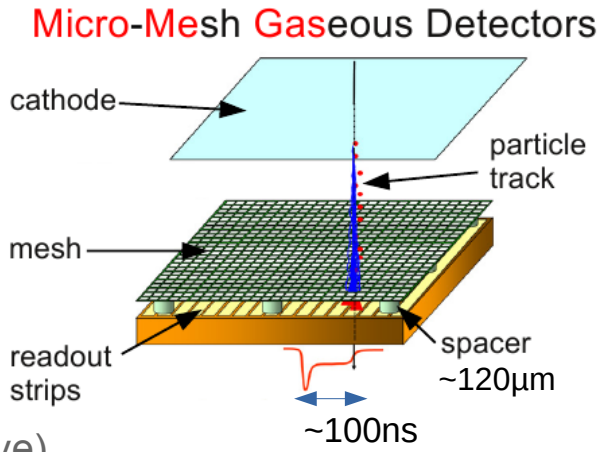
Central trackers



REQUIREMENTS ON MPGD DETECTOR READOUT

Micro-Pattern Gaseous Detector characteristics

- Detection of gas ionization from charged particles
- Small gaseous amplification gap → short signals ~ 100 ns
- Gain 5-10k → typical signal amplitude ~35 fC, max ~200-250 fC

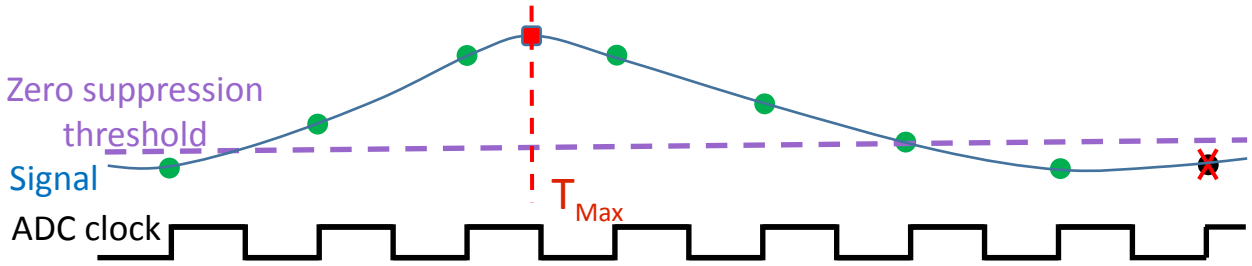


Required readout performance

- Threshold ~3 fC to get factor 10 on signal / threshold
- Noise level ~0.5 fC
- Readout time resolution << detector resolution (~10 ns or above)
- Stand channel occupancy ~10 kHz
- Resistant to mild radiation (10 krad, 10^{11} n_{eq}/cm^2) and magnetic field (1.8 T)

Readout strategy

- Analog amplification and shaping, continuous ADC readout
- Correction of baseline, common mode noise + digital shaping
- Zero-suppression: selection of samples above threshold + neighbors
- Integrated reconstruction of signal amplitudes and times
- Continuous readout mode, non-ZS samples sent to DAQ permanently



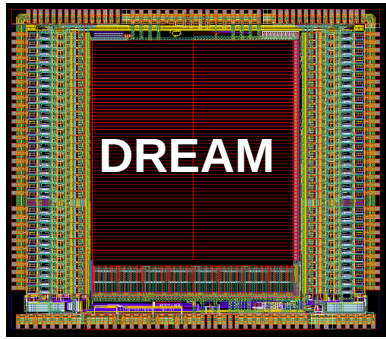
SALSA : VERSATILE READOUT CHIP FOR MPGD

Motivations of the SALSA project

- To develop a new versatile multi-channel readout chip in the framework of the EPIC MPGD trackers and beyond
  - for MPGD trackers but not only, also for MPGD TPCs, photon detectors,...
  - with possible future developments for other kinds of detectors (calorimeters, non-MPGD photon detectors) and/or specific constraints
  - adapted to both streaming readout DAQs and triggered ones
- Integrated per-channel sample ADC at high rate, and digital processing (DSP)
- Large ranges in term of signal amplitudes, electrode capacitances, peaking times, signal rates
- TSMC 65nm technology for improved performances and sustainability

Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Sao Paulo University (USP) + associated institutes designed the **SAMPA** chip (ALICE TPC), experts in on-chip ADC and digital processing
- IRFU developed several MPGD front-end chips (**AFTER**, **AGET**, **DREAM**,...) and other kinds of chips (**SAMPIC** and **HGCROC** TDC,..), experts in low-noise radiation-hard generic front-ends
- Large amount of complementary competences on front-end, on digitization and on digital processing
- Blocks developed by CERN in TSMC 65nm technology also reused



SALSA CHIP TARGET SPECIFICATIONS, COMPARED TO EPIC MPGD REQUIREMENTS

Versatile front-end characteristics → EPIC MPGD needs

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1 nF → **200 pF**
- Large range of peaking times: 50-500 ns → **100-200 ns**
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC → **0-250 pC**
- Large range of input rates, up to 100 kHz/ch with fast CSA reset → **< 25 kHz**
- Both polarities (depends on kind of detector) → **negative**

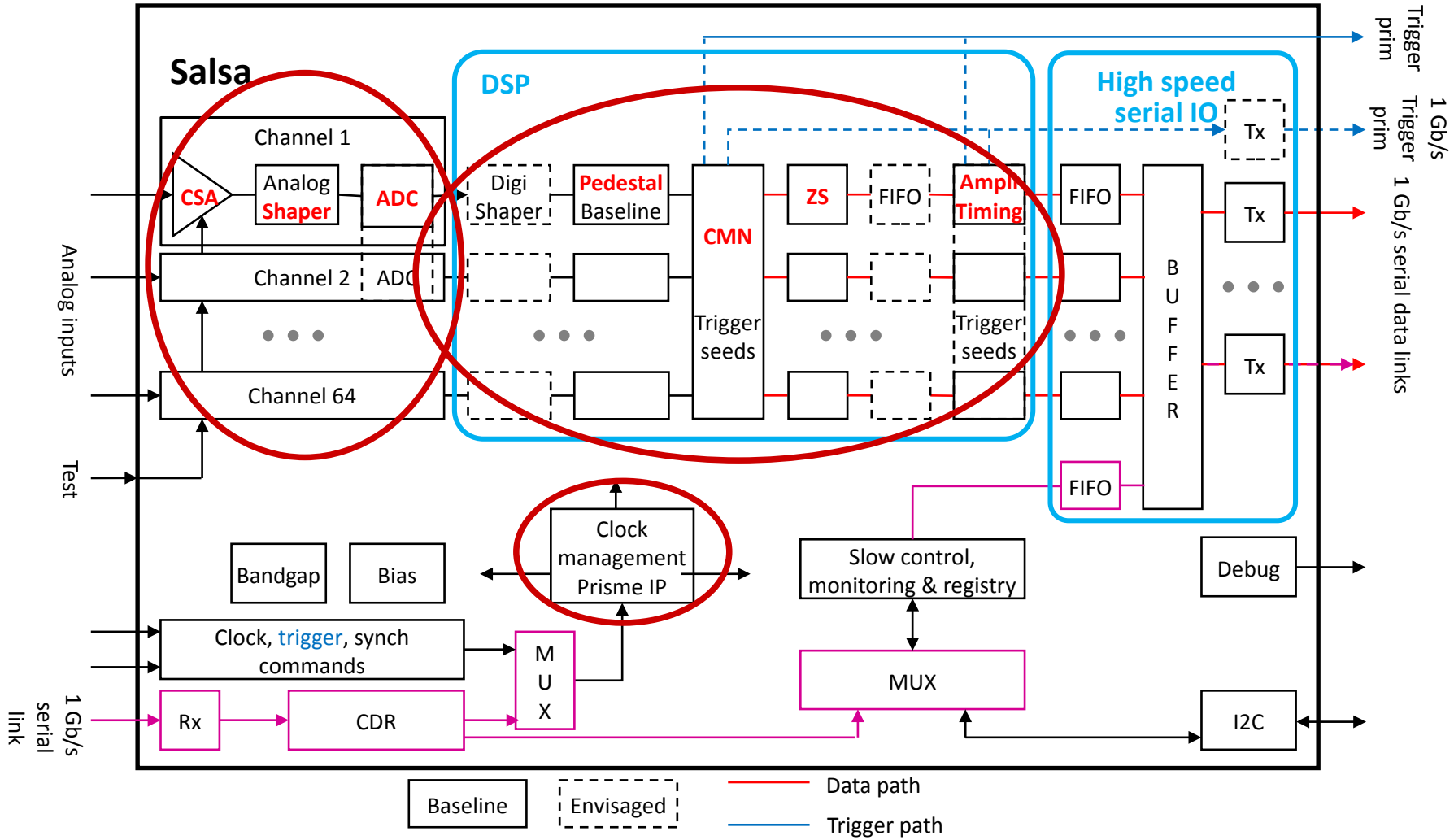
Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s → **50 MS/s**
- Integrated DSP for internal data processing and size reduction, treatment processes to be configured according to user needs → **all processes**
- Continuous readout, triggered mode also available → **continuous readout**
- Four 1 Gb/s output data links → **1 (or 2) gigabit link used at EPIC**

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, > 300 Mrad, > 10^{13} n_{eq}/cm^2) → **10 krad, 10^{11} n_{eq}/cm^2**

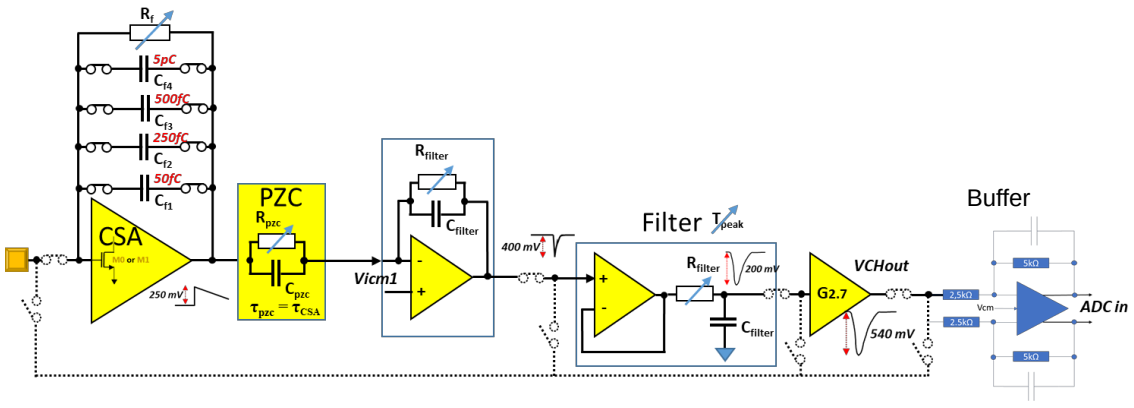
SALSA CHIP PRELIMINARY ARCHITECTURE



SIGNAL AMPLIFICATION AND DIGITIZATION

Front-end stage

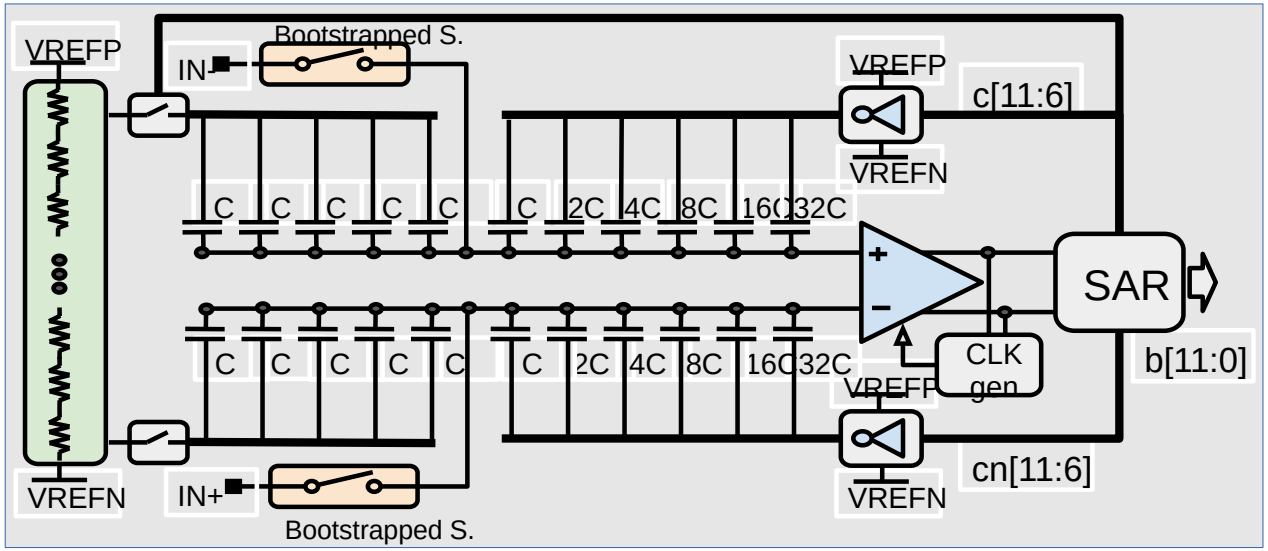
- Charge Sensitive Amplifier + Pole-Zero Cancellation + shaper
- 4 gain ranges: 0-50 fC, 0-250 fC, 0-500 fC and 0-5 pC
- 8 peaking times 50 to 500ns
- 2 polarities
- Integrated anti-saturation circuit
- Front-end elements can be by-passed
- Integrated test pulses



Scheme from P. Baron

ADC block

- 12 bits 5-50 MS/s SAR ADC
- Expected 10-11 ENOB bits
- Also evaluation of new ADC developed at IRFU for DRD7



Scheme from H. Hernandez

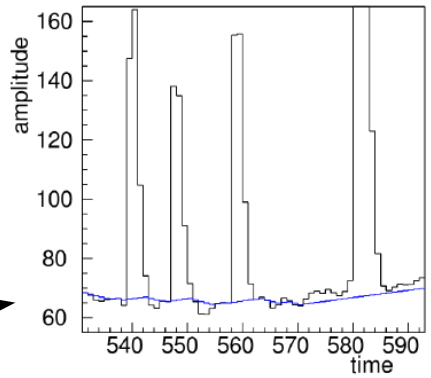
DSP DATA PROCESSING, PRELIMINARY VERSION

General remarks

- Data processing, reduction and formatting from ADC values to output links
- Each process can be deactivated individually by user
- Process parameters through ASIC registers
- Part of codes from SAMPA chip
- Most of DSP features determined, details still under study

Baseline corrections

- Pedestal subtraction with fixed value per channel
- Common mode correction to reduce common noise impact, based on median value of samples of all channels for each sample time
- Baseline slope following algorithm



Plot from SAMPA doc

Digital shaping

- Cancellation of signal tail or peaking time correction with cascade of 4 first order IIR filters
- Algorithm from SAMPA, 2 x 4 parameters

$$y[n] = a_1 y[n-1] + b_0 x[n]$$

DSP DATA PROCESSING, PRELIMINARY VERSION

Zero suppression

- Keep samples above fixed thresholds
- Tunable algorithm (add neighbor samples, to drop too short set of samples, keep 1 sample over N, etc...)

Feature reconstruction

- To further reduce data flux by extracting reconstructed data → peak finding algorithm, with extraction of amplitude + time + width
- Peak finding and data extraction algorithms under study

Trigger management

- Samples kept when trigger signals received, with configurable latency
- Followed or not by zero suppression, feature reconstruction, etc…

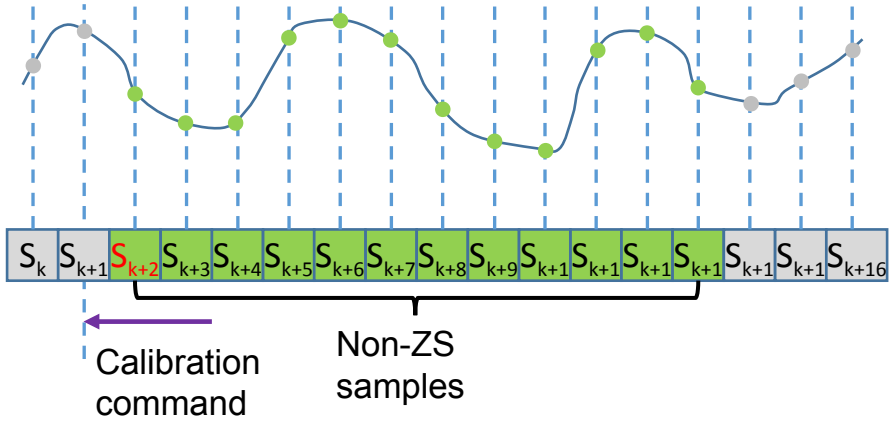
Trigger generation

- Trigger primitives generated when samples above threshold, with conditions on number of samples, multiplicity, etc...
- Possibility to reduce latency by placing trigger generation early in the processing chain
- Nature of trigger primitives to be defined (logic signal, data on specific fast link, etc…)

DSP DATA PROCESSING, PRELIMINARY VERSION

Calibration data

- Generated on demand with specific synchronous commands
- Generation of calibration data of several types
  - non-ZS data
  - test pulses injected at front-end on one or several channels



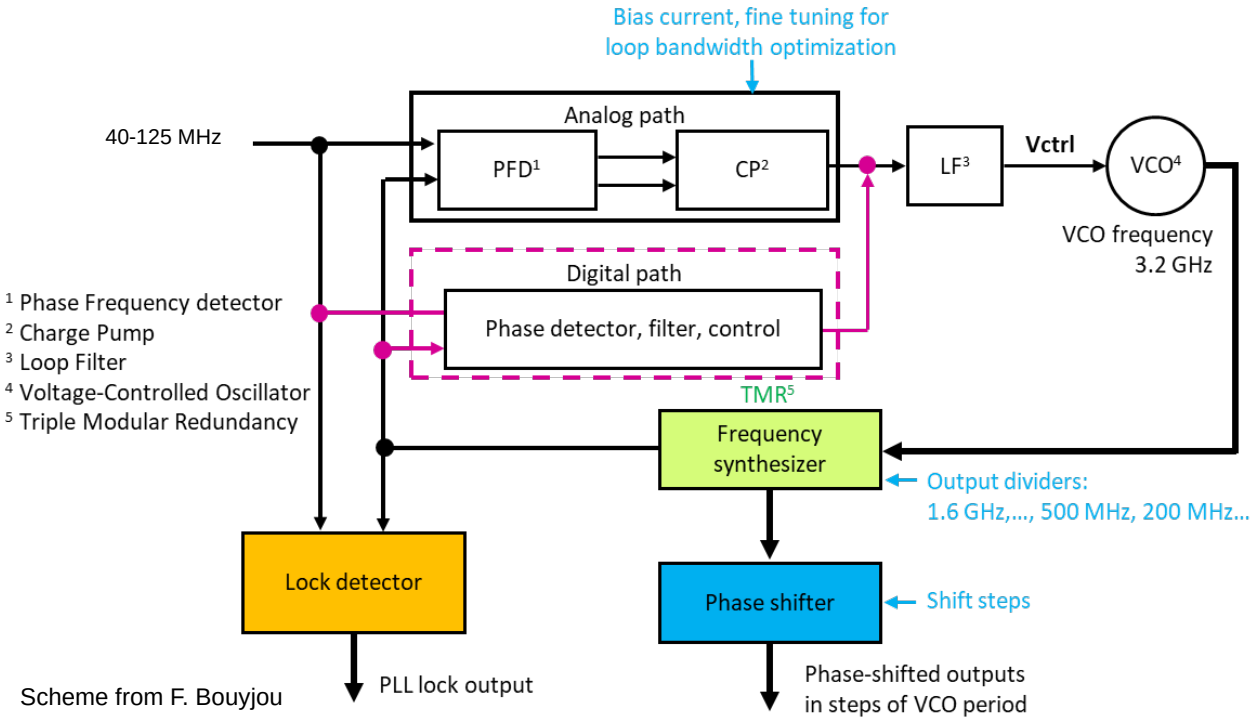
Information data

- Monitoring data like chip configuration, internal chip status (currents, voltages), environmental data (temperature, radiation, etc...)
- Slow-control responses
- Software scaler histogram to evaluate occupancy per channel
- Generated on demand with specific synchronous commands and/or slow-control

SALSA CLOCK MANAGEMENT

Development of the "PRISME" 65nm PLL IP block for clock generation

- No existing PLL block fitting our requirements in TSMC 65nm technology
- Large frequency ranges for input (40-125 MHz) and outputs (up to 1.6 GHz)
- Low power and radiation hardness capability
- Hybrid PLL mixing analog and digital paths, with 3.2 GHz VCO frequency
- Very low internal time jitter: ~3 ps RMS up to 1 GHz
- 4 clock outputs each with programmable frequency and phase
- This block will be available for HEP community



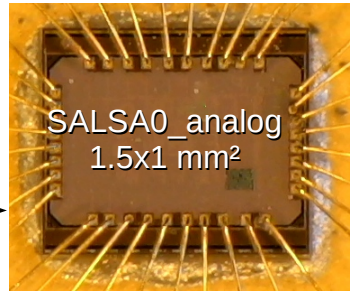
Scheme from F. Bouyjou

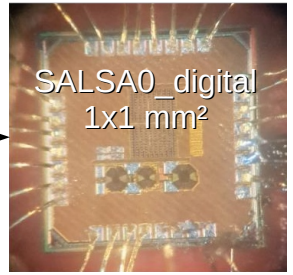
Technology	CMOS 65 nm
Power voltage	1.2V
Input reference frequency range	40-125 MHz
VCO frequency	3.2 GHz
Number of output clocks	4
Output frequency	Programmable fractions of VCO frequency, up to 1.6 GHz
Phase shifter step	< 300 ps
Time interval jitter: analog path only	< 10 ps RMS up to 1 GHz with graceful degradation beyond
Time interval jitter: with digital paths	~3 ps RMS up to 1 GHz with graceful degradation beyond
Power consumption	< 3 mW, < 6 mW with digital regulation
Size	~0.1 mm²
Radiation mitigation	TMR, SEL free, TID up to 4 MGy

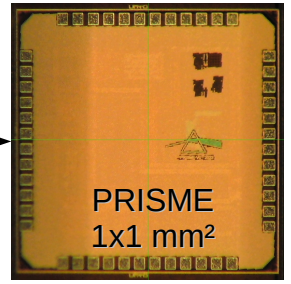
TIMELINE OF THE SALSA PROJECT

Steps of SALSA development

- 2020-22: Discussions and reflections on the project
- 2022-23: **SALSA0** prototypes to study first designs
  - **SALSA0_analog** featuring 4 front-end channels
  - **SALSA0_digital** featuring an ADC block
- 2023: **PRISME** prototype to test PLL block + first version of general services (blocks partly from CERN)
- 2023-24: **SALSA1** prototype to test full front-end + ADC chains
- 2023-25: **SALSA2** prototype to test fully featured ASIC including DSP, but with small number of channels (≤ 32)
- 2025-26: **SALSA3** as pre-serial prototype with nominal number of channels

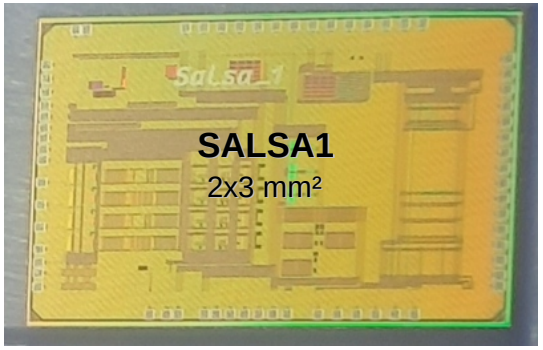






Current status

- **SALSA0** prototypes tested in 2023-2024, performance evaluation and bug fixes of frontend and ADC blocks
- **PRISME** prototype tested from early 2024, bug fixes on PLL block, performance evaluation ongoing, radiation tests in November
- **SALSA1** prototype submitted April 2024, produced, packaging ongoing
- **SALSA2** architecture and DSP design ongoing, submission foreseen ~ March 2025



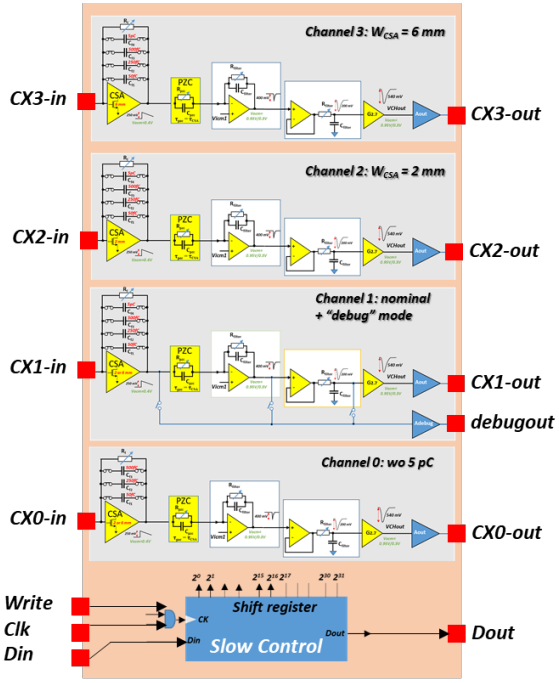
TESTS ON FRONT-END STAGE

SALSA0_analog prototype

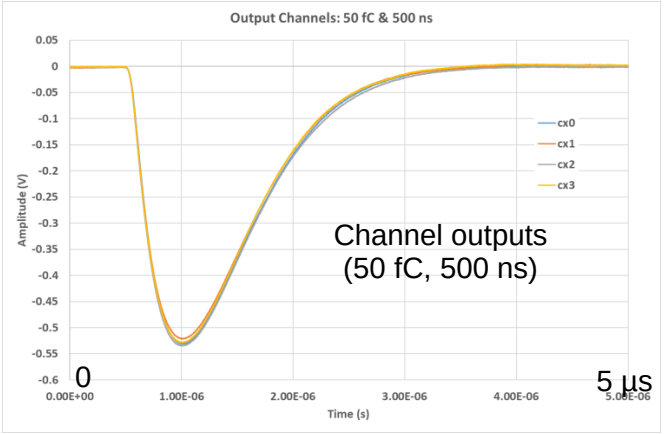
- 4 front-end channels with slight differences between them
- CX1 channel with debug output for monitoring
- CX0-2-3 with different input transistors, CX0 without 5 pC gain range

Test results

- Test-bench with configurable input capacitance, input signal generation with configurable amplitude and rate, programmable oscilloscope, etc...
- Almost all configuration parameters (gains, peaking times, anti-saturation,...) tested ok
- Measurements in agreement with simulations: bias currents, power consumption, DC values, etc...
- Some discrepancies concerning transfer functions and noise levels especially at 50 fC gain range
- Origin due to parasitic resistances in the chip, understood and reproduced in simulations. Corrected in the CSA design for SALSA1

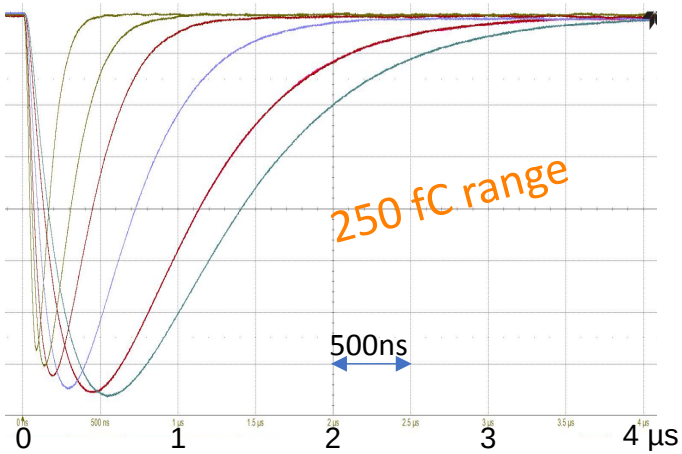


Scheme from P. Baron

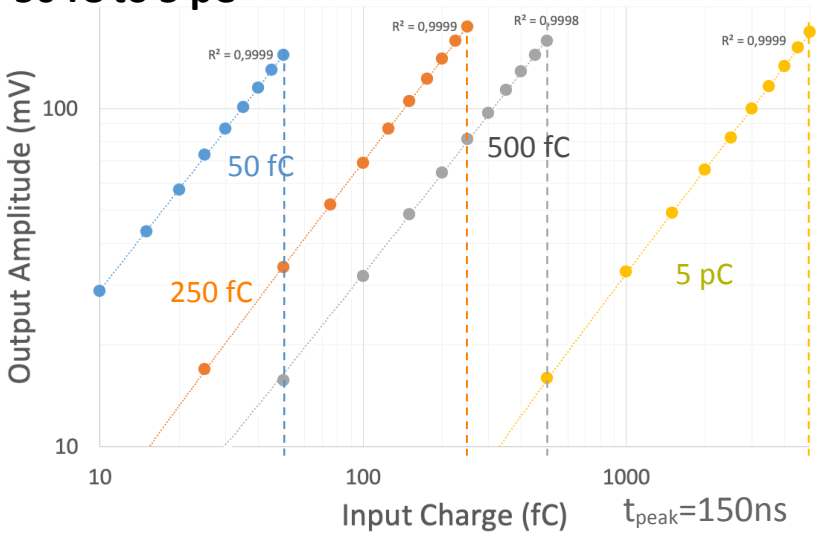


MAIN RESULTS WITH 120 PF INPUT CAPACITANCE

Peaking time programmable from **50 ns to 500 ns** with no tail

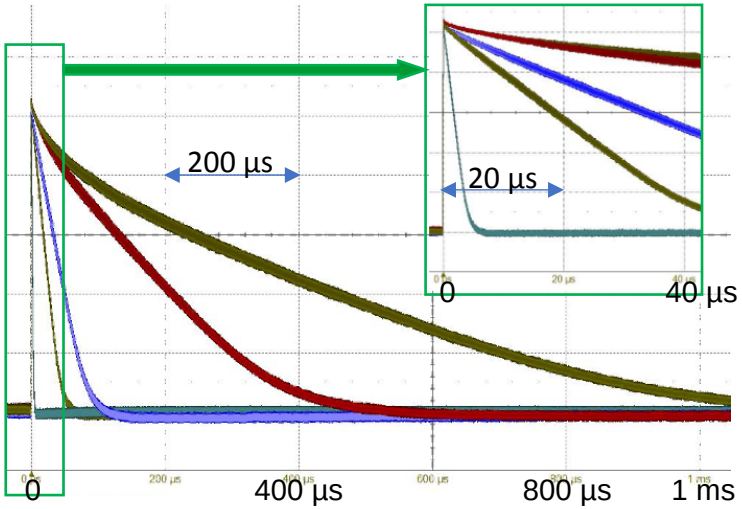


Gain programmable => dynamic range from **50 fC to 5 pC**

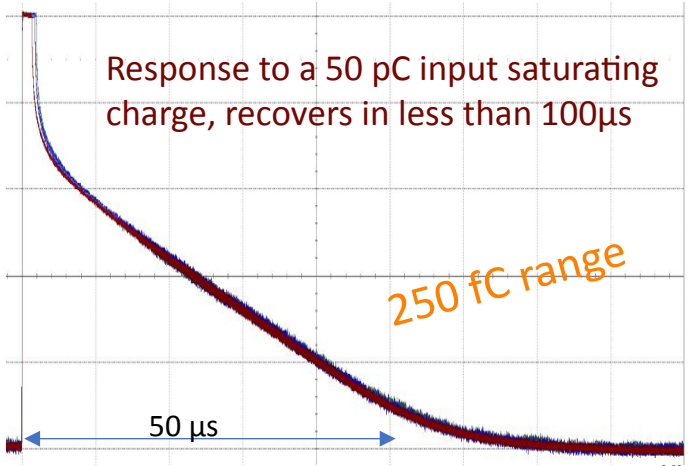


Preliminary

T_{fall} CSA programmable from 5 µs for high rate to 1 ms for low noise



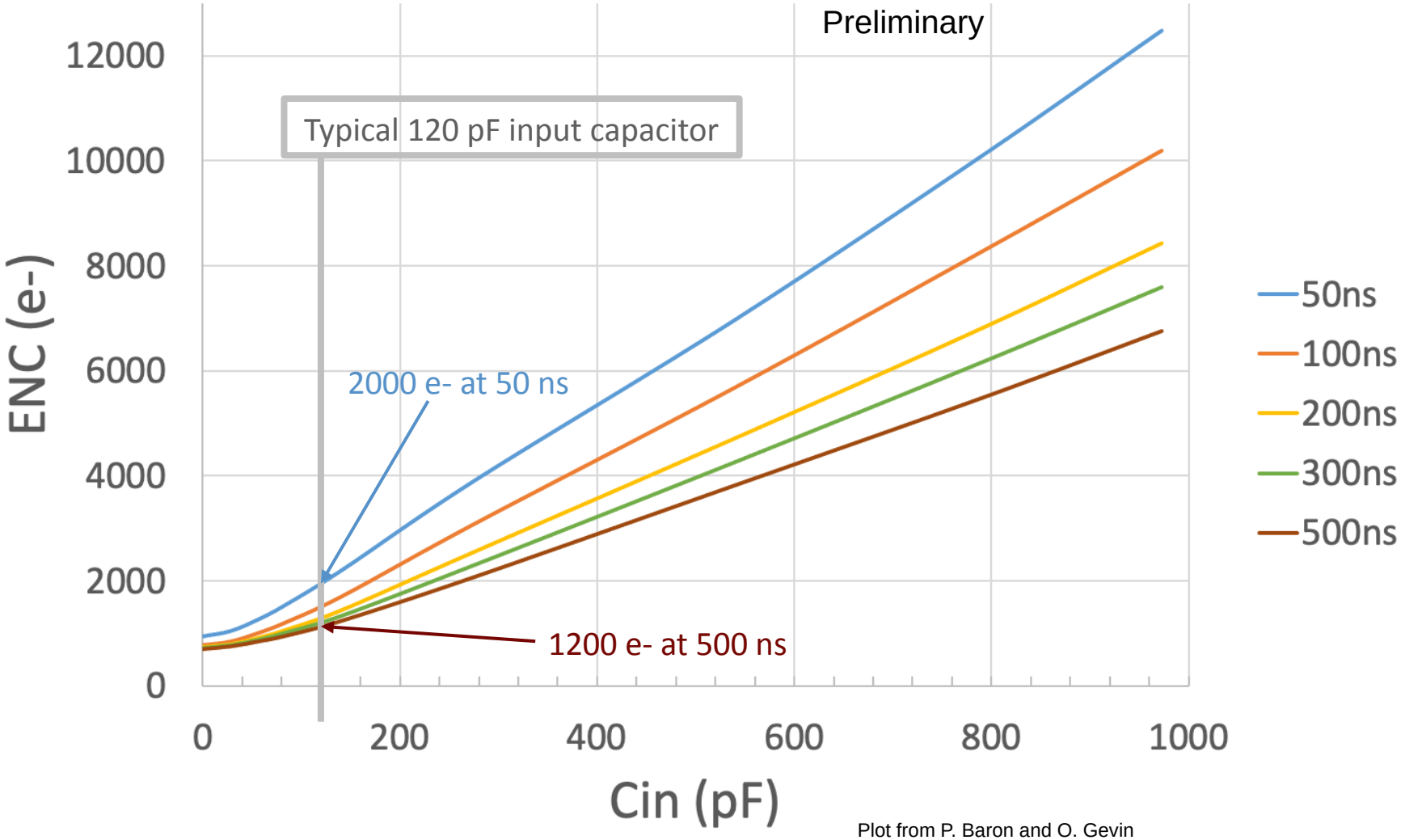
CSA anti-saturation circuit => **fast recovering**



Plots from P. Baron and O. Gevin

MAIN NOISE RESULTS: TYPICAL CASE

Equivalent Noise Charge in the **250 fC range** at different peaking times

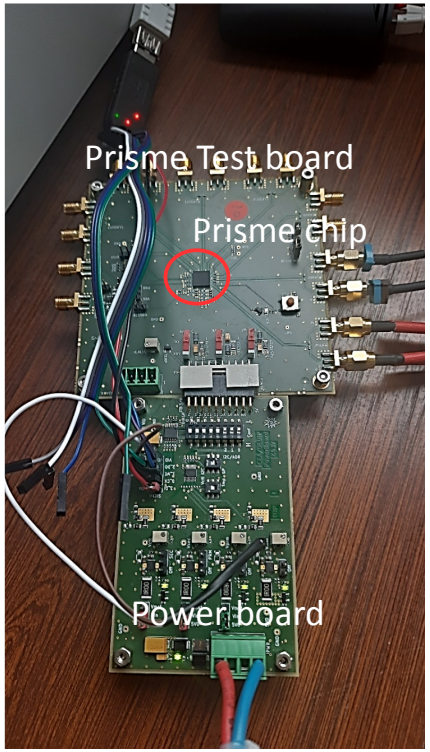


Plot from P. Baron and O. Gevin

STATUS OF PRISME PLL PROTOTYPE

Test bench

- Power boards + PRISME test boards
- Low jitter clock generator from CERN + high precision signal generator, high end 80GS/s scope and phase noise analyzer

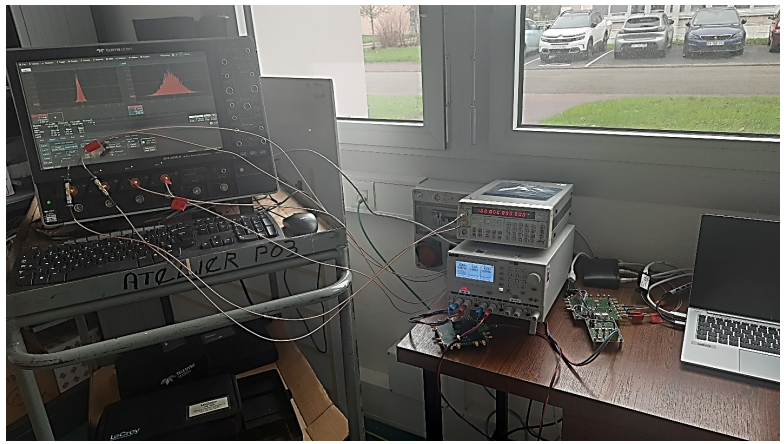


Generic results

- I2C working to read and write registers
- Temperature probe ok, radiation probe ok
- LVDS high speed I/O interface ok up to 1.2 Gb/s
- Clock outputs with adjustable phase and frequencies ok
- Radiation TID tests foreseen in November

Tests on PLL block

- PLL block functional with digital branch working as expected, nominal internal 3.2 GHz reached
- Wide input frequency range achieved 80-105 MHz
- Random jitter component as low as 2.5 ps RMS
- But deterministic component larger than expected, up to 50 ps RMS
- Origin identified in simulation from low frequency noise of 3 GHz oscillator
- Solution found, design corrected
- Possible updated chip to be submitted end of 2024



CONCLUSIONS AND PROSPECTS

Present status

- Specifications of DSP almost finalized. Still open to suggestions
- SALSA0 and PRISME prototypes with promising performance measurements; helpful to fix bugs, and verify simulations
- SALSA1 prototype (front-end + ADC) produced, tests starting in November
- SALSA2 prototype (fully featured, reduced number of channels) development ongoing: DSP architecture and features
- Grant from EIC eRD109 R&D and Generic EIC R&D programs
- Grant from French and Brazilian ANR and FAPESP research agencies obtained in 2024

Next steps

- Completion of tests on PRISME prototype, radiation tests in November
- Tests of SALSA1 from November 2024
- Submission of SALSA2 in 2nd quarter 2025
- Design of SALSA3 pre-serial ASIC in 2025, production and tests in 2026
- Full production in 2027, 5000 ASICs foreseen for EPIC, probably more produced for other projects
- Compatible with the EIC project timeline
- Expressions of interest welcome !