EICROC ASIC: status and plans

EIC France 10 oct 2024

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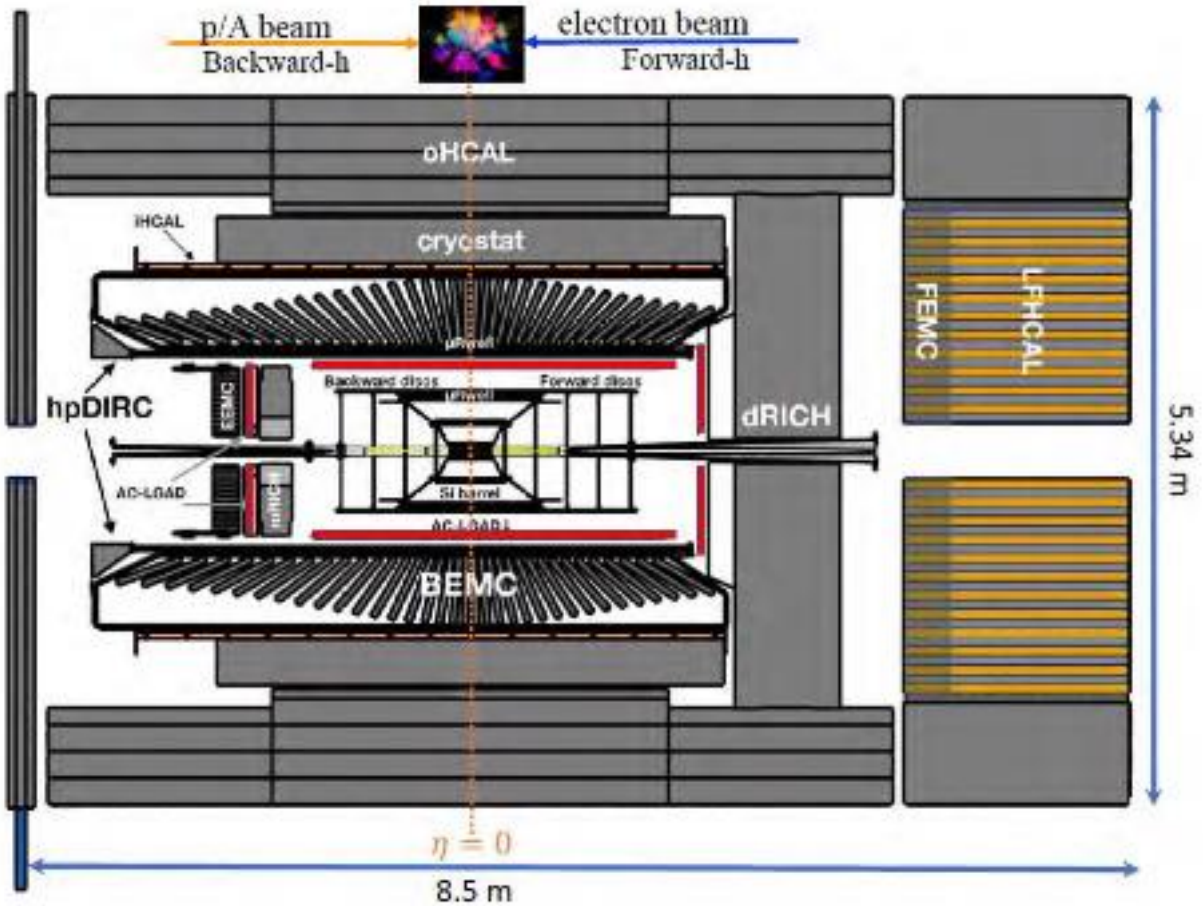
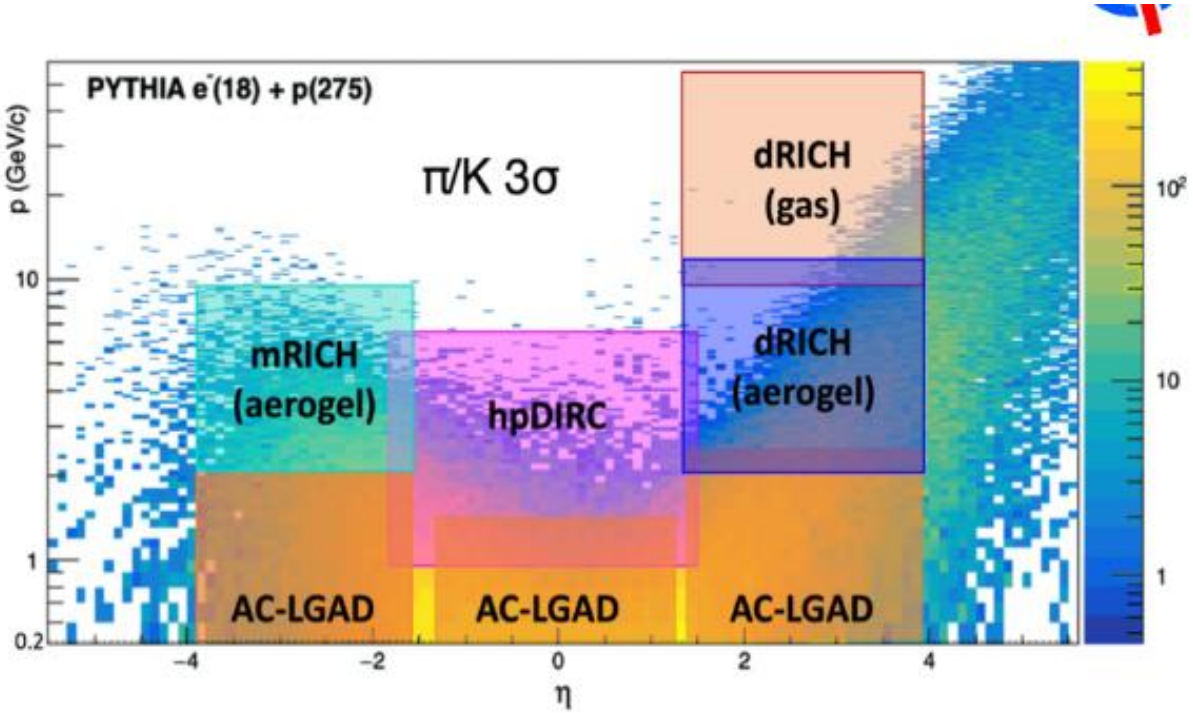
Organization for Micro-Electronics desiGn and Applications

EIC ToF detectors

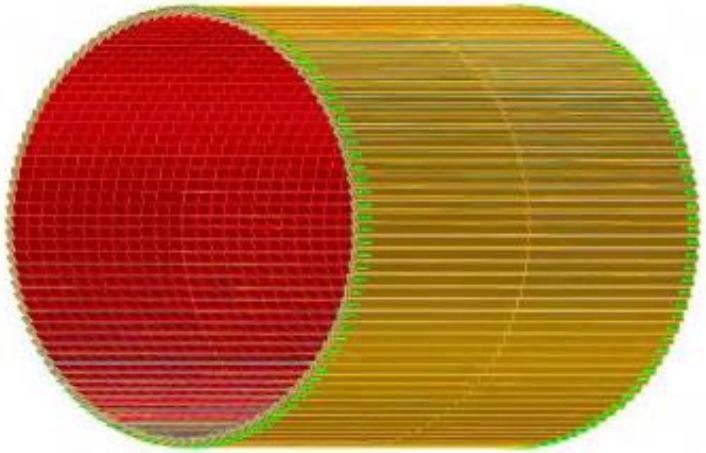




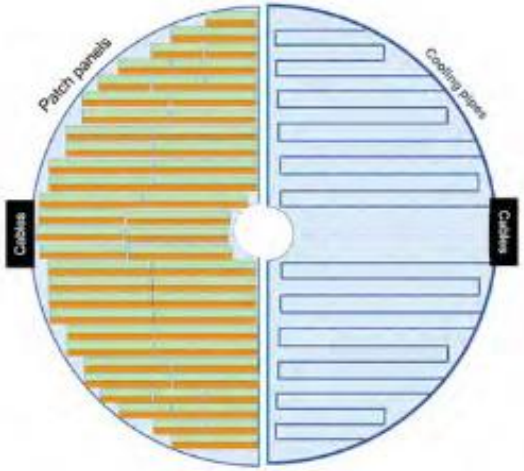
Specifications of ePIC AC-LGAD detectors

From S. Nanda : https://indico.cern.ch/event/1232761/contributions/5321425/

BToF



FToF



Roman Pots

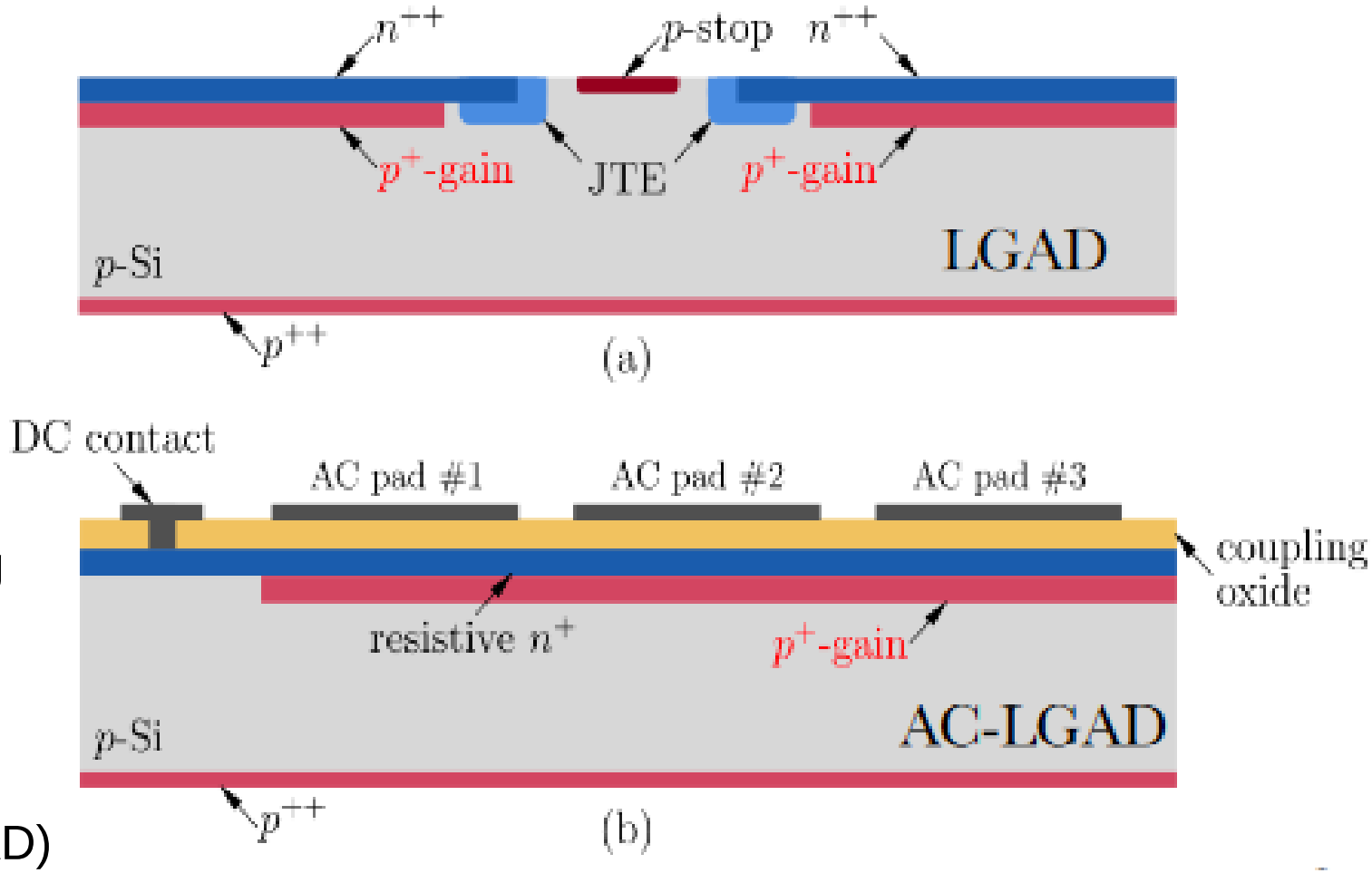
4D Trackers

	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10.9	0.5*10 (strips)	2.4M	30 ps	30 μm in φ	0.01 X0
Forward TOF	2.22	0.5*0.5 (pixels)	8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5 (pixels)	0.28M	30 ps	20 μm in x and y	0.05 X0
RPs/OMD	0.14/0.08	0.5*0.5 (pixels)	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

DC LGAD and AC LGAD

- MIP timing detectors (HGTD, ETL) use DC LGAD sensors
  - ~10 fC/MIP
  - Area : (1.3 mm)²
  - Good timing resolution : 30-50 ps
  - Poor position resolution : ~400 µm
  - « dead zone » between pixels

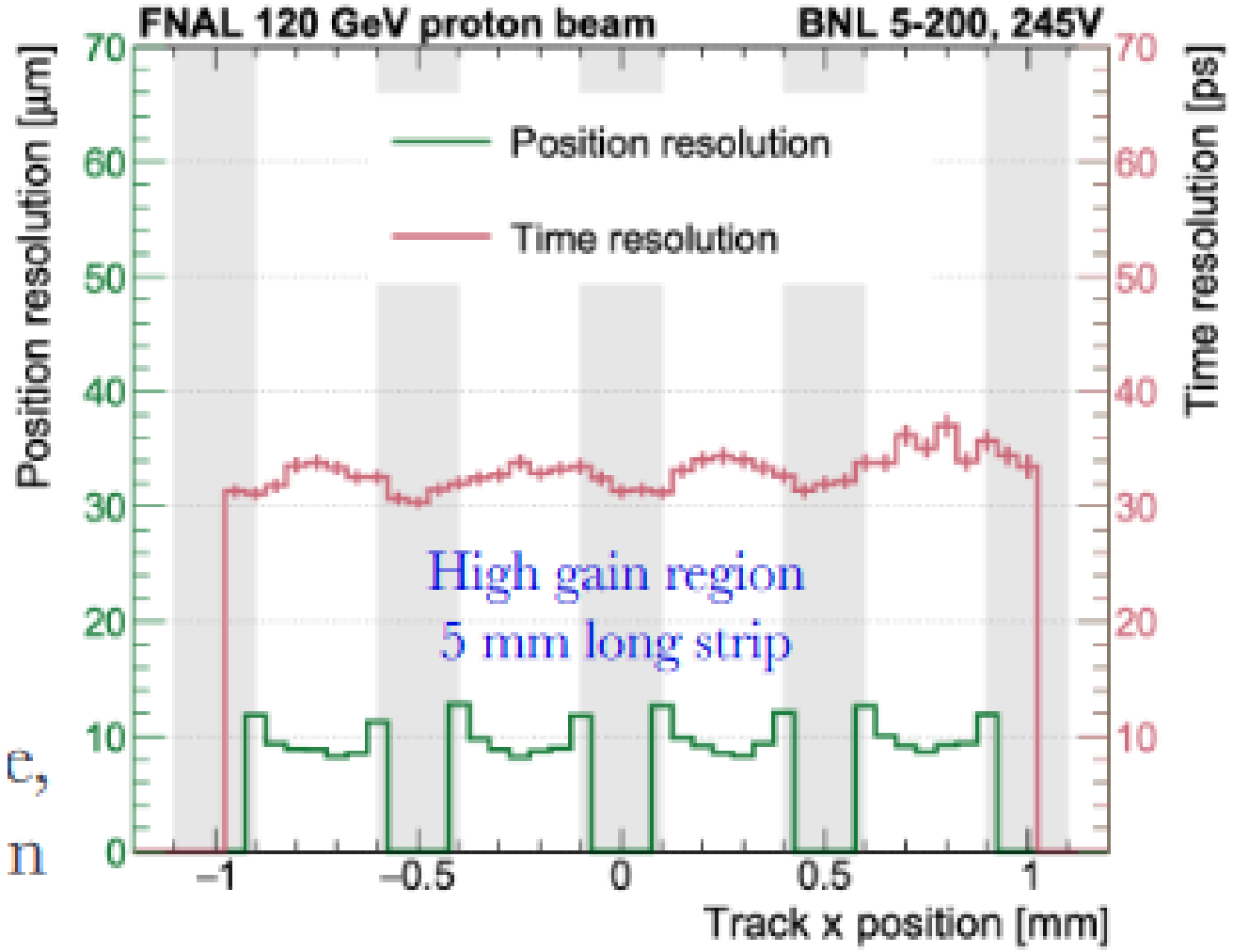
- AC LGADs for EIC
  - Resistive layer to get signal sharing
  - Area (500 µm)²
  - Good position resolution : < 50 µm
  - No dead area
  - Good timing resolution (as DC LGAD)



AC LGAD performance

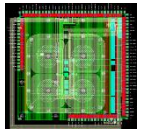
- Here for strips : 500 µm x 5 mm
  - ~30-35 ps timing resolution
  - ~10 µm position resolution
  - Oscilloscope readout
  - Still preliminary results and improvements underway on gain uniformity
  - Chosen as baseline for several EIC detectors

- New and promising detector



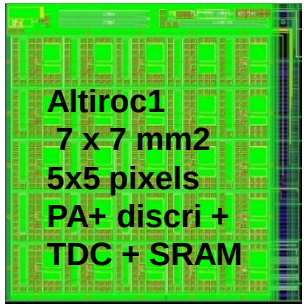
Experience in ATLAS HGTD Timing detector: ALTIROC (TSMC 130n)

2016



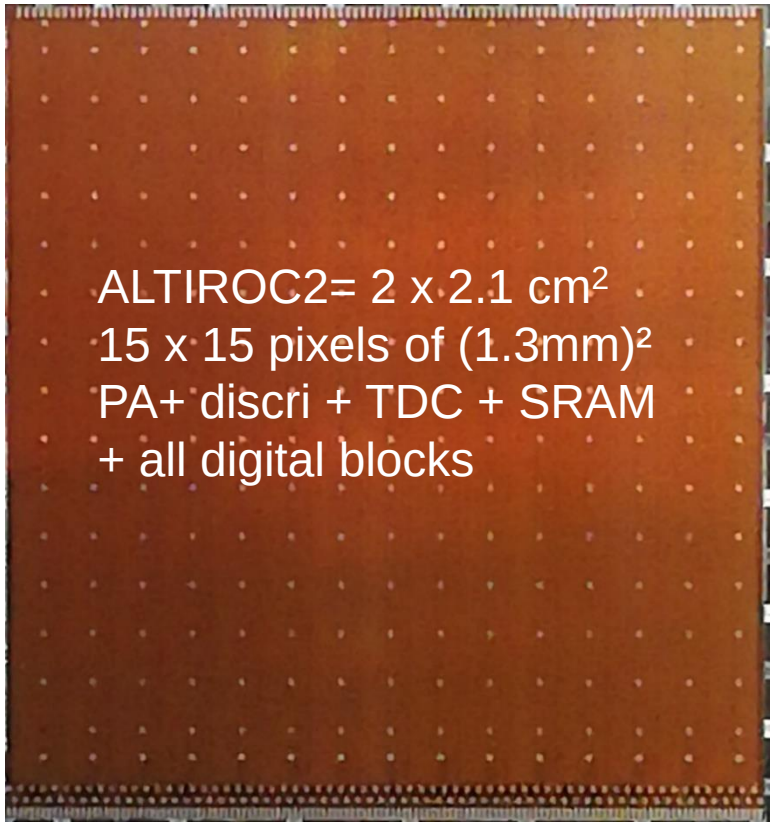
Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

2017



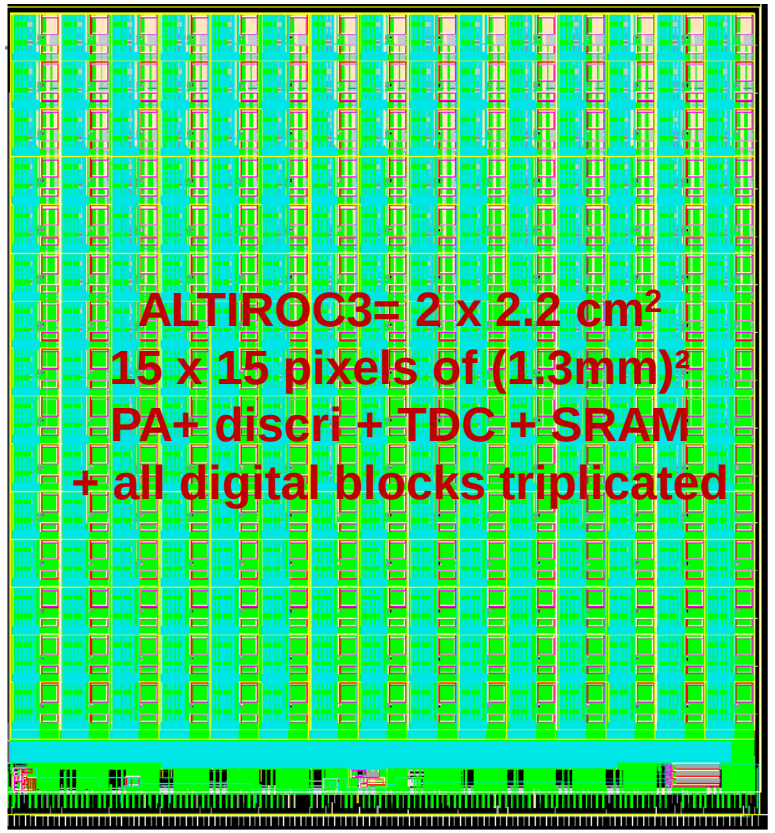
Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

2019



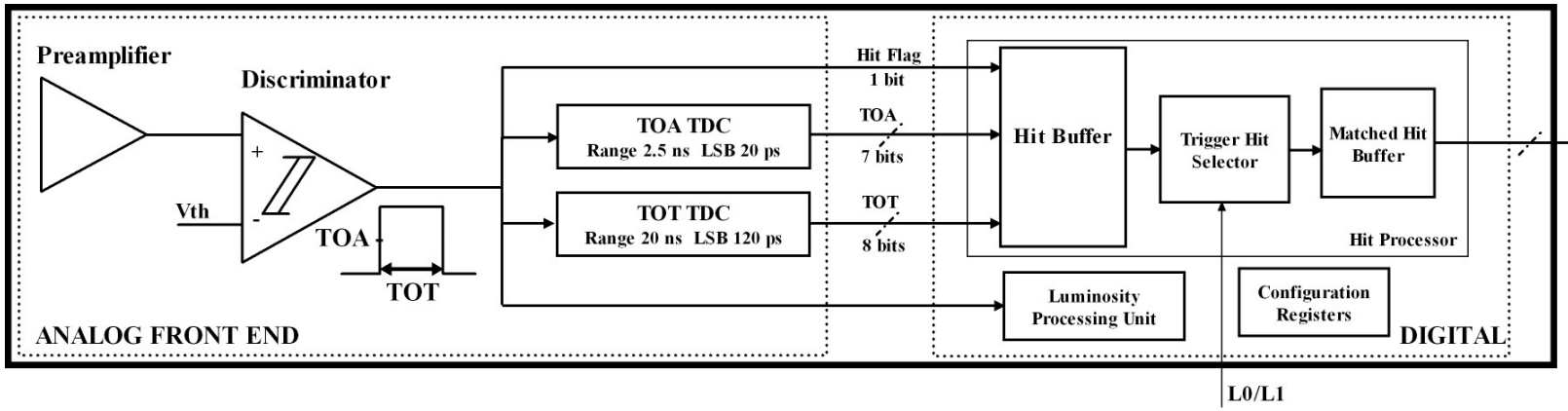
ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

2022



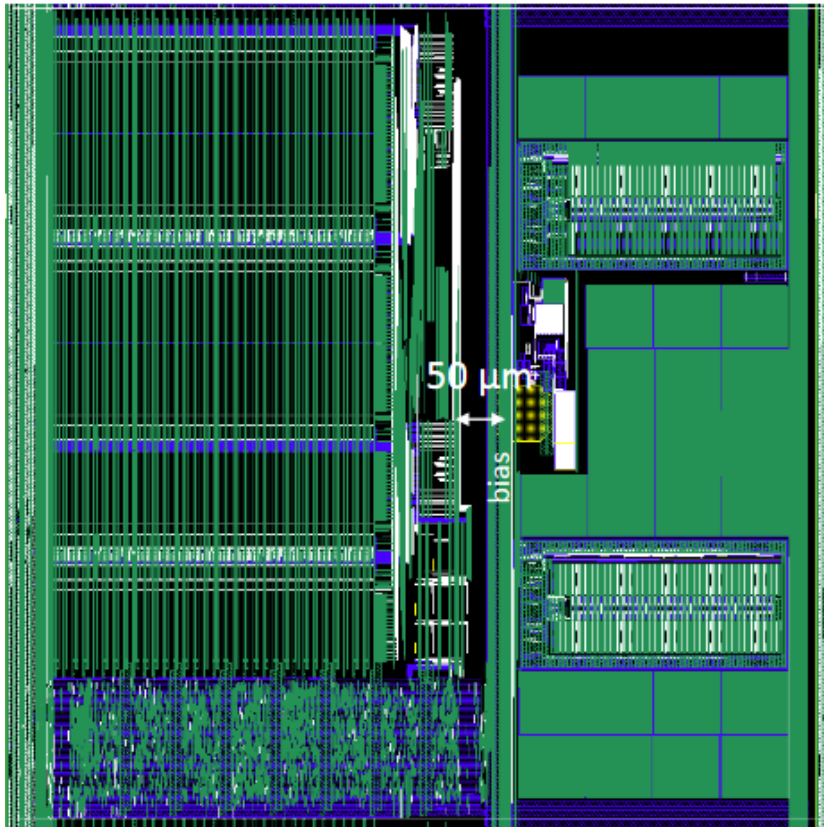
ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

ALTIROC pixel scheme and layout



HGTD detector
1.3 x 1.3 mm² DC LGAD sensors

One pixel : 1.3x1.3mm²

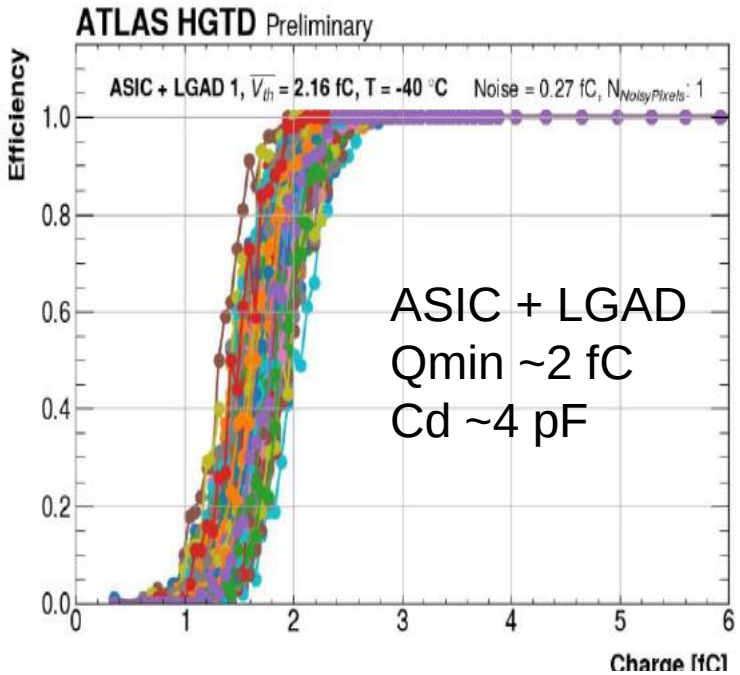


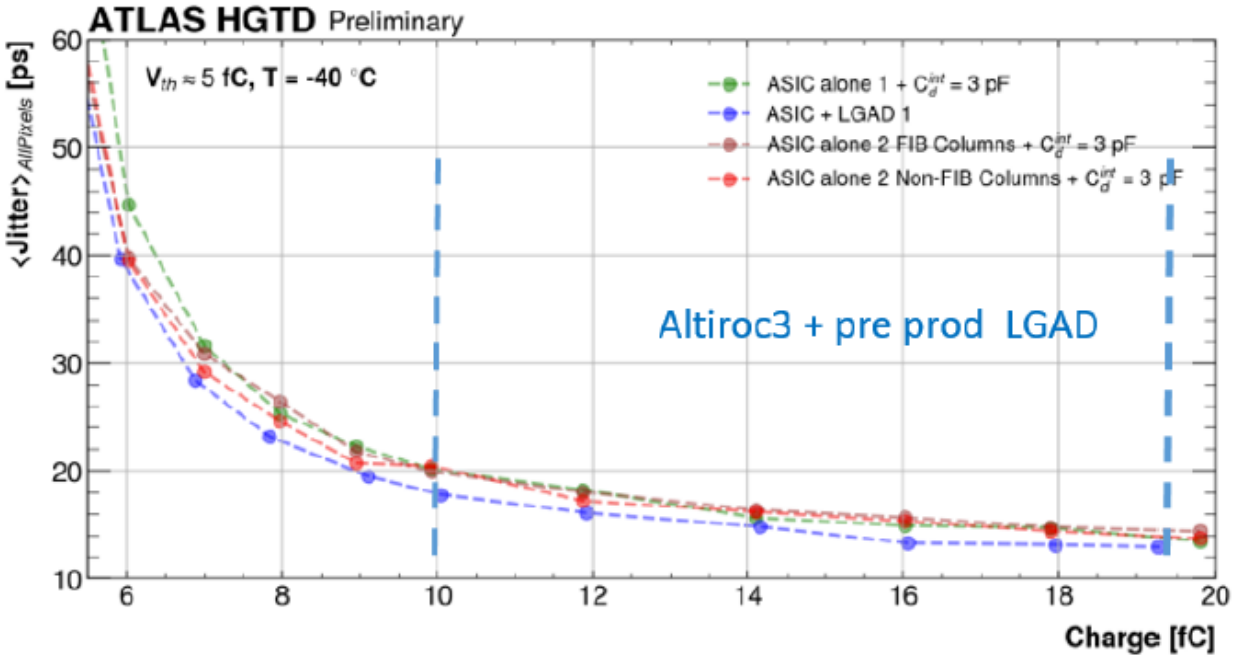
- **1 GHz preamplifier and discriminator**
  - Transimpedance architecture.
  - < 1 mW power preamp + discri

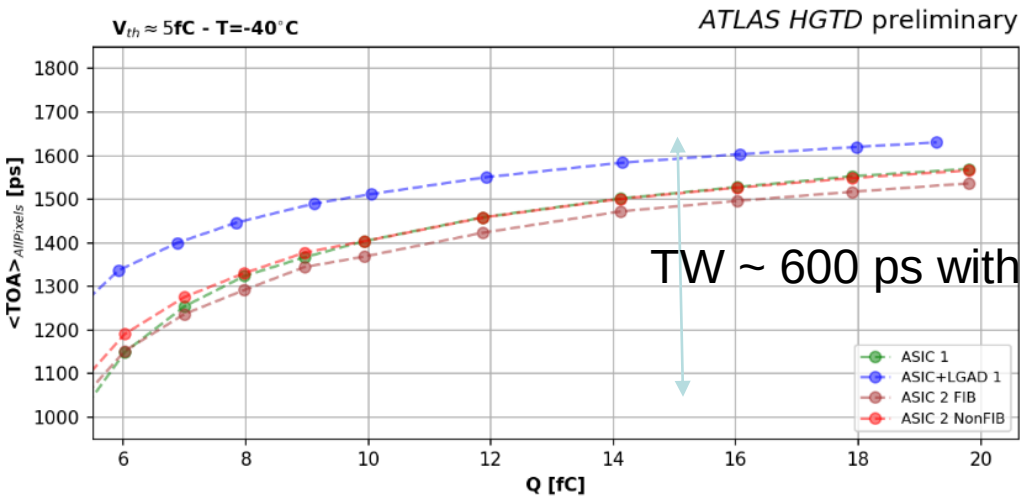
$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

- **2 vernier TDCs for ToA and ToT**
  - ToA 20 ps bin 7 bits dynamic range (2.5 ns)
  - ToT 40 ps bin 9 bits range (25 ns)
- **Hit buffer:** SRAM 1536 x 19 bit (38 µs latenccy)
  - Circular buffer to store timing data for each bunch-crossing, until a L1 trigger arrives
- **Matched Hit Buffer:** 16 positions FIFO
  - Control Unit: looks for data related to a trigger event when requested by the End Of Column
- **Luminosity process unit**
  - checks if hits are within 2 programmable windows
- **I2C configuration registers**

ALTIROC performance with DC LGAD sensor : test pulse injection



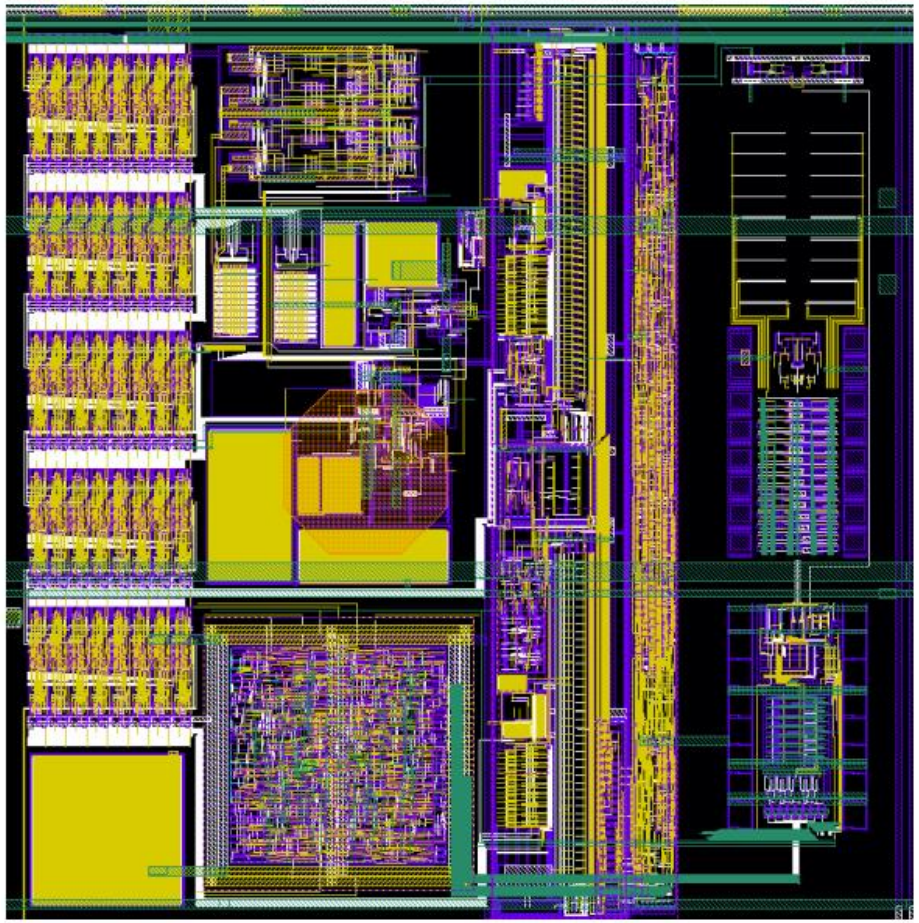


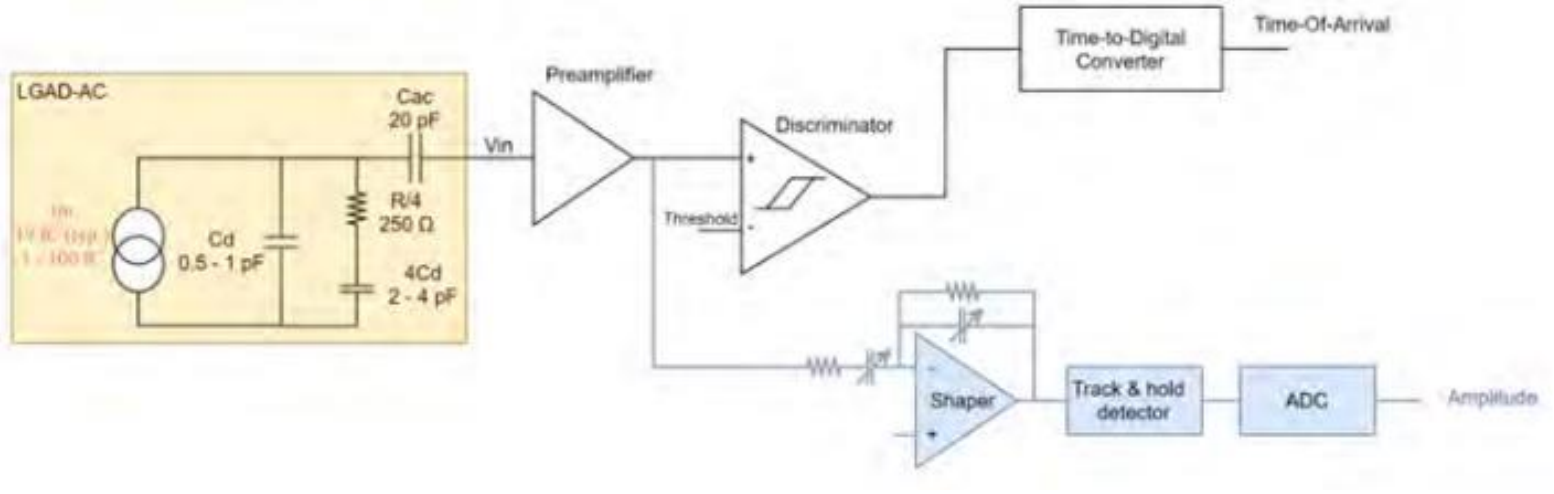


TW ~ 600 ps with a calibration signal that mimics an LGAD signal

Adaptation to EIC : EICROC

- Shrink into 500 x 500 µm
- Analog frontend similar to ALTIROC
- Need ADC instead of ToT for charge measurement 8-bit 40 MHz from AGH Krakow
- TDC taken from HGCROC by CEA Saclay
- I²C configuration
- Simple digital readout



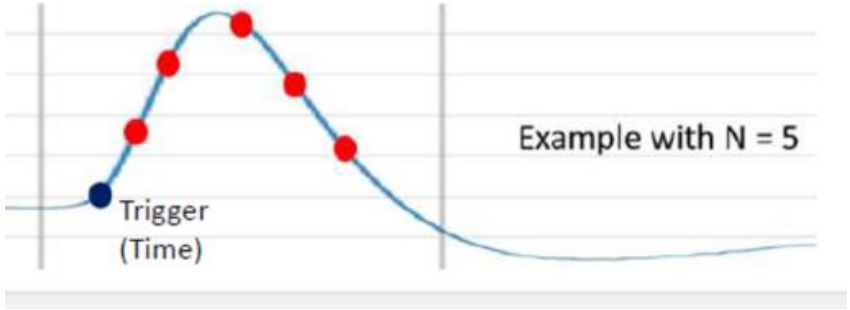


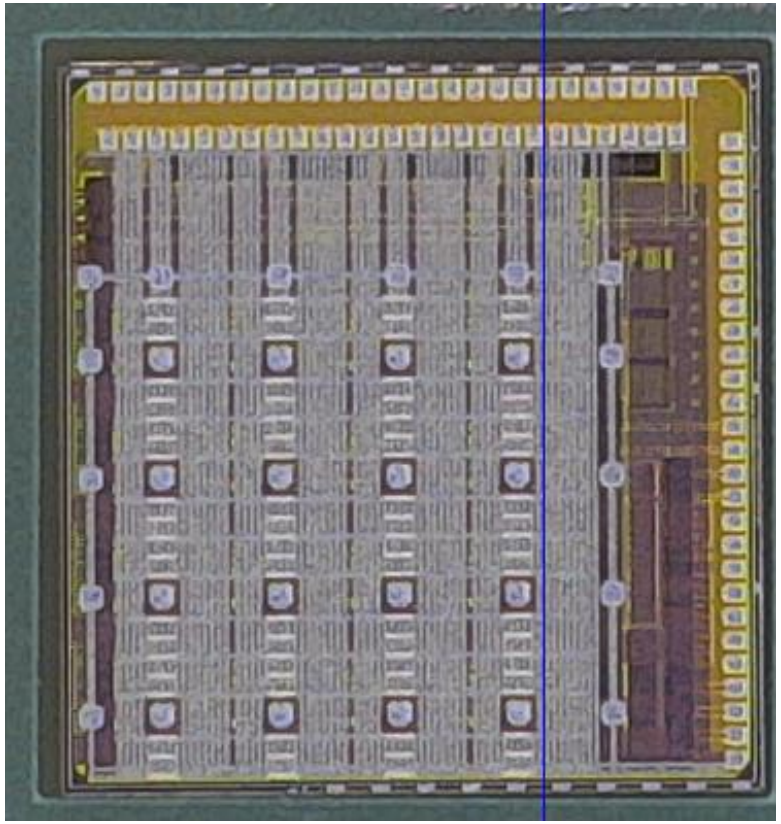
Slow control | PA +discri | TOA TDC | 8b 40M ADC

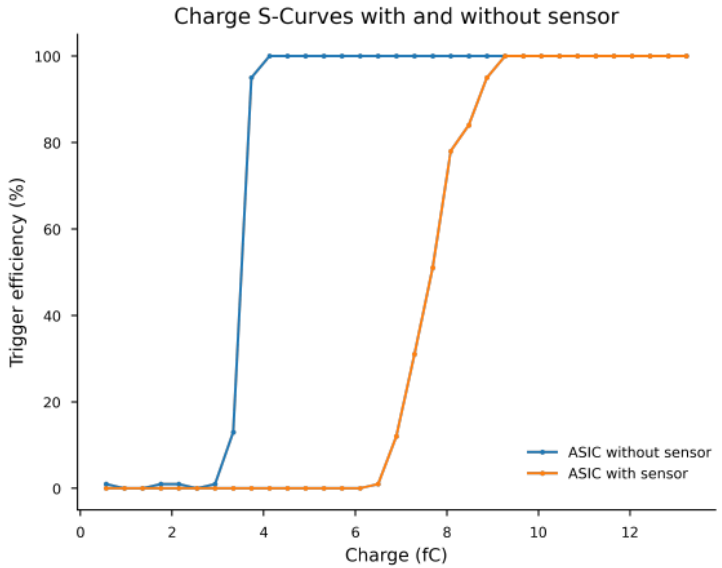
OMEGA Microelectronics | Irfu | AGH

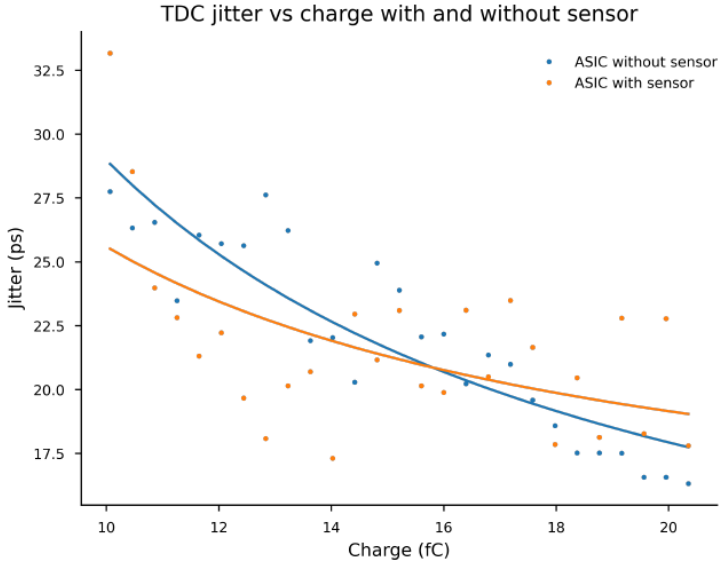
EICROC0 : 4x4 pixels

- EICROC0 : 4x4 test chip for (500µm)² pixels
  - Readout : TDC data and 8 ADC values
  - Performance : see talk by Arzoo







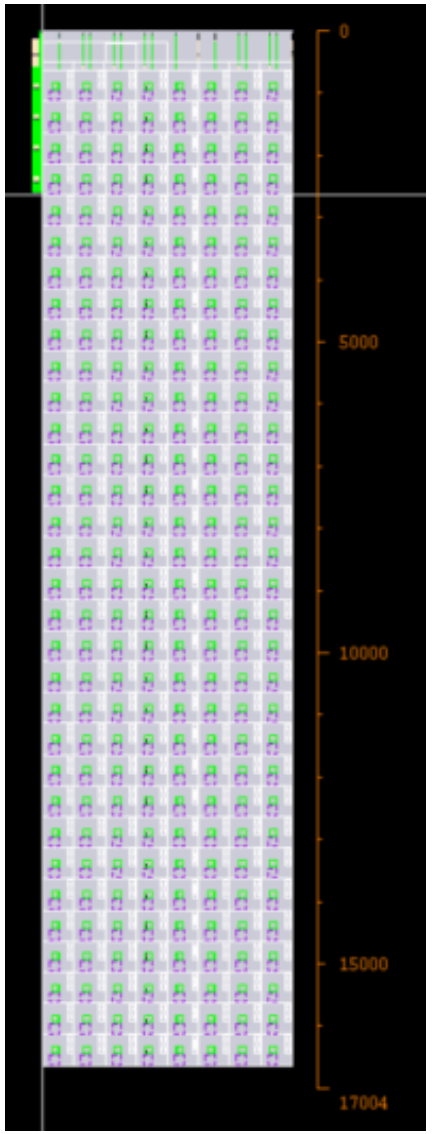


EICROC1 8x32 or 32x32

- EICROC1 : 8x32 = 256 pixels or 32x32 = 1024
  - Layout complete. DRC/LVS OK
  - Still EICROC0 digital architecture and Readout
  - 2/8 data outputs : 1 for 128 pixels (4x32)
  - Looking to increase R/O speed. Possibility to skip pixels by SC
  - Looking to improve testability.
  - Verifications in progress (~2 months)
  - 32x32 would allow tests with final sensor

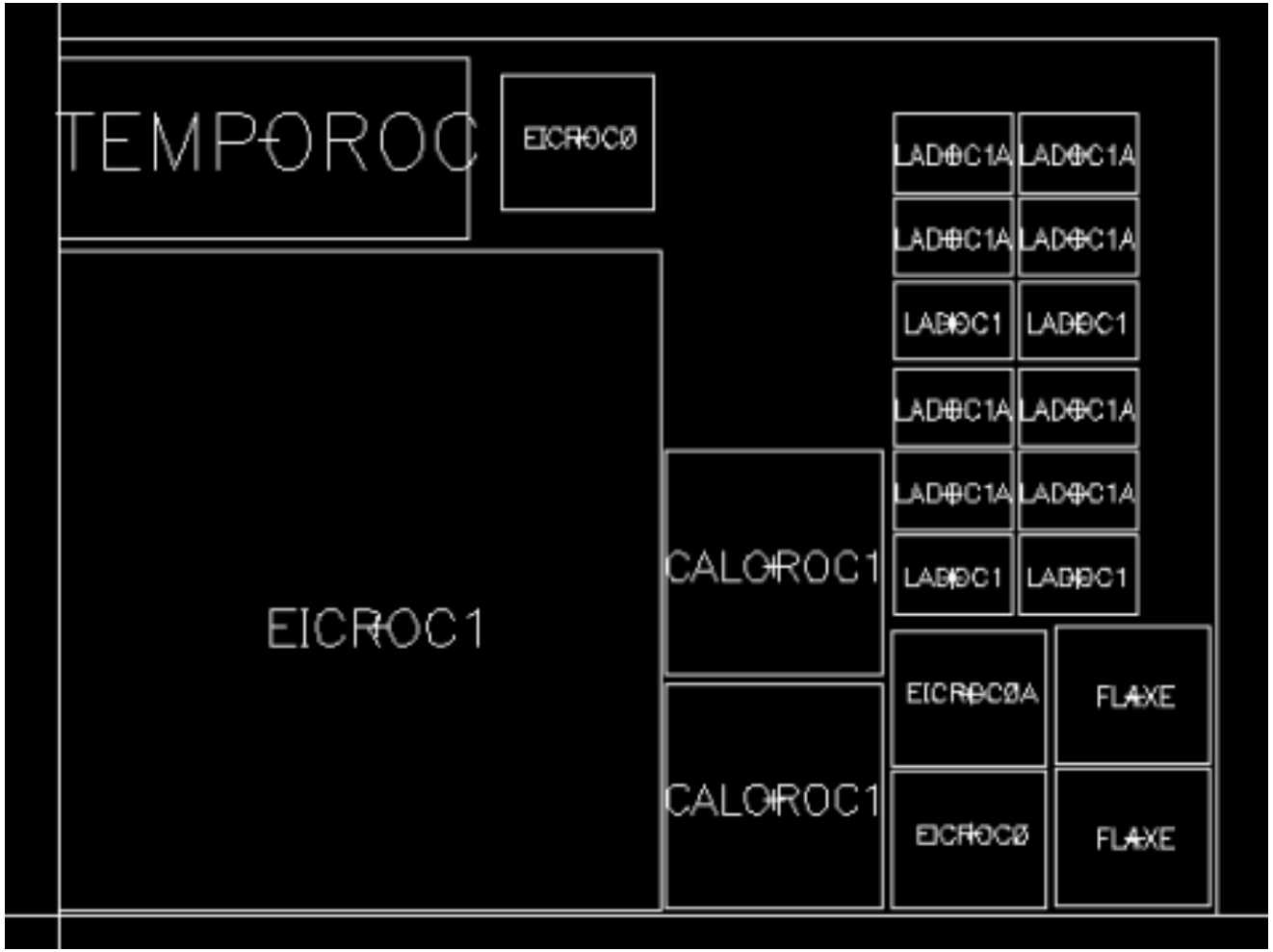
- EICROC1 addresses floorplan issues
  - Power drops along column, threshold uniformity
  - TDC uniformity and dependance on number of channels triggering

- Variants of EICROC0 will also be submitted
  - Lower power in the ADC branch (100 µW)



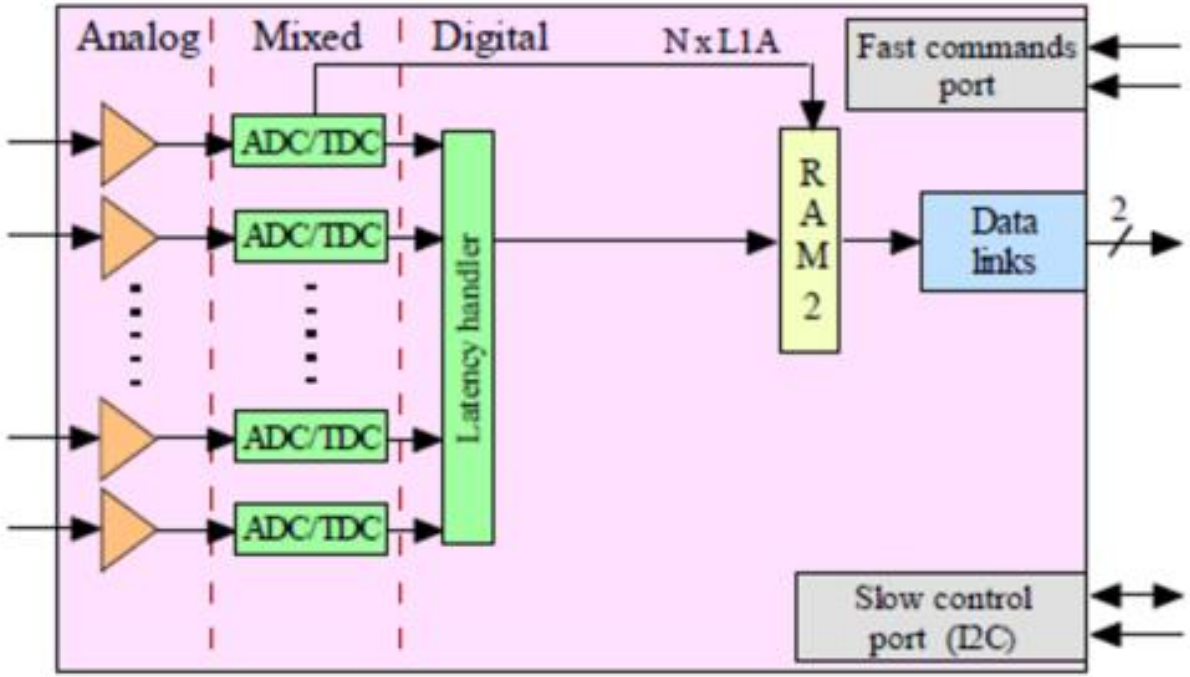
EIC reticle 2024

- TSMC now requires to fully populate the reticle of 24x32
  - Cost ~300 k€
- For EIC we would have
  - EICROC1
  - 2 or 3 EICROC0/A/B
  - 2 CALOROC1A/1B
  - ~60% of reticle area
- Possible additionnal partners
  - ~20% of reticle area
  - Still space available (if ready in time !)



EICROC2 : 32x32 with EIC backend

- EICROC2 needs to address EIC digital architecture
  - Auto-trigger
  - Data driven zero-suppressed readout
  - Only readout hit channels and neighbours
  - Will depend a lot on the (low?) occupancy
  - Triplication and SEE tolerance
  - ~~200 MHz clock and fast commands~~

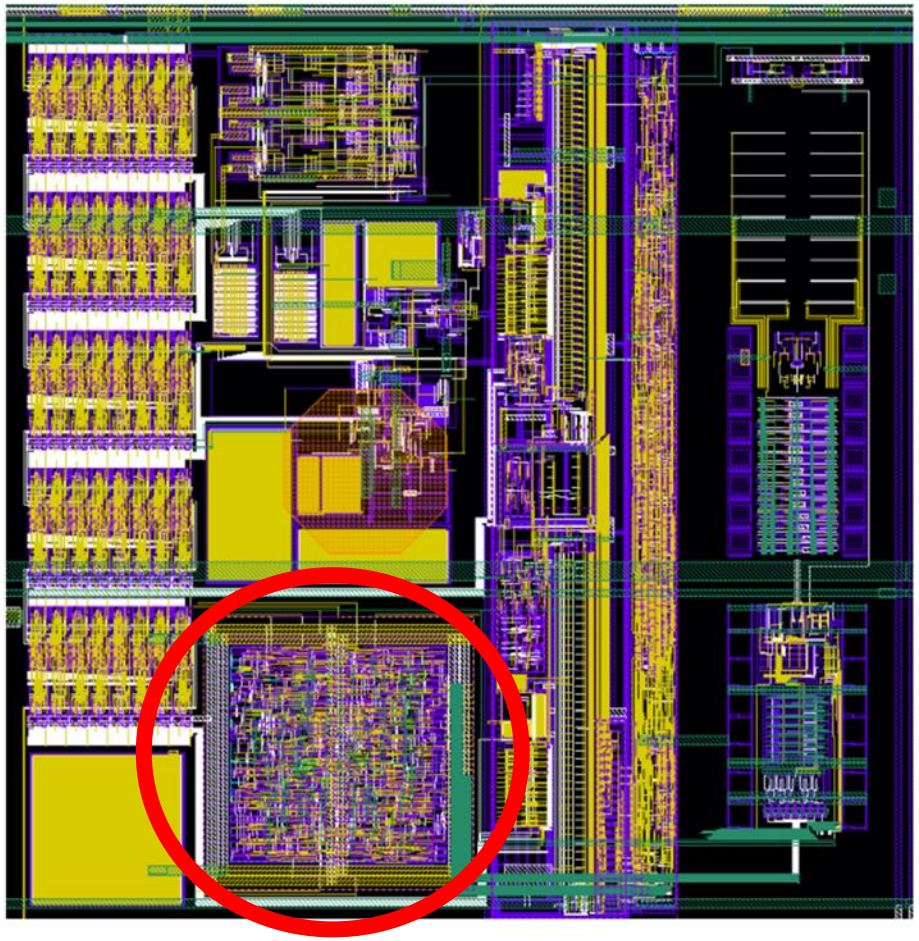


- Several EIC functions will be tested in CALOROC (see talk by F Dulucq)
  - Sparse readout
  - Output links 160-1280 Mb/s

- Possible submission Q3-Q4 2026

Technology choice 65/130n

- Little impact on analog/digital performance
  - Analog similar in 65/130
  - Possibly more significant on TDC
  - Digital much simpler than LHC chips
- Update of digital part
  - Little space available => main reason for 65 !
- sizeable cost impact : ER 700 k$ vs 300 k$
  - But possibly more partners (but EICROC 50% of reticle)
- Prepare for design in 65 nm
  - Make an EICROC0/65n to test analog part and TDC



AoT vs DoT

- HGCROC/CALOROC designed Analog on Top (1D chip)
  - Analog inputs on one side / digital outputs on the other side
  - All digital data re-synchronized when transferred to digital blocks

- ALTIROC was designed Digital on Top (2D chip)
  - Powerful tools to verify digital part functionnality/timings in all corners on all the chip area
  - But needs more manpower for digital design (RTL, P&R, IRD, TB, UVM…)
  - Possible help from colleagues at Clermont

- Choice will depend on complexity (occupancy) and manpower availability

Conclusion

- EICROC is a 1k-channels ASIC to readout AC-LGAD pixels
  - Very promising new family of detectors
  - Combines both good timing and position resolution (30 ps 10 µm)
  - Targeting 1 mW/ch
  - Re-use of many blocks from ATLAS HGTD and CMS HGCAL
- Still several choices lying ahead
  - Technology choice 65nm / 130nm
  - Analog on Top / Digital on Top
- Importance of module tests