EIC France 2024

Electron-Ion Collider

9-11 October

IJCLab Orsay

Roman Pots: Characterization of first AC-LGAD read-out chip (EICROC0)

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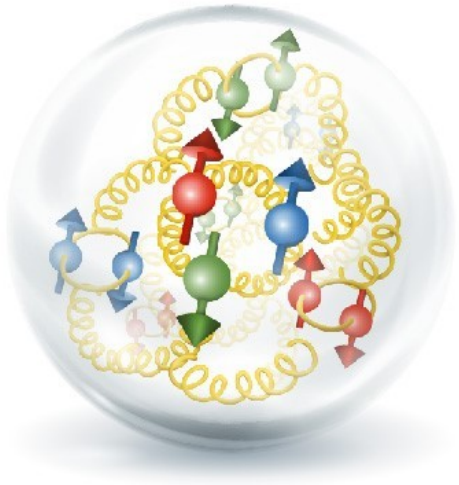
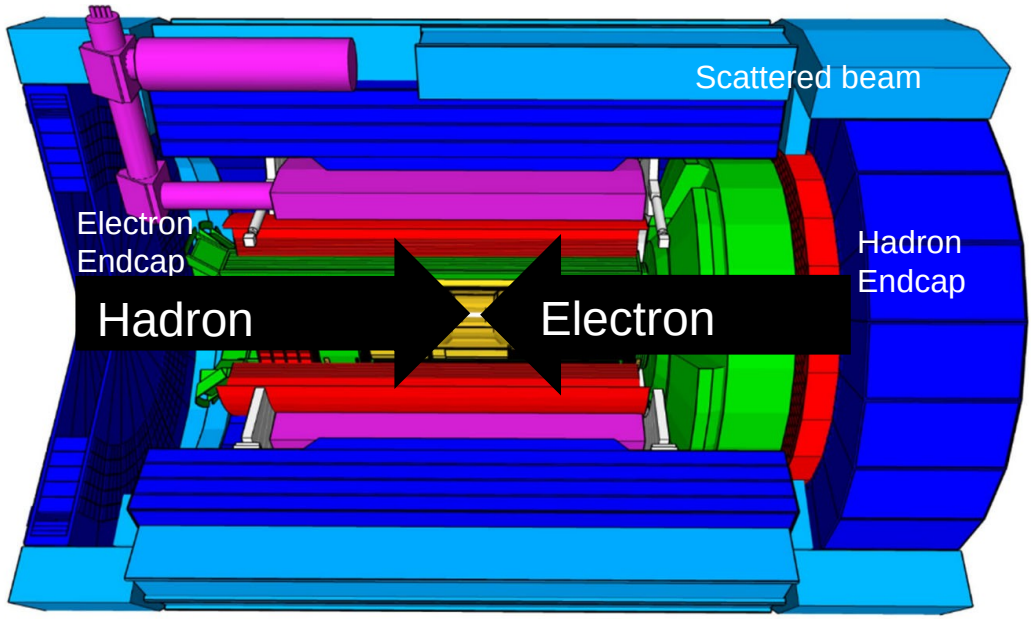
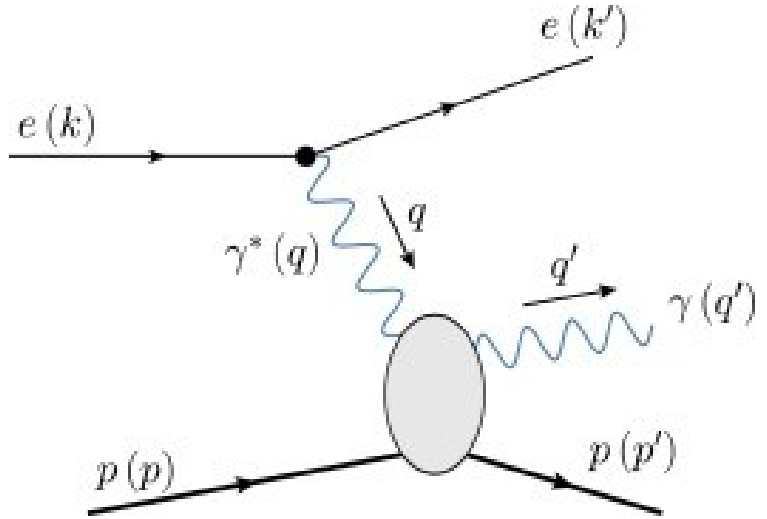
Motivation : EIC Quest

- Understand nucleon properties like mass and spin emerging from their partonic structure
- Behavior of sea quarks and gluons, and their spins, distributed in space and momentum inside the nucleon
- Study mechanism through which quark-gluon interactions give rise to nuclear binding
- Investigating saturation point for the density of gluons in nuclei at high energies





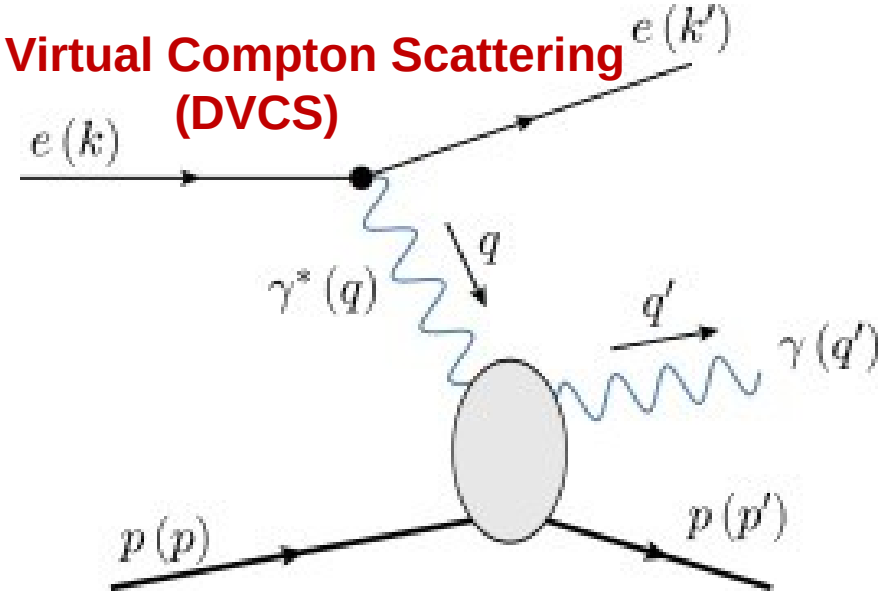
Large rapidity (-4 < η < 4) coverage;
and far beyond in far-forward/far-backward detector regions
Far-Forward: θ<2.1⁰ (~37mrad)



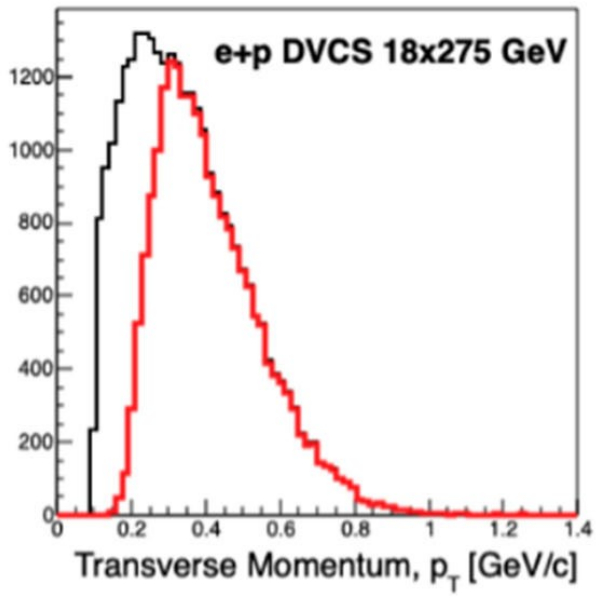
Deep Virtual Compton Scattering (DVCS)

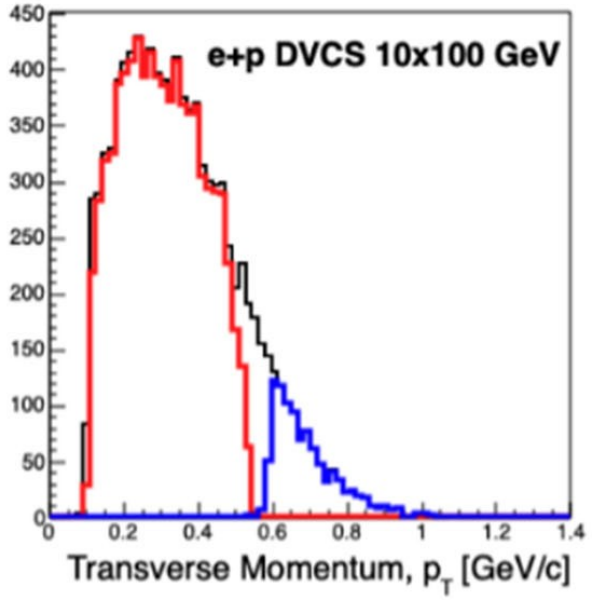
Roman Pots: Essential for exclusive processes

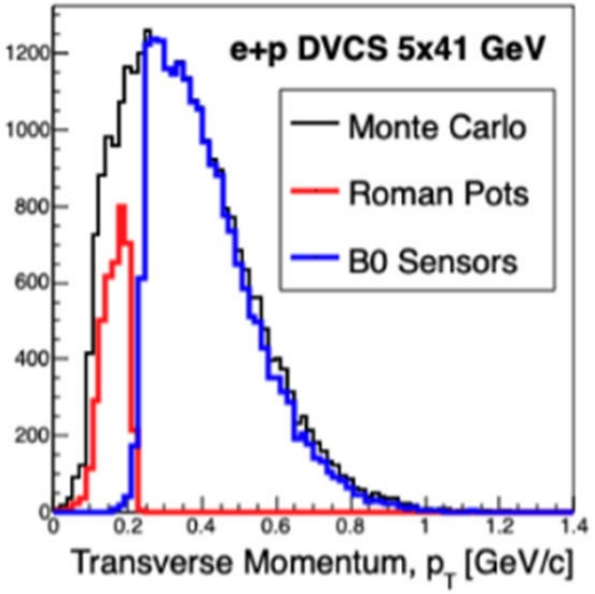
Deep Virtual Compton Scattering (DVCS)



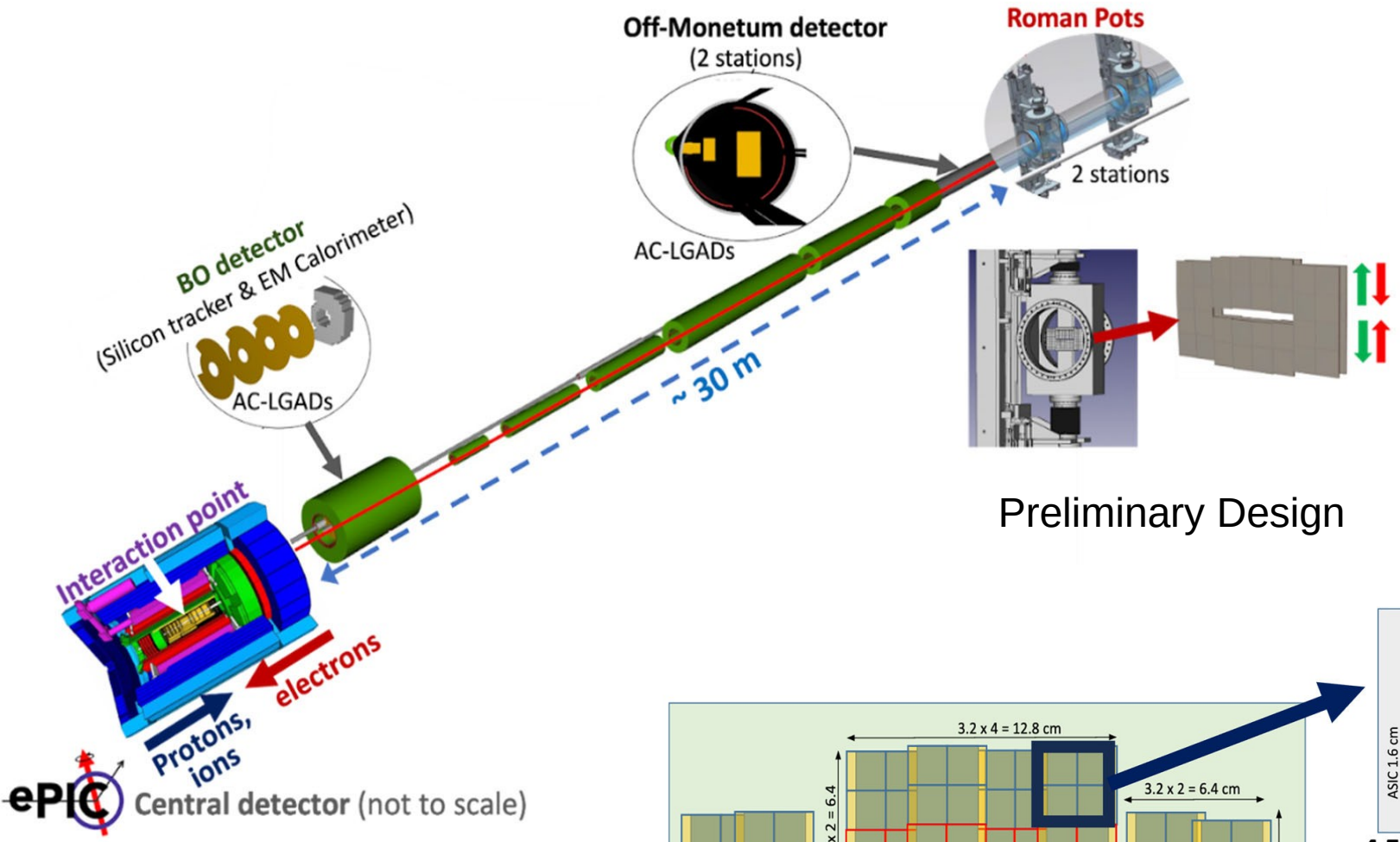
- Crucial to reconstruct proton transverse momenta (with a resolution of ~ 10 MeV/c) in exclusive processes.
  Requires position resolution of < 50 μm.
- Require time resolution ~35 ps to account for head on collision between the electron and proton beam, to be obtained by Roman pots.





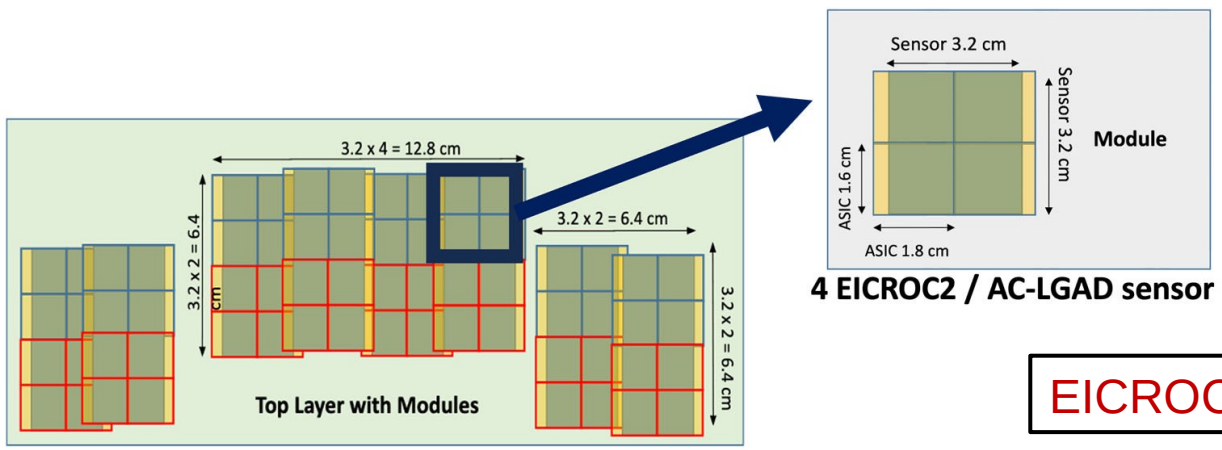


Roman Pots



Preliminary Design

- Aim is to identify and characterize exclusive, diffractive, and tagged events using detectors integrated with the outgoing hadron beamline, (**far-forward detectors**).
- Scattered angle < 5mrad
- Detector system to be placed directly within vacuum surrounding the scattered hadron beam.

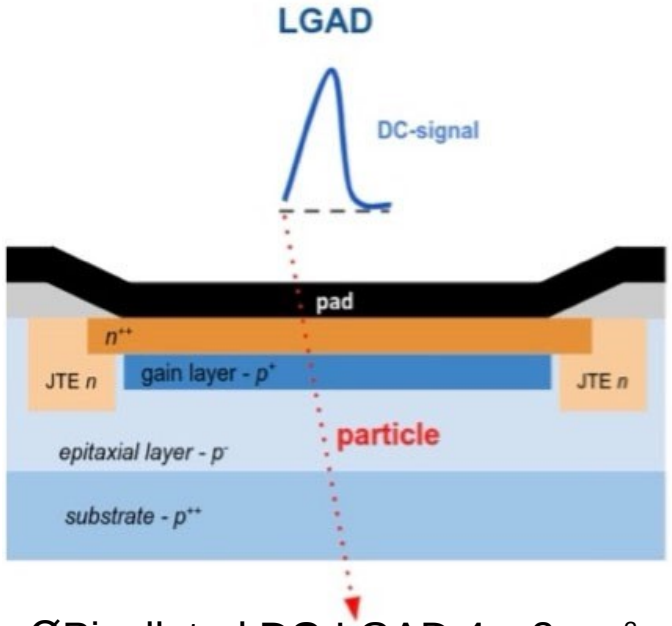


EICROC2: 32x32 pads

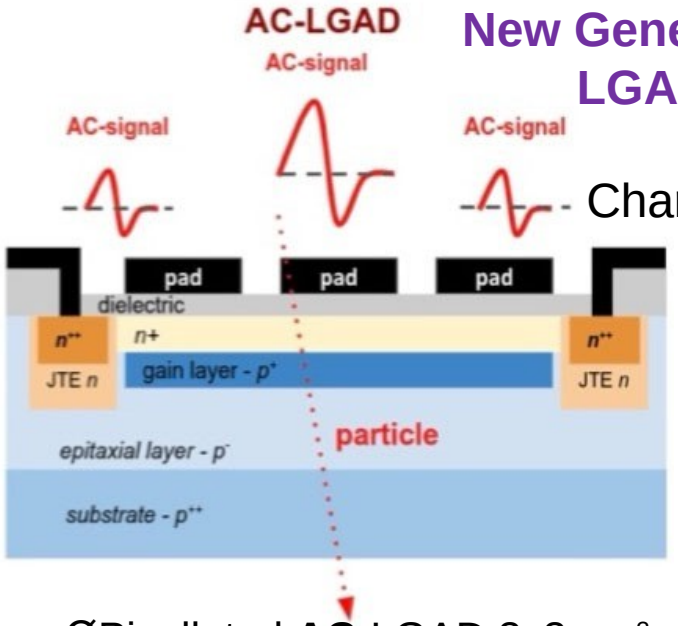
LGAD Sensor (Design Credit : @BNL)

High Granularity Timing Detector (HGTD)

ALTIROC (15x15) readout chip (@OMEGA)



ØPixellated **DC**-LGAD 4 x 2 cm^2
ØPixel size: 1.3 x 1.3 mm^2



New Generation LGAD

Charge sharing

ØPixellated **AC**-LGAD 3x3 cm^2
ØPixel size: 0.5x0.5 mm^2

EICROC AC-LGAD readout chip (@OMEGA)

CMOS 130 nm

1D ⟶ 4D

AC-LGADs are best choice for Roman Pots: Simultaneous spatial and timing measurements.

EICROC Project

Design& performance characterization of EICROC2 (32x32) chip intended to readout large surface pixelated AC-LGAD

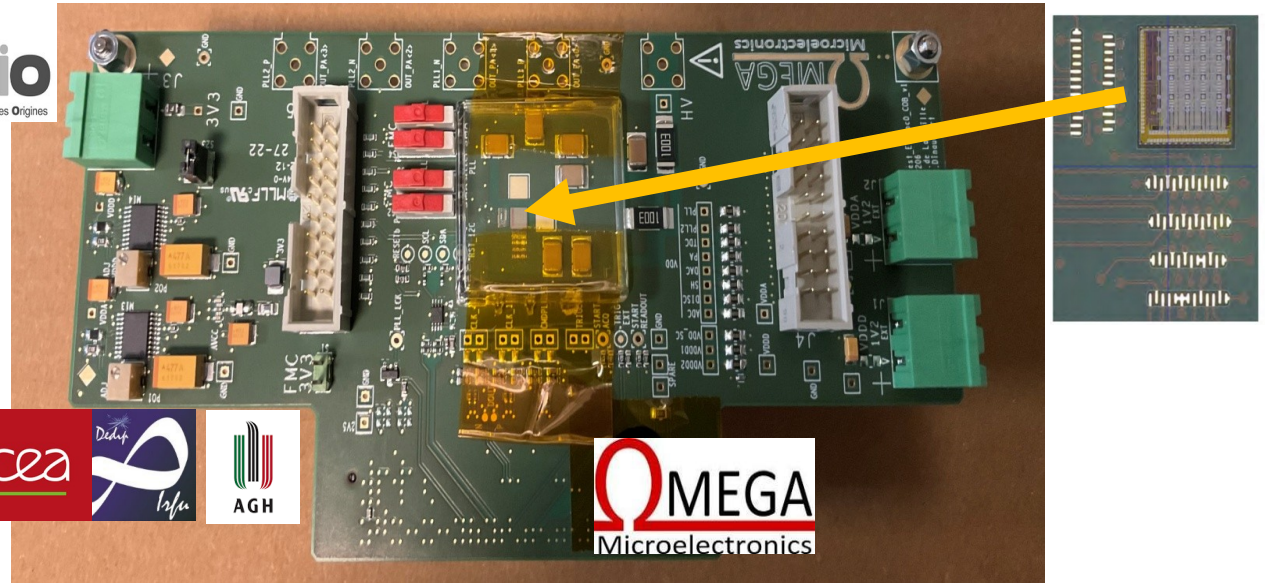
- Design challenge is to fit all the components within a 0.5x0.5 mm^2 pad.
- Challenge to accommodate for low sensor capacitance (< 1 pF), low electronic noise (~ 1 mV/channel) and jitter to reach the required timing resolutions (20-30 ps),sensitivity to small charges (~ 3 fC) per pixel, and to estimate the amplitude of the central hit pixel for time-walk correction but also of its neighbors (containing the induced cross-talk and charge sharing).
- Achieve good position resolution (~ 20 microns) while ensuring a very low power dissipation, << 1mW/channel.
- Cooling mechanism in vacuum: studies being performed @ IJCLab.
- EICROC0: 1st ASIC prototype has 16 channels

Design Credit for ASIC Development: @ OMEGA withTDC @ CEA/Irfu/DEDIP

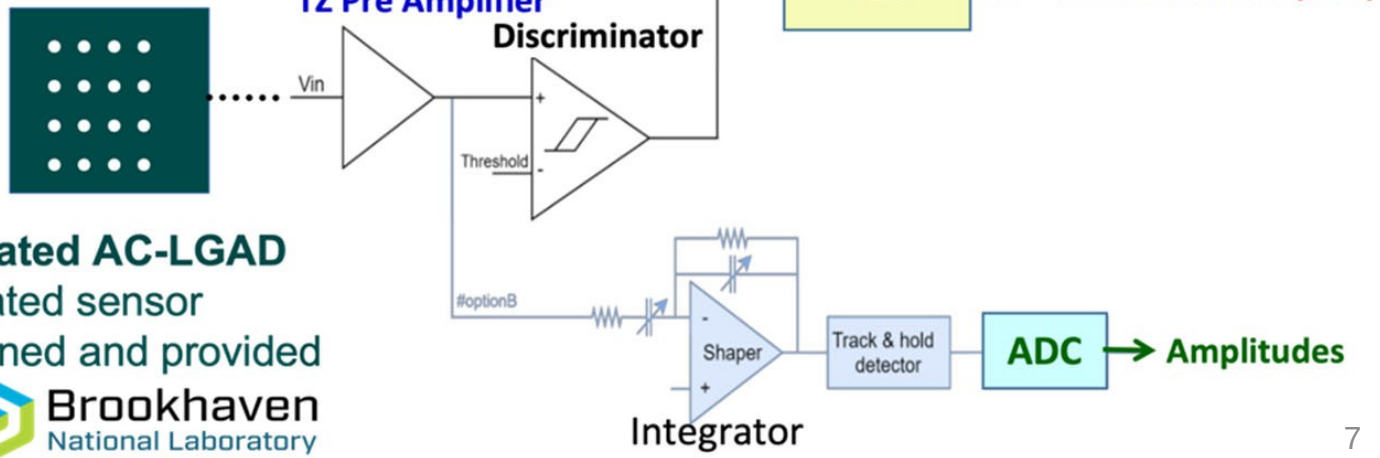
EICROC0 1st prototype (4x4 pads)

EICROC0 Test Board

EICROC0 chip



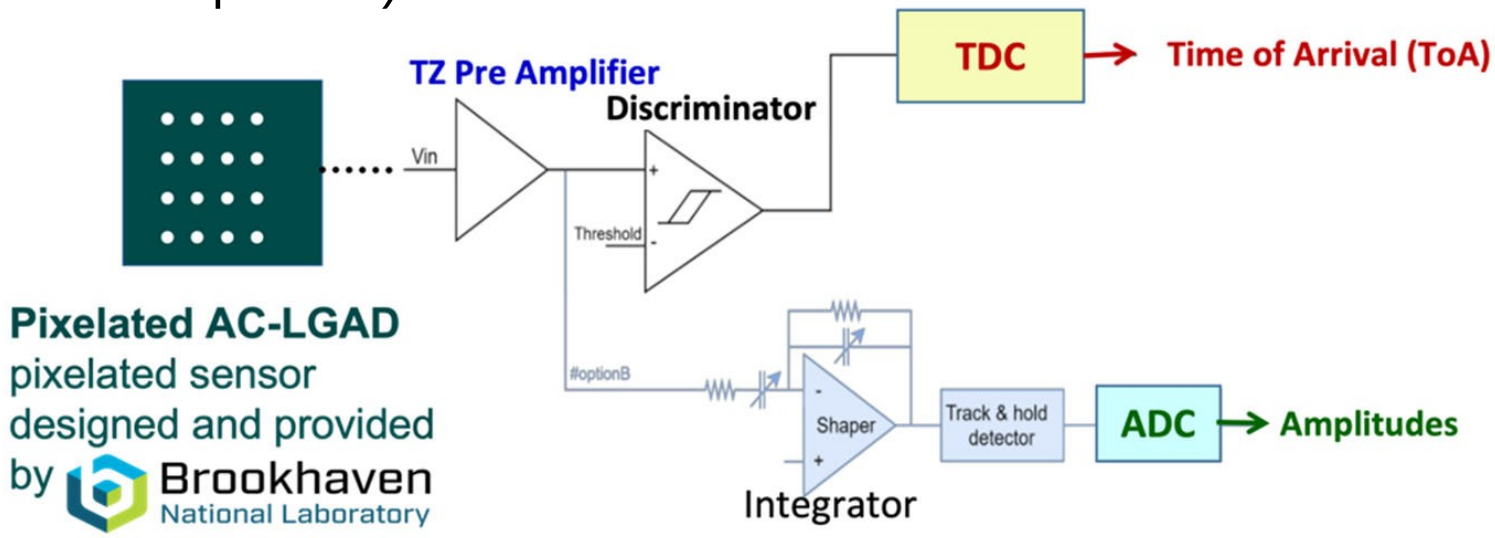
EICROC0
Test
board



Pixelated AC-LGAD
pixelated sensor
designed and provided
by Brookhaven National Laboratory

EICROC0 features

- An analogical fast Transimpedance (TZ) pre-amplifier and a discriminator taken from ALTIROC ASIC design (ATLAS/HGTD).
- 10-bit Time-to-Digital Converter (TDC) measuring the Time-of-Arrival (ToA), designed by CEA/Irfu/DEDIP.
- 8-bit (40 MHz) Analogical-to-Digital Converter (ADC), designed and adapted by AGH University of Science and Technology (Krakow, Poland) from the HGCROC 10 bit ADC.
- Compared to the ALTIROC chip, holding 2 TDCs, one to measure the TOA and the second one associated to the Time-over-Threshold, an ADC has been preferred to measure the signal amplitude to avoid nonlinear behavior of a ToT TDC as a function of injected charge.
- I^2C communication (firmware + software developments)
- Digital readout: FIFO depth 8(200ns)
- 5 slow control bytes per pixel:
  - 6 bits local threshold,
  - 6 bits ADC pedestal,
  - 16 TDC calibration bits,
  - several on/off and probes.



1 channel/pixel schematics

EICROC0 characterization outline

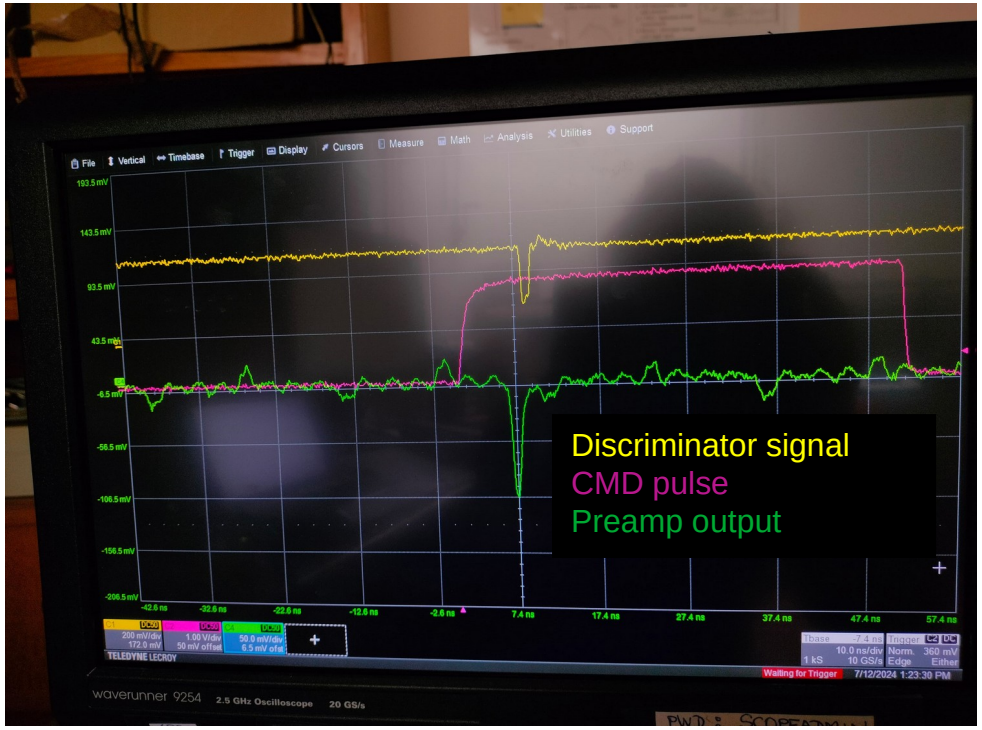
Detector characterization involves:

1. Internal Charge injection system, referred as CMD Pulse signal (**0-25 fC**).
2. Preamplifier signal, which is divided and sent to Discri/TDC (ToA) and to integrator/ADC (measure signal amplitude).
3. Signals are first observed on the oscilloscope.
4. Digital output data consist of 8 time samples; [TDC, ADC, Hit bit] / time sample for each of the 16 channels.

0;89;0;0;75;0;0;96;0;0;135;0;139;158;0;0;124;0;0;91;1;0;109;0

1 sample — TDC ADC — Hit Bit

5. Discriminator threshold adjustment is performed by measuring S-curve, i.e., efficiency as a function of threshold.
6. TDC quantization step has been measured to calibrate TDC scale.
7. TDC is characterized by measuring average time and jitter as a function of injected charge, and Determining minimum detectable charge.
8. For ADC, pedestal (corresponding to lowest charge value) is subtracted.



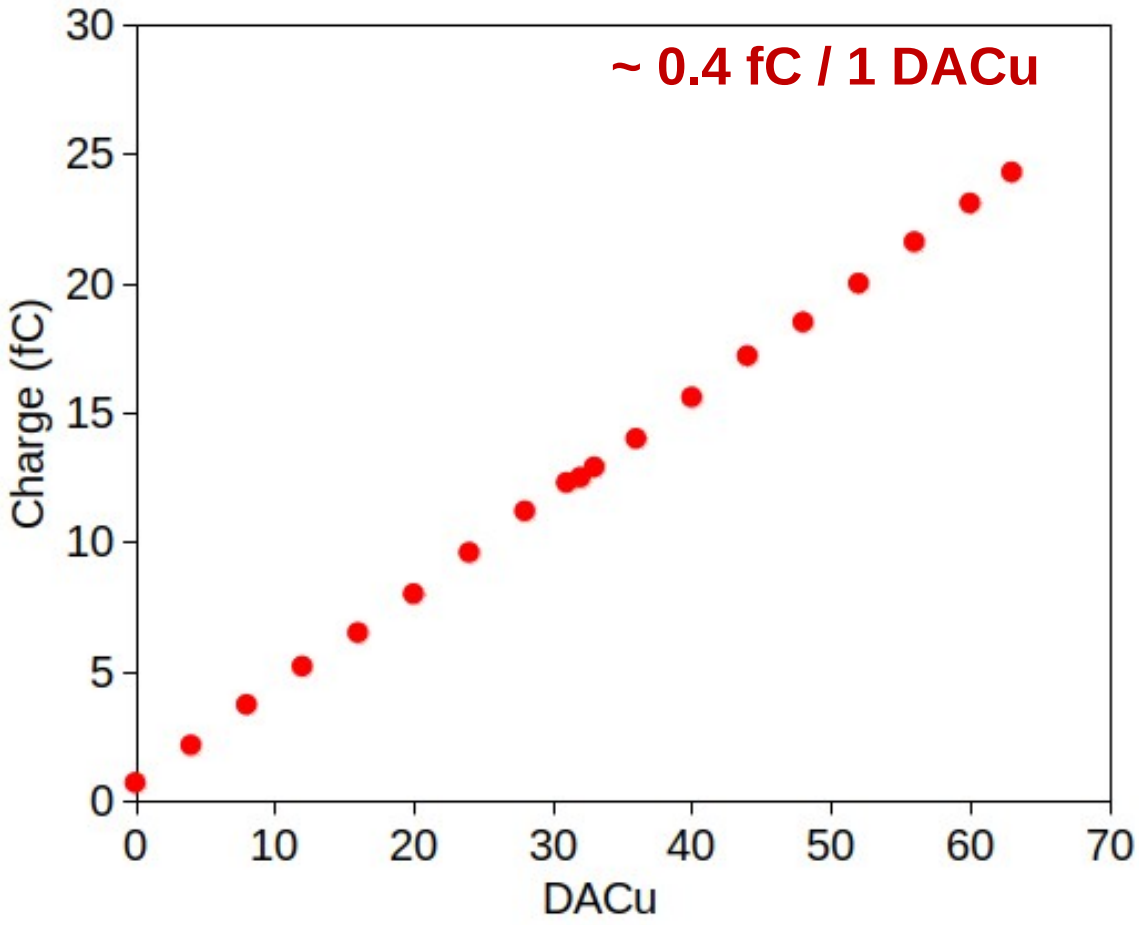
Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0) #00	Pixel (1,0) #04	Pixel (2,0) #08	Pixel (3,0) #12
Line 1	Pixel (0,1) #01	Pixel (1,1) #05	Pixel (2,1) #09	Pixel (3,1) #13
Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15

Jointly @IJCLab and @OMEGA

Charge injection system linearity

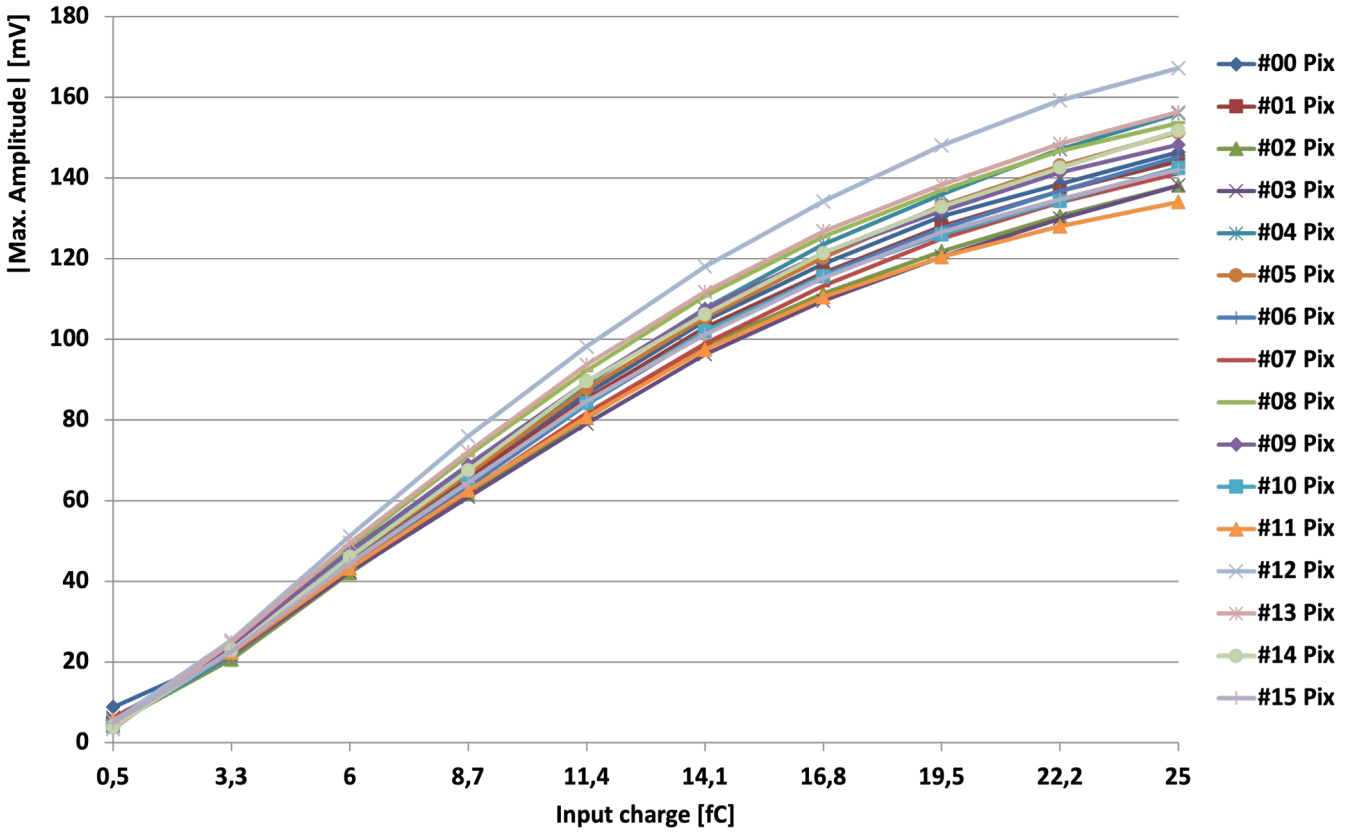
- For measurements without sensor, charge injection system is used.
- Voltage is measured as a function of the DAC set value of the associated register (0x20C) in order to check its behavior.
- DAC value is changed from 0 to 63 and voltage is measured using multimeter.

C = 100 fF,
Charge [fC] = C [fF] * Voltage [mV]

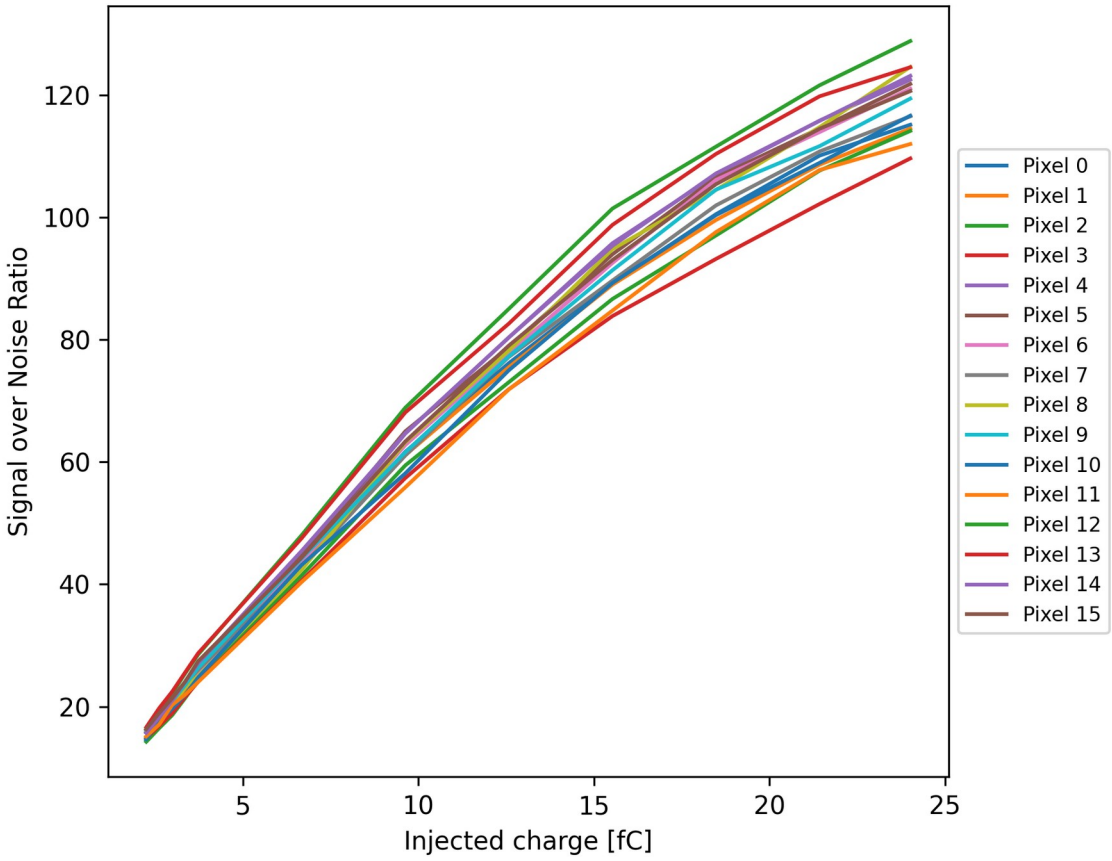


Probe preamplifier measurements

Maximum Amplitude vs Charge

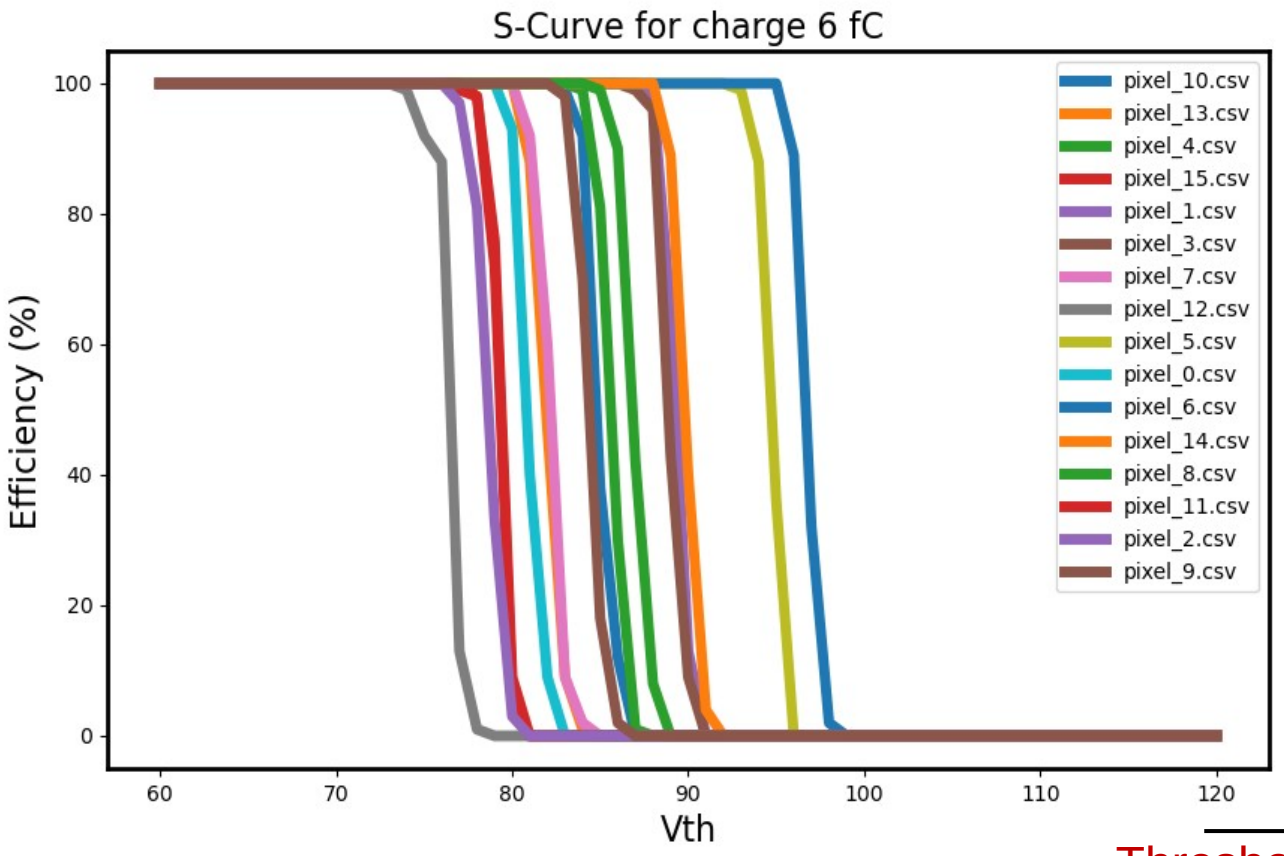


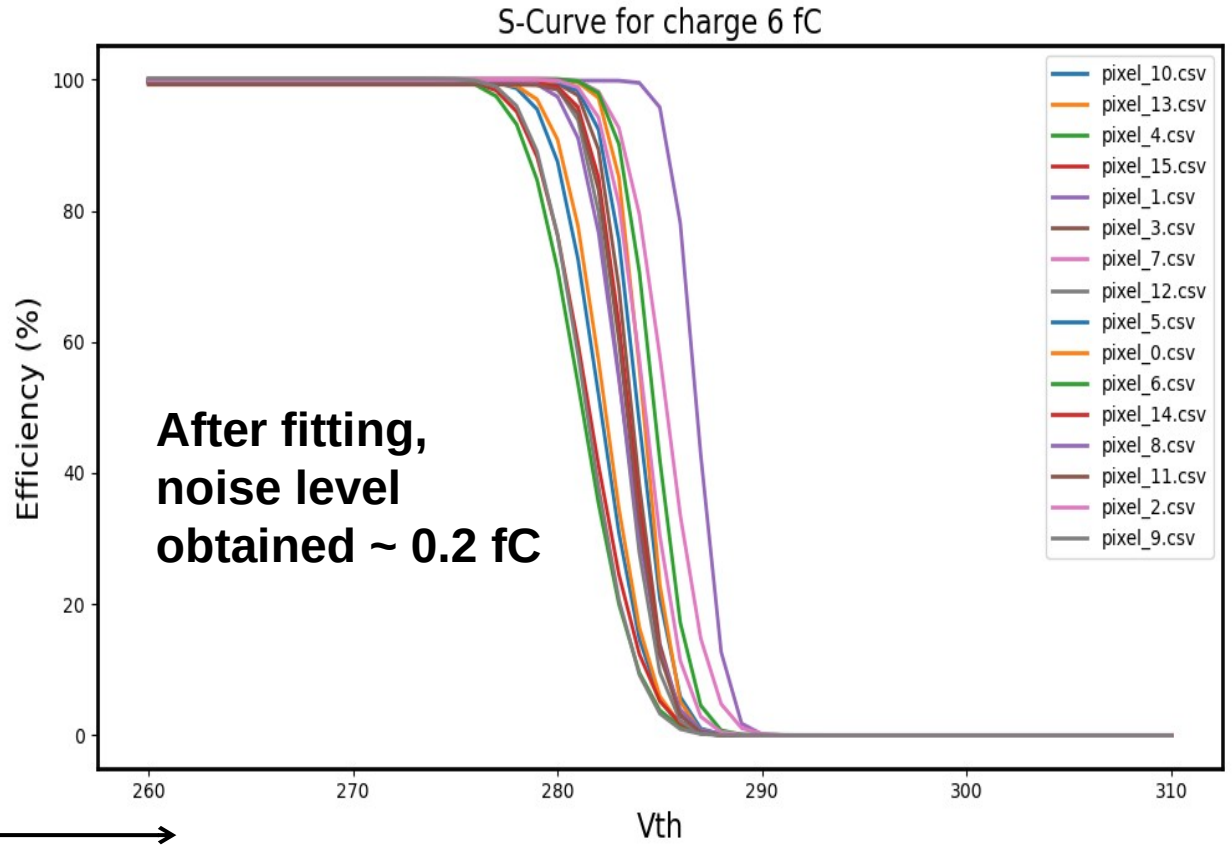
Signal/Noise ratio vs Charge



S-curve (Efficiency vs threshold voltage)

- To correct the response of all channels towards the injected charge, discriminator threshold adjustment is done at a specific charge injection to align all channels.



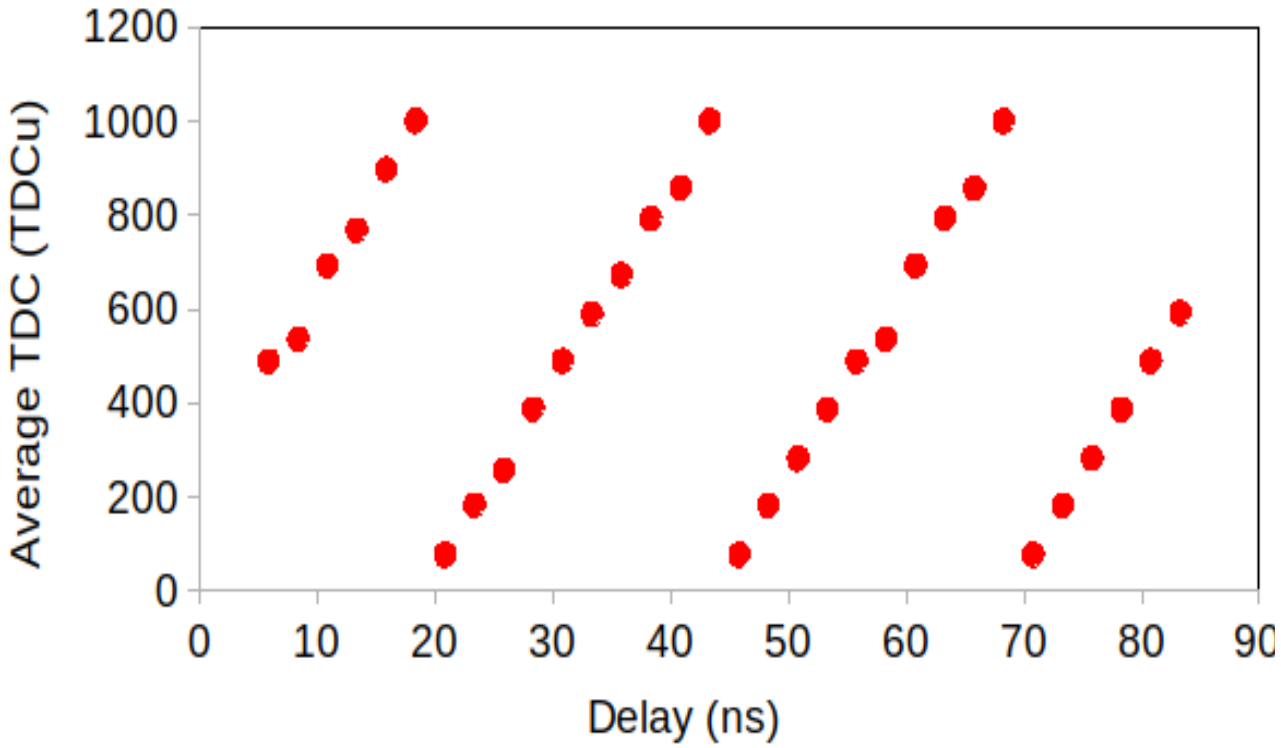


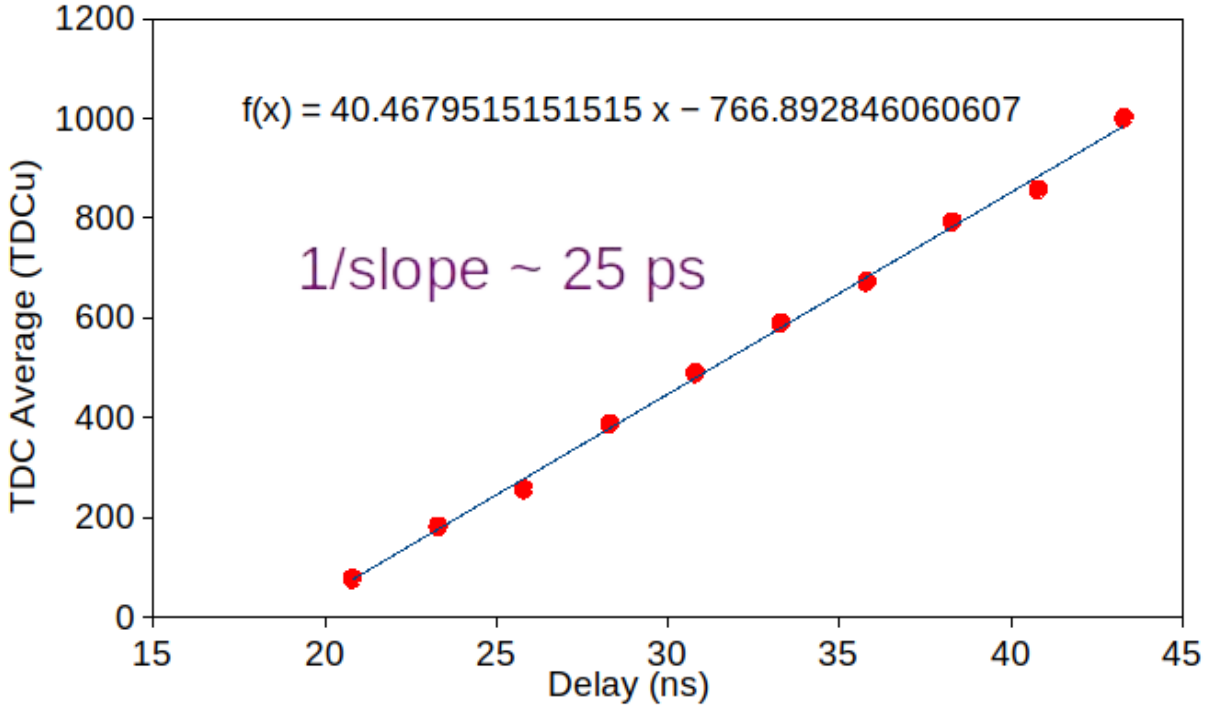
Threshold adjustment

Measurements performed to align all the pulses, and then obtain a minimum threshold to detect a minimum charge: for neighboring charge selection.

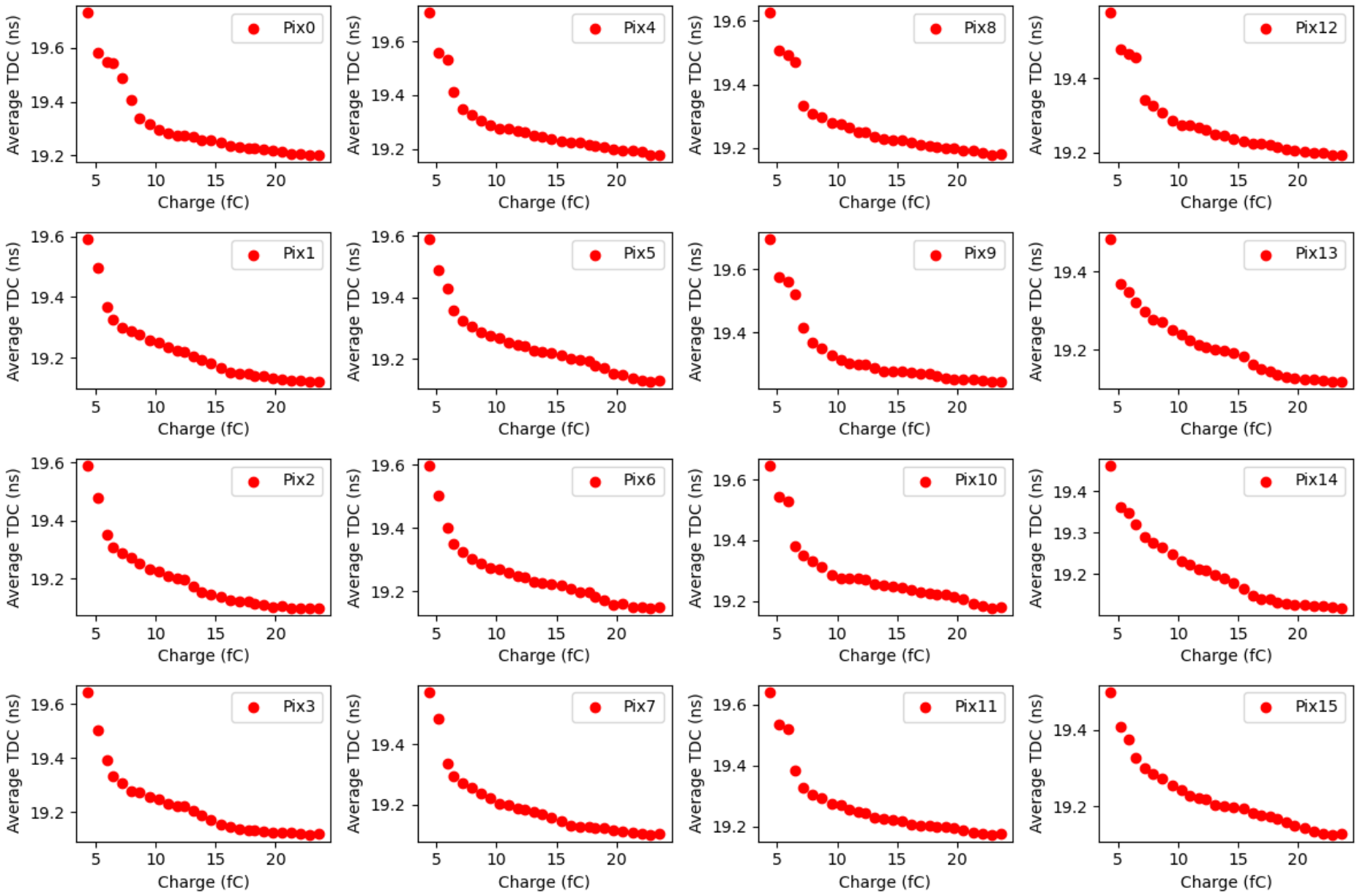
TDC Quantization Step

- To determine the TDC Least Significant Bit (time/TDC unit): average TDC values have been plotted as a function of CMD pulse delay
- For each pixel, obtained a value of ~ 25 ps = **TDC design value!**

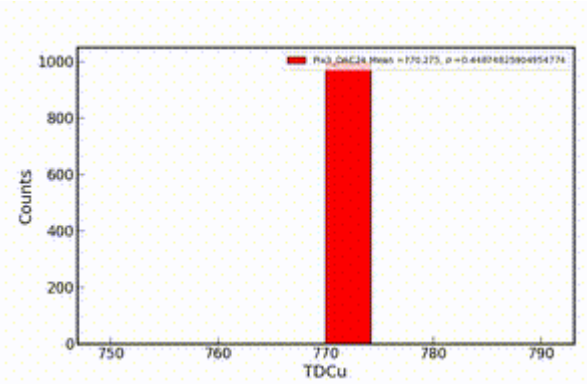




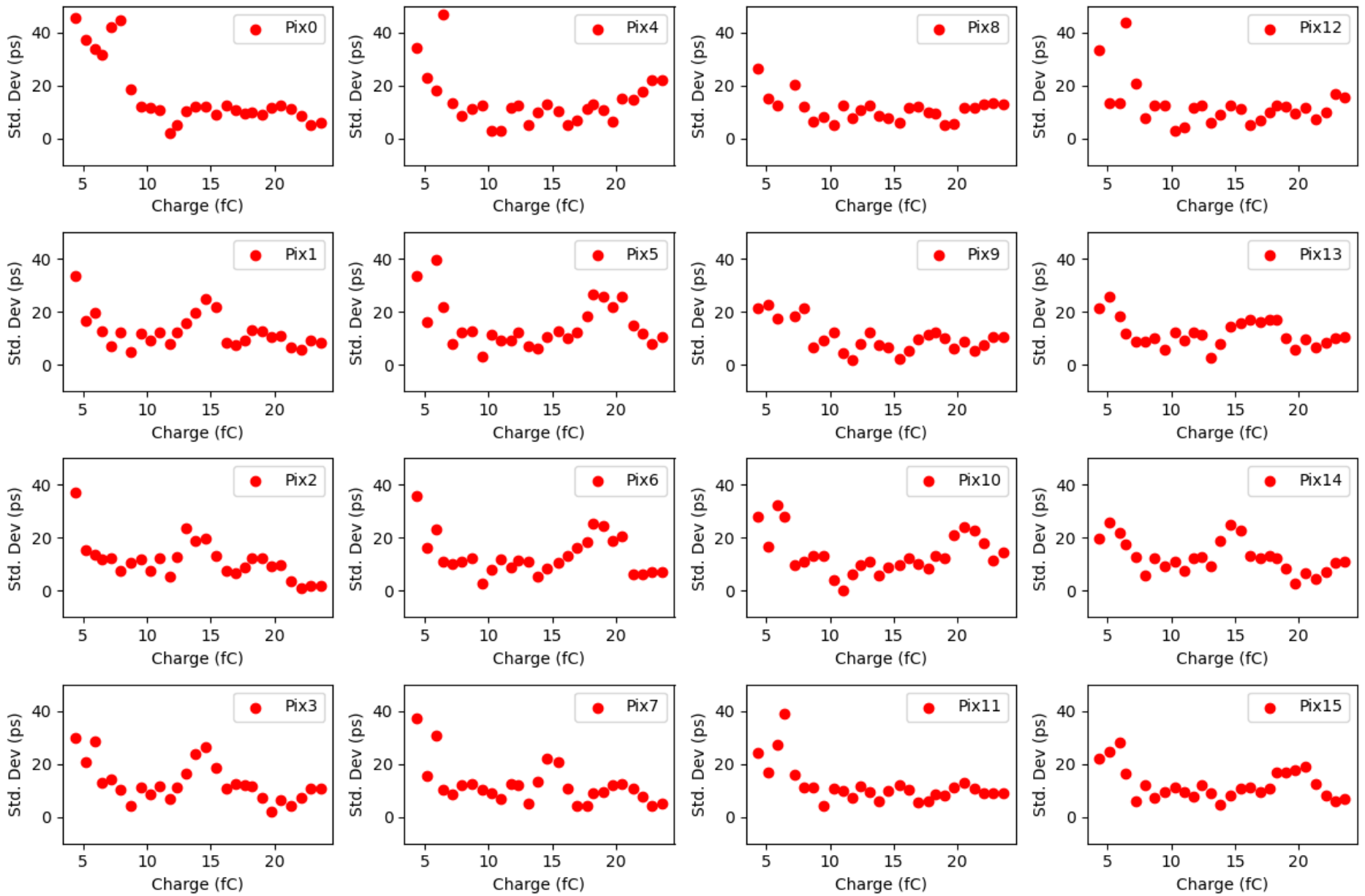
Average TDC Time as a function of charge



Global Threshold: 275 DACu +
Individual threshold adjusted

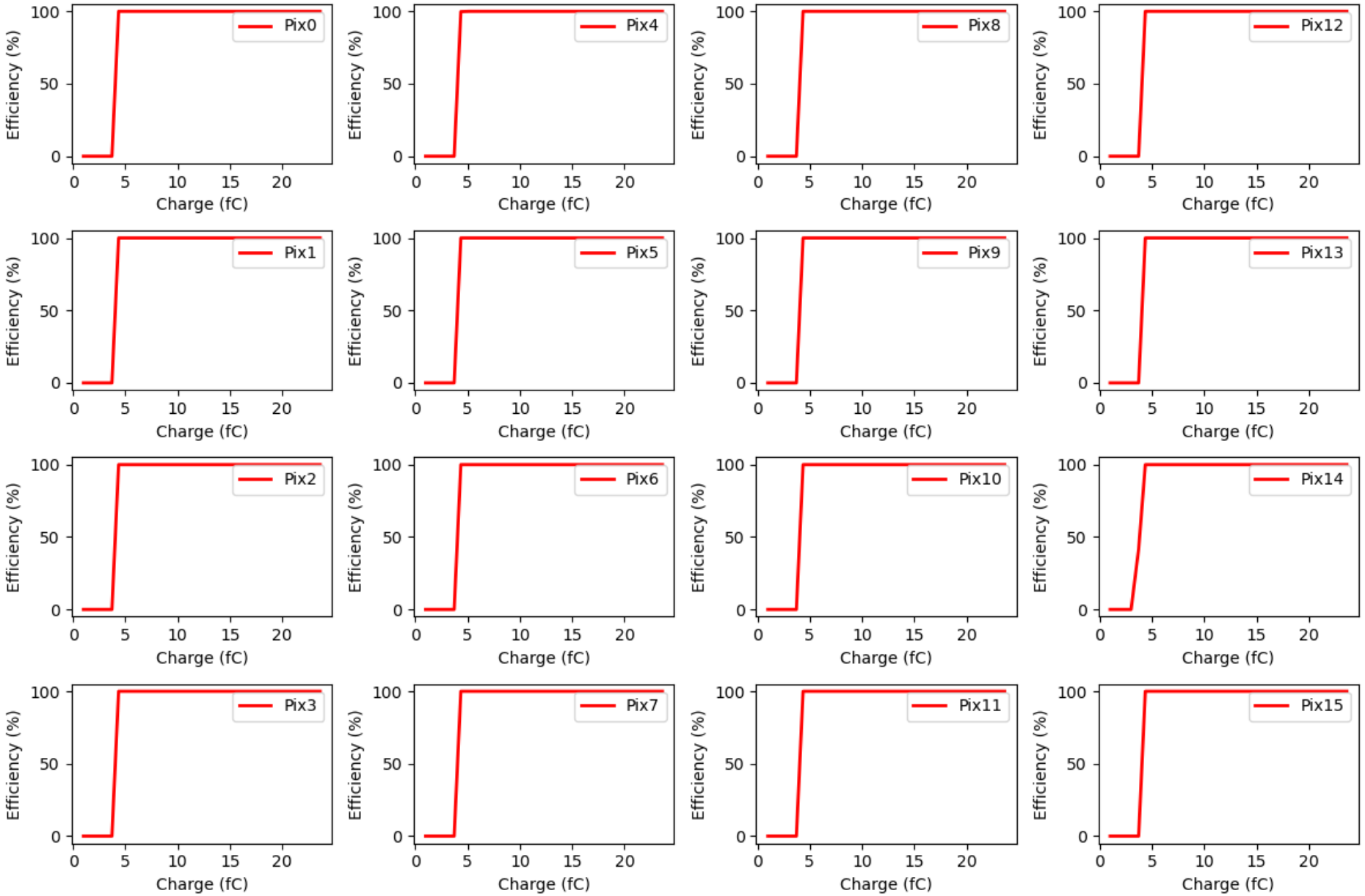


TDC Jitter

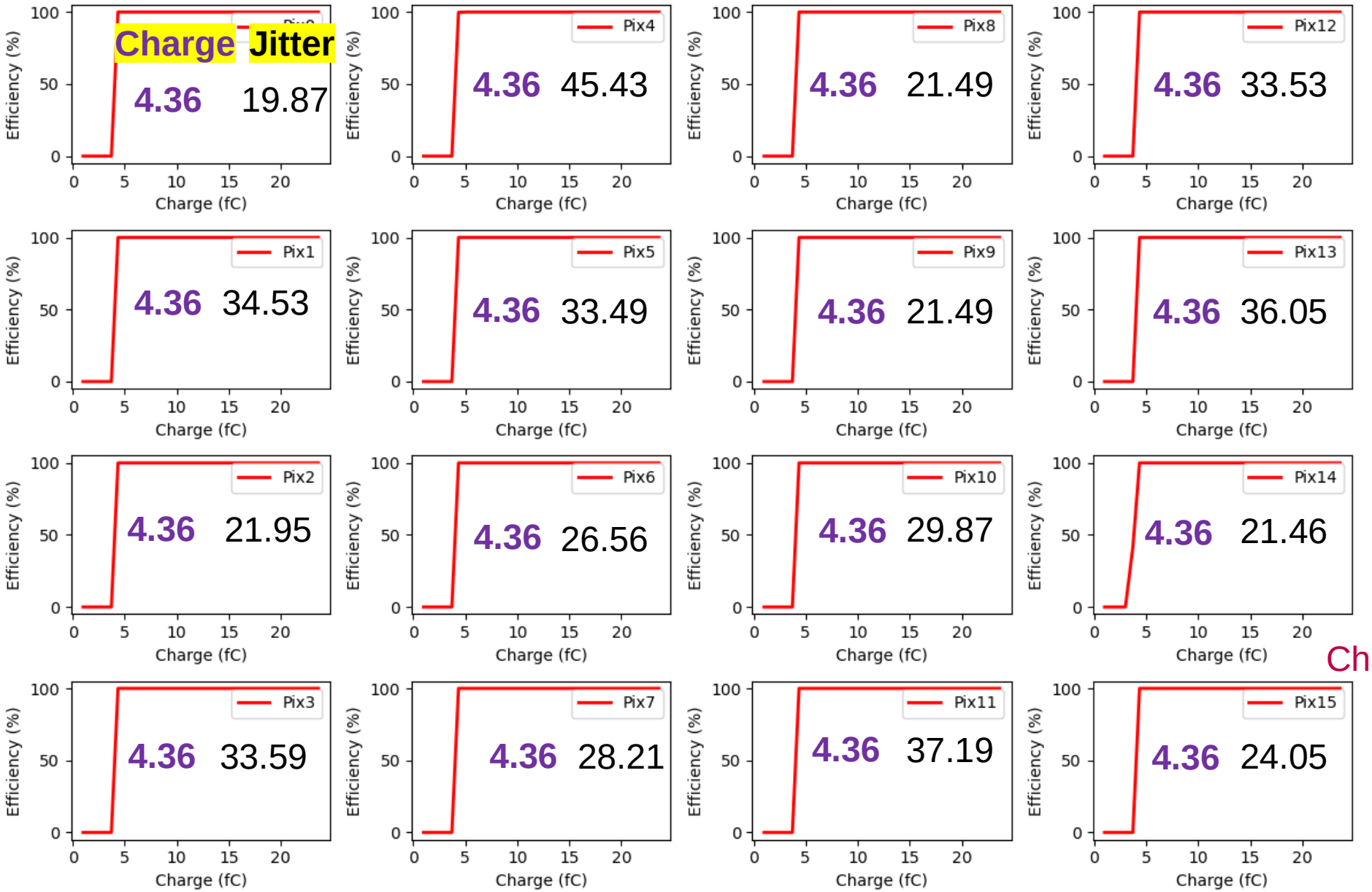


- At 23 fC,
- σ ~ 10 ps

Minimal Charge



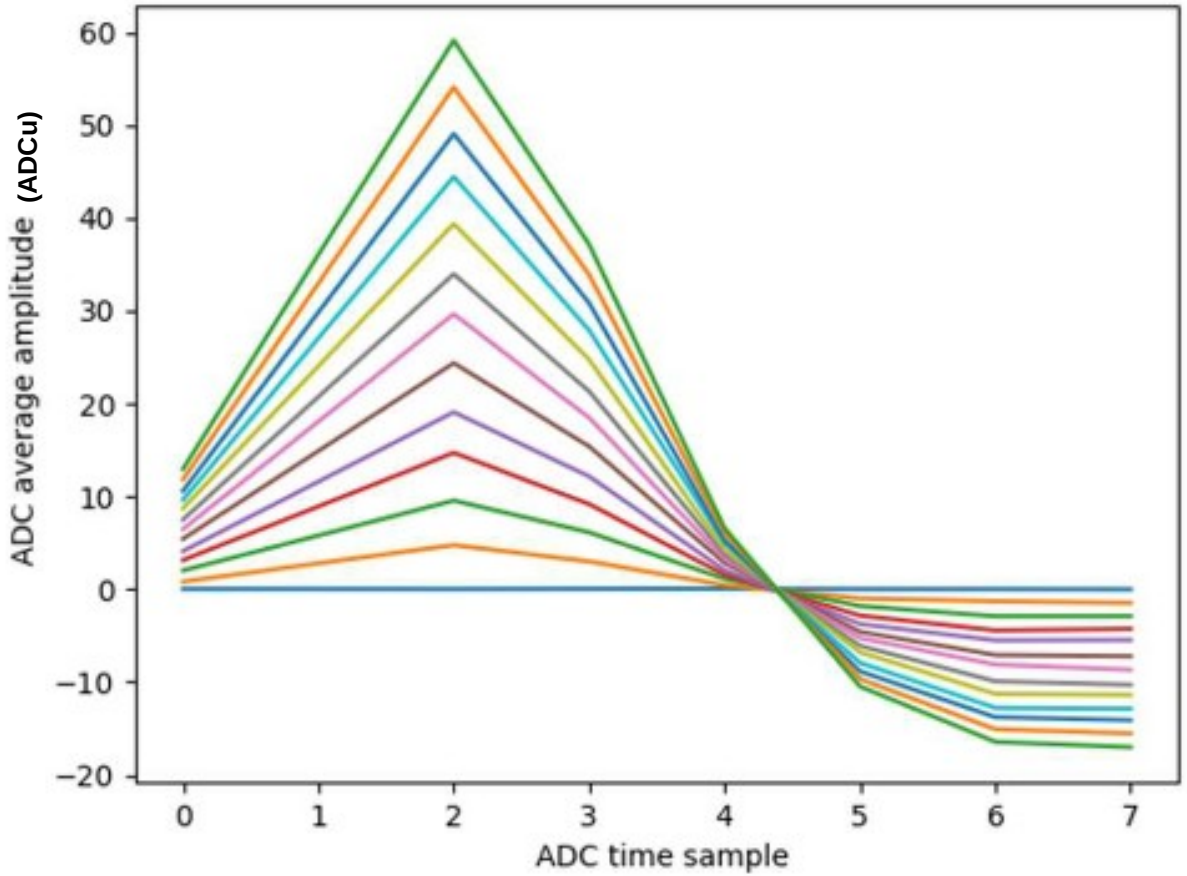
Minimal Charge

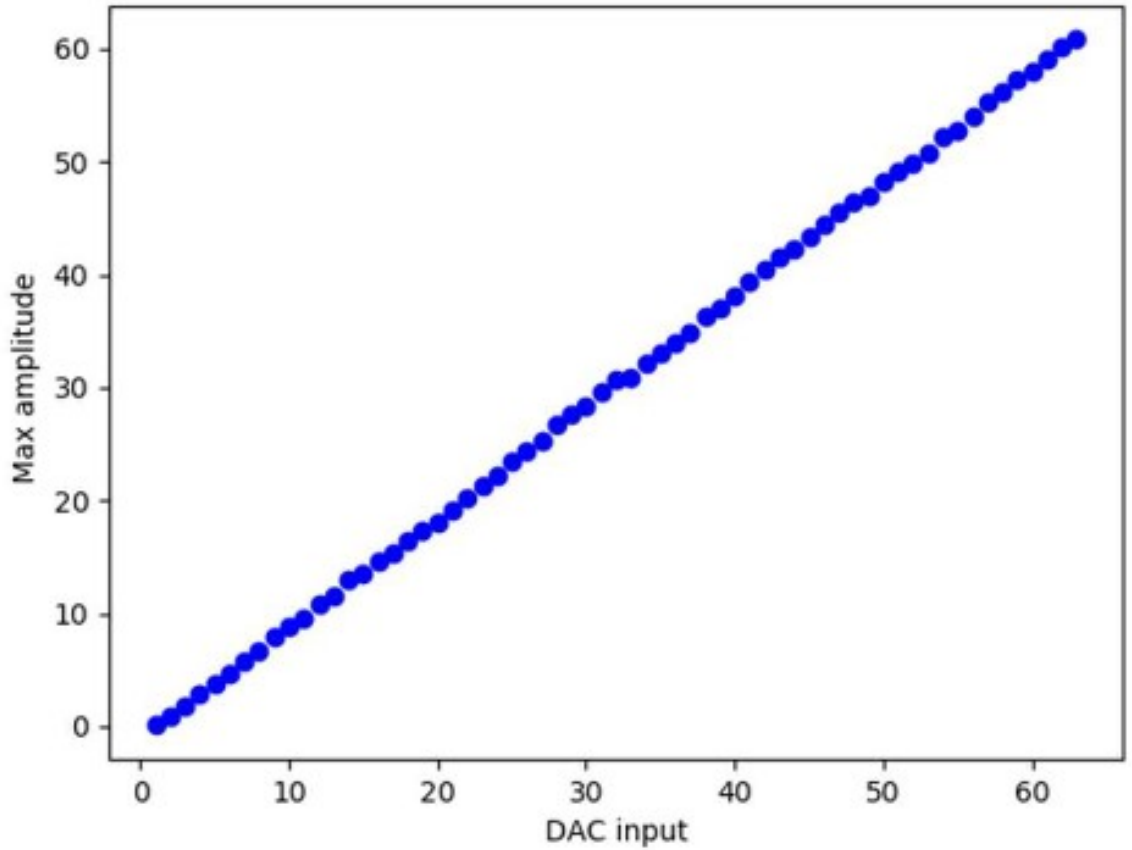


Charge sensitivity
~ 4 fC

ADC studies: Charge Scan for Pix1

Amplitudes as a function of time with pedestal subtraction (w.r.t. lower charge).





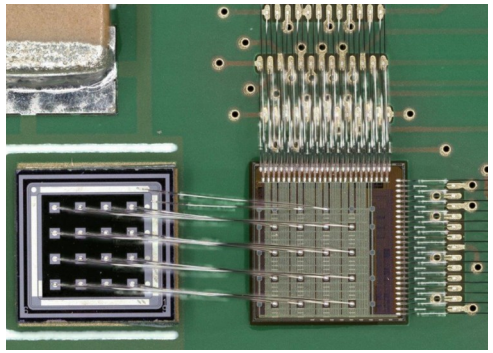
(Charge)

Summary

- Characterization of EICROC0 ASIC performed for understanding the response of TDC and ADC as a function of charge.
- Preamplifier: S/N ratio ~40 (low charge), ~110 (25 fC)
- Discriminator performance: 100% efficiency obtained with charge ~ 4 fC (charge sensitivity).
- TDC: Quantization step of 25 ps, Jitter ~10 ps at 23 fC charge, noise level ~0.2 fC.
- ADC: response checked, characterization of all channels on-going.

Future Work:

- Evaluation of crosstalk.
- Testing with an AC-LGAD sensor:
  - Beta source measurements to evaluate charge sharing among the neighboring pixels.
  - Infrared Laser tests to evaluate spatial resolution.
- ePIC simulations to determine maximum occupancy per pixel per second.



❖ **Next foreseen ASIC iterations:**

Refer to @Nathalie Seguin-Moreau's talk!!

- **EICROC0A**: 4x4 pads(idem EICROC0) including 8-bit low power ADC.
- **EICROC1**: 8x32 pads to study floor planning, ground distribution.
- **EICROC2**: 32x32 pads.

THANKS