Proposal for DMAPS Upgrade of the Belle II Vertex Detector

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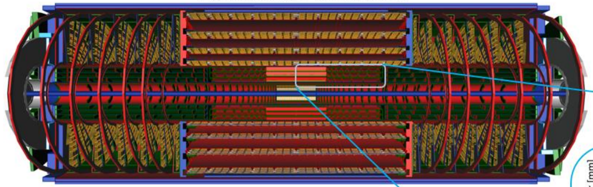
On behalf of the Belle II VTX Upgrade Group

Pixels for HEP at CPPM

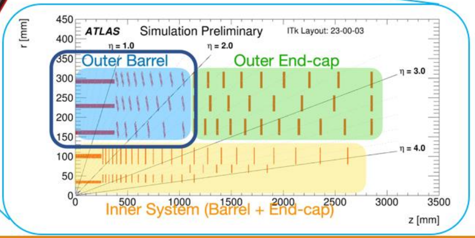
CNRS NUCLÉAIRE & PARTICULES — amU Aix Marseille Université — CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

- ATLAS and ITk project

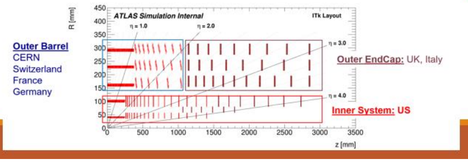
ITK View from simulation:

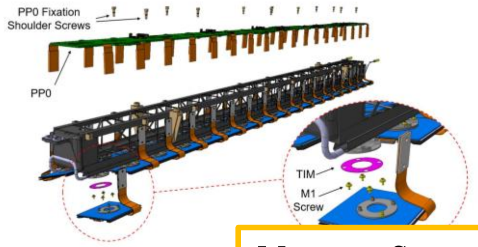


- ITK Pixel belong to Atlas Inner Tracker (ITK) for HL-LHC
  - 13 m^2 all Hybrid Pixel detector ~ 7 time bigger than the current pixel detector
  - 9400 Modules ~ 5 times more module than the current pixel detector



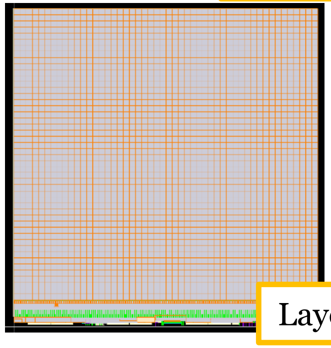
- Detector construction: 4 Systems/clusters



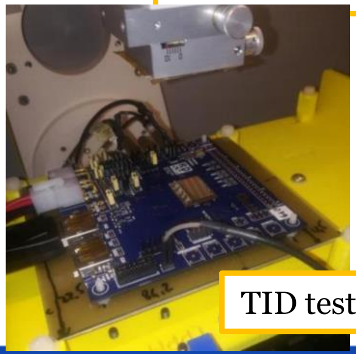


Montage Stave Outer Barrel

ITkPix-v1 on PCB

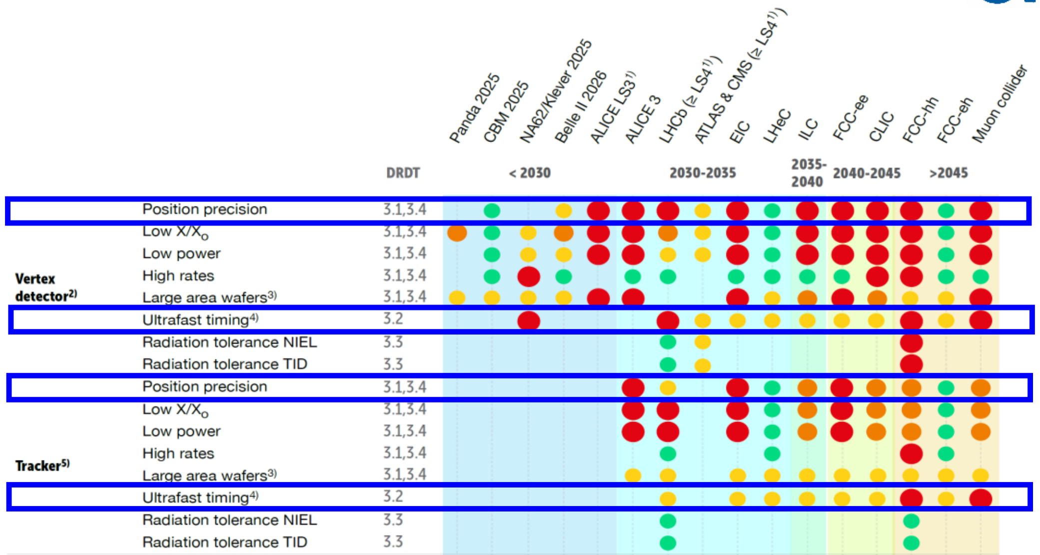


Layout ITkPix-v1

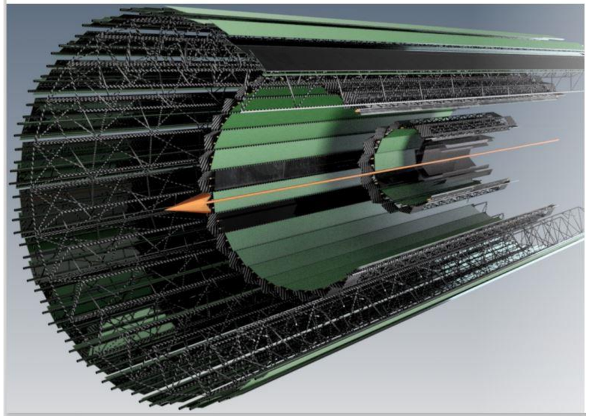


TID tests in Marseille

- Future Colliders and Future Projects



Future projects (timeline ECFA)



Design VTX for Belle-II upgrade

Other projects:
28nm
Monolithic pixels – TJ65/LF150/TJ180
RD53
……

DEPHY project

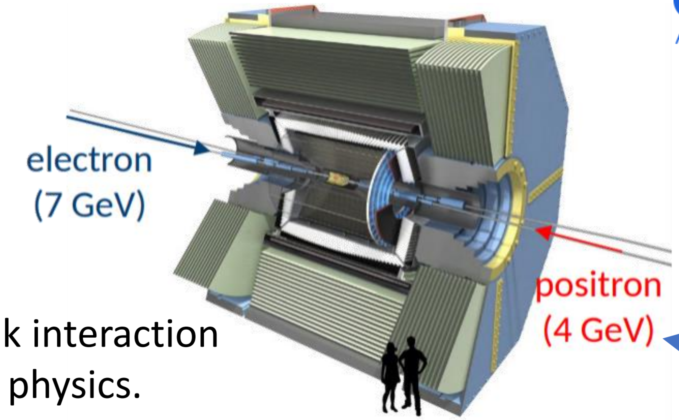
- A project led by the CPPM, led by Mr. Barbero / CPPM (support J. Baudot / IPHC)
- A general theme:
  - – Pixel trace and vertex detectors in technologies relevant to future projects which are characterized in the first place by:
    - High counting rates/occupancy rates.
    - Medium to high radiation resistance.
- 2 Work Packages:

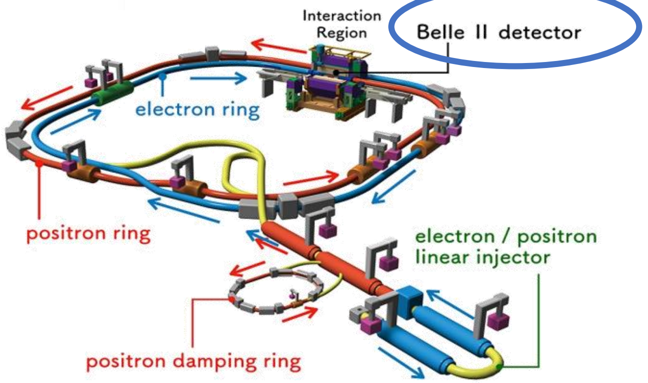
  – **Hybrid Pixels**: Exploration of technologies implementing Advanced process nodes -e.g. 28 nm- (RS: Barbero / RT: Menouni) / DRD7 (Timing 7.3 / Radiation 7.4 / Tools 7.7)

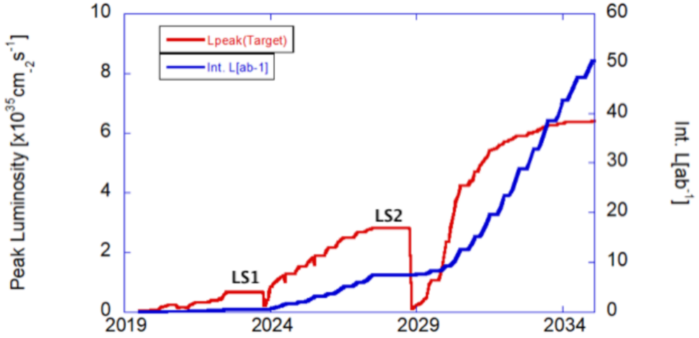
  – **Monolithic Pixels**: Exploring Depleted MAPS Technology, 2 Main directions, exploitation of current developments / potential of new technologies (RS: Baudot / RT: Pangaud) / (DRD3.1 / DRD7.6)

BELLE II Experiment

- Located at the SuperKEK-B collider in Tsukuba,Japan
- Asymmetric e^{+}- e^{-} collider at 4 / 7 GeV and $\sqrt{s}$ = 10.58 GeV
- Belle II is an experiment designed to make precise measurements of weak interaction parameters and find New Physics beyond the Standard Model of particle physics.
- Restart beam operation in 2024 after a **long shutdown (LS1)**
- Target instantaneous luminosity of **$6\text{x}10^{35}$ cm^{-2} s^{-1}** , currently **$0.47\text{x}10^{35}cm^{-2}s^{-1}$**
- Target integrated luminosity of **50 ab^{-1}** , currently **0.43 ab^{-1}**
    - Machine related beam background will increase with high luminosity
    - Efficiency, resolution and performance of data tracking could degrade with higher occupancy from background
    - Extrapolation to this target luminosity has large uncertainty and limited safety margins
- A **long shutdown (LS2)** is foreseen around 2028 and provides the opportunity to install an upgraded detector



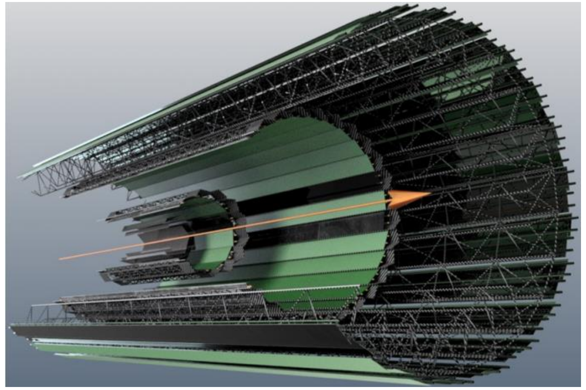


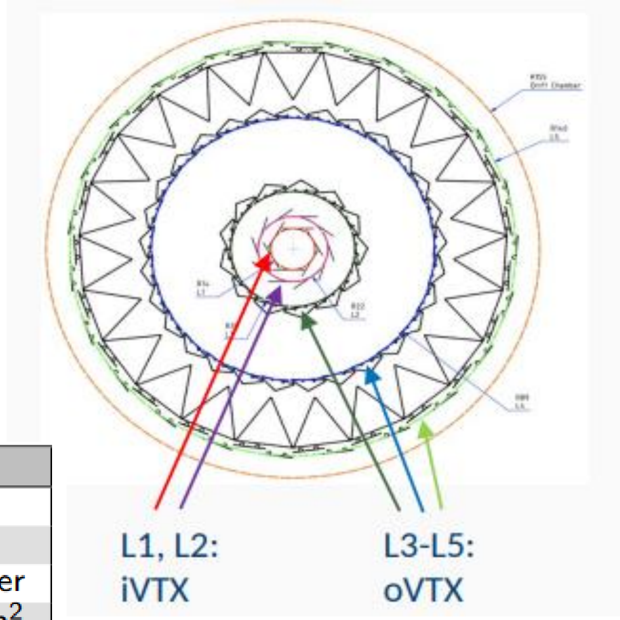


A new vertex detector concept VXD is proposed

The VTX Upgrade proposal

- A new fully pixelated CMOS detector to replace the VXD → VTX
- Improved tracking resolution and space-time granularity
- Reduced material budget less than 2%X0 instead of 3.8%X0 (sum of all layers)
- 5 straight layers with **D**epleted **M**onolithic **A**ctive CMOS **P**ixel **S**ensors (**DMAPS**) process
- L1 and L2 (iVTX)
  - All silicon ladders
  - Air cooling (constrains power)
- L3 to L5 (oVTX)
  - Carbon fiber support frame
  - Cold plate with liquid cooling





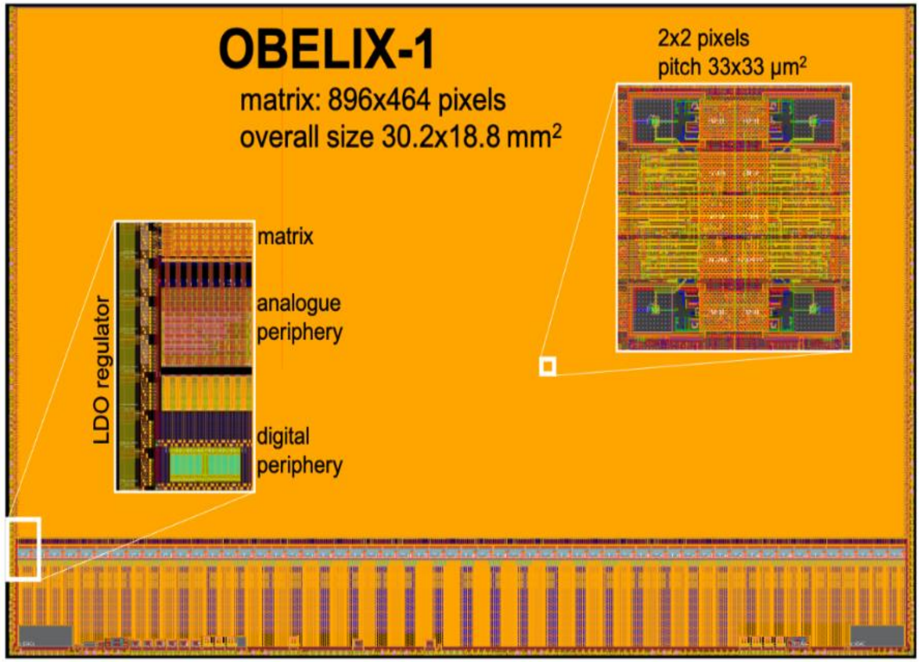
	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	8	18	26	
# Sensors	4	4	8	16	48	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.1	0.1	0.3	0.5	0.8	$\% X_0$

The OBELIX sensor

Sensor specifications :

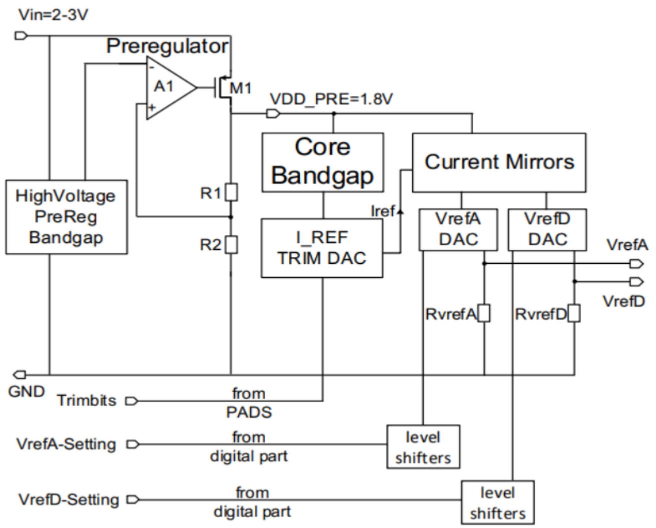
The **O**ptimized **BEL**le II p**IX**el sensor

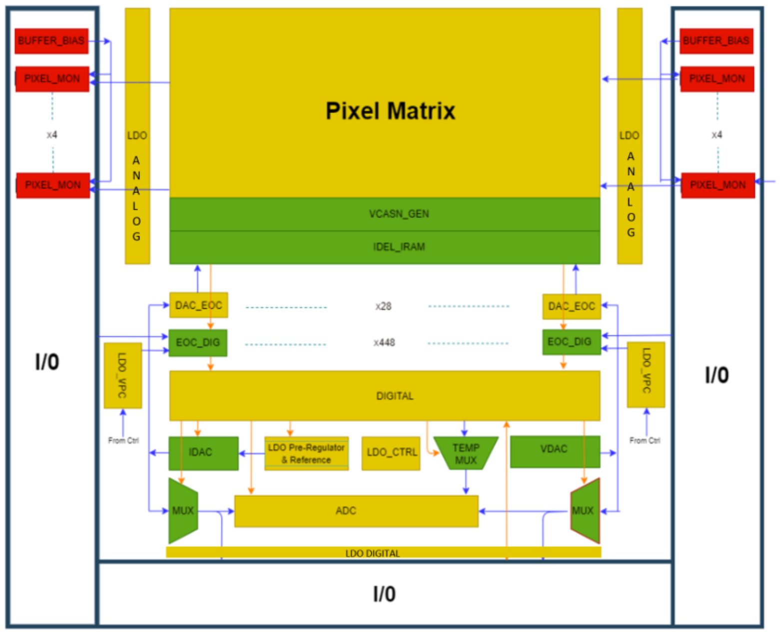
- Main design **based on the TJ-Monopix2 chip**
- Tower Jazz 180 nm process
- **Hit rate up to 120MHz/cm²**
- TID tolerance : 10 MRad / year
- NIEL tolerance : 5×10^{13} n_{eq}/cm^2/year
- Spatial resolution < 15µm
- **Power < 200 mW/cm²**
- Time precision < 100 ns
- Trigger at 30KHz average frequency with 5-10 µs latency



- 464 rows and 896 columns
- **Overall sensor dimensions around 30.2x18.8 mm²**
- Pixel pitch 33x33 µm²

The OBELIX power management





- Power distribution is a major concern as OBELIX is larger than TJ-Monopix2, leading to performance degradation

- On chip regulators are being developed in OBELIX to compensate the voltage drop and minimize the material budget dedicated to power distribution:
  - Two analog **LDO (Low Dropout)** regulators will be implemented to supply the matrix from both sides
  - A digital LDO in the bottom side of the chip to supply the digital blocs
  - A preregulator to supply LDO references generator
  - A VPC (Voltage pre-charge) LDO to reset and recharge bit-lines between each read cycle

- The LDO generates the output voltage of 1.8 V ± 10% necessary for the technology to power the chip

- Wide input supply voltage range of 2V to 3 V

OBELIX_V1 : Digital Blocks

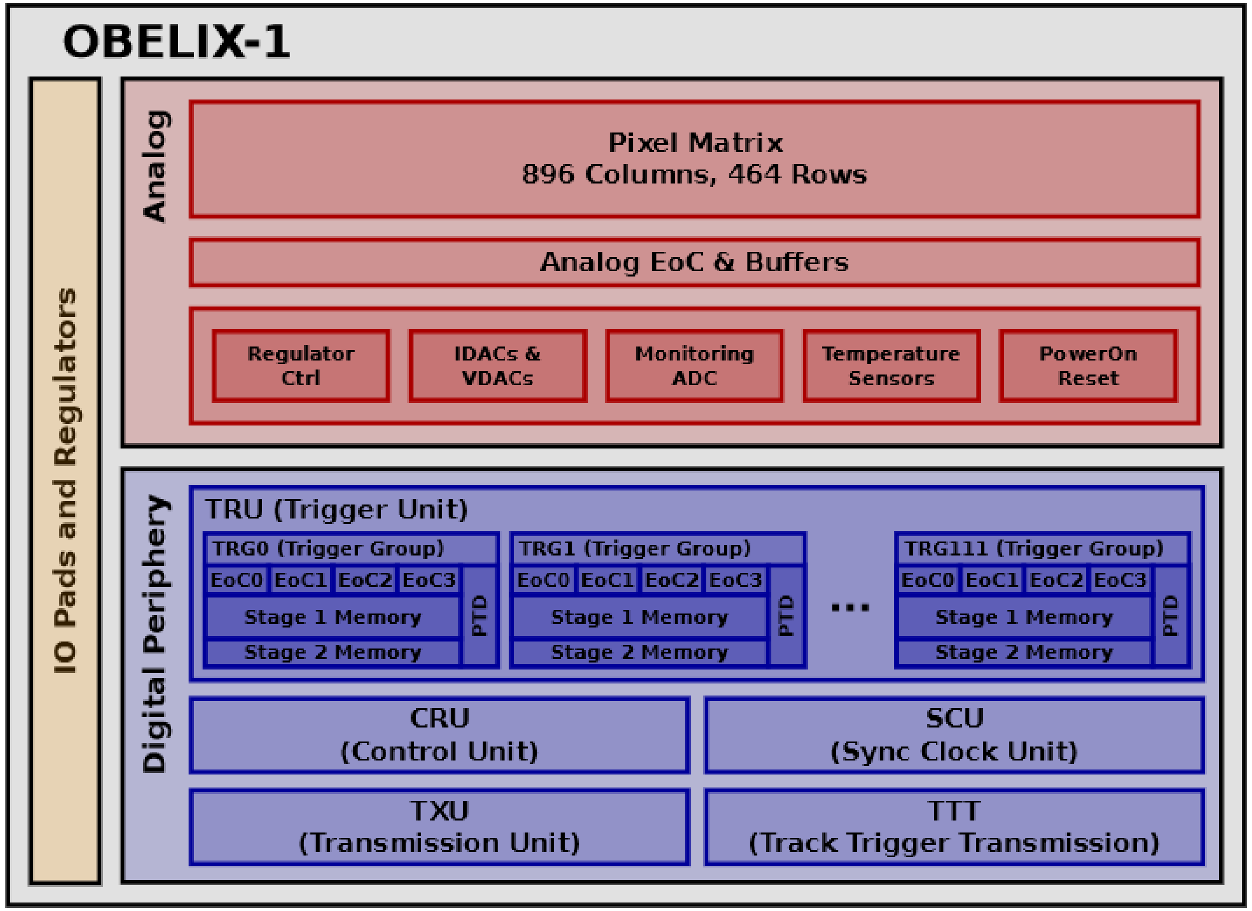


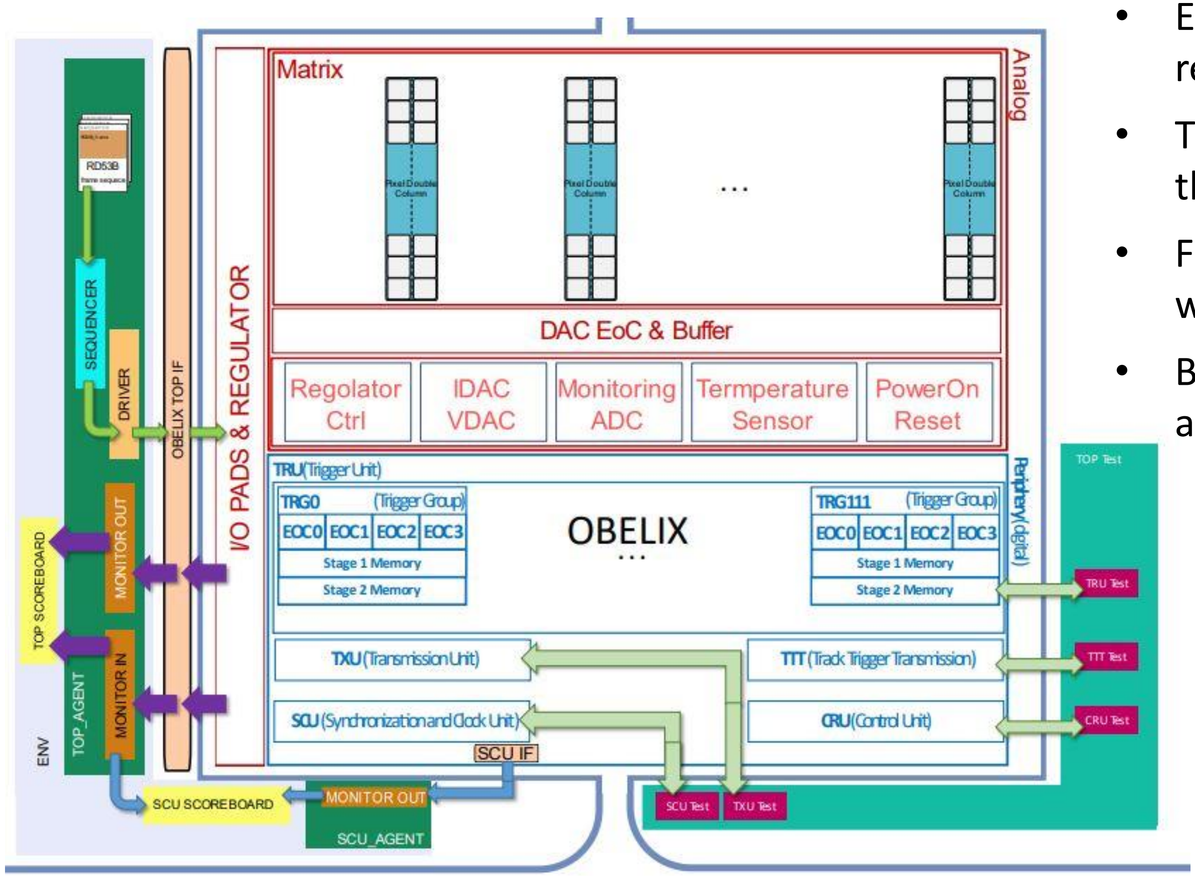
Figure : Module division of Obelix top

- Module division : 4 main parts + 2 features
- **SCU – sync & clk divider**: digital clk divider, synchronize circuit & clk divider, RxDat format conversion, main function: clock divider, Rx_data SIPO synchronization
- **CRU – Control Unit**: Implementation RD53B interface, which almost keeps the same design as TJ-Monopix 2, main functions: command decoder, global register configuration
- **TRU – Trigger Unit**:Manage pixel data from the matrix-EOC and wait for the trigger to pick them for output
- **TXU – TX Unit**: generate output data and sequential output, main functions: data framing, serializer
- **TTT**, track trigger transmission
- **PTD**, peripheral Time to Digital
- **Should be submitted at the end of 2024**

- Current participating institutions:

OBELIX_V1 : Verification

- UVM:
  - Universal Verification Methodology
  - Based on SystemVerilog
  - Verification plan outlining OBELIX features to be scrutinized from the design top point of view
  - System operation emulation approach
  - Access to inner blocks of the design from the top module w/o changing the design (bind construct) e.g. SCU
  - In the TOP_SCOREBOARD the reference model is computed decoding the command and payload RD53B input frame received from the MONITOR_IN and decoding the 8b10b stream received from the MONITOR_OUT of the TOP_AGENT



COCOTB data flow

UVM output data flow

UVM input data flow

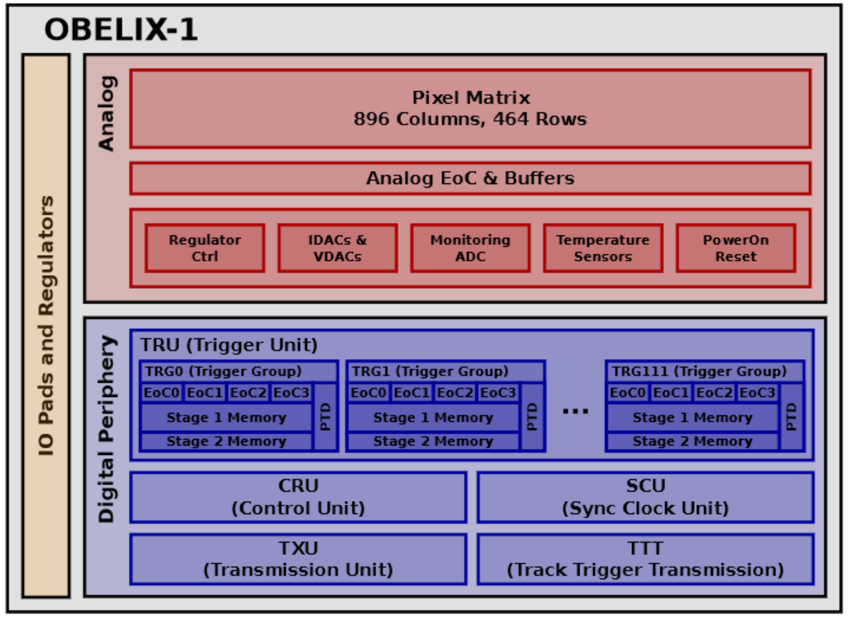
- COCOTB:
  - Based on Python
  - Easier to access more intuitive respect to UVM
  - The test for OBELIX developed by the designer to verify each module
  - Fully integrated with CI/CD Gitlab work flow
  - Based on multiple test for specific aspect of the design

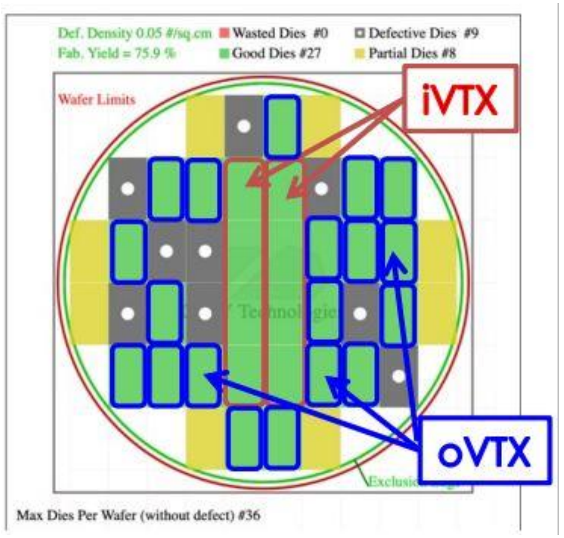
Conclusions

- The CPPM team works on hybrid pixel technologies, either for the ATLAS ITk project (RD53 / TSMC 65 nm), or in R&D for future colliders in TSMC 28 nm
- ATLAS ITk is now nearing full blown production, aiming for installation in 2027. The TSMC 28 nm technology seems a good focal point of interest for future development
- Beautiful developments have occurred in Depleted MAPS technologies, with prototypes produced in 10 different technologies
- Among others, the community is now focusing on AMS prototypes, LF (110nm and 150nm), and TJ 180nm and TPSco 65nm
- Obelix: the overall design work has been completed, except for some detail modifications
- Next two months will focus on the integration of the entire chip and design verification
- Obelix is about to be submit at the end of this year (2024)

Back up slides

The **O**ptimized **BEL**le II p**IX**el sensor



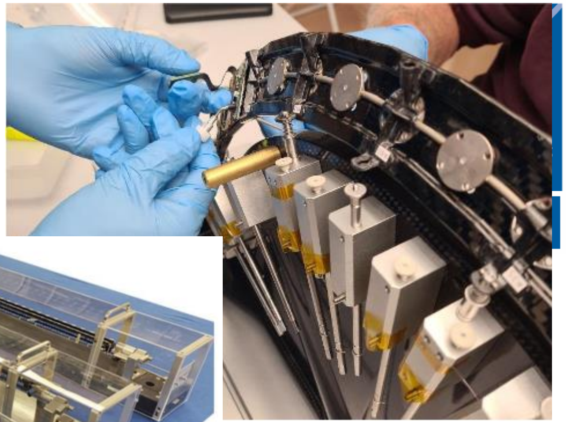


- Main design based on the TJ-Monopix2 chip with TJ180nm
- Chip size optimized to maximize the number of 4 contiguous sensor
- **Pixel Matrix**
  - Transplant from TJ-Monopix2 – radiation tolerance granted
  - Possible power optimisation
  - Freq 10-30MHz
- **New digital periphery**
  - New EoC adapted to Belle II trigger – 30KHz & with 5-10µs latency
  - Main Clk at 160MHz, Single output at 320Mb/s
  - Signal digitization: ToT (7 bits, 20 MHz)
  - RD53B* control protocol
- **Power Pads**
  - Power regulator added
  - Simplified system integration

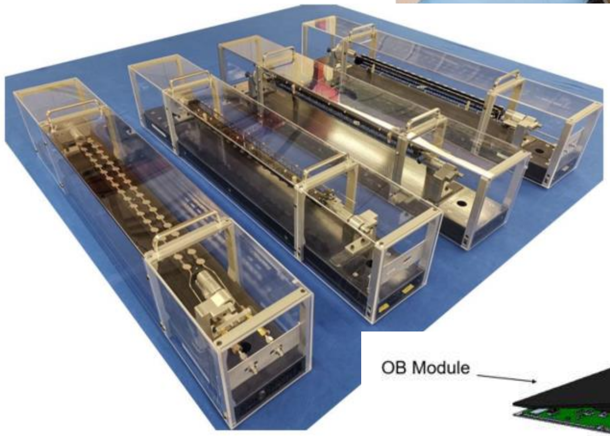
- **RD53B protocol:**
- RD53B users guide - CERN Document Server

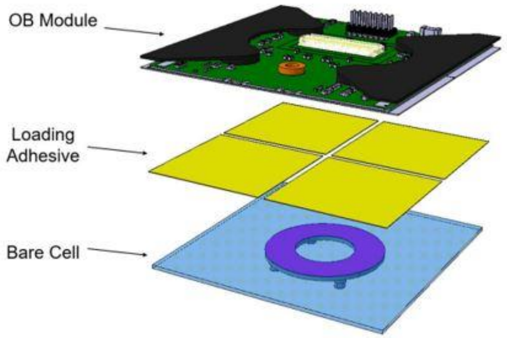
ATLAS and ITk detector

Mechanical activities at CPPM

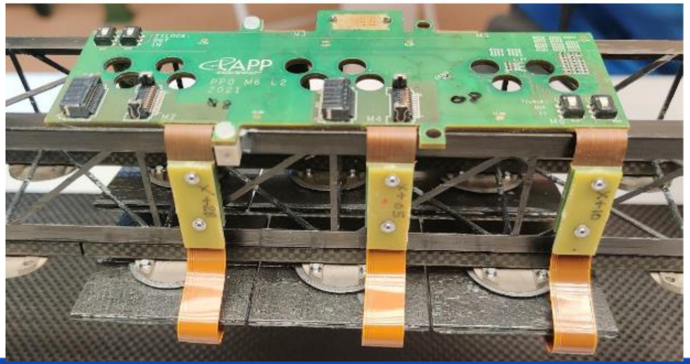


- CPPM is involved in:
  - **Designing and procuring the multipurpose tool called Handling frame.** This tool is used to handle local support all along the assembly and testing phase of the project to safe the operation and secure these fragile object up to the final integration at CERN
  - **Designing tool and qualifying the cell loading process.** This consists to define the glue deposition process and the module accurate loading on cell
  - **Designing and defining the cell integration on local support process.** This consists to set the services (pigtail and Patch panel) integration and connection, loaded cell integration into the local support
  - **Setting the testing facilities for single module at reception and loaded local support prior** to delivery to CERN
- **Outer barrel assembly and integration** will be split in 6 sites, CPPM will be one of them (~ 1500 modules to handle)→ **setting a clean room** (dust and humidity control, ESD protections, temperature control)dedicated for all construction operations
- On **local support** we will be involved in all metrological QC control of local support and procurement of the micro screws used to fix cell on local support
- CPPM is **in charge of designing the service trolley used to pack all services before ITK pixel insertion inside the strips detector**



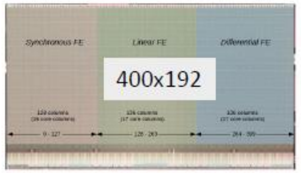


[1] A modified version developed in Japan combines 'Module Assembly' and 'Cell Loading' in a single step



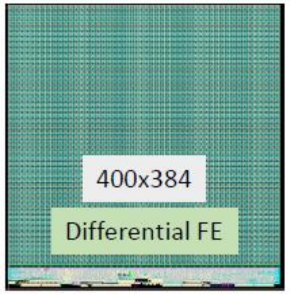
RD53 Projects

- **RD53 collaboration** was established to design and develop pixel chips for **ATLAS/CMS phase 2 upgrades**
- The RD53 project includes 24 institutes - ~20 designers
- **Extremely challenging requirements for HL-LHC**
  - **Hit rates**: 3 GHz/cm², Small pixels: 50 x 50 µm²
  - **Radiation**: **500 Mrad** - 10^{16} neq/cm² over 5 years
- Technology: **TSMC 65nm CMOS**



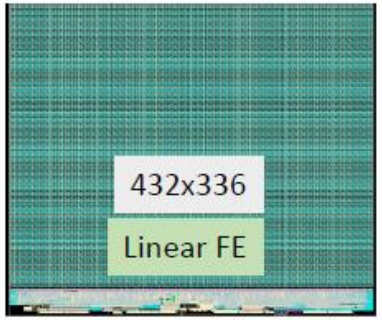
RD53A
Size: 20 x 11.5 mm²
submitted in August 2017

→



RD53B-ATLAS (ITkPix-V1)
size: 20 x 21 mm²
Submitted in March 2020

→



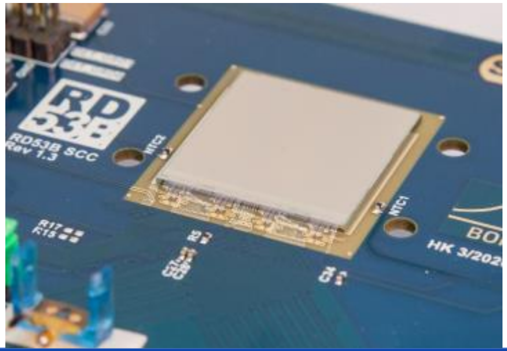
RD53B-CMS (CROC-V1)
size: 21.6 x 18.6 mm²
Submitted in May 2021

RD53C-ATLAS (ITkPix-V2)
Submitted in March 2023

→

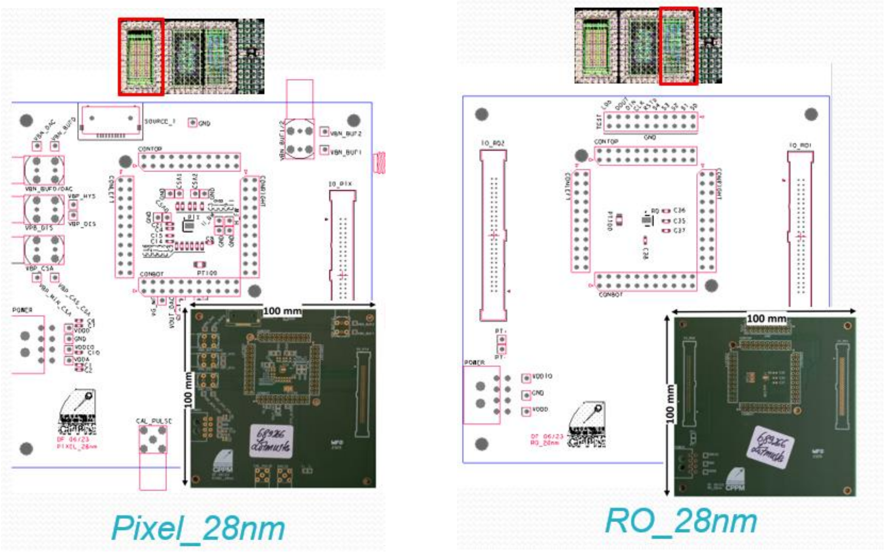
RD53C-CMS (CROC-V2)
size: 21.6 x 18.6 mm²
Submitted in Sept 2023

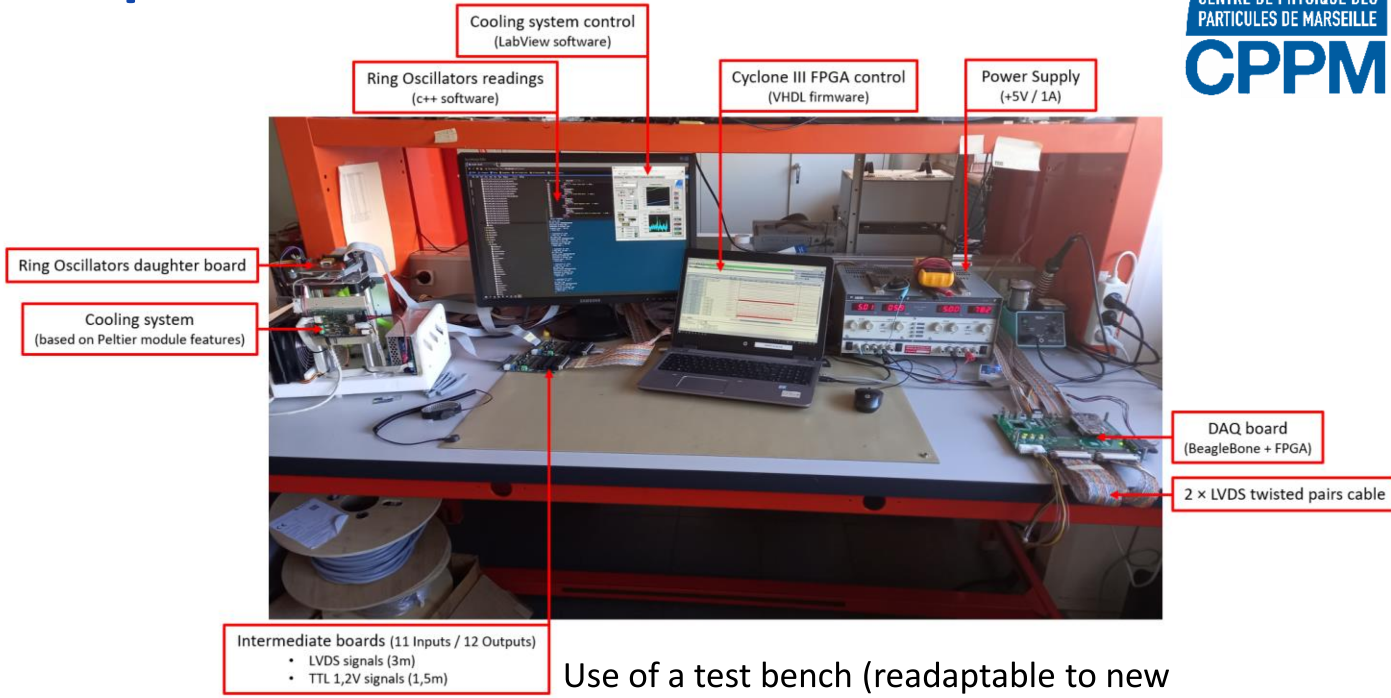
- Characterization of the TSMC 65nm process in radiation
- **Several prototypes to qualify IP blocs (Analog FE, ADC, DAC, CDR/PLL, ShuntLDO …)**
- **RD53A chip,** Large-scale demonstrator with 3 FE flavors, Submitted in August 2017 and tested in an intensive way
- **ATLAS and CMS chips** are two instances of **the same common design**, having different sizes and different Analog Front-End
- **RD53B chip (preproduction)**
  - ITkPix-V1 (ATLAS chip) submitted in March 2020
  - CROC-V1 (CMS chip) submitted in May 2021
- **RD53C chip (Production)**
  - ITkPix-V2 (ATLAS chip) received in July 2023 and is still under tests and characterization
  - CROC-V2 (CMS chip) is submitted in September 2023



Future hybrid pixel in 28 nm at CPPM

The 28nm prototype was received on June 23 2023





Use of a test bench (readaptable to new needs) based on BeagleBone DAQ board

On-going

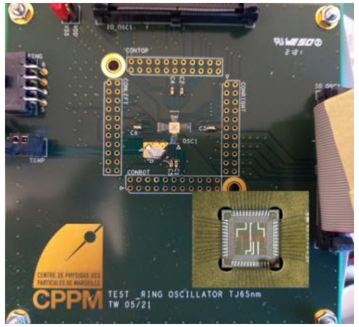
- **Test setup in preparation**
  - Adaptation of the setup based on **board beaglebone**
  - Functional tests in Q4 2023 followed by irradiation tests (TID and SEE) in Q1 2024

- **Forecast:**
  - The signing of a 3-way NDA took place -- facilitation of the next designs
  - Use of the CERN PDK in the future and expected submission in Q3 2024

Monolithic pixels -- Exploratory R&D TJ65

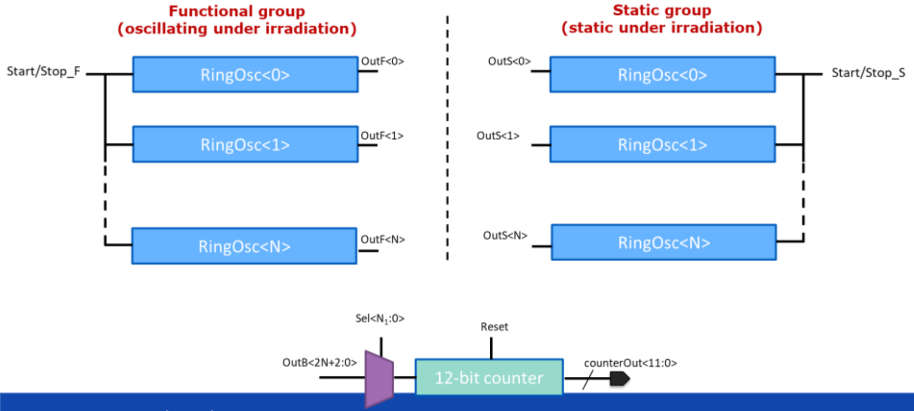
- **Check basic performance**
- **Dedicated prototype(s) for high count rates (>> 100 MHz/cm²)**
- **Temporal resolution around 100 ps**
- **Radio tolerance >>10^{15} neq/cm²**

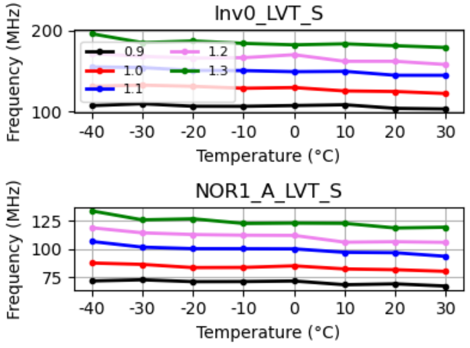
* Submitted December 2020, back in summer 2021



DUT board

- **The CPPM has contributed with a series of Ring Oscillators** whose aim is to study the resistance to ionizing radiation of standard cells of the digital libraries of the technology
- The chip contains 48 ring oscillators based on different standard cartridges. These differ in cell type, varying transistor lengths, multiple transistor thresholds, and two injection strategies
- 2 banks of 24 lines to test two configurations:
  - "Functional" bank for which oscillation is activated during irradiation
  - "Static" bank: for which there is no oscillation during irradiation





Freq vs t°C pour 2 RO et 5 Vddd

Test settings

- DUT board connected to DAQ
- The Vddd voltage : between 0.9 and 1.3V
- RO values -- C++ script & recorded data -- python
- Temperature tests : between -40 and 80°C
  - **Each RO showed a decrease in frequency as the temperature increased** (5-10% over 70°C)
  - Temperature has an impact on frequencies
- 2 chips were irradiated : 830 and 520 Mrad

Test results

- **Similar frequency degradations** were observed for both chips with differences between the different types of RO
- Several weeks of annealing at different temperatures (-20, 25 and 80°C) were carried out following the irradiation
- **An absence of cold recovery, a slight recovery at room temperature and reverse annealing** were observed
- **Frequency degradation is limited (12 to 25% for a total dose of 830 MRad)** regardless of the type of Ring Oscillator. Cell size is an important parameter (small cells are more affected than large ones)
- New production of wafers in Engineering Run took place with a different level of metallization than the previous one. Irradiations are planned for early next year to compare the two types of metallization

PCIe400 : a common readout board for LHCb

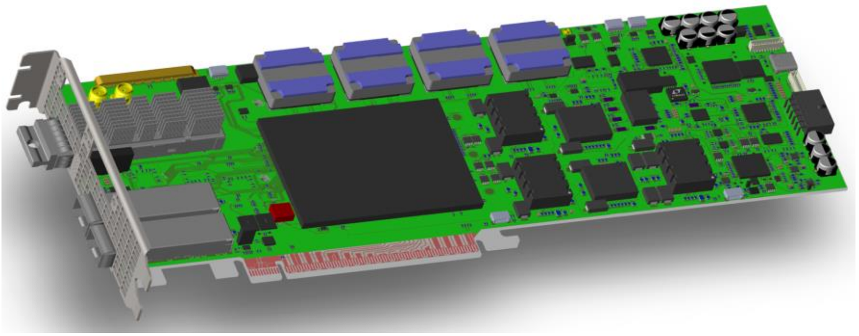
Designed for LS3 enhancement as a stepping stone for Upgrade II

- Increase the bandwidth x4 compared to current readout board
- Distribute LHC master clock to front-end in O(10) ps pk-pk
- Explore new DAQ topologies with a network interface on-board

Designed around latest and largest Altera's FPGA Agilex 7 M-series

- 4 Million of logic elements and 32 GB of High Bandwidth Memory
- Modern commercial links to back-end : PCIe GEN 5 & 400GbE
- Up to 48 link at 25 Gbps for front-end

PCIe400 Synoptic



PCIe400 is part of ECFA DRD7 efforts to prepare future developments

- 7.3b2 Timing distribution techniques
- 7.5b From front-end to back-end with 100GbE

Project groups 5 laboratories in IN2P3 and LHCb Online CERN group

- Prototypes should arrive in October 2024
- A production of ~100 boards is foreseen in 2026-2027