Assembly and Testing of HGTD Modules

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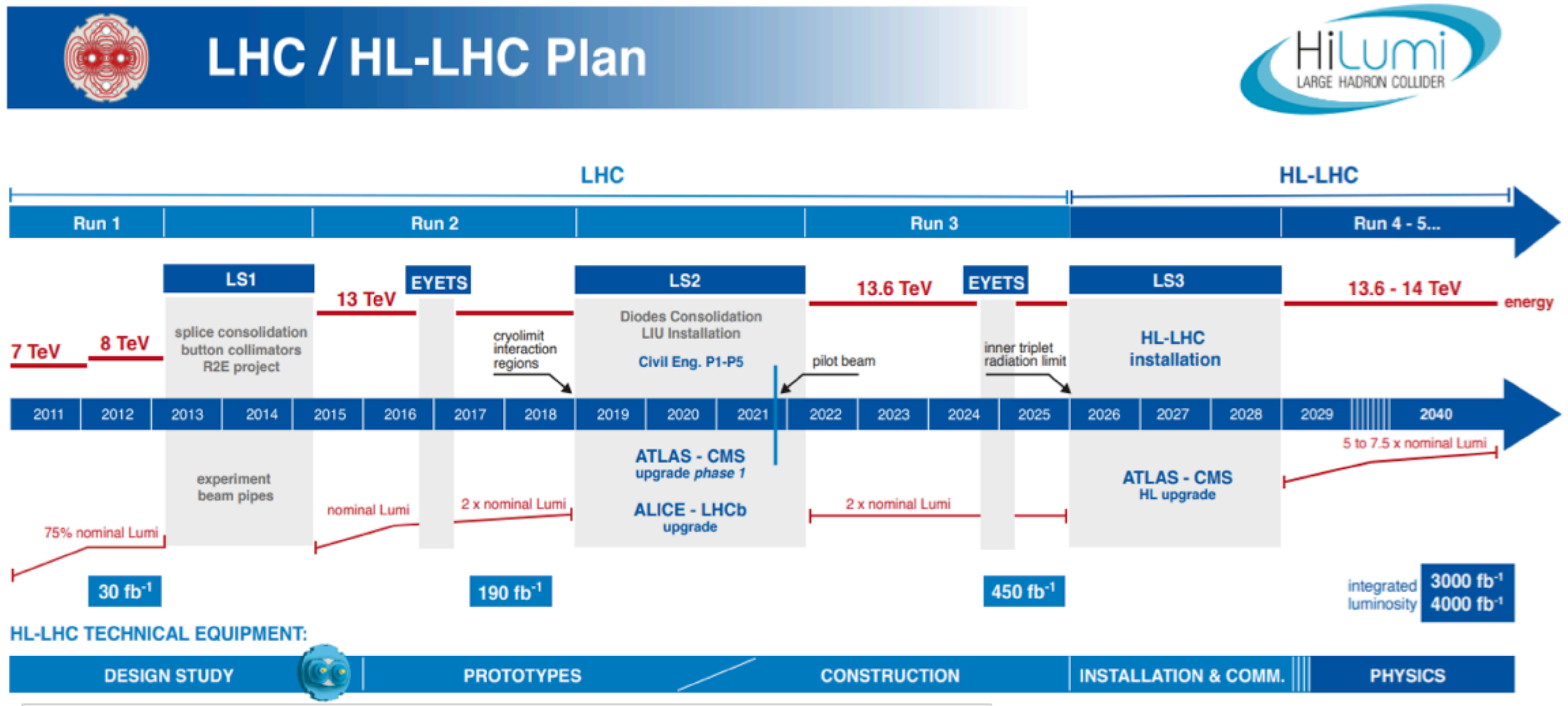
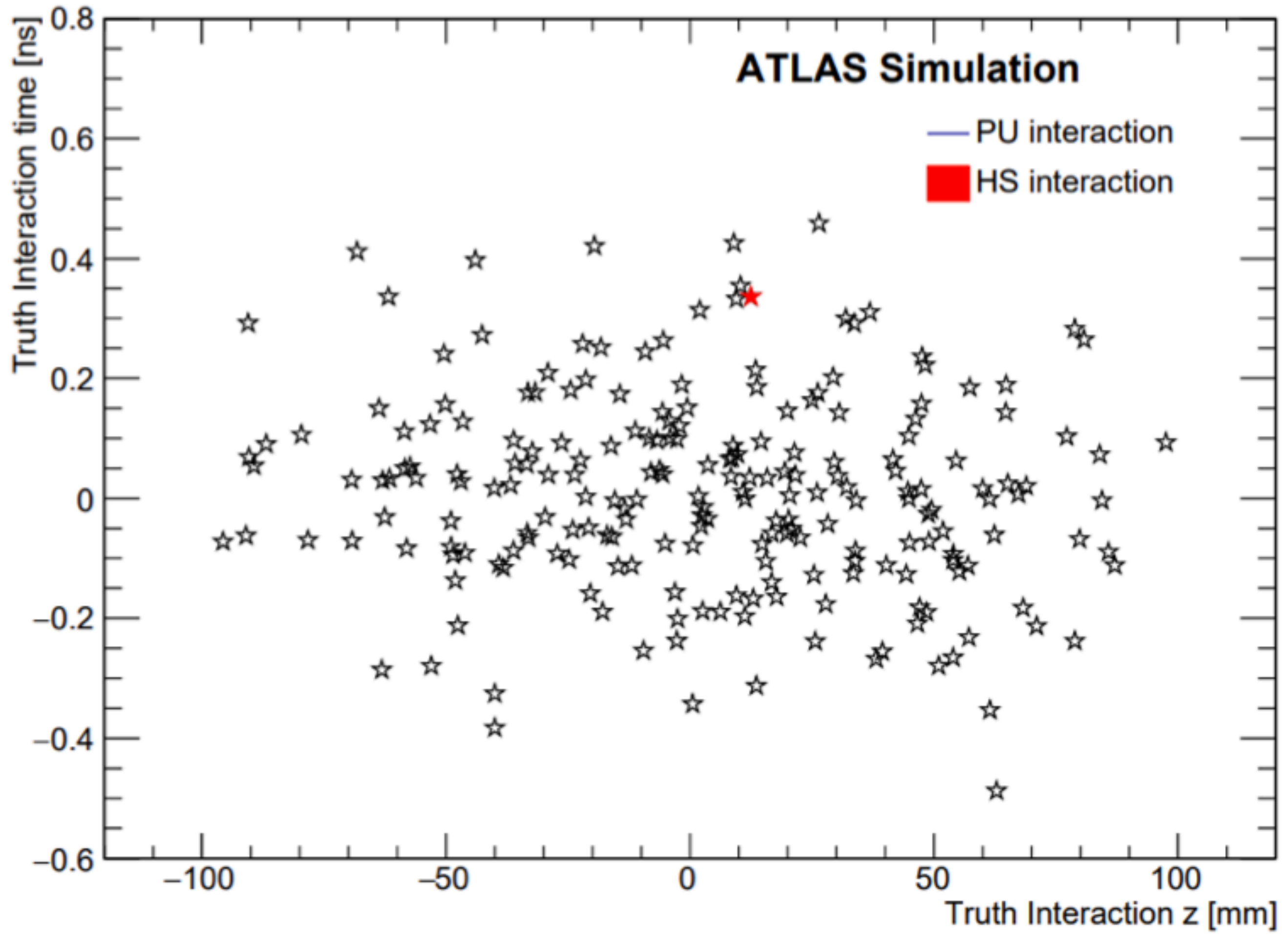
ATLAS EXPERIMENT

CERN

High-Luminosity LHC



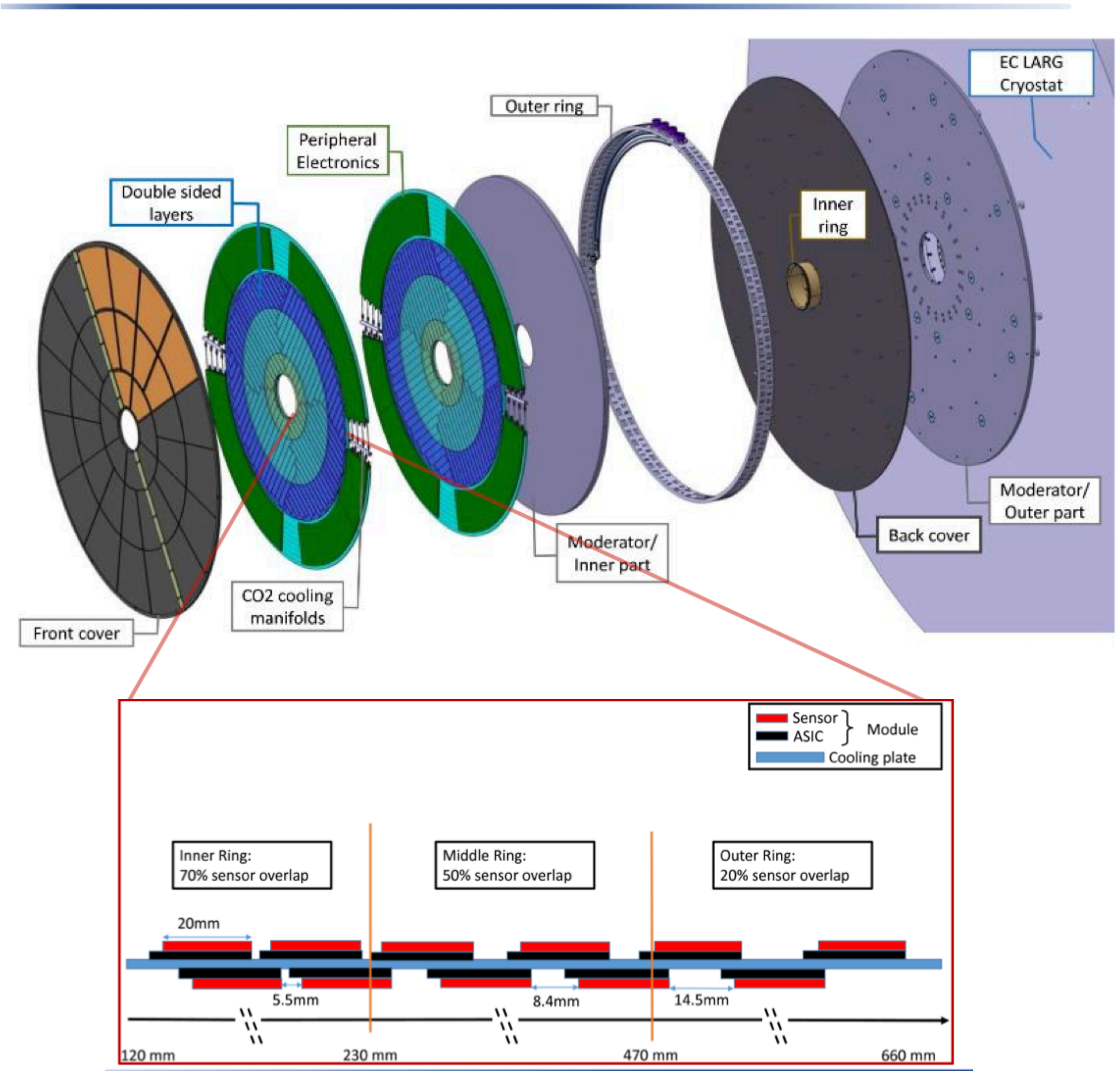


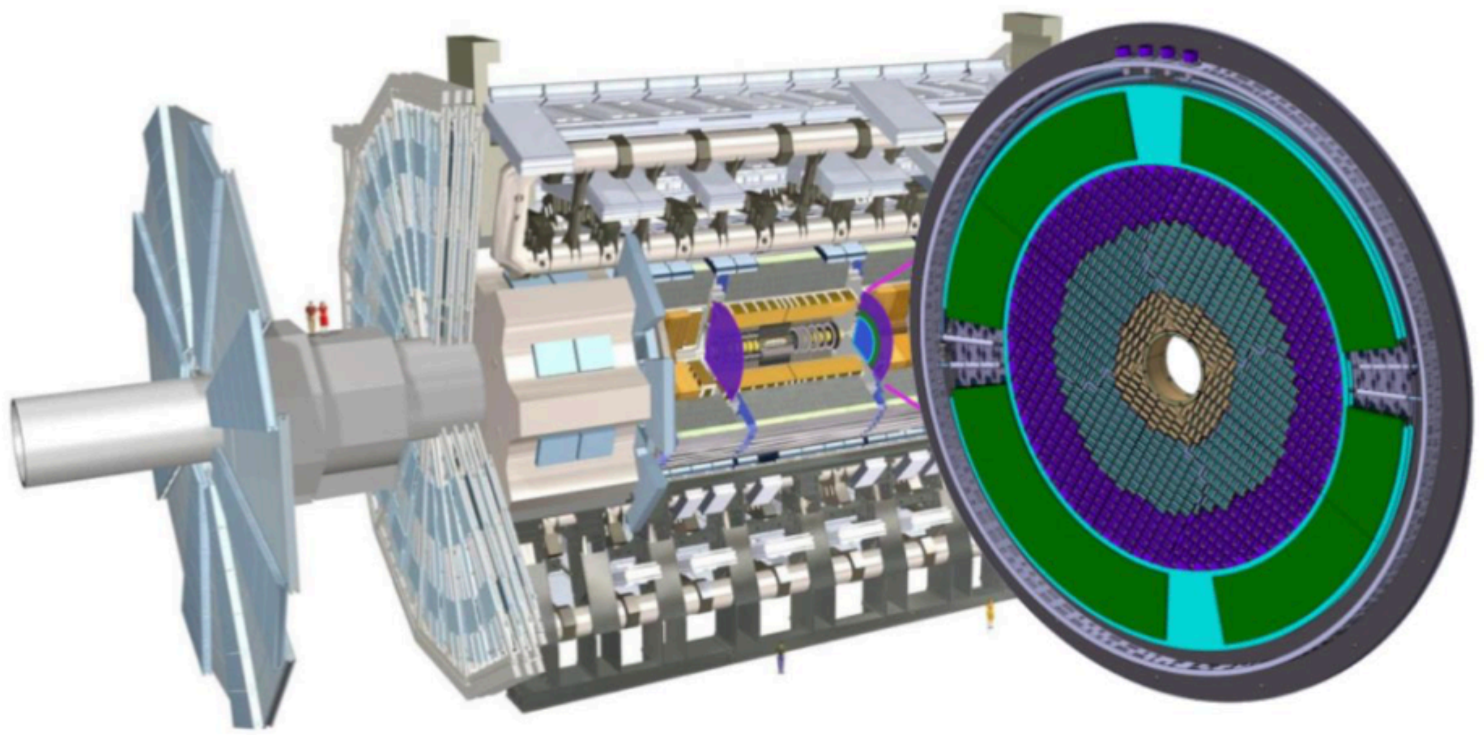
- LHC upgrade to HL-LHC: Planned to start operating in 2029
- Instantaneous luminosity $7.5 \times 10^{34} \mathrm{cm}^{-2}\,\mathrm{s}^{-1}$
- Increase in luminosity results in more pile-up and radiation damage
- ATLAS experiment also needs to be upgraded to meet the new requirements

- High Granularity Timing Detector (HGTD) proposed in front of the end-cap calorimeter for pile-up mitigation

- Adding timing information in the end-cap region improves pile-up rejection and vertex reconstruction

High Granularity Timing Detector

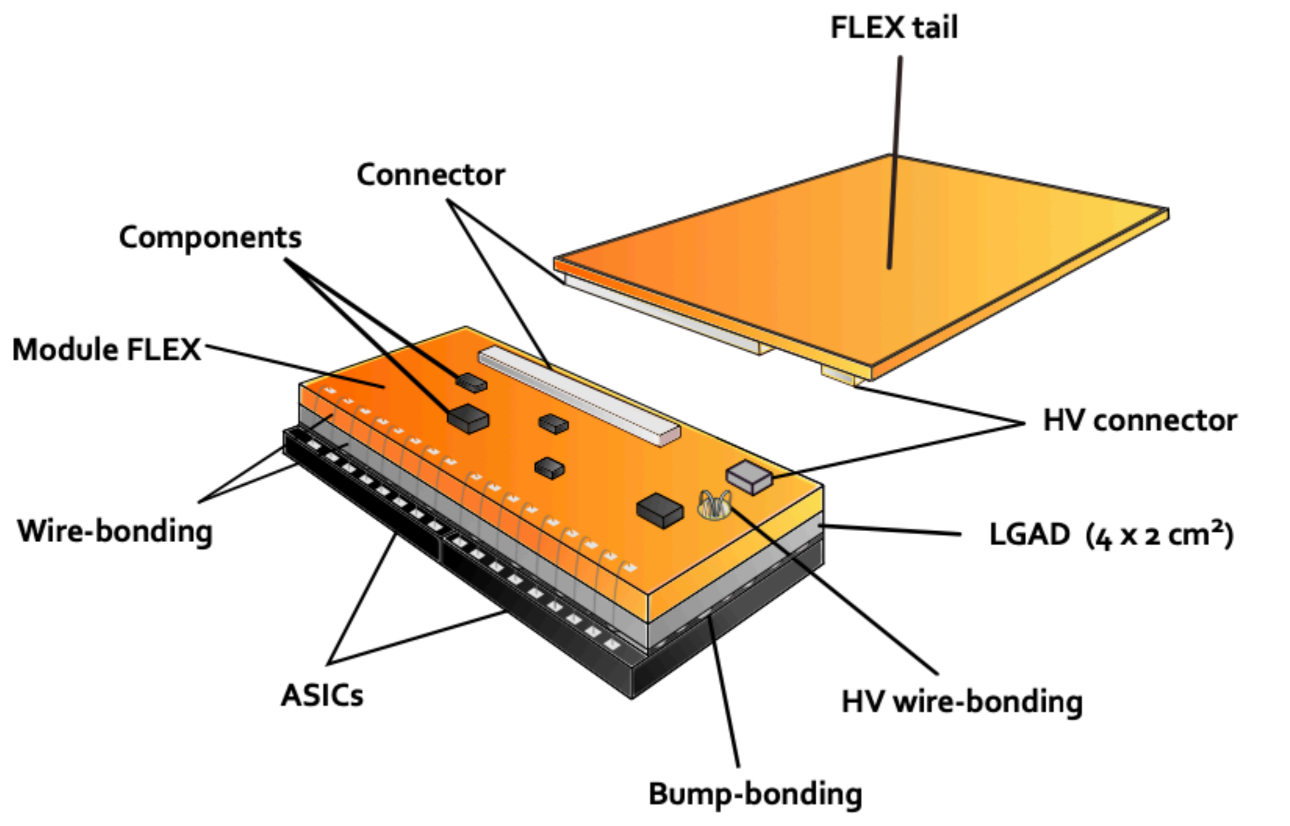




- Placed between the updated Inner Tracker (ITk) and the Liquid Argon Calorimeter
- Active area coverage: $2.5 < |\eta| < 4.0$
- Targets per track resolution 30-50 ps
- Operating temperature -30°C (CO_2 dual phase cooling)
- It consists of 8032 modules
  - ~2000 modules will be assembled at IJCLab (France)

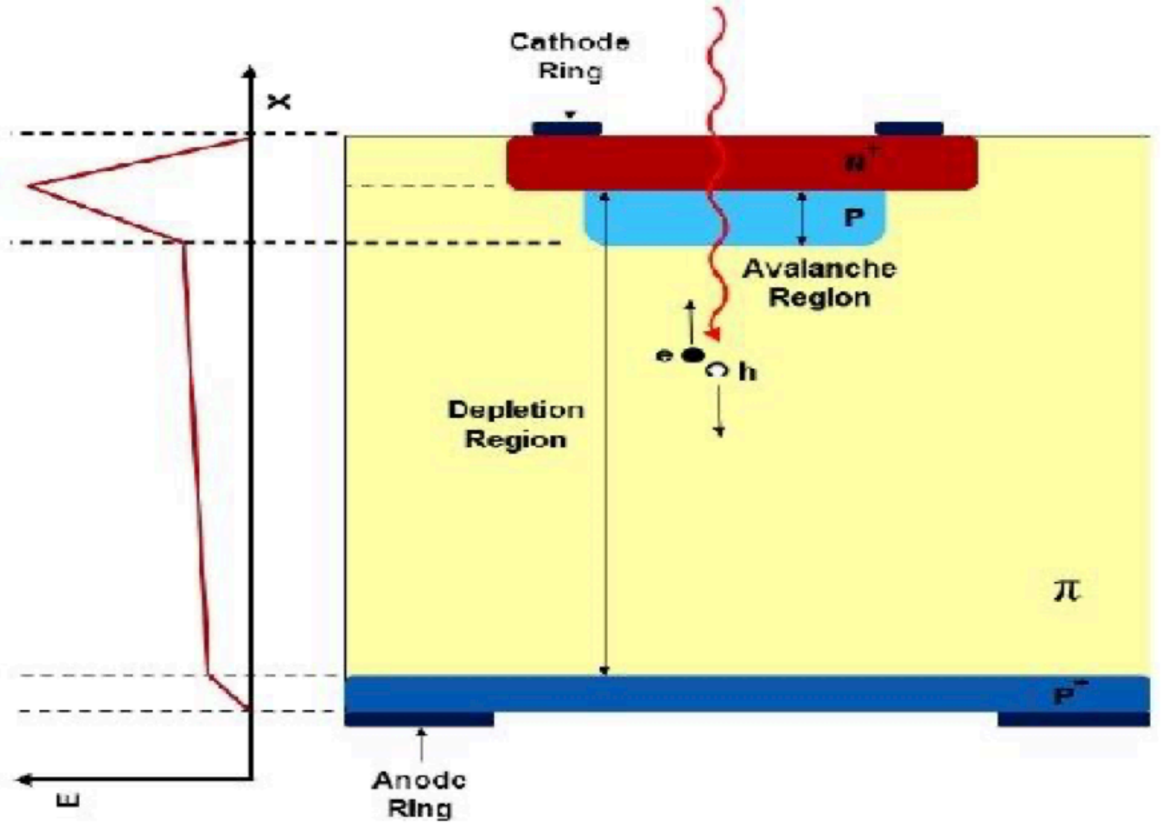
The HGTD modules

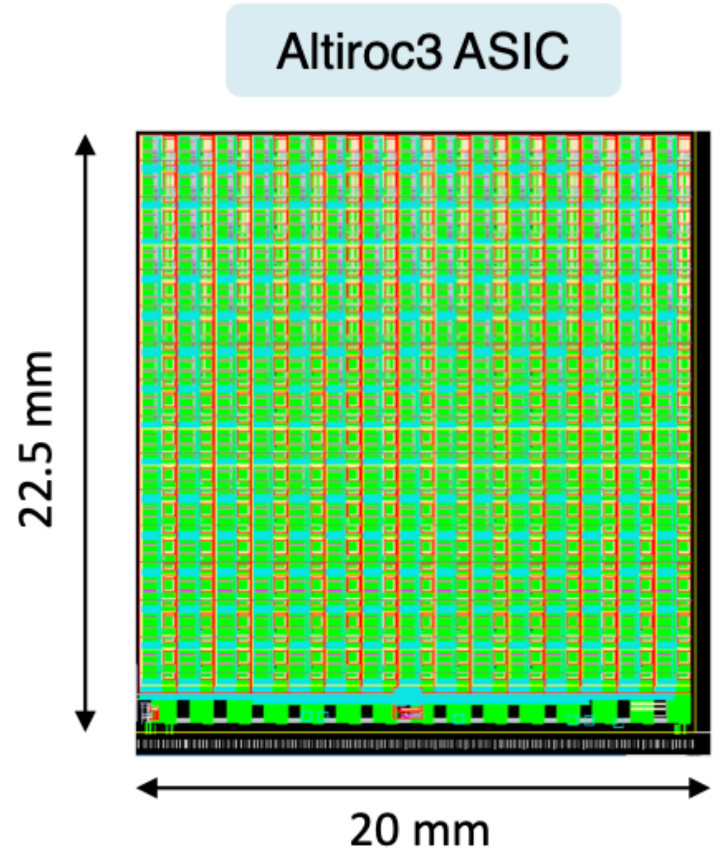
- An HGTD module consists of
  - Two LGAD sensors (2 cm × 2 cm)
  - Two ALTIROC ASICs (2 cm × 2 cm)
  - A module flex
  - A flex tail



*not to scale

- **L**ow **G**ain **A**valanche **D**etectors (LGAD)
- p-n junction based n on p silicon detector
- The usage of LGADs has a beneficial effect on time resolution
  - Vendors: IHEP-IME and USTC-IME



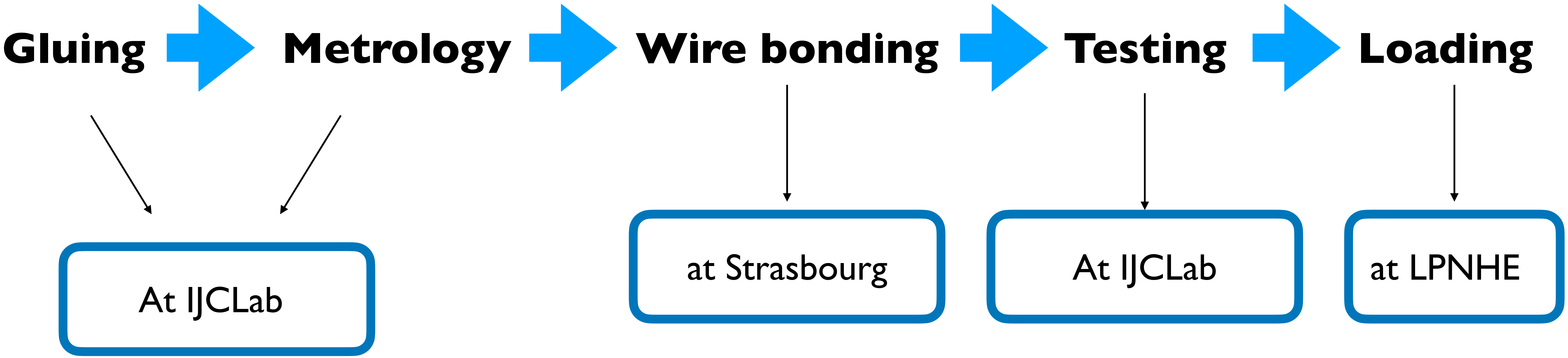


- **A**TLAS **L**GAD **T**iming **I**ntegrated **R**ead-**O**ut **C**hip
- 225 readout channels (15×15)
- Provides TOA and TOT information
- Provides luminosity in hits per ASIC per bunch crossing

- The sensor and the ASICs are connected through a flip-chip bump bonding process called hybridisation
  - Process done at IFAE (Spain) and NCAP (China)

Module assembly in France

on



Gluing → **Metrology** → **Wire bonding** → **Testing** → **Loading**

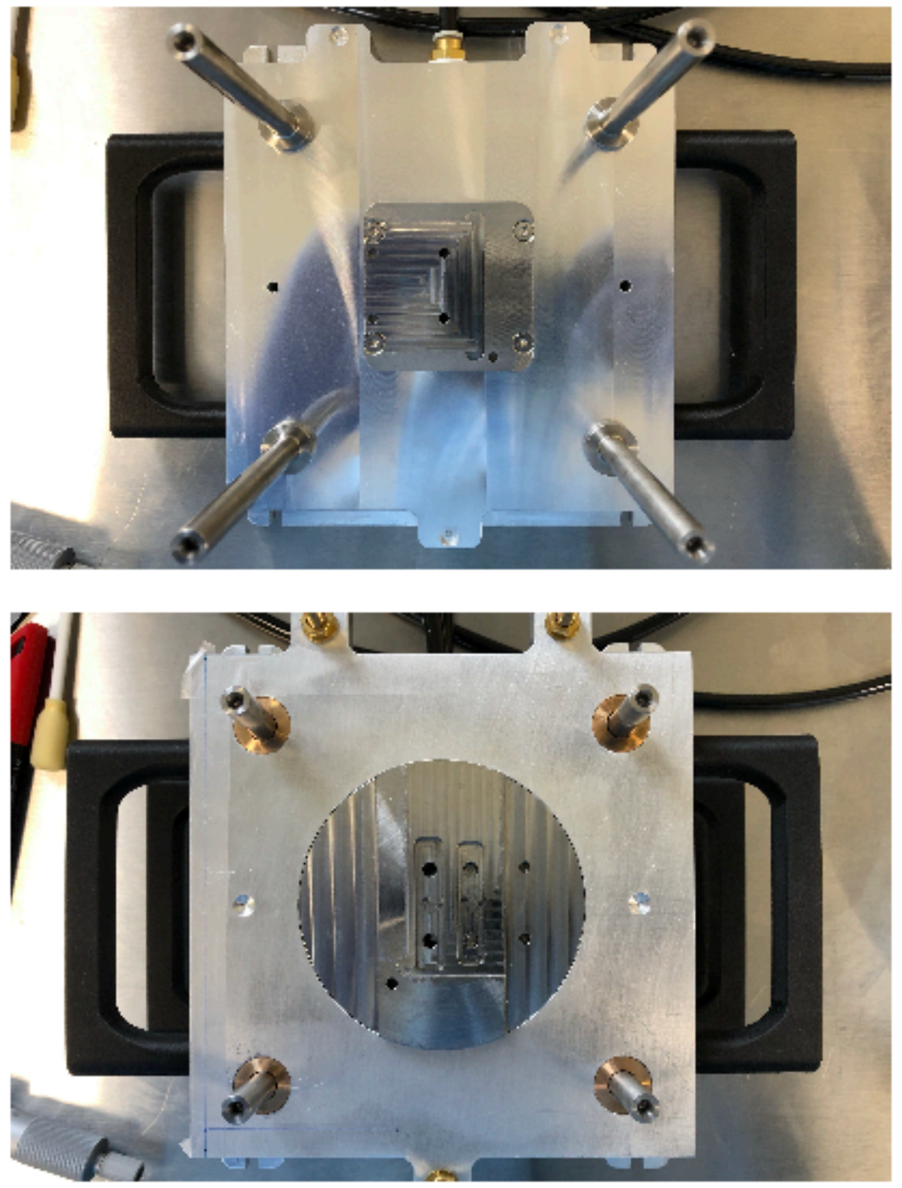
At IJCLab

at Strasbourg

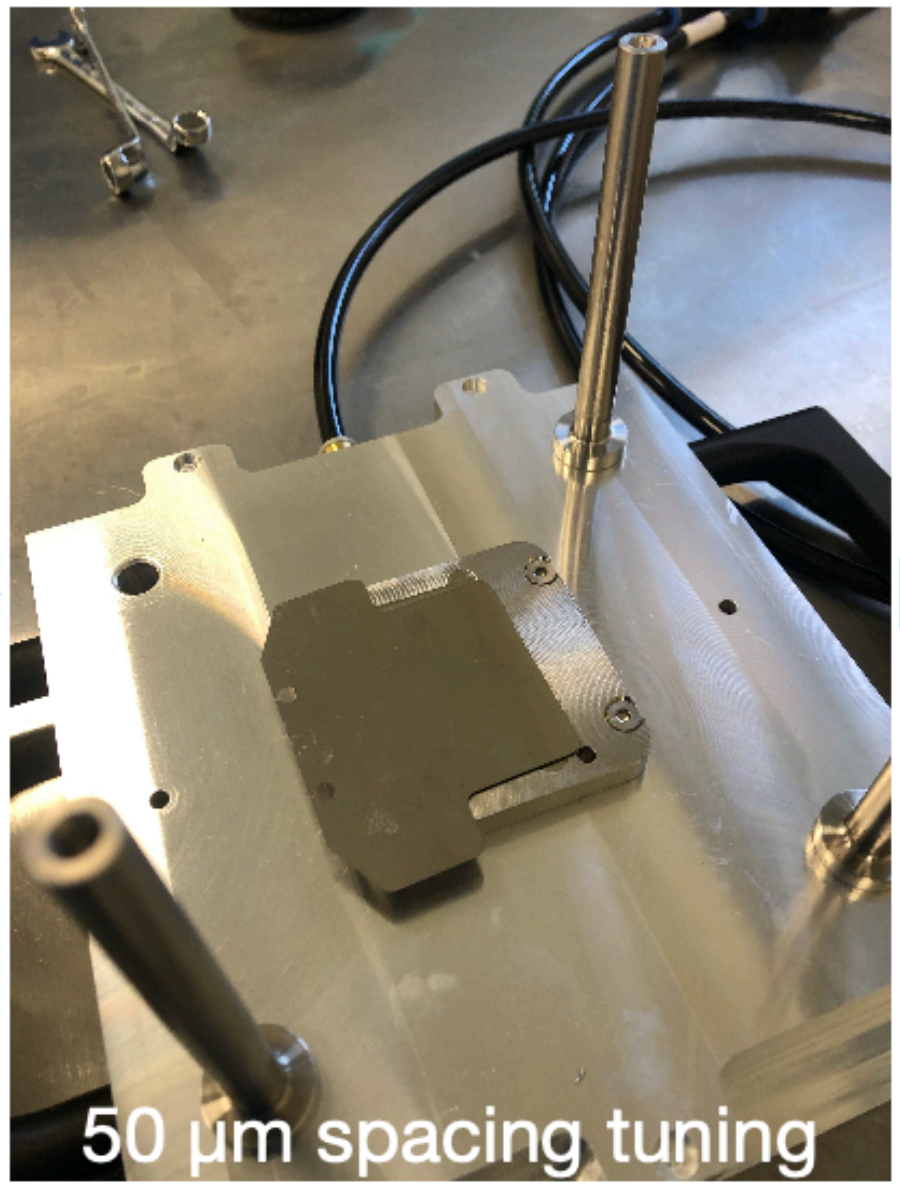
At IJCLab

at LPNHE

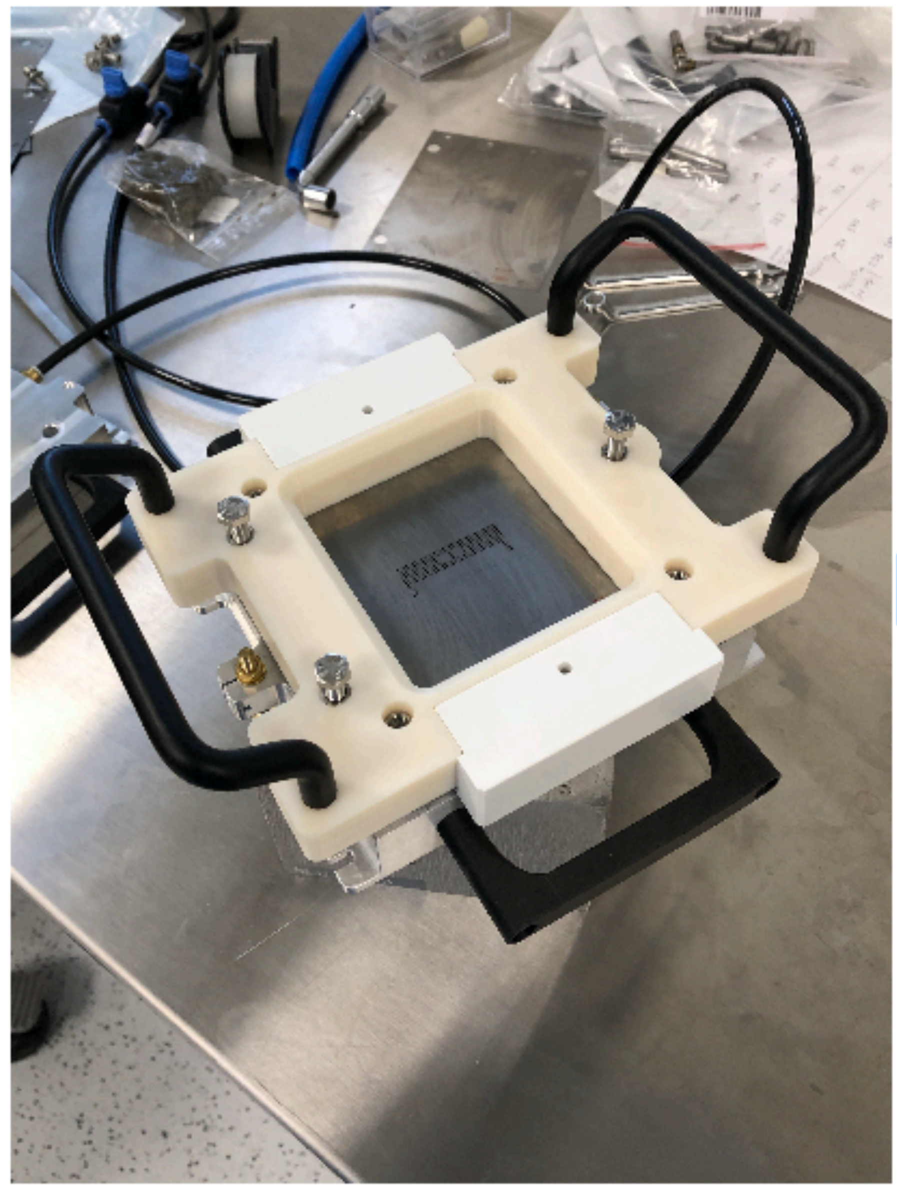
Assembly procedure at IJCLab



Pieces are held in inlays with vacuum and aligned with a jig (mechanical alignment)

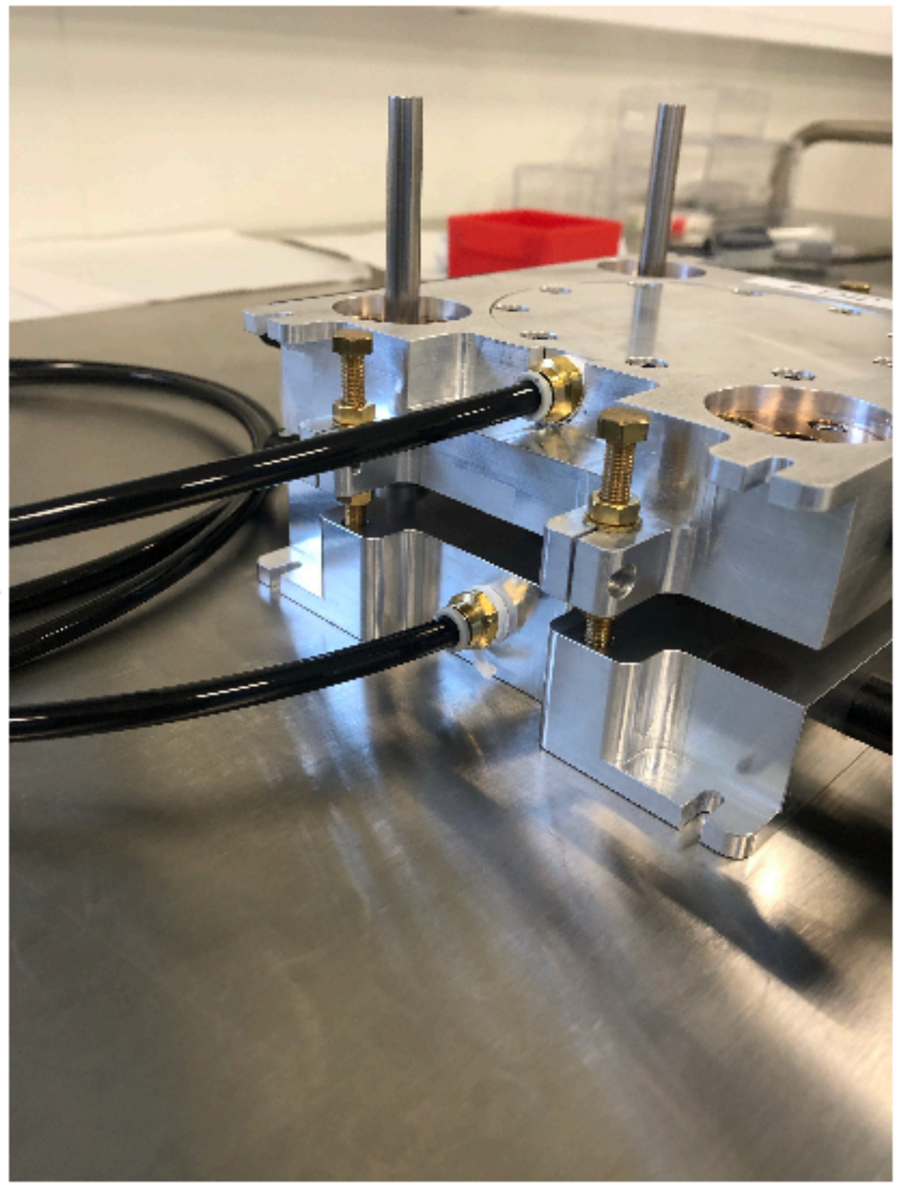


Vertical distance tuned with a calibrated thickness and controlled with small-step screws



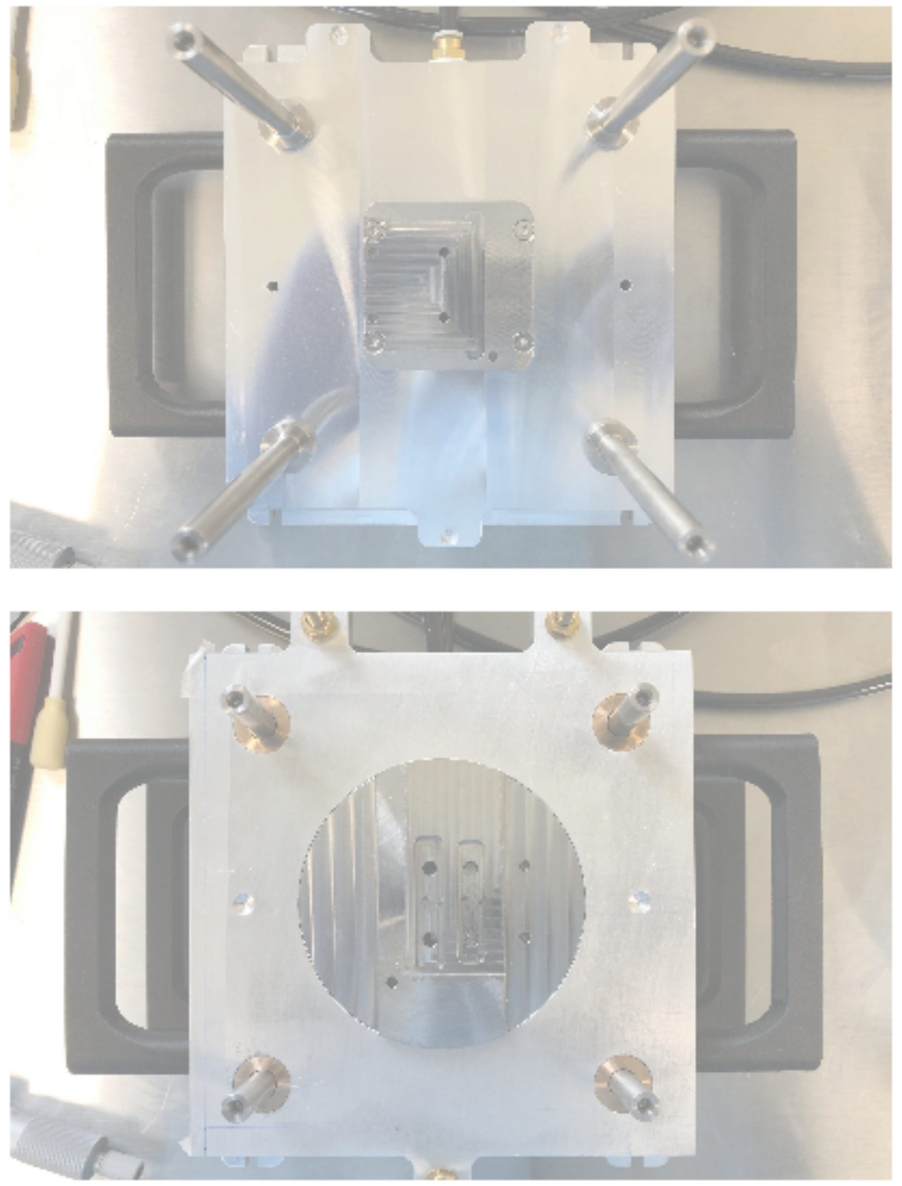
A frame is used to hold in place a stencil for glue deposition and align dots with module flex surface

Glue dots are deposited on flex with the stencil



Close the jig, elements are hold in place. Cure glue for 7-8 hours

Assembly procedure at IJCLab



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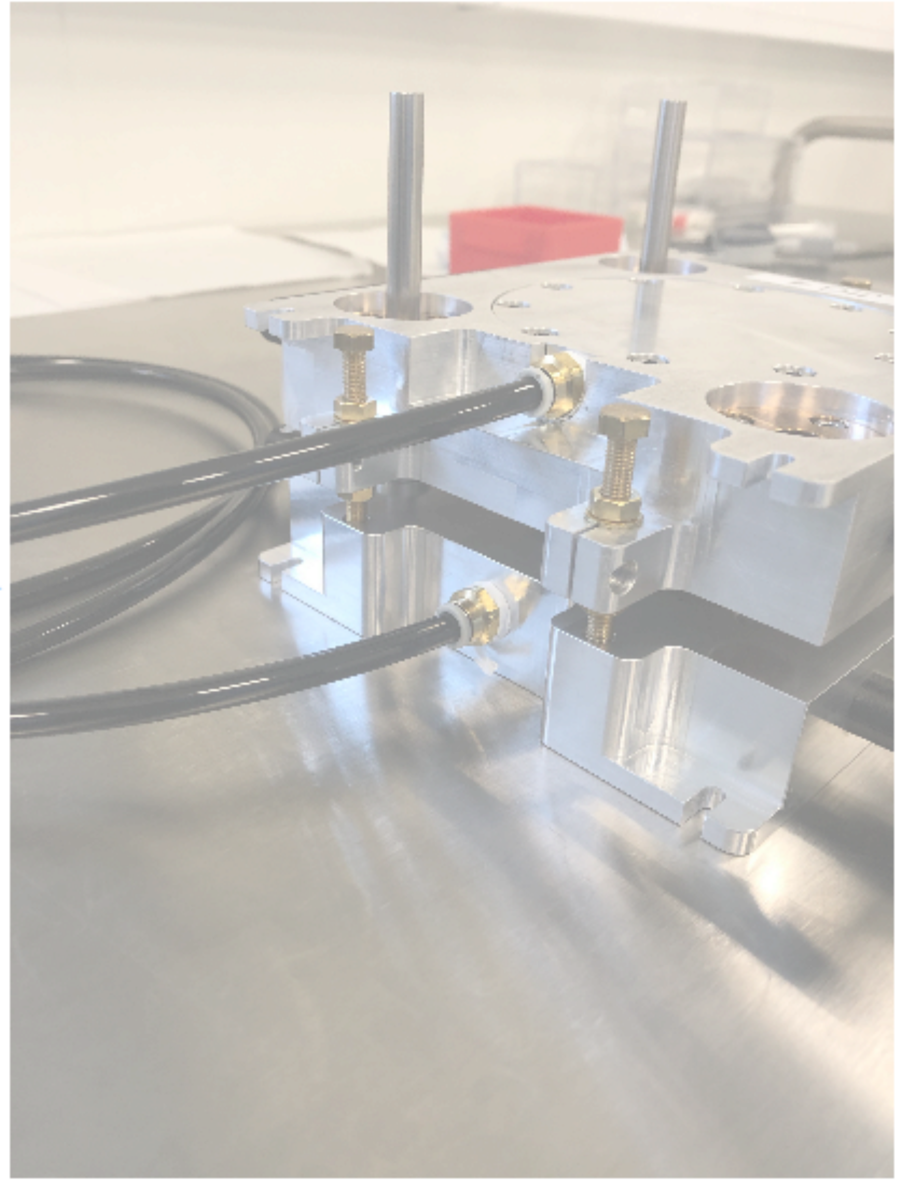
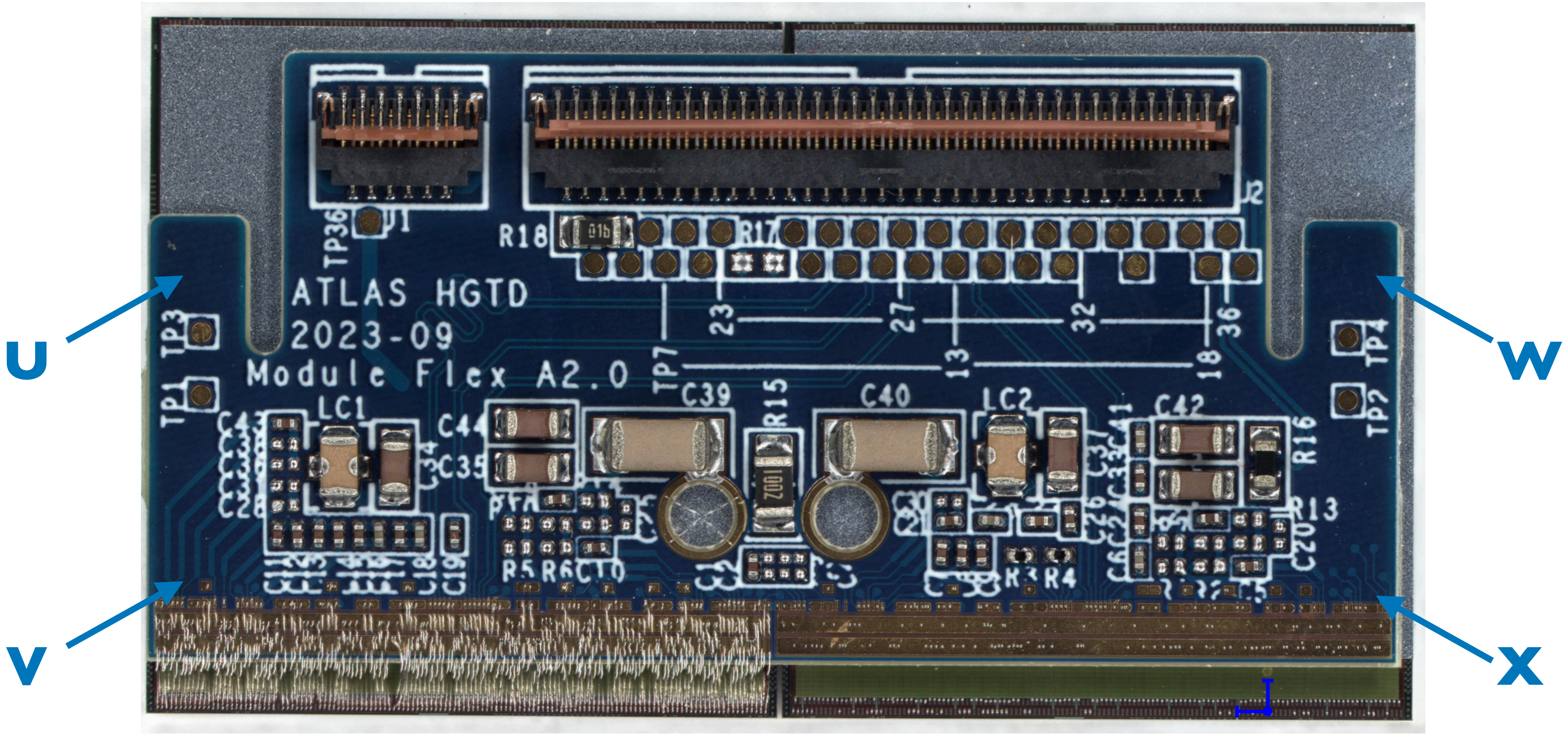
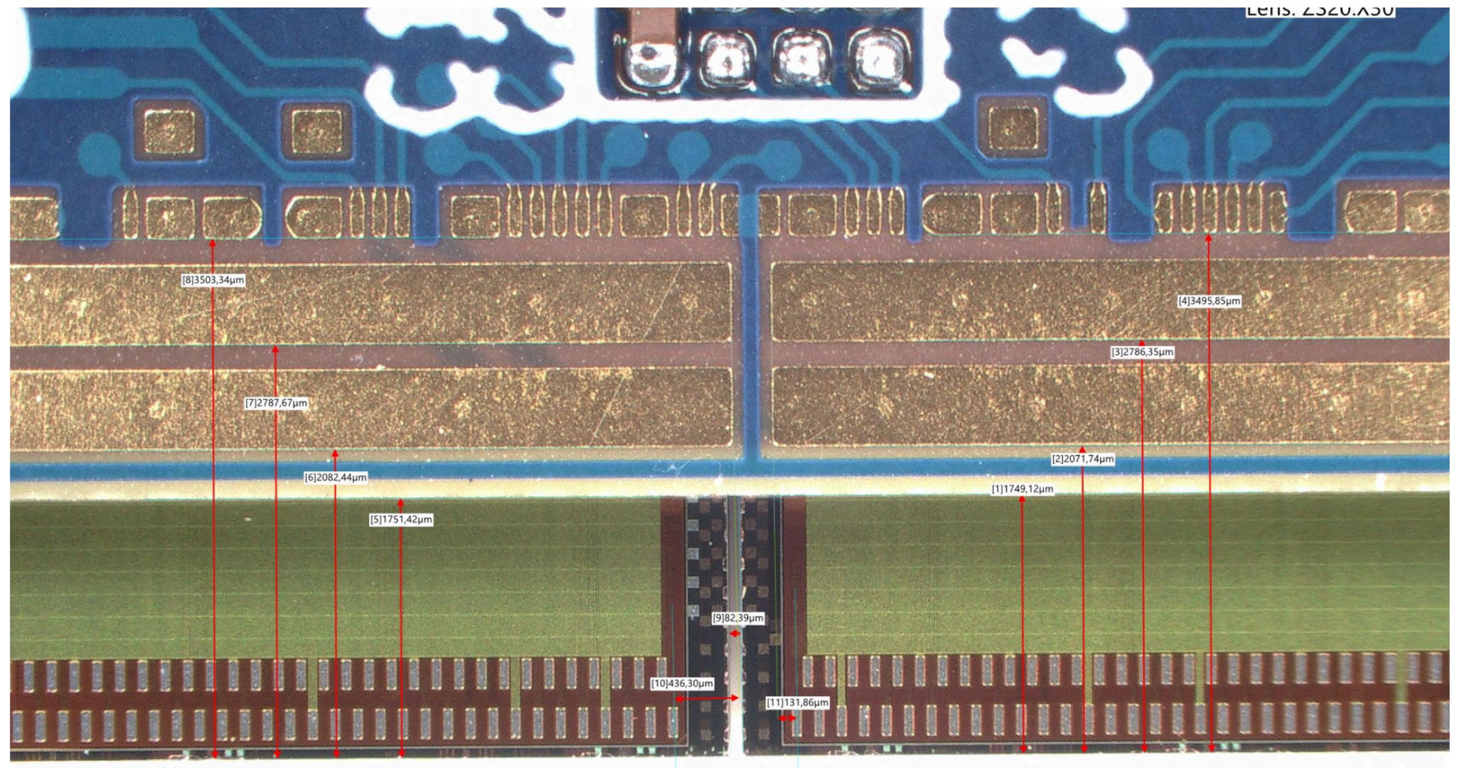


Close the jig, elements are hold in place. Cure glue for 7-8 hours

Metrology and wire bonding

- After gluing process we need to confirm good metrology
  - Distance between two ASICs
  - ASIC-flex distance
  - Thickness/weight
- Once confirmed, modules are sent to Strasbourg to get wire bonded
  - Connecting pads on the ASICs with the pads on the flex
  - Once fully wire-bonded, modules are ready to be tested



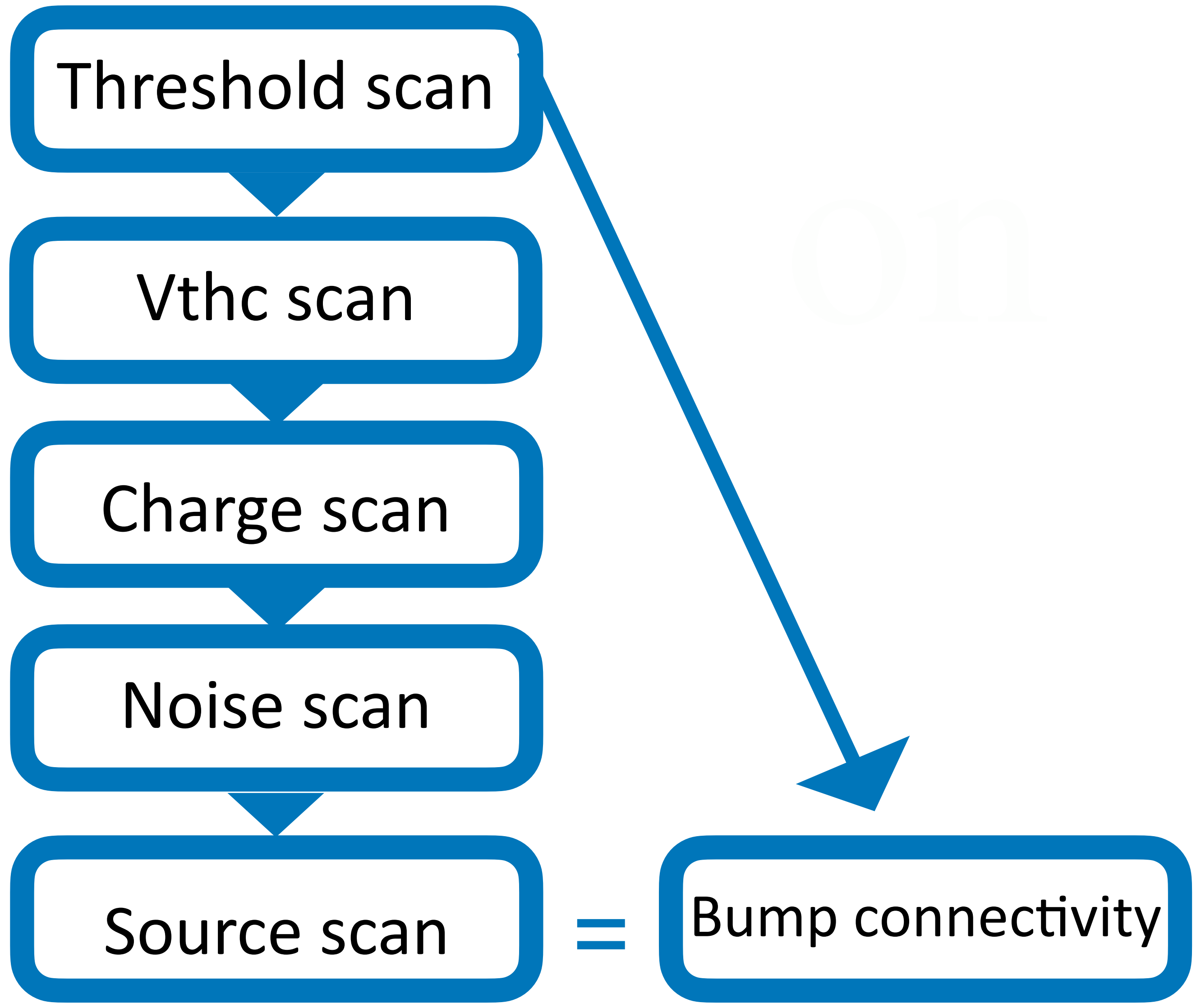


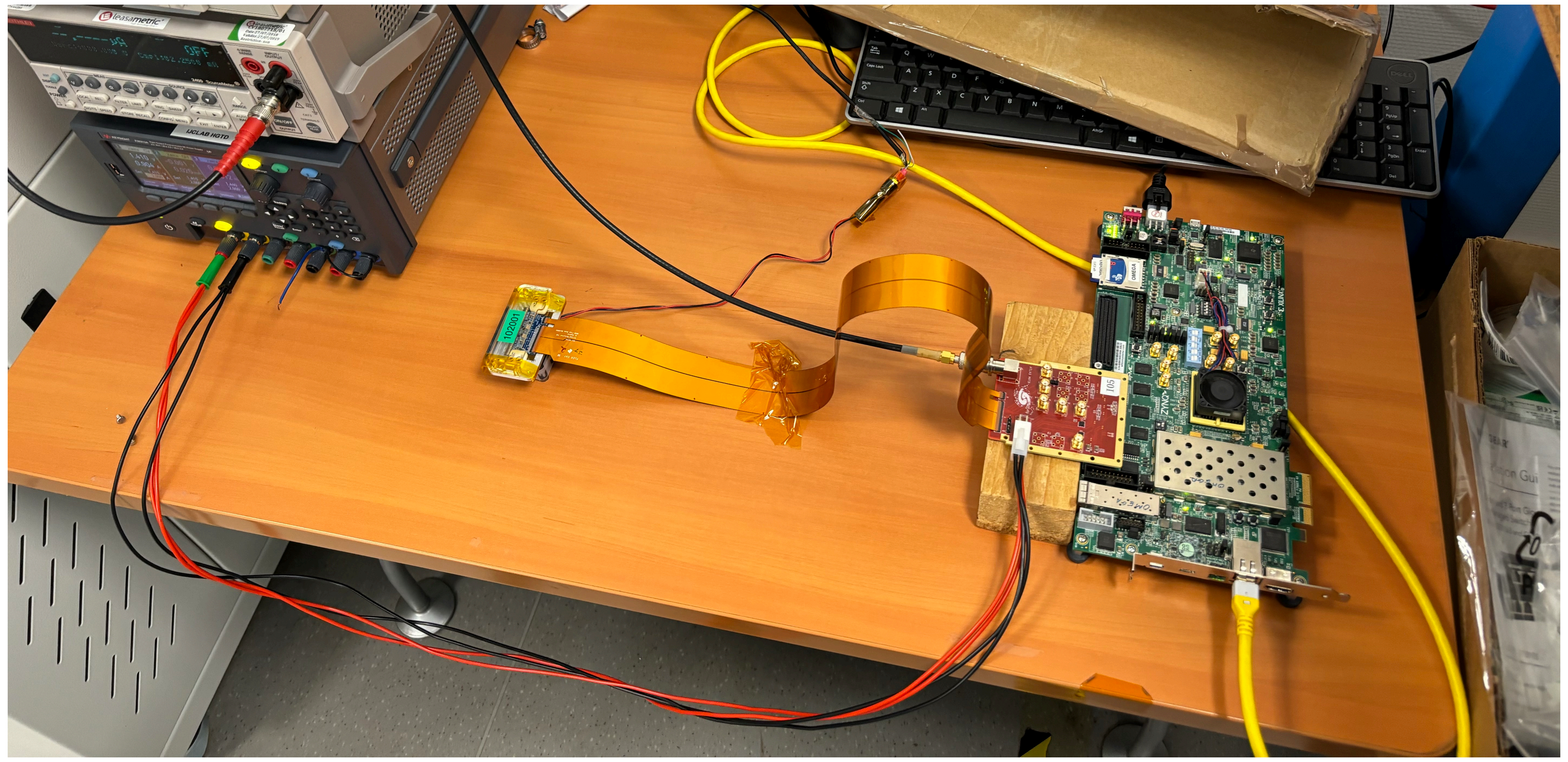
Metrology overview - ALTIROC3 full modules

- 13 ALTIROC3 full modules assembled at IJCLab - 8 thick and 5 thin modules

SN	ASIC version	Sensor thickness	Sensor gap [um]	Hybrid-flex distance	Glue [mg]	Thickness U	Thickness V	Thickness W	Thickness X	Assembly
20WMO321000001	ALTIROC3	Thick(800um)	200	1.701 / 1.722	7	1.798	1.7542	1.76	1.746	Old inlays
20WMO321000002	ALTIROC3	Thick(800um)	154	1.655 / 1.643	14	1.789	1.78	1.7	1.81	By hand
20WMO321000003	ALTIROC3	Thick(800um)	96	1.823 / 1. 828	17	1.766	1.81	1.844	1.78	Current inlays
20WMO321000004	ALTIROC3	Thin (300um)	88	1.81 / 1.825	18	1.257	1.254	1.285	1.28	Current inlays
20WMO321000005	ALTIROC3	Thin (300um)	87	1.75 / 1.749	8	1.22	1.22	1.23	1.24	Current inlays
20WMO321000006	ALTIROC3	Thick(800um)	81	1.765 / 1.769	12	1.763	1.752	1.739	1.74	Current inlays
20WMO321000007	ALTIROC3	Thick(800um)	87	1.778 / 1.756	15	1.73	1.753	1.739	1.731	Current inlays
20WMO321000008	ALTIROC3	Thin (300um)	95	1.772 / 1.77	14	1.26	1.25	1.266	1.268	Current inlays
20WMO321000009	ALTIROC3	Thin (300um)	84	1.78 / 1.77	11	1.277	1.25	1.25	1.276	Current inlays
20WMO3210000010	ALTIROC3	Thin (300um)	89	1.77 / 1.767	10	1 287	1.27	1.28	1.27	Current inlays
20WMO3210000011	ALTIROC3	Thick(800um)	91	1.753 / 1.77	9	1.71	1.693	1.692	1.712	Current inlays
20WMO3210000012	ALTIROC3	Thick(800um)	86	1.8 / 1.85	12	1.706	1.716	1.707	1.7	Current inlays
20WMO3210000013	ALTIROC3	Thick(800um)	87	1.772 / 1.766	11	1.716	1.699	1.691	1.71	Current inlays

Testing setup and procedure

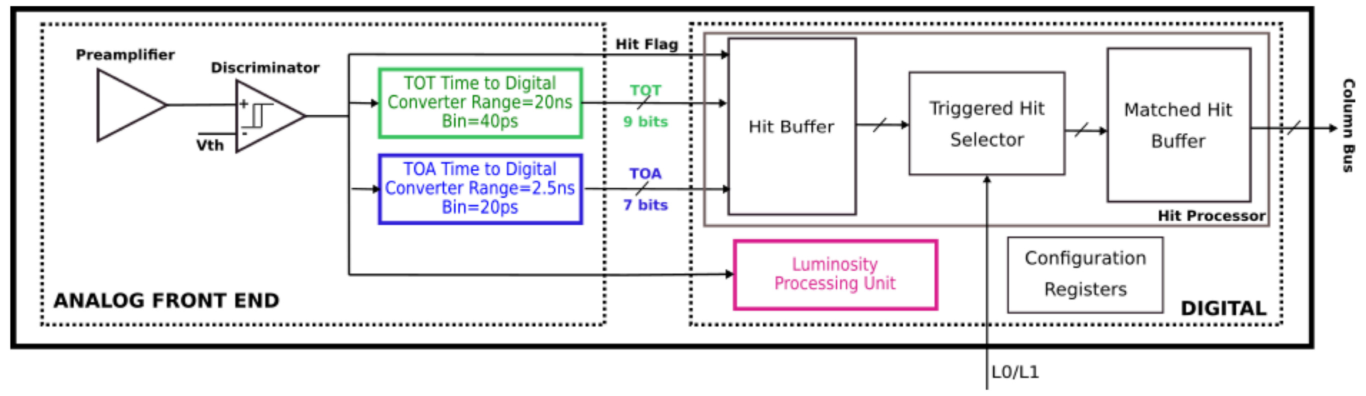




- FPGA- based system
- Module connected with the flex tail to the interface board that connects to FPGA
- While running tests, module placed on top of the fan to regulate its temperature
- Low voltage and HV power supply

- Goals of the tests:
  - Verify module connectivity, functionality, performance (timing, efficiency, noise, bumps connectivity)
- The biggest focus for the module assembly side of the project was to test bump connectivity
  - Studying the difference between thick and thin sensors
  - As to study how do thermal cycles affect bump connectivity

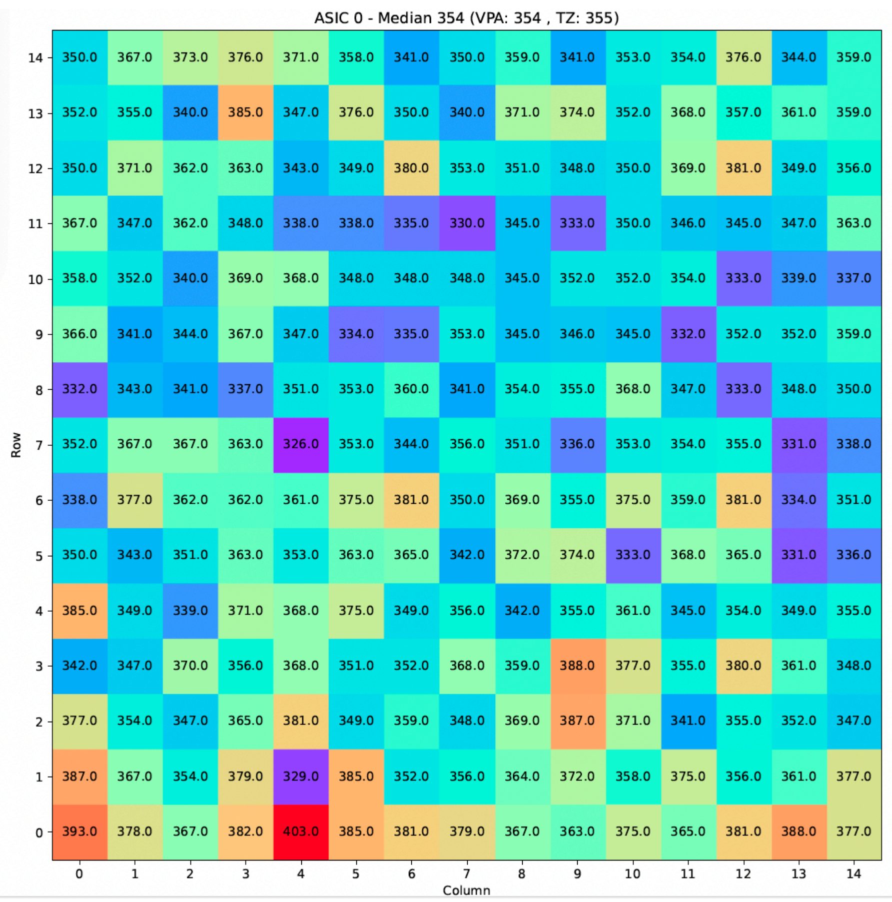
Electrical tests



- Software for the electrical tests of ALTIROC3 modules developed

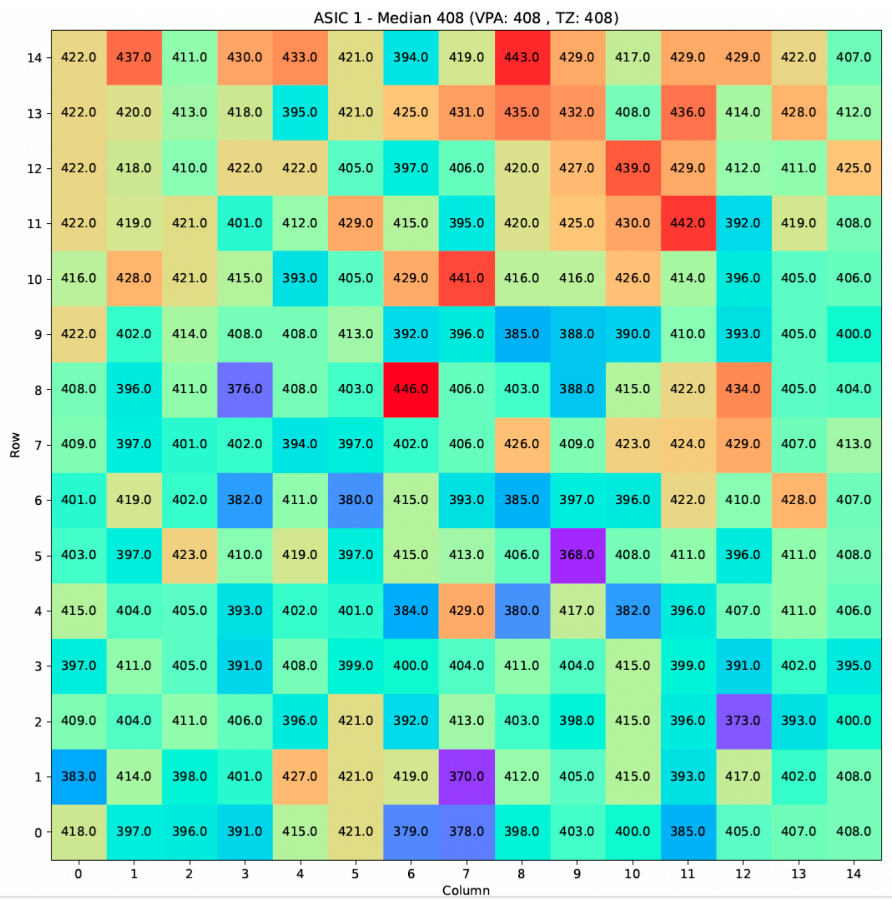
- Tuning of the modules
  - Threshold scans - used to determine the operational threshold where the module starts to register signals above the noise level
    - confirmation of preamplifier working correctly
  - Charge scan - measuring the response of module to different amounts of charge
    - tuning modules to lowest detectable charge

Threshold scan



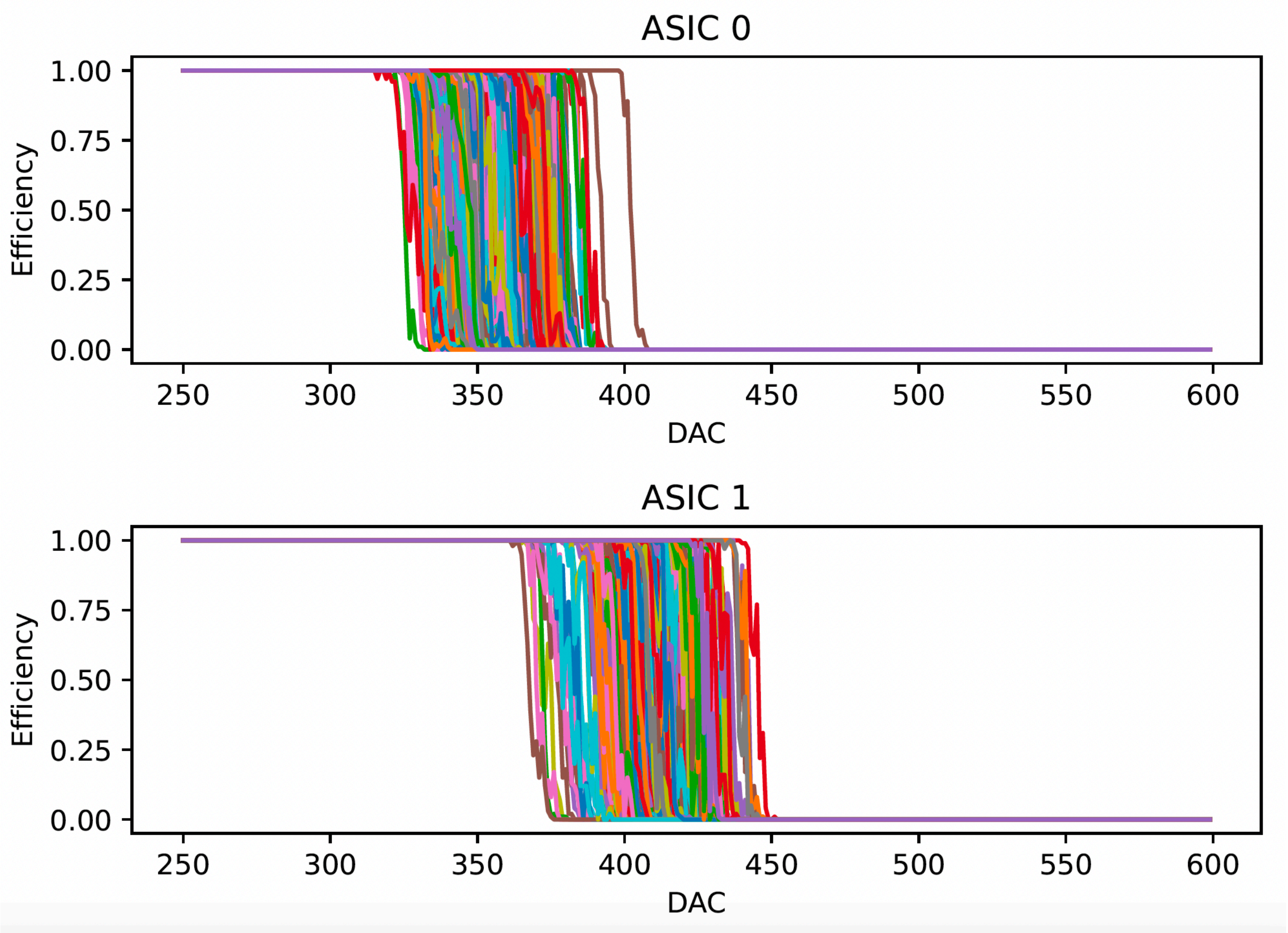
ASIC 0 - Median 354 (VPA: 354 , TZ: 355)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	350.0	367.0	373.0	376.0	371.0	358.0	341.0	350.0	359.0	341.0	353.0	354.0	376.0	344.0	359.0
13	352.0	355.0	340.0	385.0	347.0	376.0	350.0	340.0	371.0	374.0	352.0	368.0	357.0	361.0	359.0
12	350.0	371.0	362.0	363.0	343.0	349.0	380.0	353.0	351.0	348.0	350.0	369.0	381.0	349.0	356.0
11	367.0	347.0	362.0	348.0	338.0	338.0	335.0	330.0	345.0	333.0	350.0	346.0	345.0	347.0	363.0
10	358.0	352.0	340.0	369.0	368.0	348.0	348.0	348.0	345.0	352.0	352.0	354.0	333.0	339.0	337.0
9	366.0	341.0	344.0	367.0	347.0	334.0	335.0	353.0	345.0	346.0	345.0	332.0	352.0	352.0	359.0
8	332.0	343.0	341.0	337.0	351.0	353.0	360.0	341.0	354.0	355.0	368.0	347.0	333.0	348.0	350.0
7	352.0	367.0	367.0	363.0	326.0	353.0	344.0	356.0	351.0	336.0	353.0	354.0	355.0	331.0	338.0
6	338.0	377.0	362.0	362.0	361.0	375.0	381.0	350.0	369.0	355.0	375.0	359.0	381.0	334.0	351.0
5	350.0	343.0	351.0	363.0	353.0	363.0	365.0	342.0	372.0	374.0	333.0	368.0	365.0	331.0	336.0
4	385.0	349.0	339.0	371.0	368.0	375.0	349.0	356.0	342.0	355.0	361.0	345.0	354.0	349.0	355.0
3	342.0	347.0	370.0	356.0	368.0	351.0	352.0	368.0	359.0	388.0	377.0	355.0	380.0	361.0	348.0
2	377.0	354.0	347.0	365.0	381.0	349.0	359.0	348.0	369.0	387.0	371.0	341.0	355.0	352.0	347.0
1	387.0	367.0	354.0	379.0	329.0	385.0	352.0	356.0	364.0	372.0	358.0	375.0	356.0	361.0	377.0
0	393.0	378.0	367.0	382.0	403.0	385.0	381.0	379.0	367.0	363.0	375.0	365.0	381.0	388.0	377.0

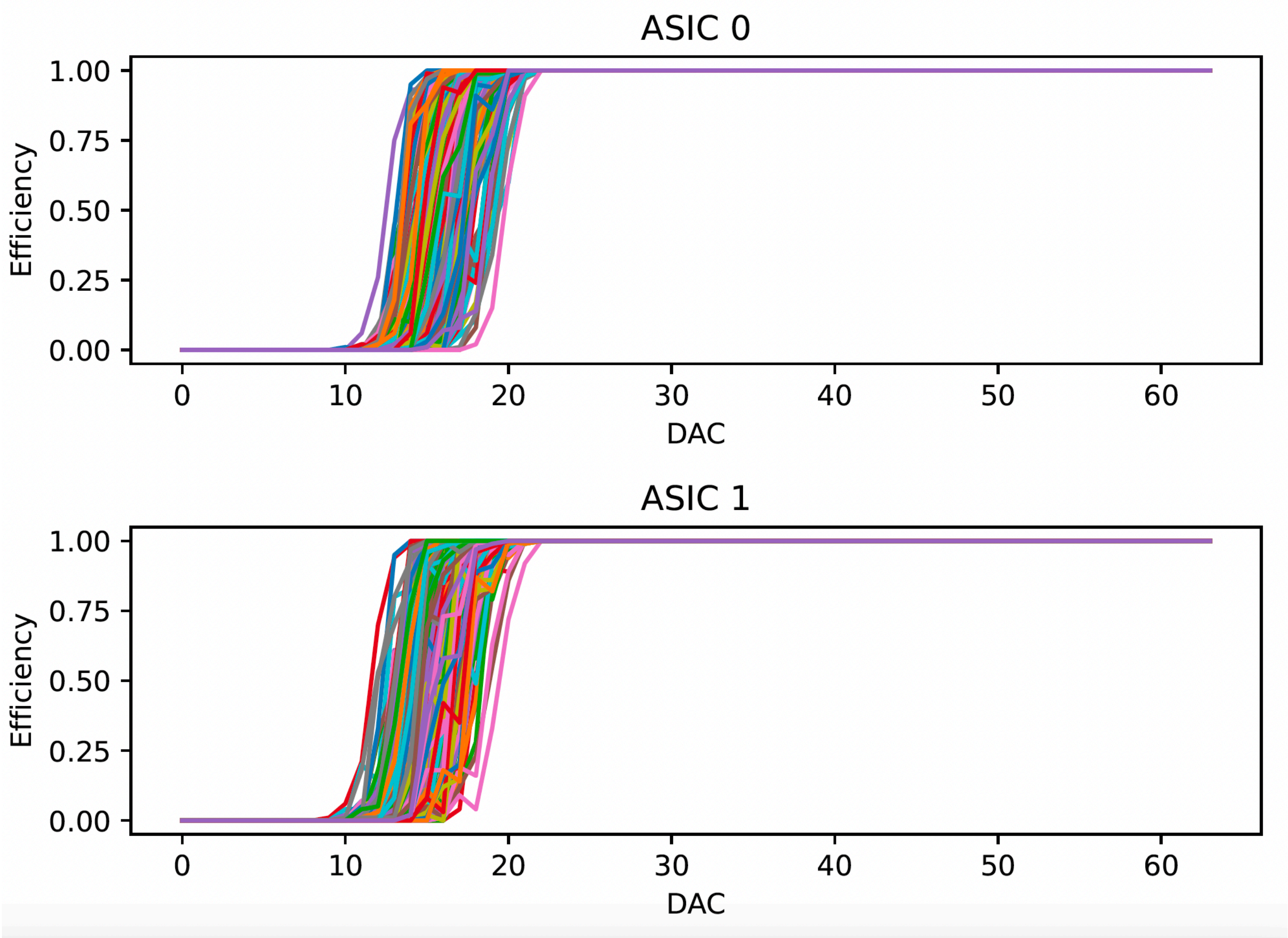


ASIC 1 - Median 408 (VPA: 408 , TZ: 408)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	422.0	437.0	411.0	430.0	433.0	421.0	394.0	419.0	443.0	429.0	417.0	429.0	429.0	422.0	407.0
13	422.0	420.0	413.0	418.0	395.0	421.0	425.0	431.0	435.0	432.0	408.0	436.0	414.0	428.0	412.0
12	422.0	418.0	410.0	422.0	422.0	405.0	397.0	406.0	420.0	427.0	439.0	429.0	412.0	411.0	425.0
11	422.0	419.0	421.0	401.0	412.0	429.0	415.0	395.0	420.0	425.0	430.0	442.0	392.0	419.0	408.0
10	416.0	428.0	421.0	415.0	393.0	405.0	429.0	441.0	416.0	416.0	426.0	414.0	396.0	405.0	406.0
9	422.0	402.0	414.0	408.0	408.0	413.0	392.0	396.0	385.0	388.0	390.0	410.0	393.0	405.0	400.0
8	408.0	396.0	411.0	376.0	408.0	403.0	446.0	406.0	403.0	388.0	415.0	422.0	434.0	405.0	404.0
7	409.0	397.0	401.0	402.0	394.0	397.0	402.0	406.0	426.0	409.0	423.0	424.0	429.0	407.0	413.0
6	401.0	419.0	402.0	382.0	411.0	380.0	415.0	393.0	385.0	397.0	396.0	422.0	410.0	428.0	407.0
5	403.0	397.0	423.0	410.0	419.0	397.0	415.0	413.0	406.0	368.0	408.0	411.0	396.0	411.0	408.0
4	415.0	404.0	405.0	393.0	402.0	401.0	384.0	429.0	380.0	417.0	382.0	396.0	407.0	411.0	406.0
3	397.0	411.0	405.0	391.0	408.0	399.0	400.0	404.0	411.0	404.0	415.0	399.0	391.0	402.0	395.0
2	409.0	404.0	411.0	406.0	396.0	421.0	392.0	413.0	403.0	398.0	415.0	396.0	373.0	393.0	400.0
1	383.0	414.0	398.0	401.0	427.0	421.0	419.0	370.0	412.0	405.0	415.0	393.0	417.0	402.0	408.0
0	418.0	397.0	396.0	391.0	415.0	421.0	379.0	378.0	398.0	403.0	400.0	385.0	405.0	407.0	408.0



Charge scan

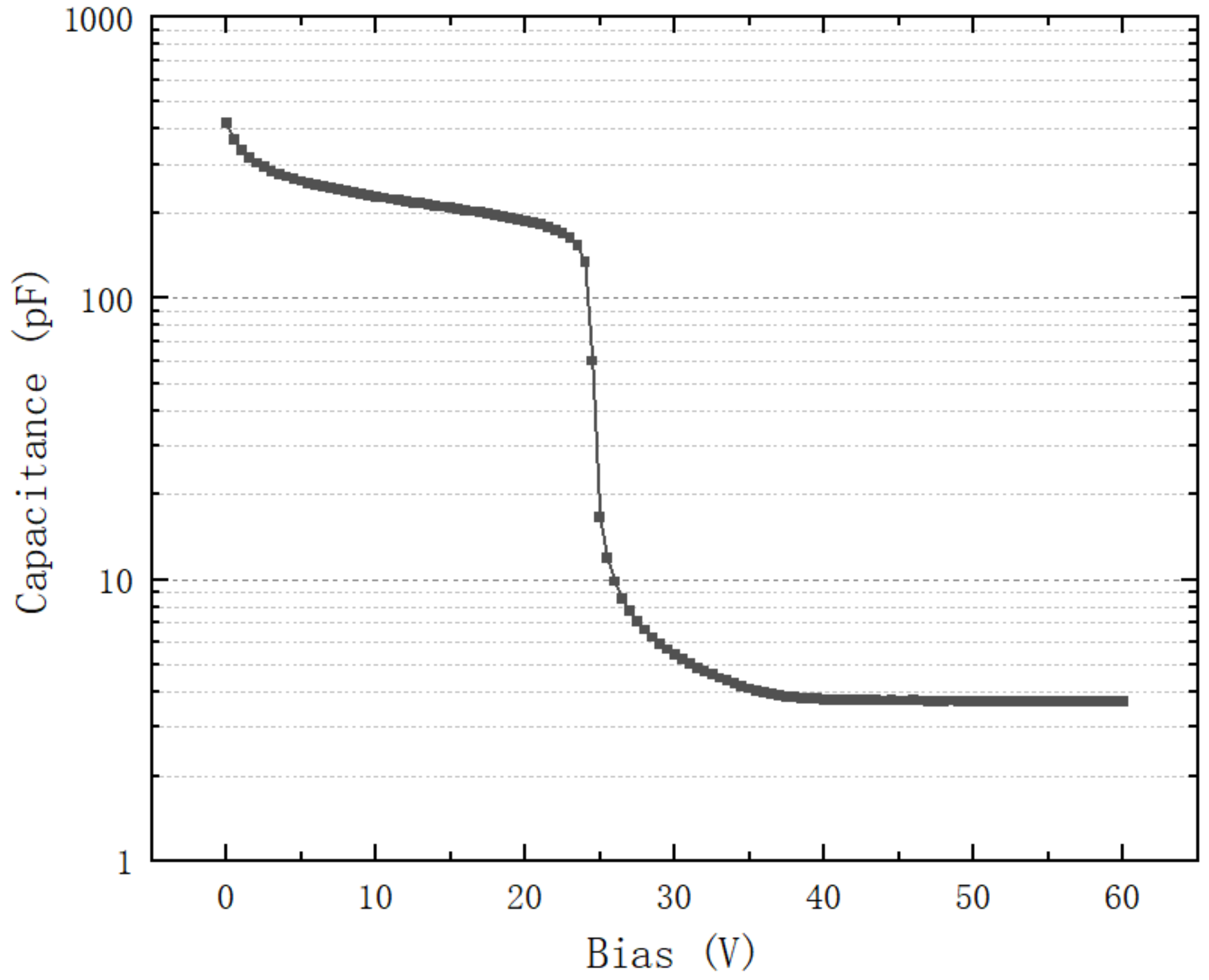


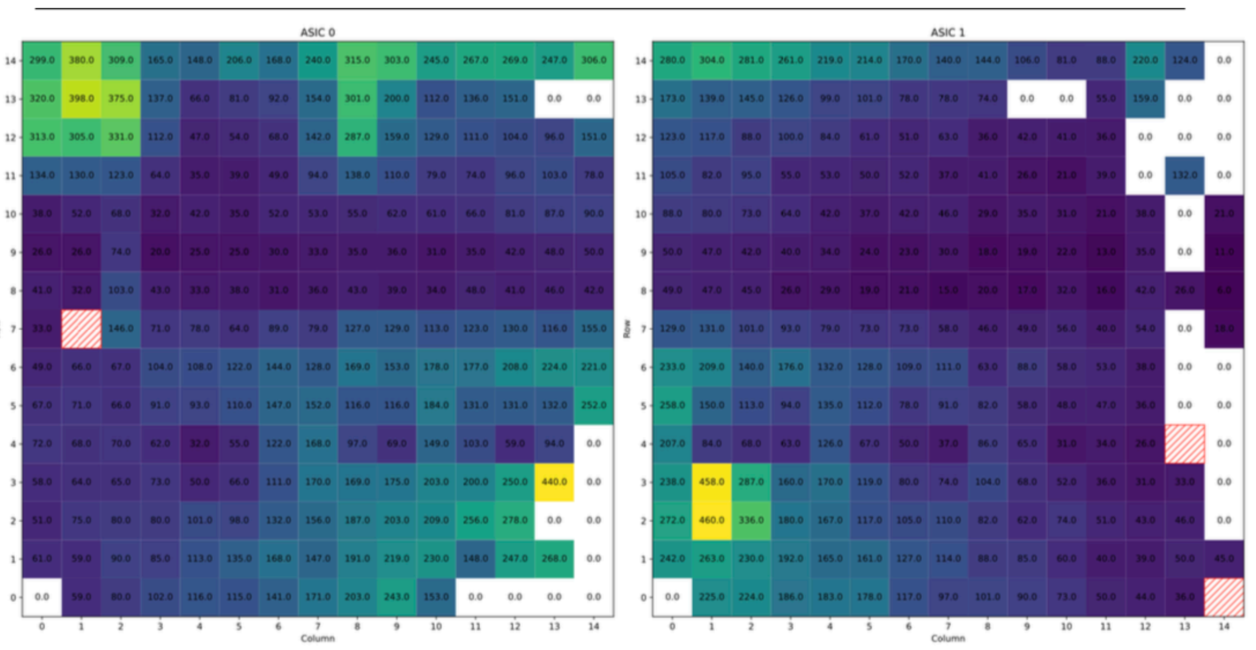
Bump connectivity tests

- The most direct method is doing the source scans
  - At IJCLab we are using Strontium-90 source
- An alternative method (and much faster) is to scan the thresholds for two different charges, and by the differences of these values conclude if the pixel is disconnected or not
  - This can also be done with the same charge but HV On/Off
- Another alternative is to check the tot map

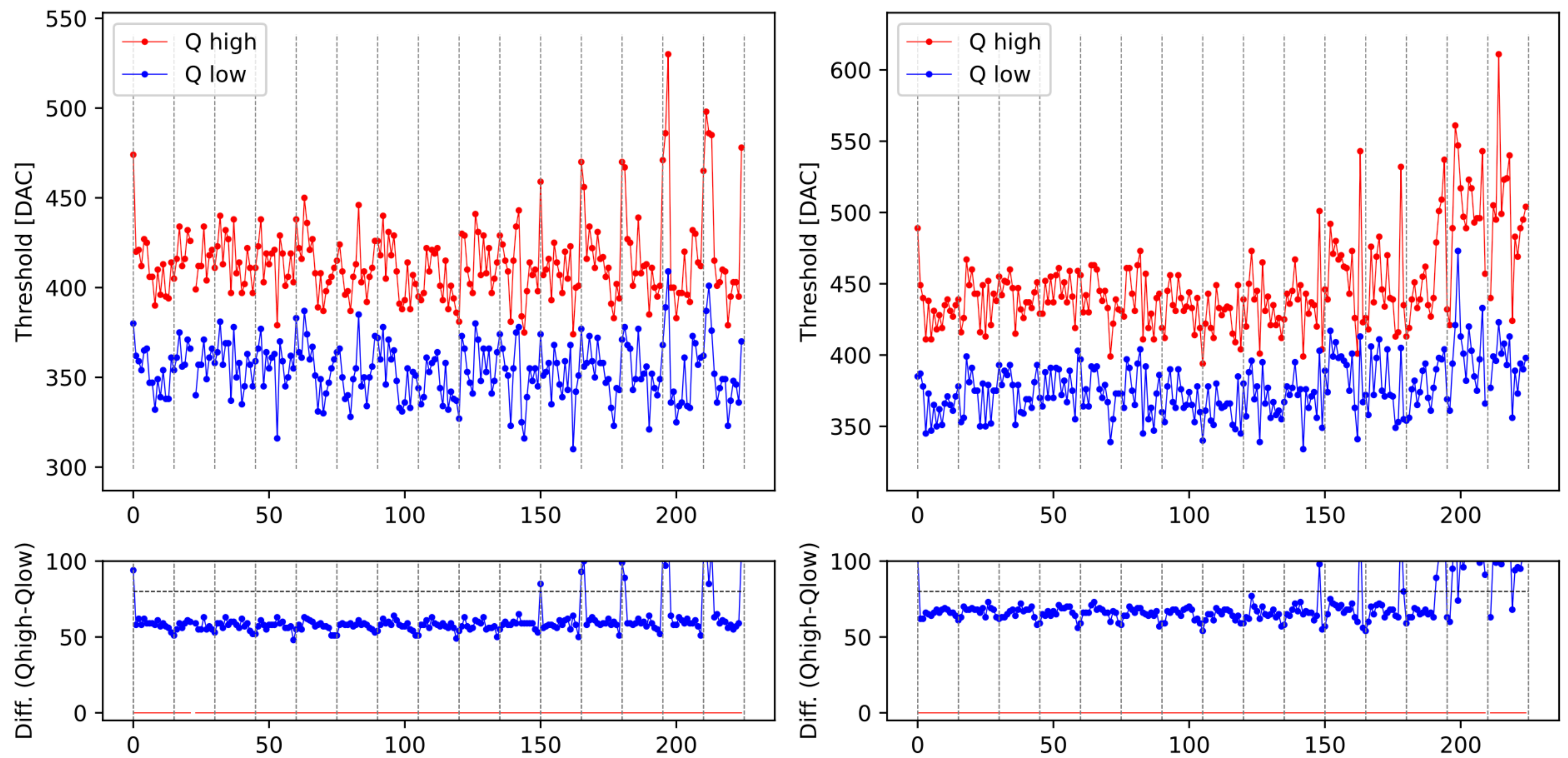
$$V_{out\_pa} = \frac{G_{pa}}{C_d} Q_{in}$$

G_{pa} ~ 15-20
C_d <= 1 pF for disconnected bump
C_d ~ 4pF (fully depleted sensor)
C_d > 100 pF for HV=0





Example of using source scan method

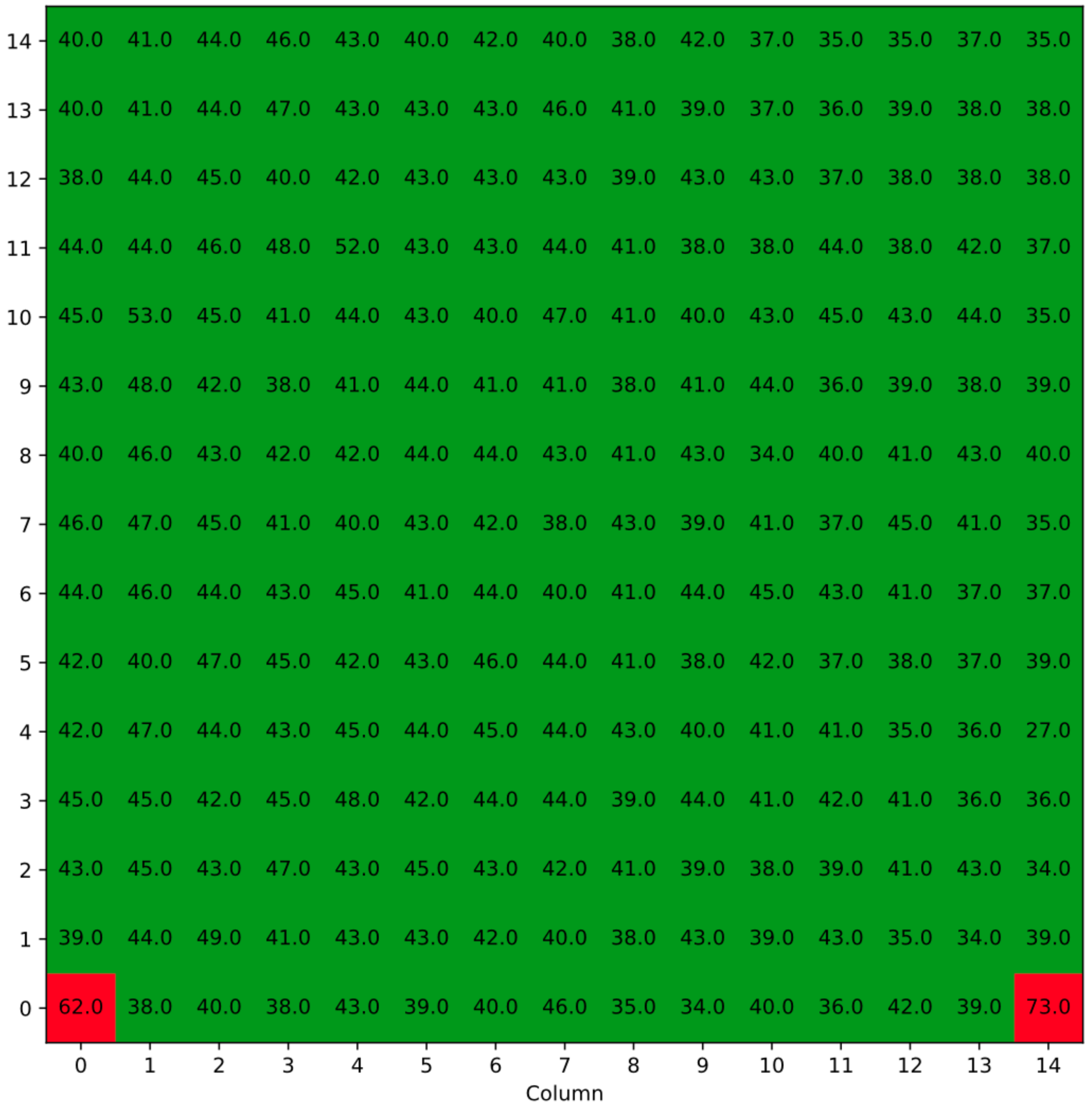


Example of using diff Qinj method

Comparison of the methods

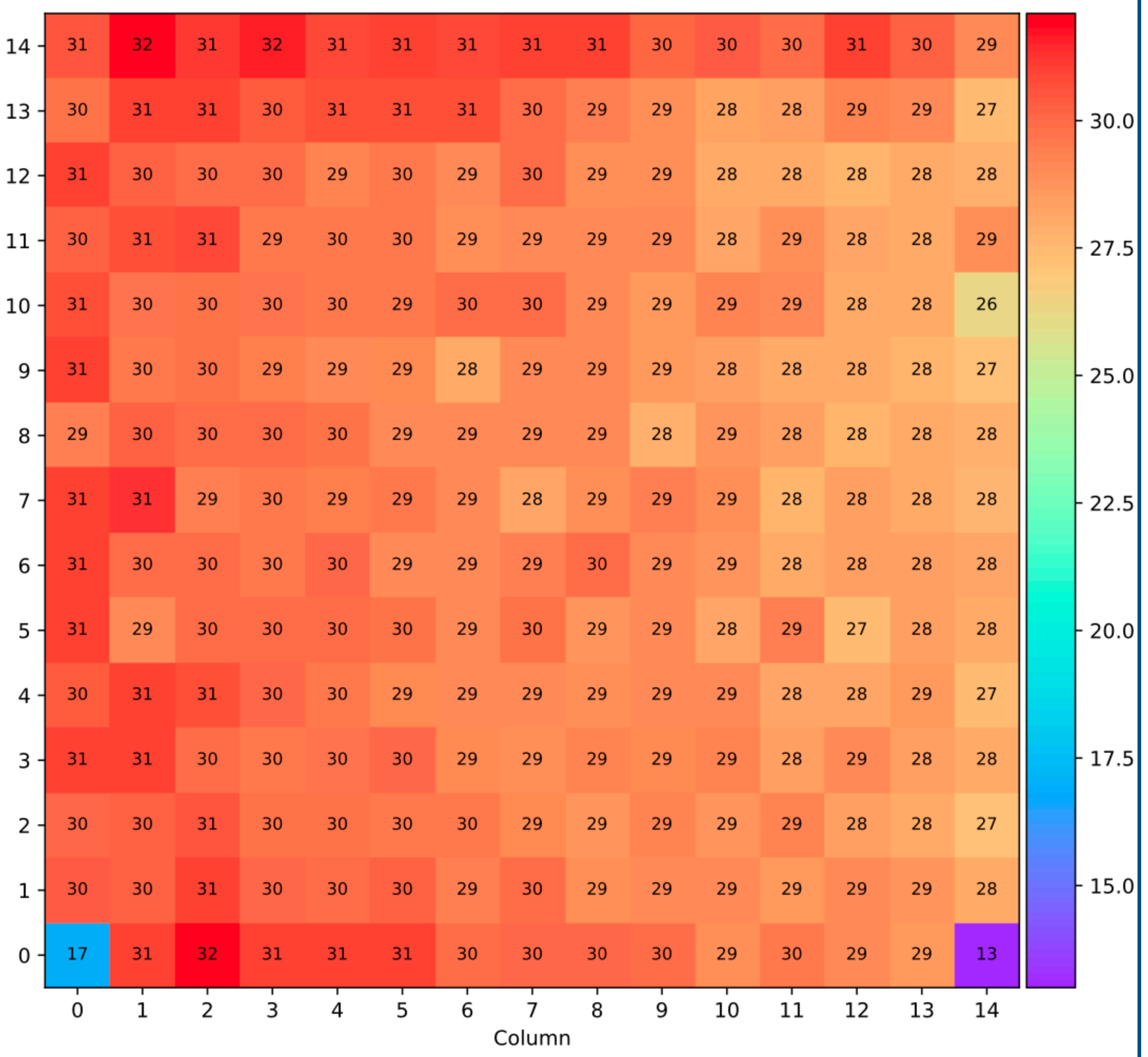
- Comparison of three different methods to check disconnected bumps
- Results consistent across all methods

Diff Qinj



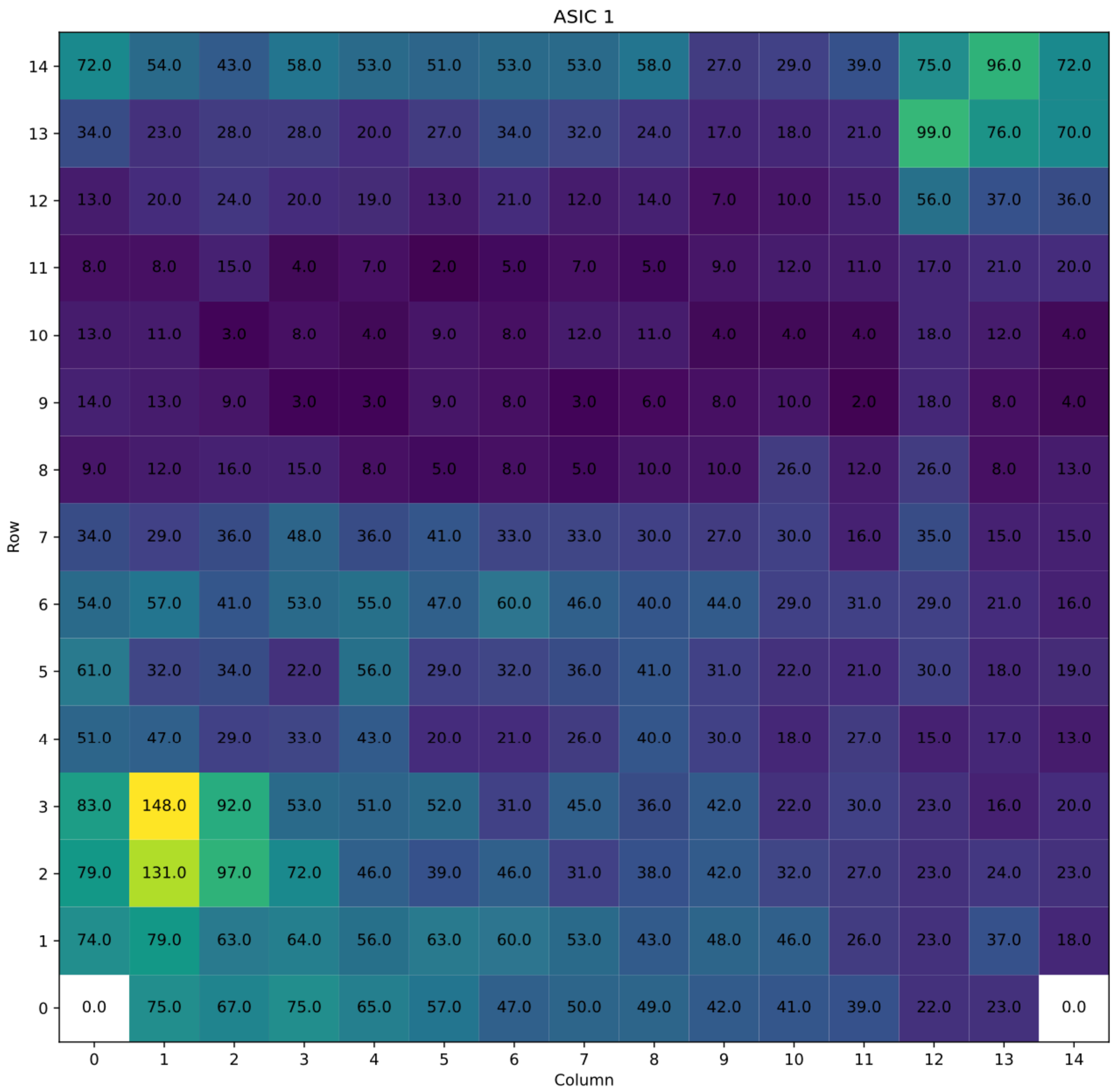
Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	40.0	41.0	44.0	46.0	43.0	40.0	42.0	40.0	38.0	42.0	37.0	35.0	35.0	37.0	35.0
13	40.0	41.0	44.0	47.0	43.0	43.0	43.0	46.0	41.0	39.0	37.0	36.0	39.0	38.0	38.0
12	38.0	44.0	45.0	40.0	42.0	43.0	43.0	43.0	39.0	43.0	43.0	37.0	38.0	38.0	38.0
11	44.0	44.0	46.0	48.0	52.0	43.0	43.0	44.0	41.0	38.0	38.0	44.0	38.0	42.0	37.0
10	45.0	53.0	45.0	41.0	44.0	43.0	40.0	47.0	41.0	40.0	43.0	45.0	43.0	44.0	35.0
9	43.0	48.0	42.0	38.0	41.0	44.0	41.0	41.0	38.0	41.0	44.0	36.0	39.0	38.0	39.0
8	40.0	46.0	43.0	42.0	42.0	44.0	44.0	43.0	41.0	43.0	34.0	40.0	41.0	43.0	40.0
7	46.0	47.0	45.0	41.0	40.0	43.0	42.0	38.0	43.0	39.0	41.0	37.0	45.0	41.0	35.0
6	44.0	46.0	44.0	43.0	45.0	41.0	44.0	40.0	41.0	44.0	45.0	43.0	41.0	37.0	37.0
5	42.0	40.0	47.0	45.0	42.0	43.0	46.0	44.0	41.0	38.0	42.0	37.0	38.0	37.0	39.0
4	42.0	47.0	44.0	43.0	45.0	44.0	45.0	44.0	43.0	40.0	41.0	41.0	35.0	36.0	27.0
3	45.0	45.0	42.0	45.0	48.0	42.0	44.0	44.0	39.0	44.0	41.0	42.0	41.0	36.0	36.0
2	43.0	45.0	43.0	47.0	43.0	45.0	43.0	42.0	41.0	39.0	38.0	39.0	41.0	43.0	34.0
1	39.0	44.0	49.0	41.0	43.0	43.0	42.0	40.0	38.0	43.0	39.0	43.0	35.0	34.0	39.0
0	62.0	38.0	40.0	38.0	43.0	39.0	40.0	46.0	35.0	34.0	40.0	36.0	42.0	39.0	73.0

Tot map



Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	31	32	31	32	31	31	31	31	31	30	30	30	31	30	29
13	30	31	31	30	31	31	31	30	29	29	28	28	29	29	27
12	31	30	30	30	29	30	29	30	29	29	28	28	28	28	28
11	30	31	31	29	30	30	29	29	29	29	28	29	28	28	29
10	31	30	30	30	30	29	30	30	29	29	29	29	28	28	26
9	31	30	30	29	29	29	28	29	29	29	28	28	28	28	27
8	29	30	30	30	30	29	29	29	29	28	29	28	28	28	28
7	31	31	29	30	29	29	29	28	29	29	29	28	28	28	28
6	31	30	30	30	30	29	29	29	30	29	29	28	28	28	28
5	31	29	30	30	30	30	29	30	29	29	28	29	27	28	28
4	30	31	31	30	30	29	29	29	29	29	29	28	28	29	27
3	31	31	30	30	30	30	29	29	29	29	29	28	29	28	28
2	30	30	31	30	30	30	30	29	29	29	29	29	28	28	27
1	30	30	31	30	30	30	29	30	29	29	29	29	29	29	28
0	17	31	32	31	31	31	30	30	30	30	29	30	29	29	13

Source scan

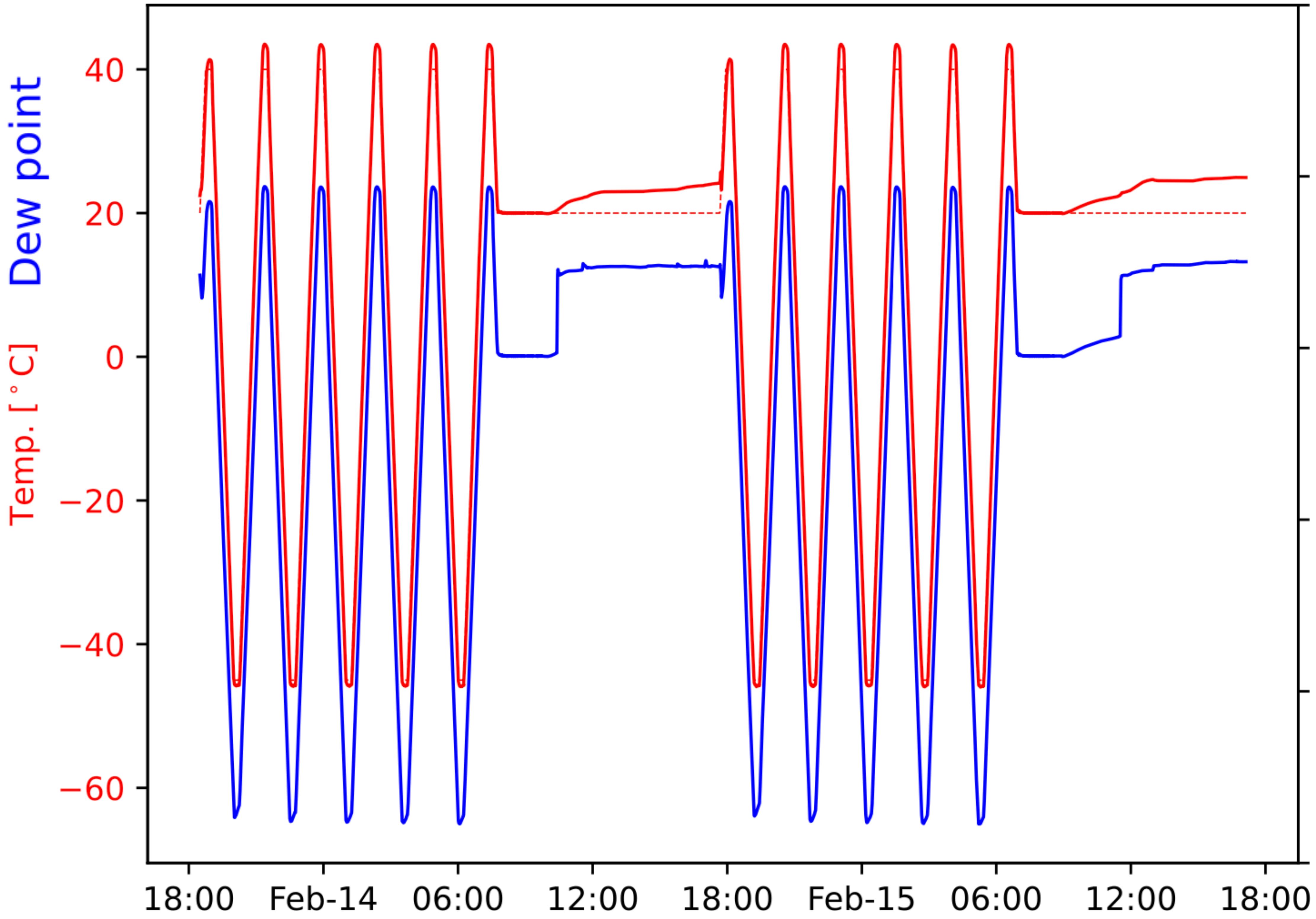


ASIC 1

Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	72.0	54.0	43.0	58.0	53.0	51.0	53.0	53.0	58.0	27.0	29.0	39.0	75.0	96.0	72.0
13	34.0	23.0	28.0	28.0	20.0	27.0	34.0	32.0	24.0	17.0	18.0	21.0	99.0	76.0	70.0
12	13.0	20.0	24.0	20.0	19.0	13.0	21.0	12.0	14.0	7.0	10.0	15.0	56.0	37.0	36.0
11	8.0	8.0	15.0	4.0	7.0	2.0	5.0	7.0	5.0	9.0	12.0	11.0	17.0	21.0	20.0
10	13.0	11.0	3.0	8.0	4.0	9.0	8.0	12.0	11.0	4.0	4.0	4.0	18.0	12.0	4.0
9	14.0	13.0	9.0	3.0	3.0	9.0	8.0	3.0	6.0	8.0	10.0	2.0	18.0	8.0	4.0
8	9.0	12.0	16.0	15.0	8.0	5.0	8.0	5.0	10.0	10.0	26.0	12.0	26.0	8.0	13.0
7	34.0	29.0	36.0	48.0	36.0	41.0	33.0	33.0	30.0	27.0	30.0	16.0	35.0	15.0	15.0
6	54.0	57.0	41.0	53.0	55.0	47.0	60.0	46.0	40.0	44.0	29.0	31.0	29.0	21.0	16.0
5	61.0	32.0	34.0	22.0	56.0	29.0	32.0	36.0	41.0	31.0	22.0	21.0	30.0	18.0	19.0
4	51.0	47.0	29.0	33.0	43.0	20.0	21.0	26.0	40.0	30.0	18.0	27.0	15.0	17.0	13.0
3	83.0	148.0	92.0	53.0	51.0	52.0	31.0	45.0	36.0	42.0	22.0	30.0	23.0	16.0	20.0
2	79.0	131.0	97.0	72.0	46.0	39.0	46.0	31.0	38.0	42.0	32.0	27.0	23.0	24.0	23.0
1	74.0	79.0	63.0	64.0	56.0	63.0	60.0	53.0	43.0	48.0	46.0	26.0	23.0	37.0	18.0
0	0.0	75.0	67.0	75.0	65.0	57.0	47.0	50.0	49.0	42.0	41.0	39.0	22.0	23.0	0.0

Thermal cycles

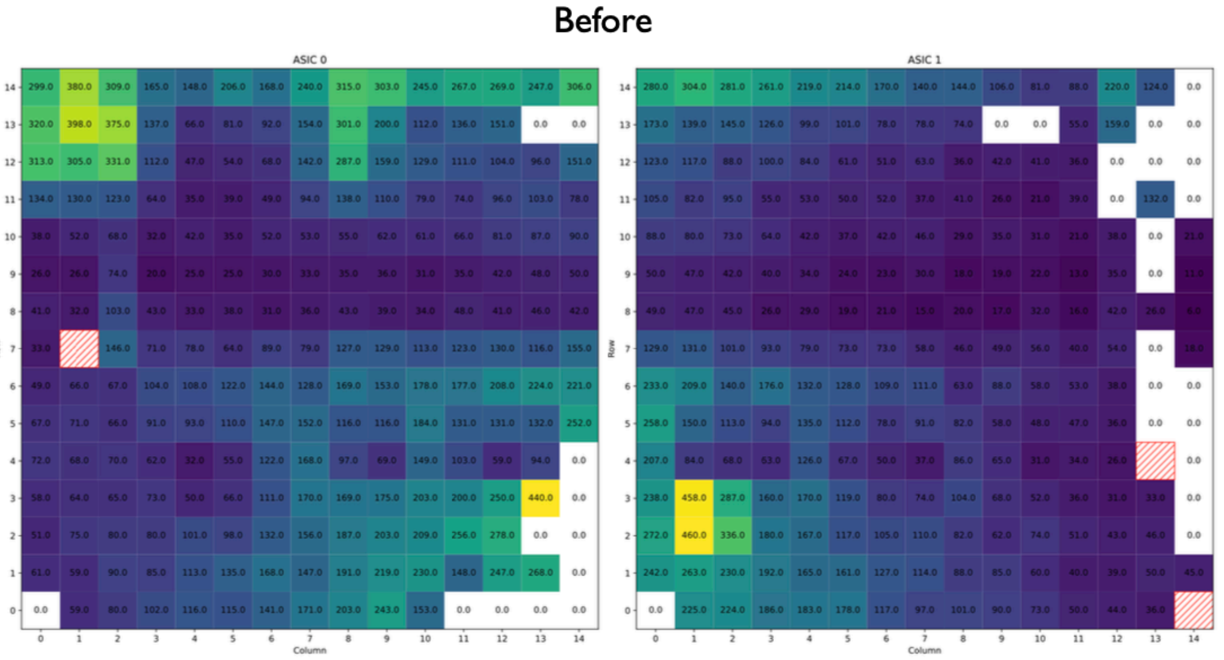
- Because of the differences in the coefficients of thermal expansion between the different materials, modules are tested in extreme operational conditions between -45 °C and 40 °C
- One cycle = 2h30min
- 1h cooling + 15min rest + 1h heating + 15 min rest

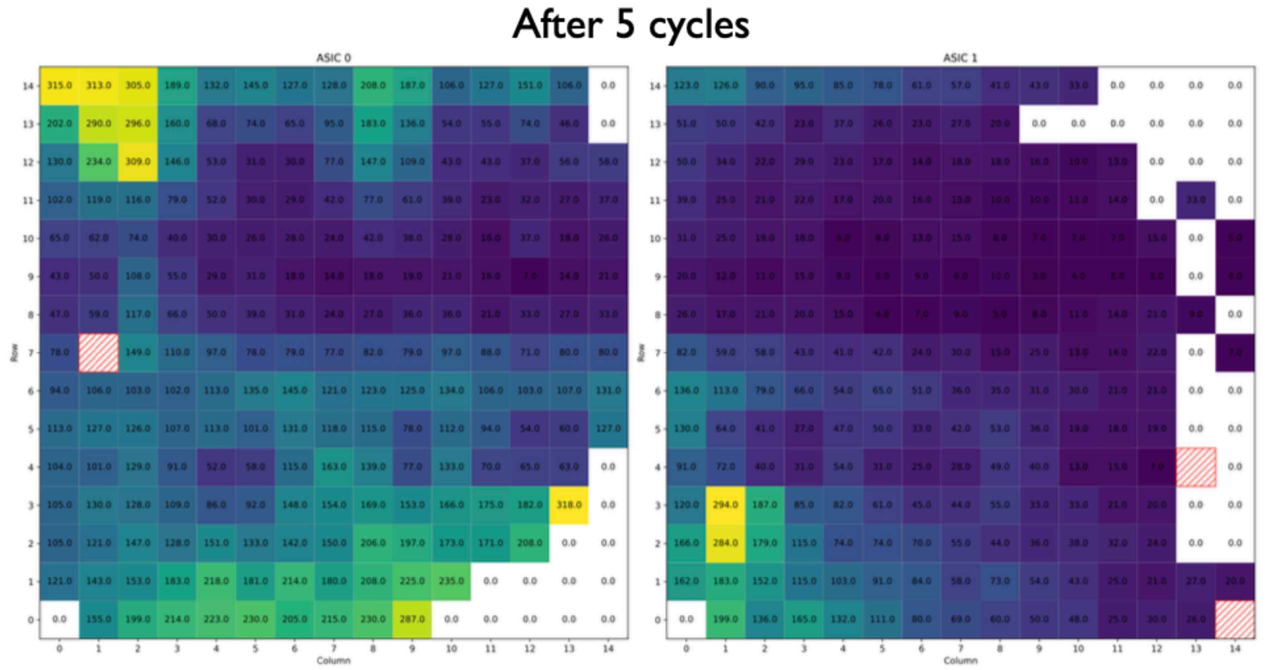


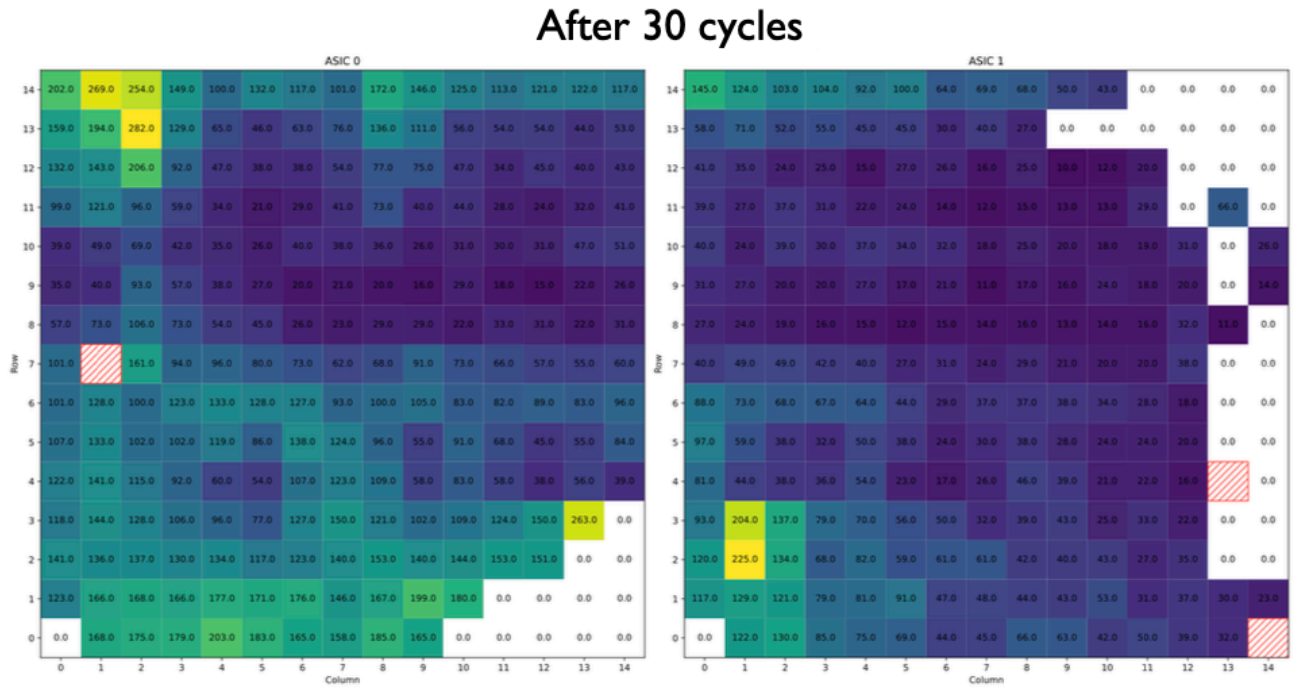
Testing thin hybrids

Initial tests

- Initial design baseline is to use thinned sensors(~300um)
- Modules with initial disconnections are weak under TC
- In most cases, disconnected bumps are on the corners and edges of the modules

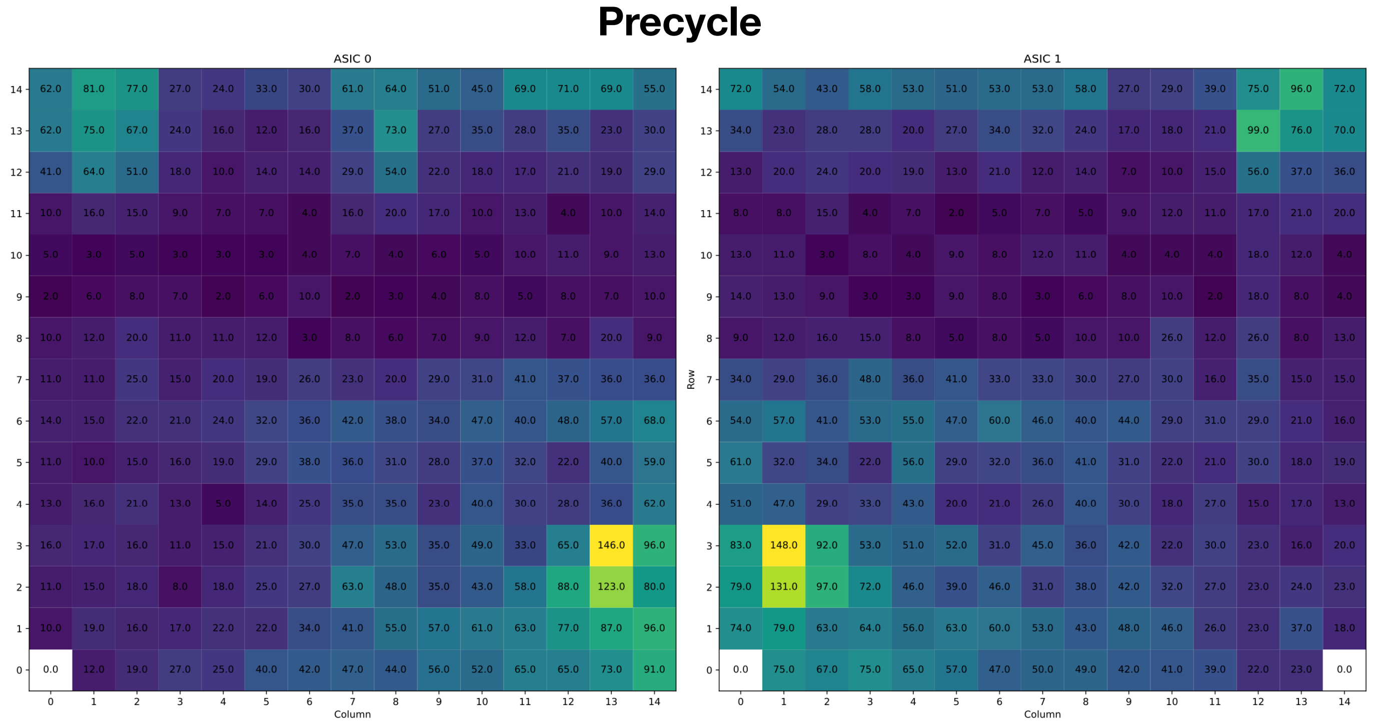


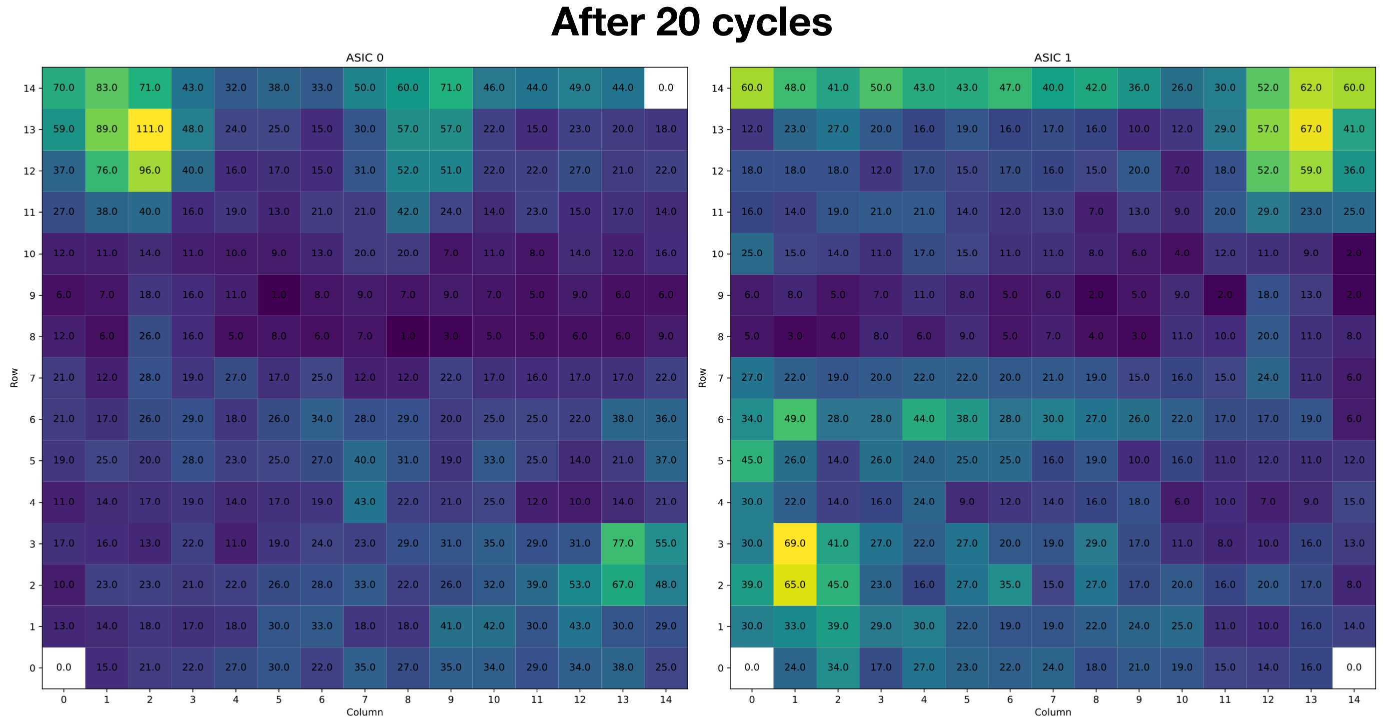


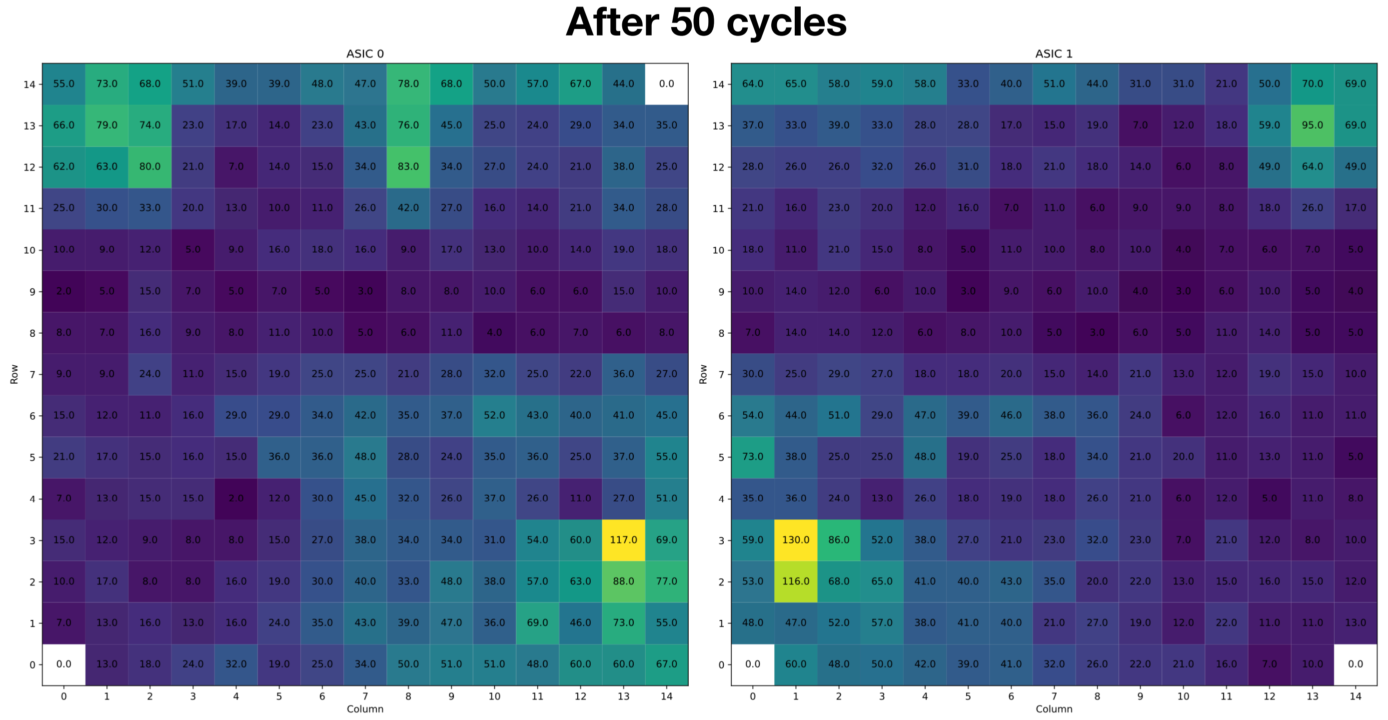


Improved hybridisation

- After improved hybridisation results much better, but still breaking after thermal cycles
- Results are much better, but some still broke after a small number of thermal cycles







Testing thick hybrids

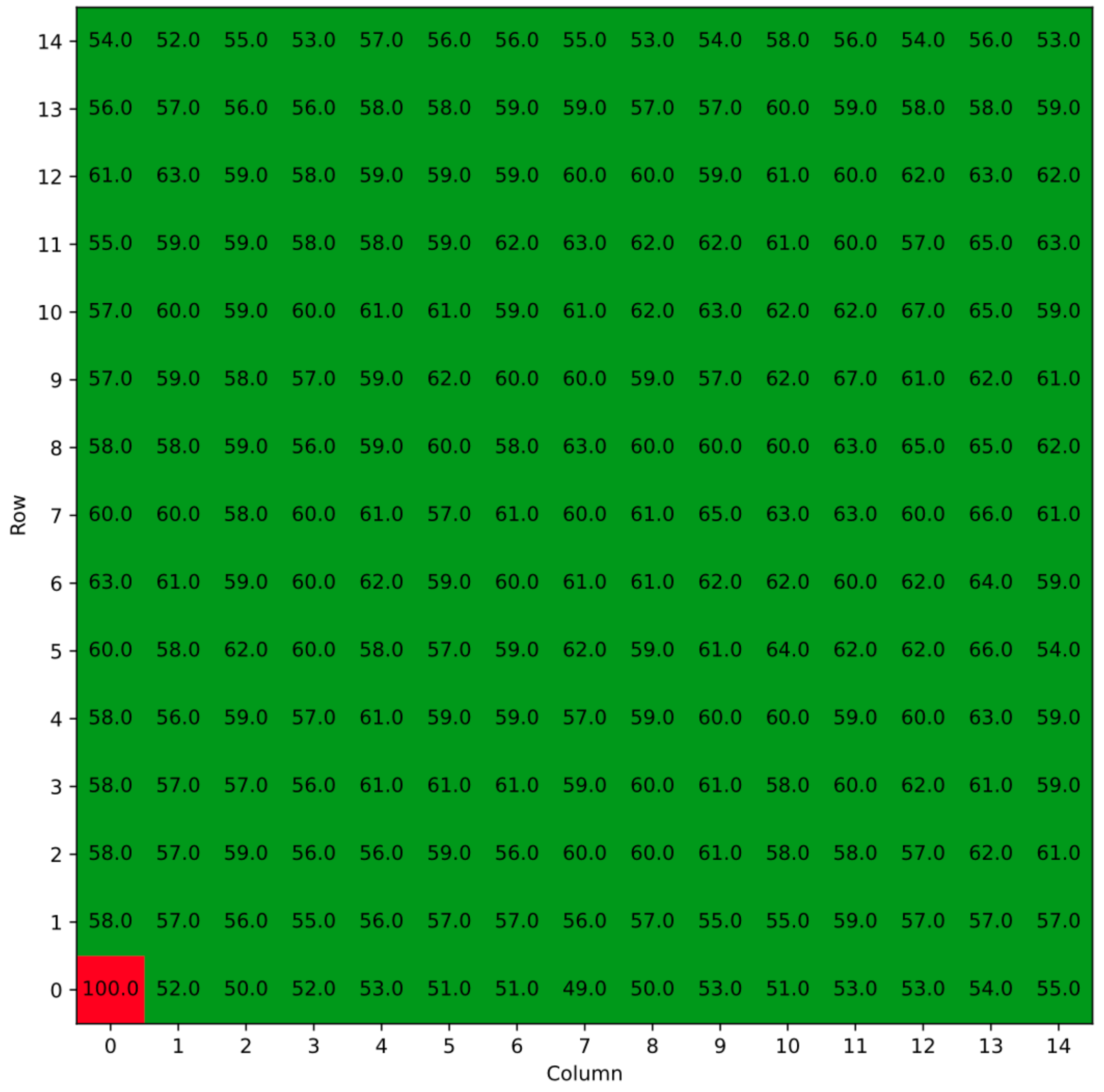
- Decision to move towards thick hybrids (sensors ~800um)

- 8 thick ALTIROC3 full modules assembled at IJCLab
  - 4 of last 5 modules (improved hybridisation) survived 120 thermal cycles with zero disconnected bumps
  - One had 2 disconnected pixel after 120 TCs and one had 1 disconnected pixel after 175 TCs

- More robust under TCs compared to thin modules

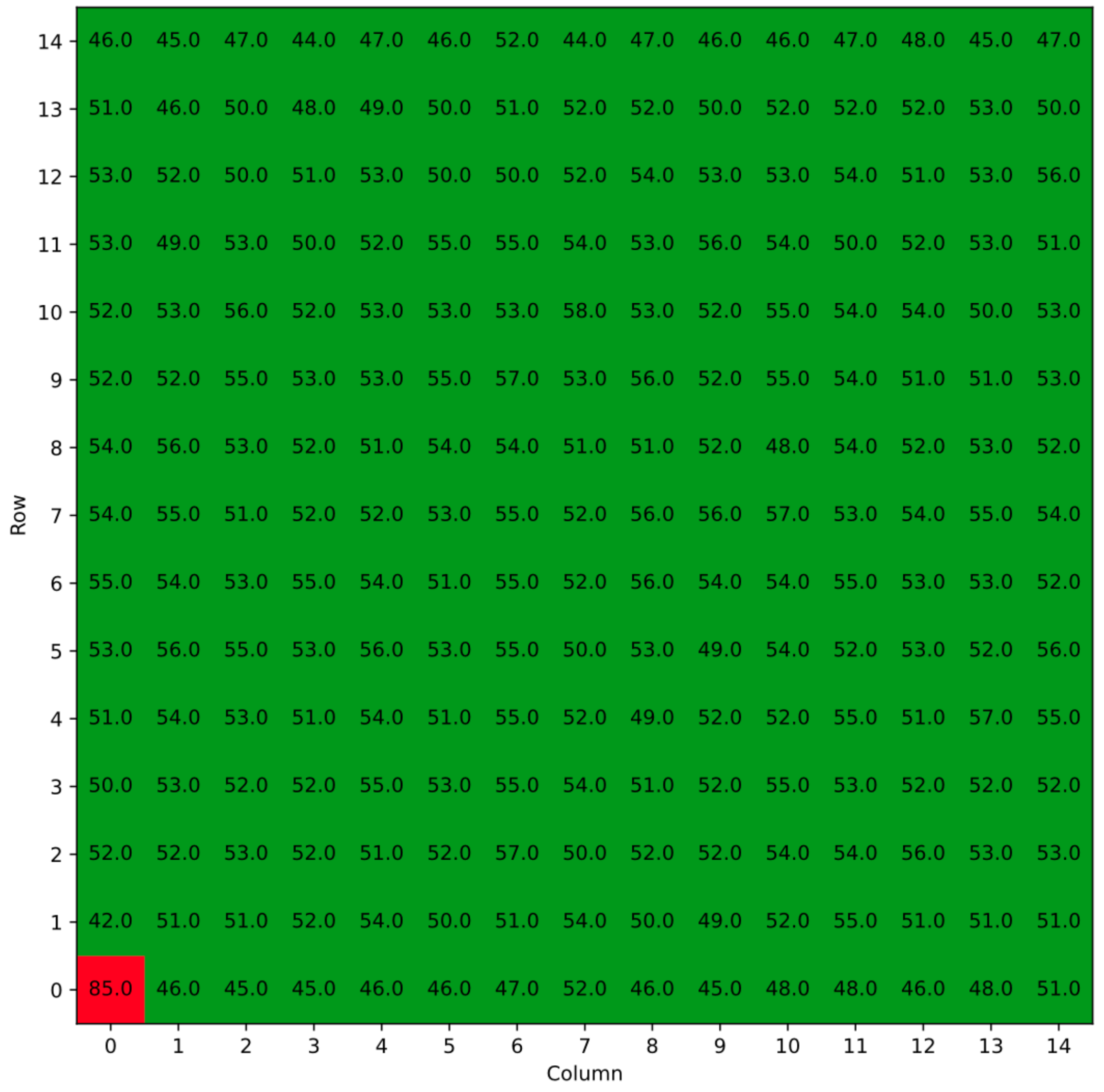
- Because of extra space in the detector, we are able to make this transition

Precycle



Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	54.0	52.0	55.0	53.0	57.0	56.0	56.0	55.0	53.0	54.0	58.0	56.0	54.0	56.0	53.0
13	56.0	57.0	56.0	56.0	58.0	58.0	59.0	59.0	57.0	57.0	60.0	59.0	58.0	58.0	59.0
12	61.0	63.0	59.0	58.0	59.0	59.0	59.0	60.0	60.0	59.0	61.0	60.0	62.0	63.0	62.0
11	55.0	59.0	59.0	58.0	58.0	59.0	62.0	63.0	62.0	62.0	61.0	60.0	57.0	65.0	63.0
10	57.0	60.0	59.0	60.0	61.0	61.0	59.0	61.0	62.0	63.0	62.0	62.0	67.0	65.0	59.0
9	57.0	59.0	58.0	57.0	59.0	62.0	60.0	60.0	59.0	57.0	62.0	67.0	61.0	62.0	61.0
8	58.0	58.0	59.0	56.0	59.0	60.0	58.0	63.0	60.0	60.0	60.0	63.0	65.0	65.0	62.0
7	60.0	60.0	58.0	60.0	61.0	57.0	61.0	60.0	61.0	65.0	63.0	63.0	60.0	66.0	61.0
6	63.0	61.0	59.0	60.0	62.0	59.0	60.0	61.0	61.0	62.0	62.0	60.0	62.0	64.0	59.0
5	60.0	58.0	62.0	60.0	58.0	57.0	59.0	62.0	59.0	61.0	64.0	62.0	62.0	66.0	54.0
4	58.0	56.0	59.0	57.0	61.0	59.0	59.0	57.0	59.0	60.0	60.0	59.0	60.0	63.0	59.0
3	58.0	57.0	57.0	56.0	61.0	61.0	61.0	59.0	60.0	61.0	58.0	60.0	62.0	61.0	59.0
2	58.0	57.0	59.0	56.0	56.0	59.0	56.0	60.0	60.0	61.0	58.0	58.0	57.0	62.0	61.0
1	58.0	57.0	56.0	55.0	56.0	57.0	57.0	56.0	57.0	55.0	55.0	59.0	57.0	57.0	57.0
0	100.0	52.0	50.0	52.0	53.0	51.0	51.0	49.0	50.0	53.0	51.0	53.0	53.0	54.0	55.0

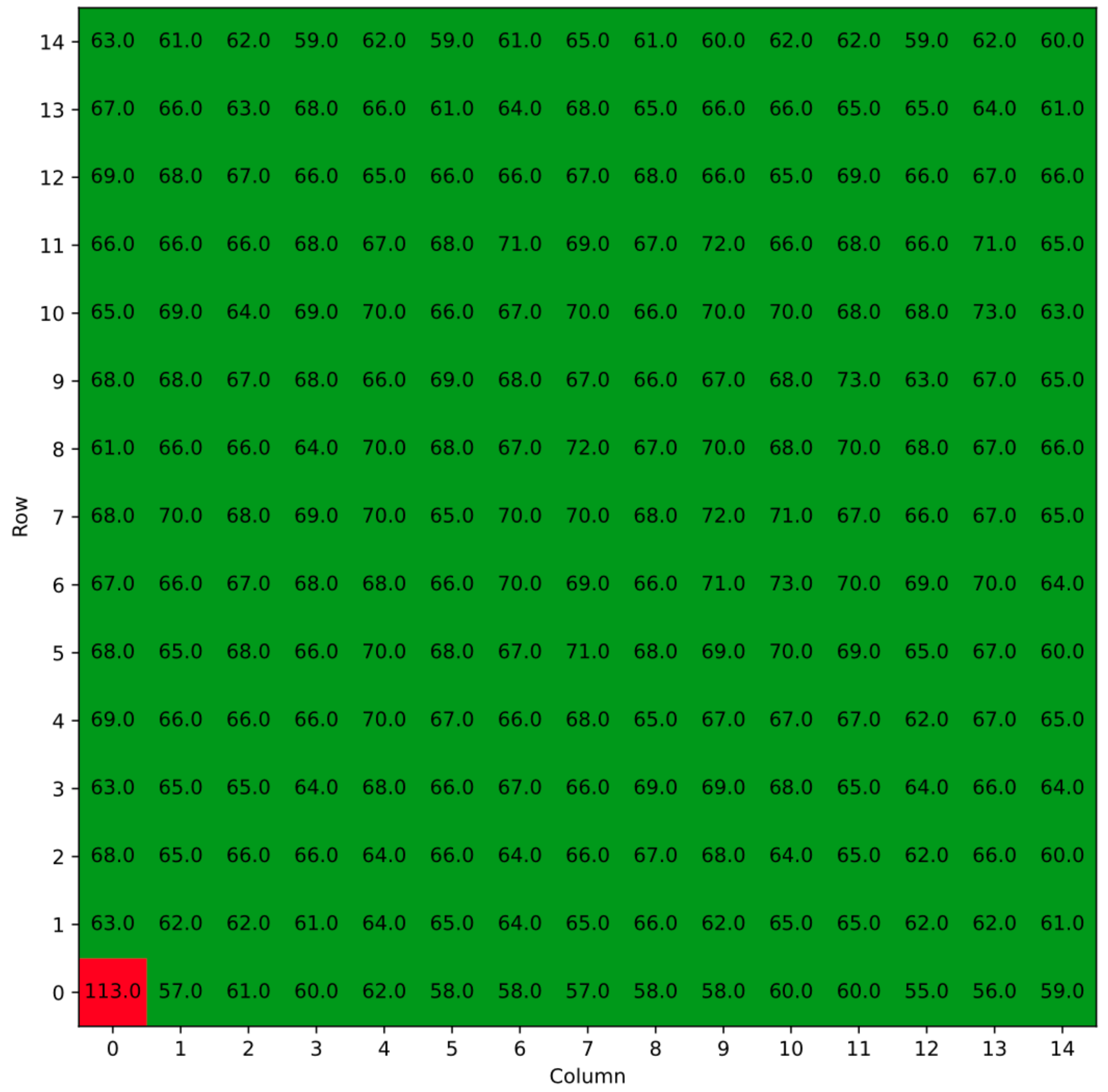
Column



Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	46.0	45.0	47.0	44.0	47.0	46.0	52.0	44.0	47.0	46.0	46.0	47.0	48.0	45.0	47.0
13	51.0	46.0	50.0	48.0	49.0	50.0	51.0	52.0	52.0	50.0	52.0	52.0	52.0	53.0	50.0
12	53.0	52.0	50.0	51.0	53.0	50.0	50.0	52.0	54.0	53.0	53.0	54.0	51.0	53.0	56.0
11	53.0	49.0	53.0	50.0	52.0	55.0	55.0	54.0	53.0	56.0	54.0	50.0	52.0	53.0	51.0
10	52.0	53.0	56.0	52.0	53.0	53.0	53.0	58.0	53.0	52.0	55.0	54.0	54.0	50.0	53.0
9	52.0	52.0	55.0	53.0	53.0	55.0	57.0	53.0	56.0	52.0	55.0	54.0	51.0	51.0	53.0
8	54.0	56.0	53.0	52.0	51.0	54.0	54.0	51.0	51.0	52.0	48.0	54.0	52.0	53.0	52.0
7	54.0	55.0	51.0	52.0	52.0	53.0	55.0	52.0	56.0	56.0	57.0	53.0	54.0	55.0	54.0
6	55.0	54.0	53.0	55.0	54.0	51.0	55.0	52.0	56.0	54.0	54.0	55.0	53.0	53.0	52.0
5	53.0	56.0	55.0	53.0	56.0	53.0	55.0	50.0	53.0	49.0	54.0	52.0	53.0	52.0	56.0
4	51.0	54.0	53.0	51.0	54.0	51.0	55.0	52.0	49.0	52.0	52.0	55.0	51.0	57.0	55.0
3	50.0	53.0	52.0	52.0	55.0	53.0	55.0	54.0	51.0	52.0	55.0	53.0	52.0	52.0	52.0
2	52.0	52.0	53.0	52.0	51.0	52.0	57.0	50.0	52.0	52.0	54.0	54.0	56.0	53.0	53.0
1	42.0	51.0	51.0	52.0	54.0	50.0	51.0	54.0	50.0	49.0	52.0	55.0	51.0	51.0	51.0
0	85.0	46.0	45.0	45.0	46.0	46.0	47.0	52.0	46.0	45.0	48.0	48.0	46.0	48.0	51.0

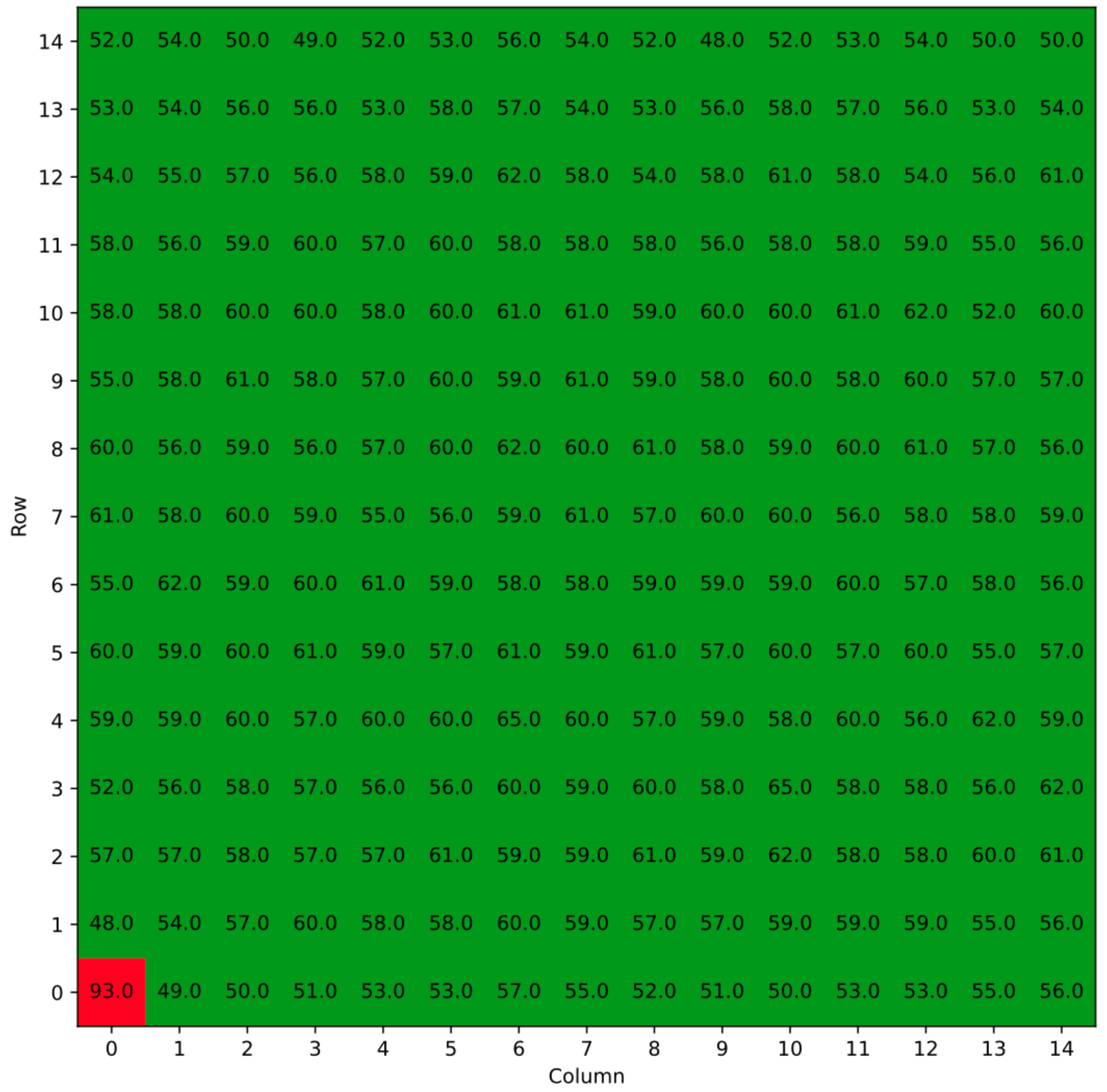
Column

After 120 cycles



Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	63.0	61.0	62.0	59.0	62.0	59.0	61.0	65.0	61.0	60.0	62.0	62.0	59.0	62.0	60.0
13	67.0	66.0	63.0	68.0	66.0	61.0	64.0	68.0	65.0	66.0	66.0	65.0	65.0	64.0	61.0
12	69.0	68.0	67.0	66.0	65.0	66.0	66.0	67.0	68.0	66.0	65.0	69.0	66.0	67.0	66.0
11	66.0	66.0	66.0	68.0	67.0	68.0	71.0	69.0	67.0	72.0	66.0	68.0	66.0	71.0	65.0
10	65.0	69.0	64.0	69.0	70.0	66.0	67.0	70.0	66.0	70.0	70.0	68.0	68.0	73.0	63.0
9	68.0	68.0	67.0	68.0	66.0	69.0	68.0	67.0	66.0	67.0	68.0	73.0	63.0	67.0	65.0
8	61.0	66.0	66.0	64.0	70.0	68.0	67.0	72.0	67.0	70.0	68.0	70.0	68.0	67.0	66.0
7	68.0	70.0	68.0	69.0	70.0	65.0	70.0	70.0	68.0	72.0	71.0	67.0	66.0	67.0	65.0
6	67.0	66.0	67.0	68.0	68.0	66.0	70.0	69.0	66.0	71.0	73.0	70.0	69.0	70.0	64.0
5	68.0	65.0	68.0	66.0	70.0	68.0	67.0	71.0	68.0	69.0	70.0	69.0	65.0	67.0	60.0
4	69.0	66.0	66.0	66.0	70.0	67.0	66.0	68.0	65.0	67.0	67.0	67.0	62.0	67.0	65.0
3	63.0	65.0	65.0	64.0	68.0	66.0	67.0	66.0	69.0	69.0	68.0	65.0	64.0	66.0	64.0
2	68.0	65.0	66.0	66.0	64.0	66.0	64.0	66.0	67.0	68.0	64.0	65.0	62.0	66.0	60.0
1	63.0	62.0	62.0	61.0	64.0	65.0	64.0	65.0	66.0	62.0	65.0	65.0	62.0	62.0	61.0
0	113.0	57.0	61.0	60.0	62.0	58.0	58.0	57.0	58.0	58.0	60.0	60.0	55.0	56.0	59.0

Column



Row	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	52.0	54.0	50.0	49.0	52.0	53.0	56.0	54.0	52.0	48.0	52.0	53.0	54.0	50.0	50.0
13	53.0	54.0	56.0	56.0	53.0	58.0	57.0	54.0	53.0	56.0	58.0	57.0	56.0	53.0	54.0
12	54.0	55.0	57.0	56.0	58.0	59.0	62.0	58.0	54.0	58.0	61.0	58.0	54.0	56.0	61.0
11	58.0	56.0	59.0	60.0	57.0	60.0	58.0	58.0	58.0	56.0	58.0	58.0	59.0	55.0	56.0
10	58.0	58.0	60.0	60.0	58.0	60.0	61.0	61.0	59.0	60.0	60.0	61.0	62.0	52.0	60.0
9	55.0	58.0	61.0	58.0	57.0	60.0	59.0	61.0	59.0	58.0	60.0	58.0	60.0	57.0	57.0
8	60.0	56.0	59.0	56.0	57.0	60.0	62.0	60.0	61.0	58.0	59.0	60.0	61.0	57.0	56.0
7	61.0	58.0	60.0	59.0	55.0	56.0	59.0	61.0	57.0	60.0	60.0	56.0	58.0	58.0	59.0
6	55.0	62.0	59.0	60.0	61.0	59.0	58.0	58.0	59.0	59.0	59.0	60.0	57.0	58.0	56.0
5	60.0	59.0	60.0	61.0	59.0	57.0	61.0	59.0	61.0	57.0	60.0	57.0	60.0	55.0	57.0
4	59.0	59.0	60.0	57.0	60.0	60.0	65.0	60.0	57.0	59.0	58.0	60.0	56.0	62.0	59.0
3	52.0	56.0	58.0	57.0	56.0	56.0	60.0	59.0	60.0	58.0	65.0	58.0	58.0	56.0	62.0
2	57.0	57.0	58.0	57.0	57.0	61.0	59.0	59.0	61.0	59.0	62.0	58.0	58.0	60.0	61.0
1	48.0	54.0	57.0	60.0	58.0	58.0	60.0	59.0	57.0	57.0	59.0	59.0	59.0	55.0	56.0
0	93.0	49.0	50.0	51.0	53.0	53.0	57.0	55.0	52.0	51.0	50.0	53.0	53.0	55.0	56.0

Column

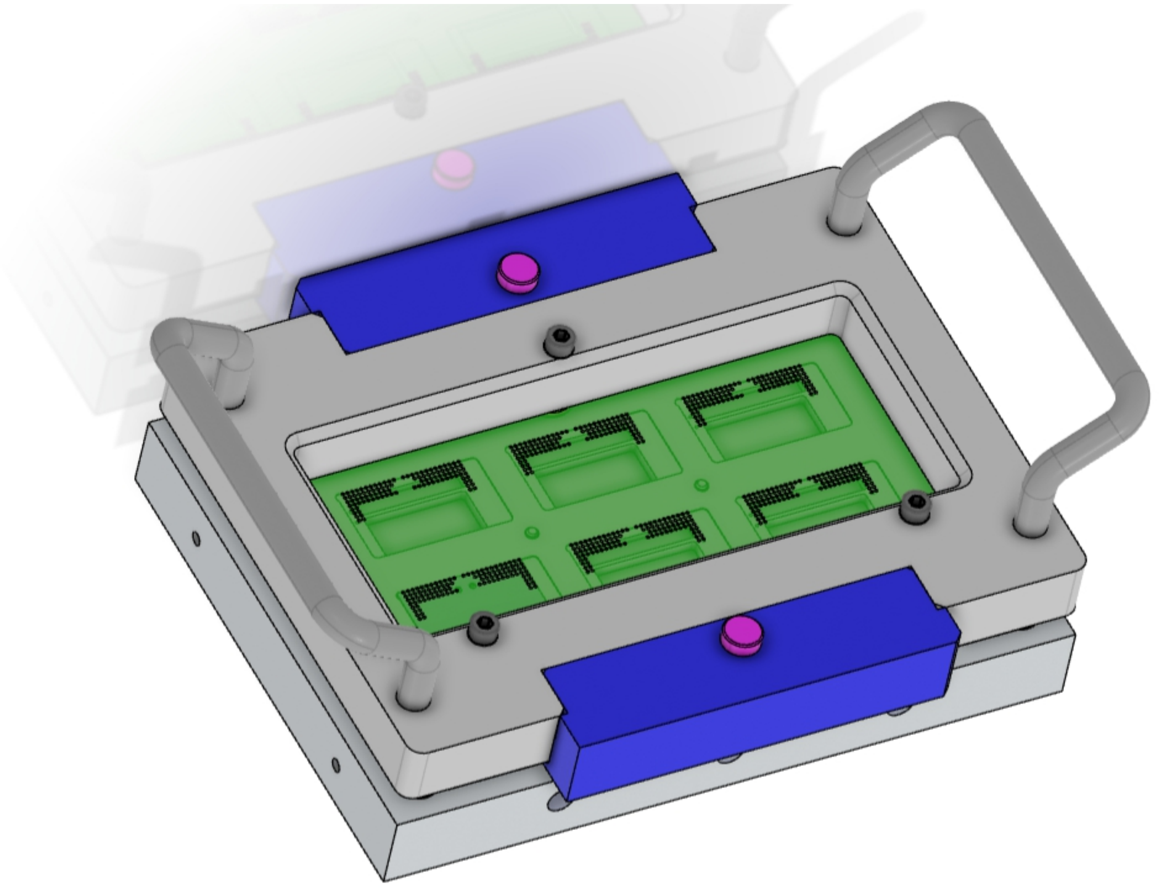
Thermal cycle overview

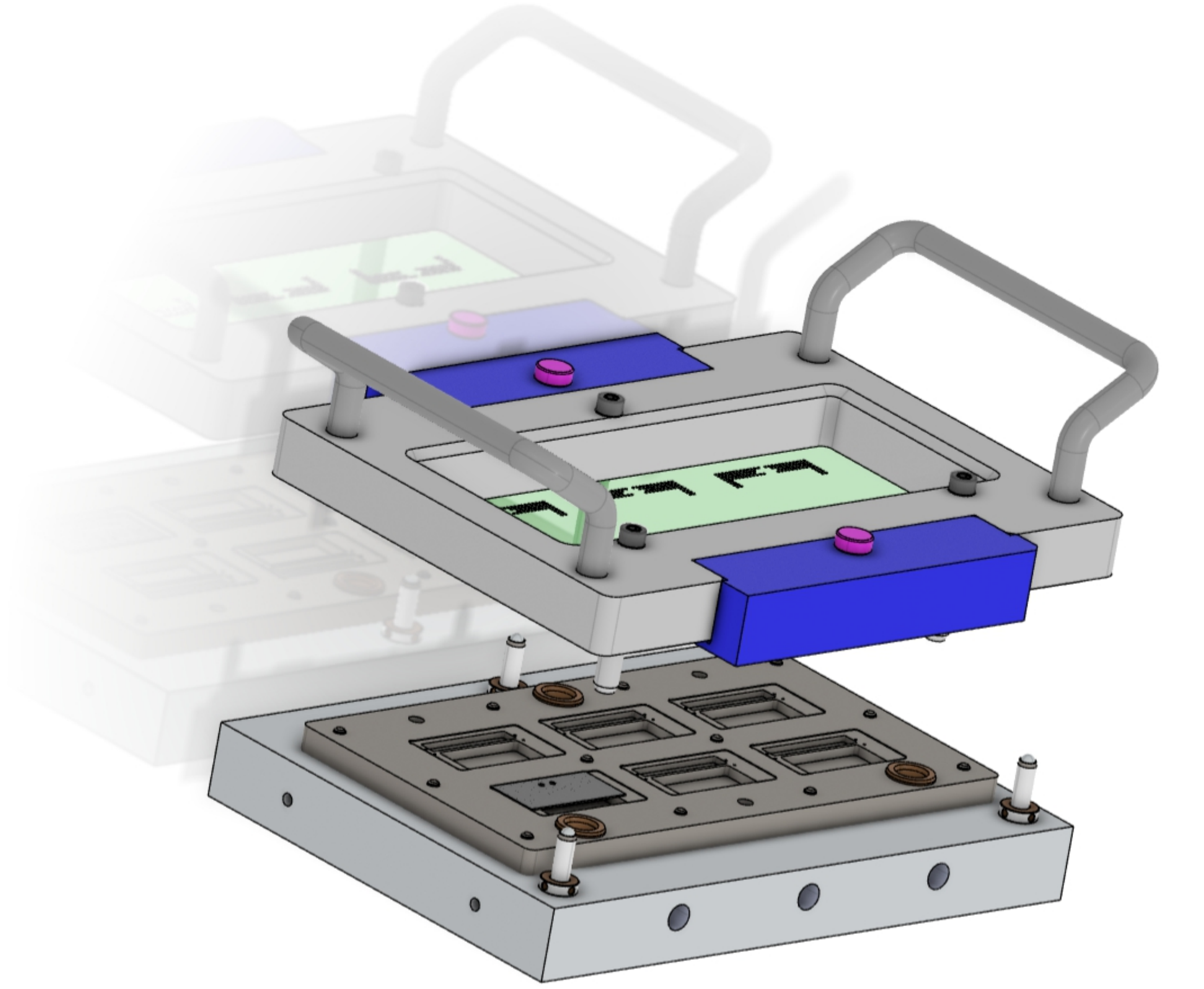
SN	ASIC version	Sensor 1	Sensor 2	UBM/flip chip	Sensor thickness	Functionality	Bump status before TC	Bump status after TC	Loaded
20WMO321000001	ALTIROC3	W15(#13)	W15(#20)	NCAP/IFAE	Thick(800um)	Only one chip working	2 pixel disconnected	2 pixel disconnected (~50TC)	YES
20WMO321000002	ALTIROC3	W22(#8)	W22(#7)	NCAP/IFAE	Thick(800um)	Both chips working	0 disconnected / 8 noisy pixels	0 disconnected (20TC)	YES
20WMO321000003	ALTIROC3	W15(#12)	W15(#8)	NCAP/IFAE	Thick(800um)	Both chips working (8 masked pixels)	11 disconnected / 8 noisy pixels	24disconnected pixels (20TC)	YES
20WMO321000004	ALTIROC3	W2-16(#48)	W2-16(#49)	PWchip bumps	Thin (300um)	2 wires not connected/ Both chips working (17 masked pixels)	~40 disconnected pixels (30TC)	~50 disconnected pixels (30TC)	NO
20WMO321000005	ALTIROC3	W2-16(#50)	W2-16(#51)	PWchip bumps	Thin (300um)	2 wires not connected / both chips working (3 masked pixels)	~30 disconnected pixels (30TC)	~45 disconnected pixels (30TC)	NO
20WMO321000006	ALTIROC3	W15(#2)	W15(#6)	NCAP/IFAE	Thick(800um)	Only one chip working	0 disconnected / 1 noisy pixels	1 disconnected (175 TC)	NO
20WMO321000007	ALTIROC3	W15(#7)	W15(#9)	NCAP/IFAE	Thick(800um)	Both chips working	0 disconnected / 6 noisy pixels	0 disconnected (175 TC)	NO
20WMO321000008	ALTIROC3	V3 W10(#1)	V3 W10(#6)	NCAP	Thin (300um)	Both chips working	All connected / 1 noisy pixel	All connected (50TC)	YES
20WMO321000009	ALTIROC3	V3 W10(#7)	V3 W10(#8)	NCAP	Thin (300um)	Both chips working	1 pixels disconnected	2 pixels disconnected (50TC)	YES
20WMO3210000010	ALTIROC3	V3 W10(#9)	V3 W10(#11)	NCAP	Thin (300um)	Both chips working	All connected	All connected (50TC)	YES
20WMO3210000011	ALTIROC3	V1-A15(#13)	V1-A15(#14)	PWchip bumps	Thick(800um)	Both chips working	All connected	All connected (120TC)	YES
20WMO3210000012	ALTIROC3	V1-A15(#15)	V1-A15(#16)	PWchip bumps	Thick(800um)	both chips working but col14 for Asic1	1 noisy pixels + col14 not working	3 pixels disconnected (180TC)	YES
20WMO3210000013	ALTIROC3	V1-A15(#17)	V1-A15(#18)	PWchip bumps	Thick(800um)	Both chips working	All connected	All connected (120TC)	YES

Plans for the future

- Preproduction is expected to start end of 2024
- The last version of ALTIROC => ALTIROC-A
- In the preprod. we will assemble 10% of the total modules using ALTIROC-A

- Improving gluing setup for multi-module assembly and testing (jig for 6 modules at the same time)





6 module jigs for module assembly

Conclusion

- High Granularity Timing Detector (HGTD) proposed in front of the end-cap calorimeter for pile-up mitigation

- Adding timing information in the end-cap region improves pile-up rejection and vertex reconstruction

- It consists of 8032 modules
  - ~2000 modules will be assembled at IJCLab (France)

- Thin modules tend to start breaking during thermal cycles
  - Initial modules had a lot of disconnected pixels even before thermal cycles
  - With improved hybridization, results are better, but we still had some disconnected pixels after ~ 20 TCs

- Thick modules are shown to be more robust
  - Decision to move towards thick hybrids
  - Multiple modules surviving more than 100 TCs without broken pixels

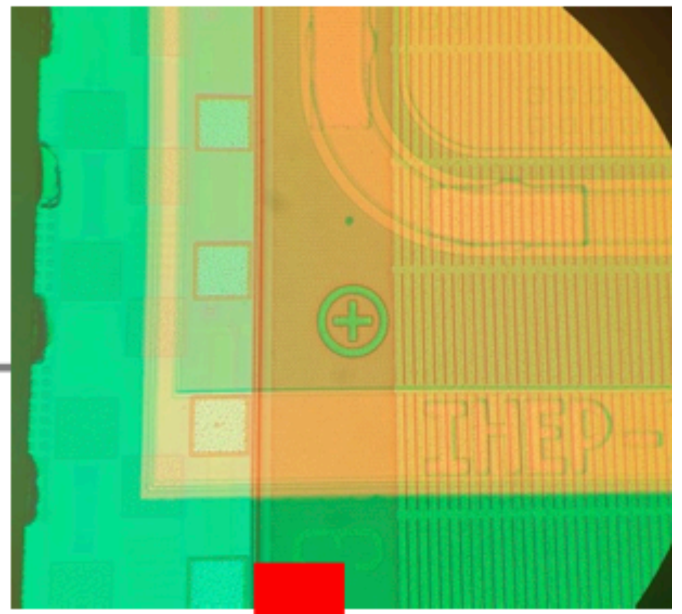
- Preproduction starting soon using the last version of ALTIROC (ALTIROC-A) and using the thicker sensors

Backup slides

Overview

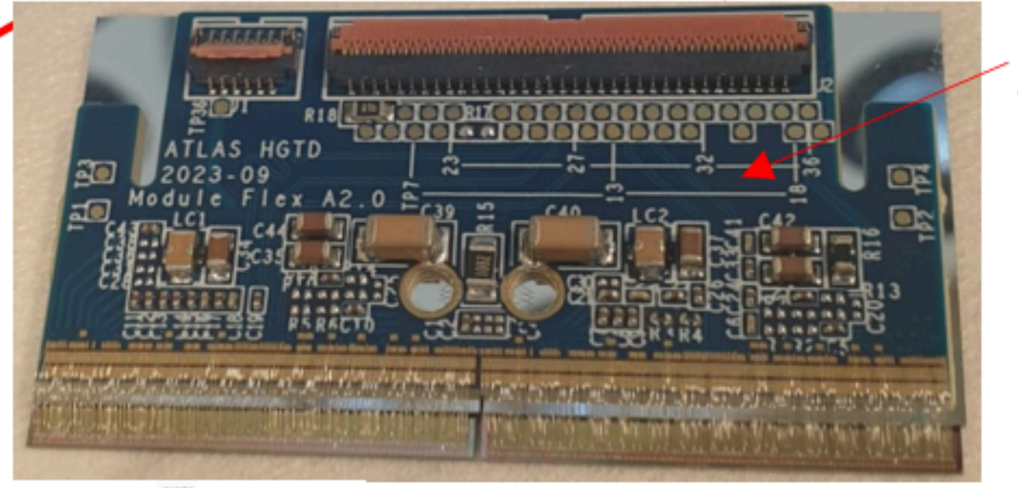
- Module and Detector Units composition (WBS items):
    - Hybridization (ALTIROC + LGAD sensor)
    - Module flex
    - Assembly (flex attach and wire-bonding)
    - Detector Unit
    - Flex tails

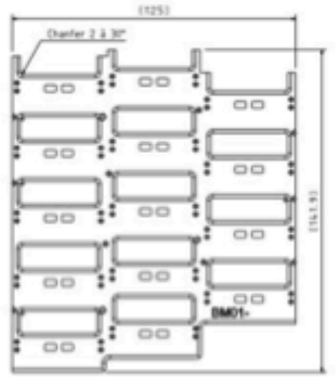
LGAD + ALTIROC



Hybrids

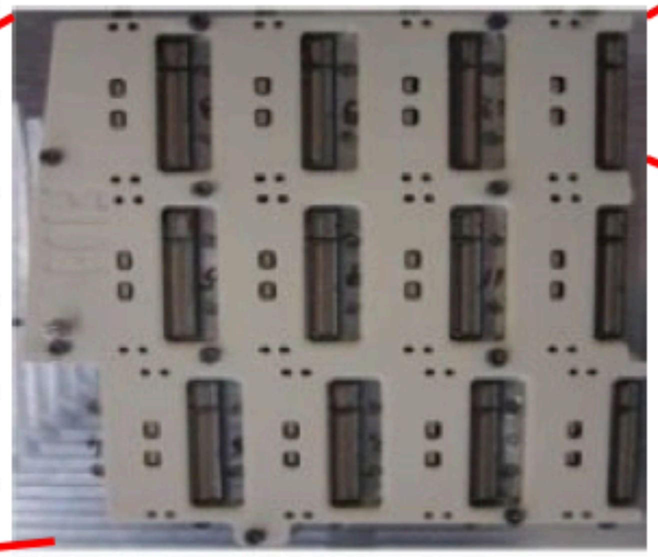
Modules





Support Unit

Support Unit + Modules: Detector Unit



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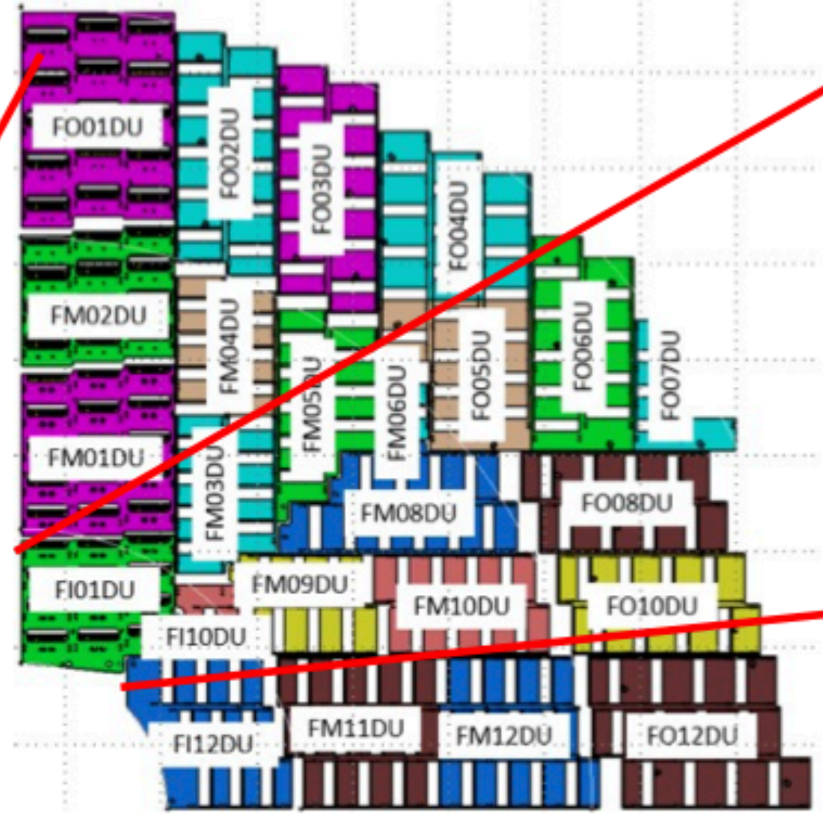
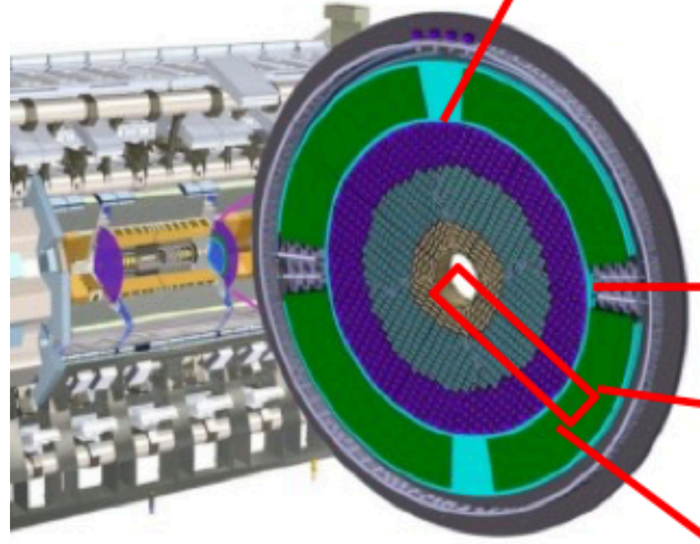
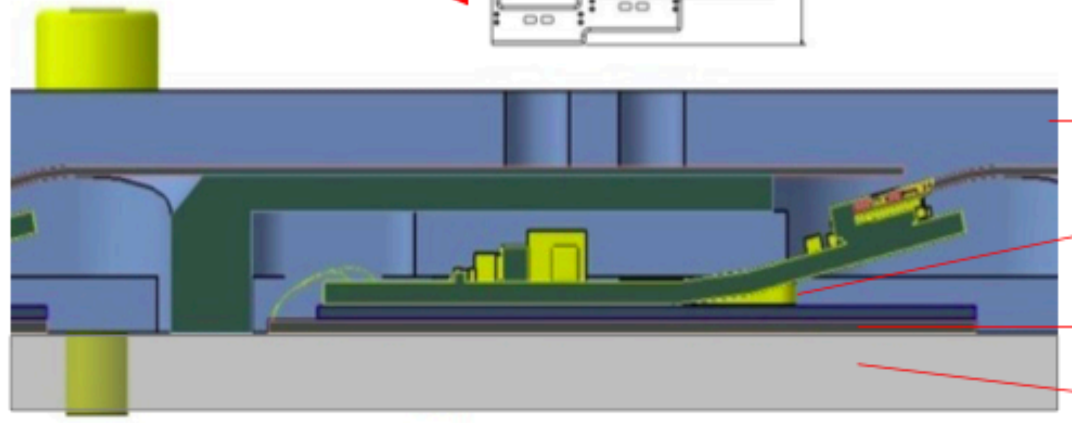
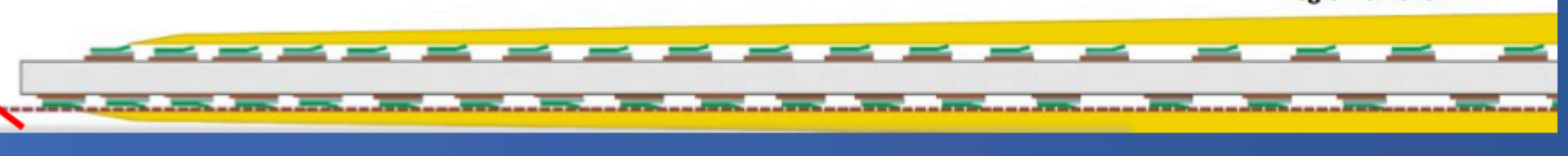




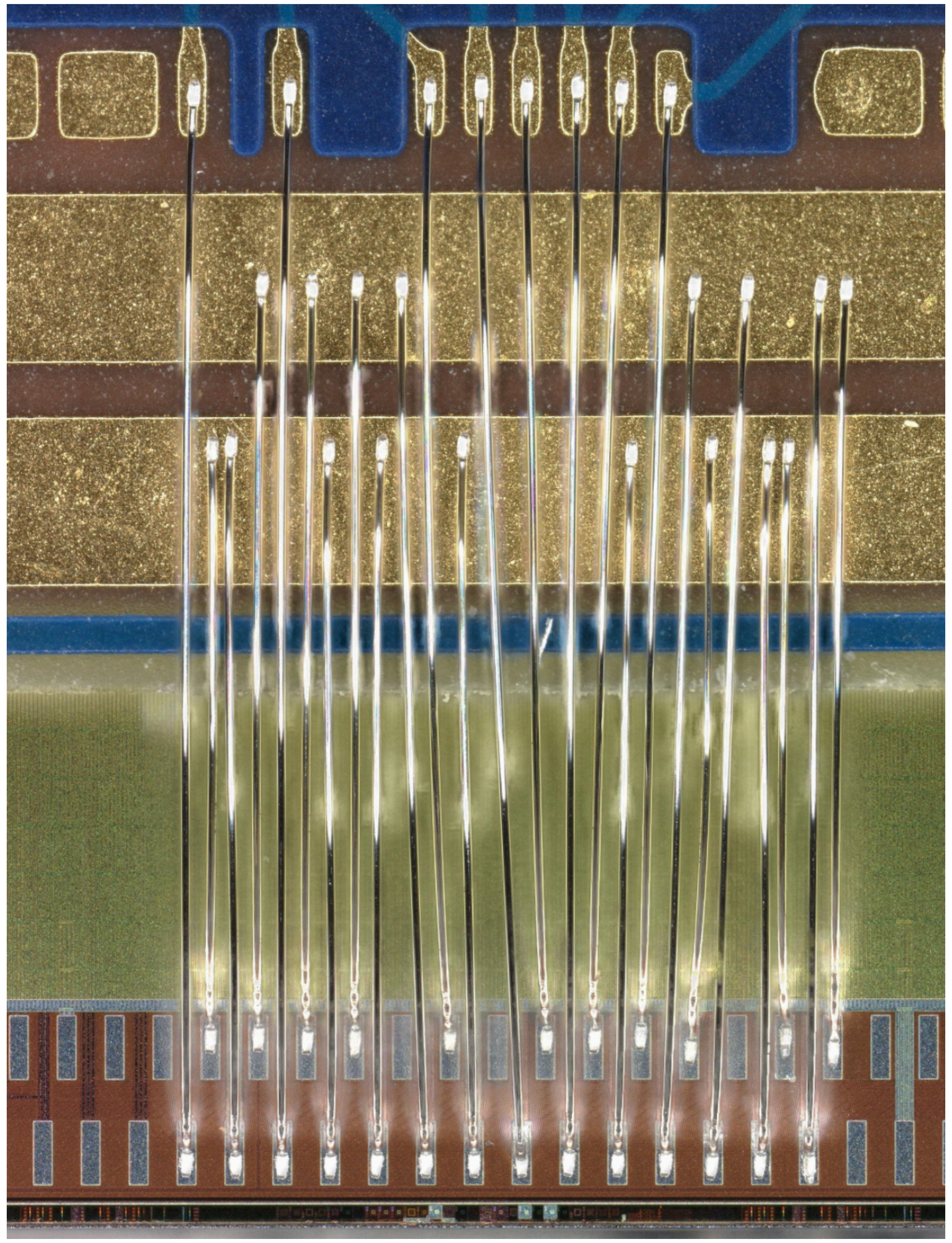


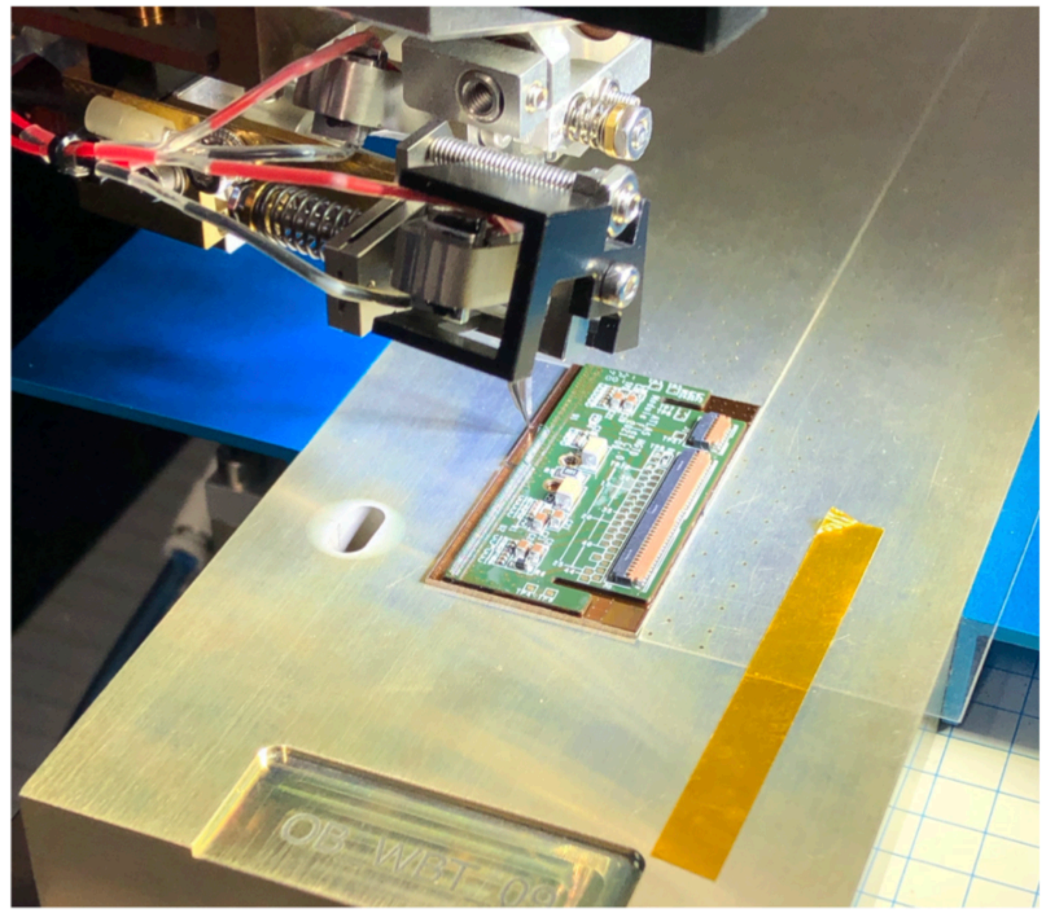


Flex Tail connects module to PEB

Wire bonding

- Wire bonding done at C4PI in Strasbourg
- Initial difficulties with wire bonding ALTIROC3 modules because of additional row of pads on the chip
  - Wires sometime have to be moved by hand (to be automatised)
- Overall the performance of wire bonding of ALTIROC3 modules very good and consistent
- Wire bonding of ALTIROC-A soon to be done and verified



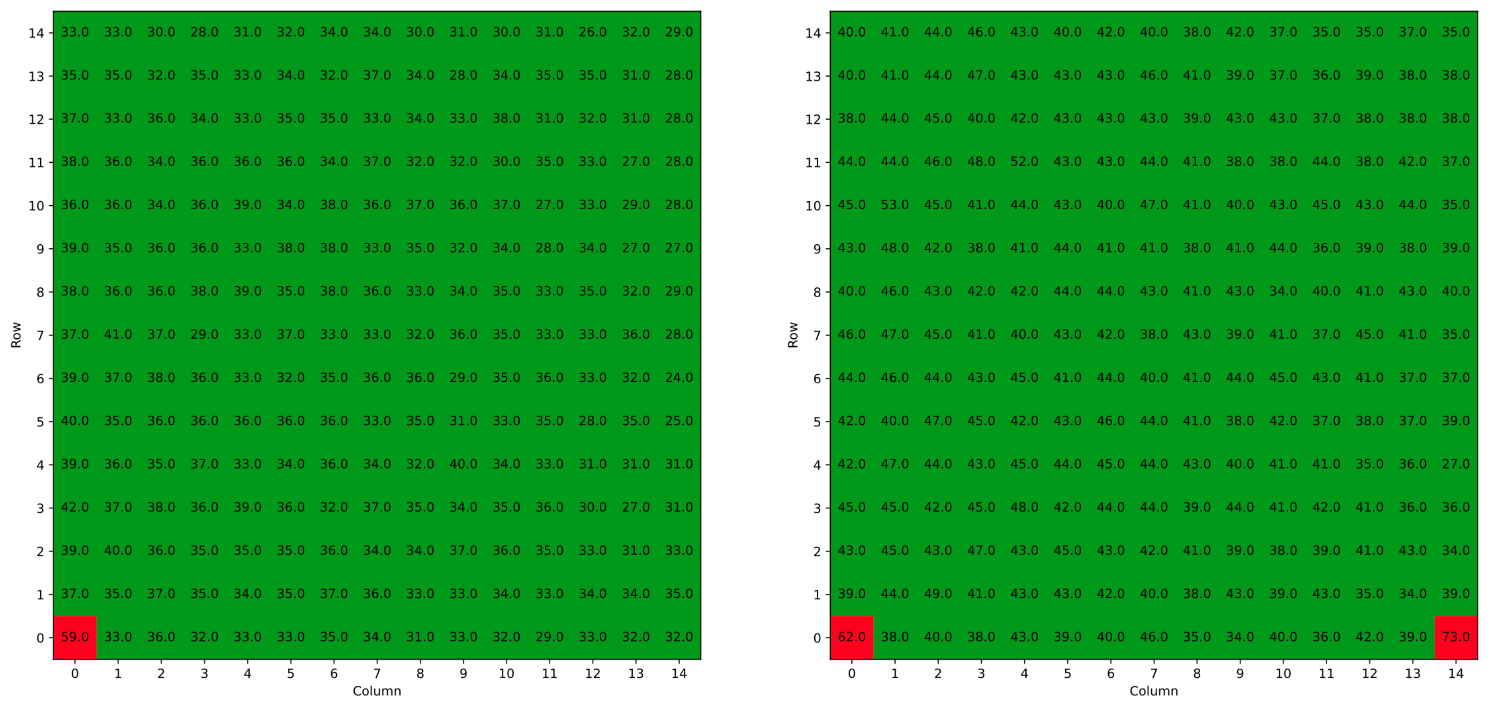


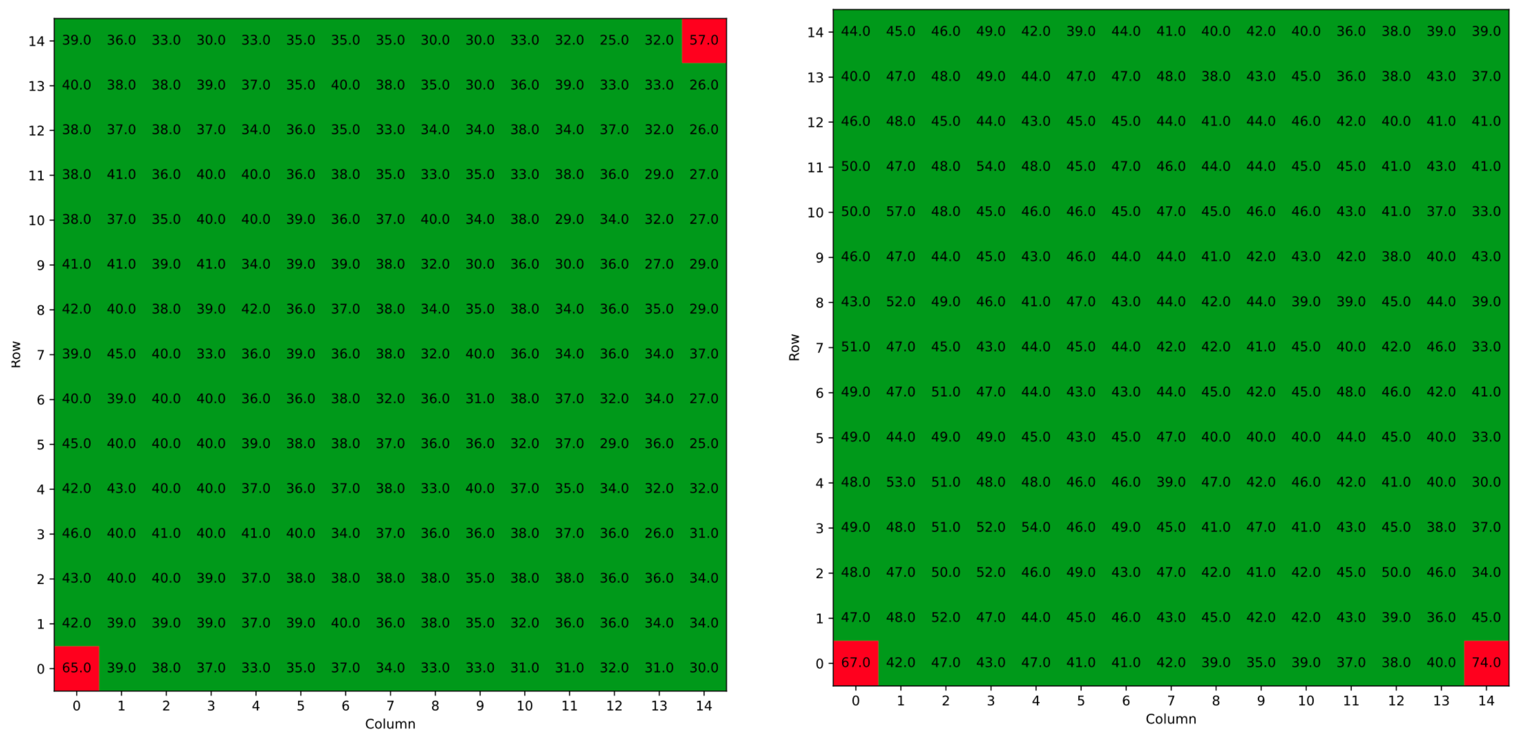
Comparison of the methods

Precycle

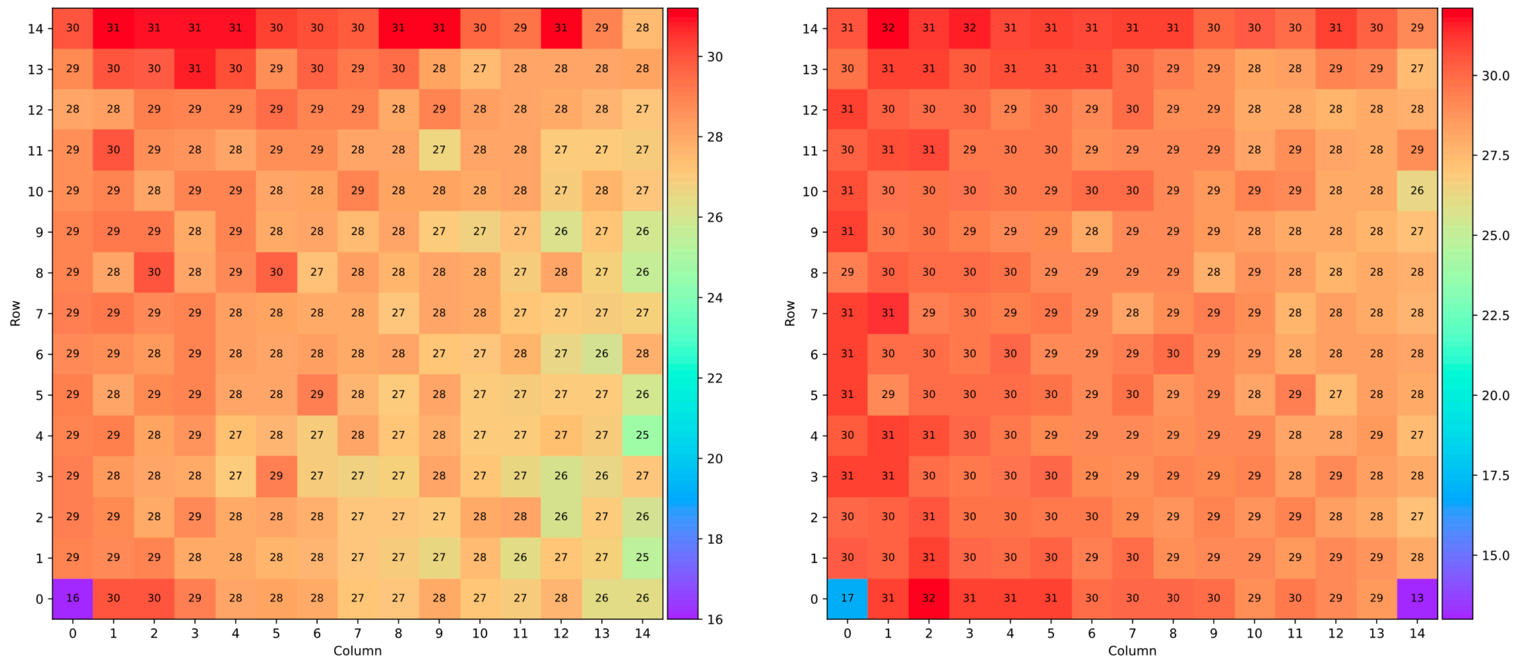
20 thermal cycles

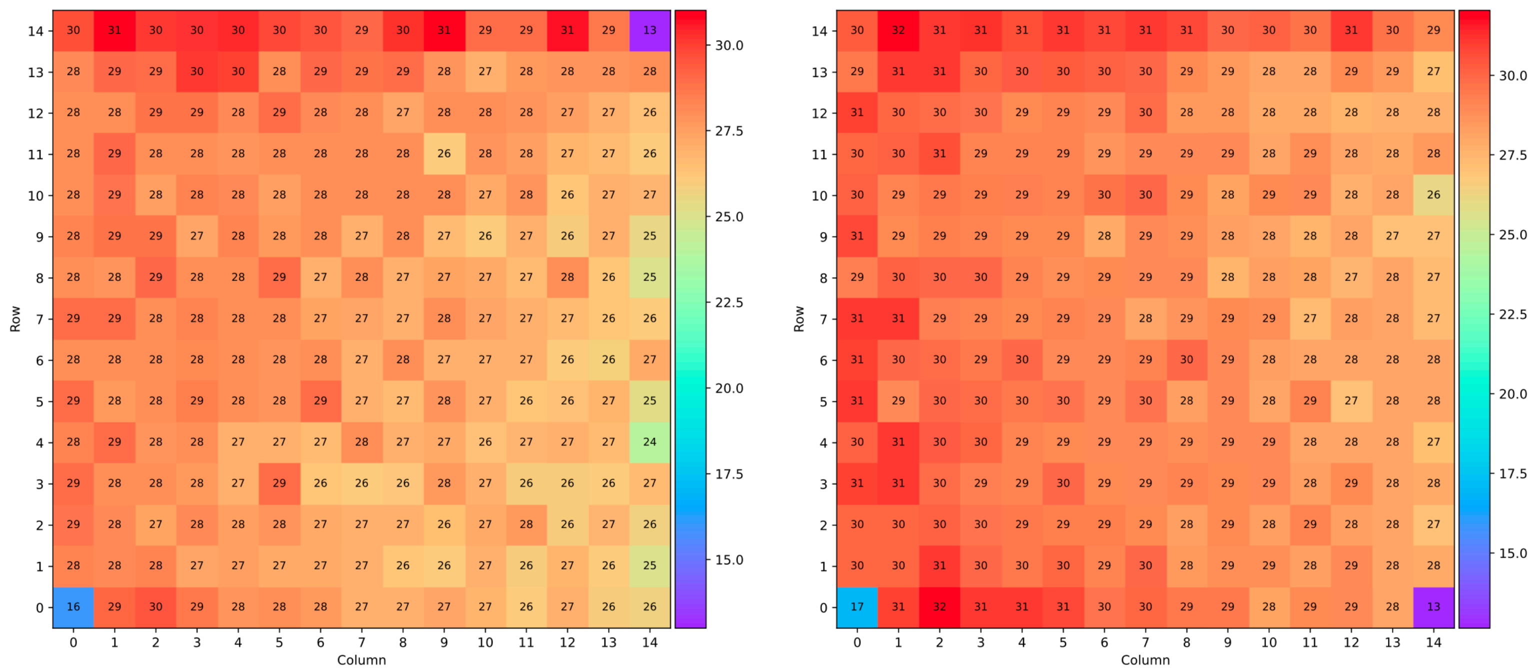
Diff Qinj



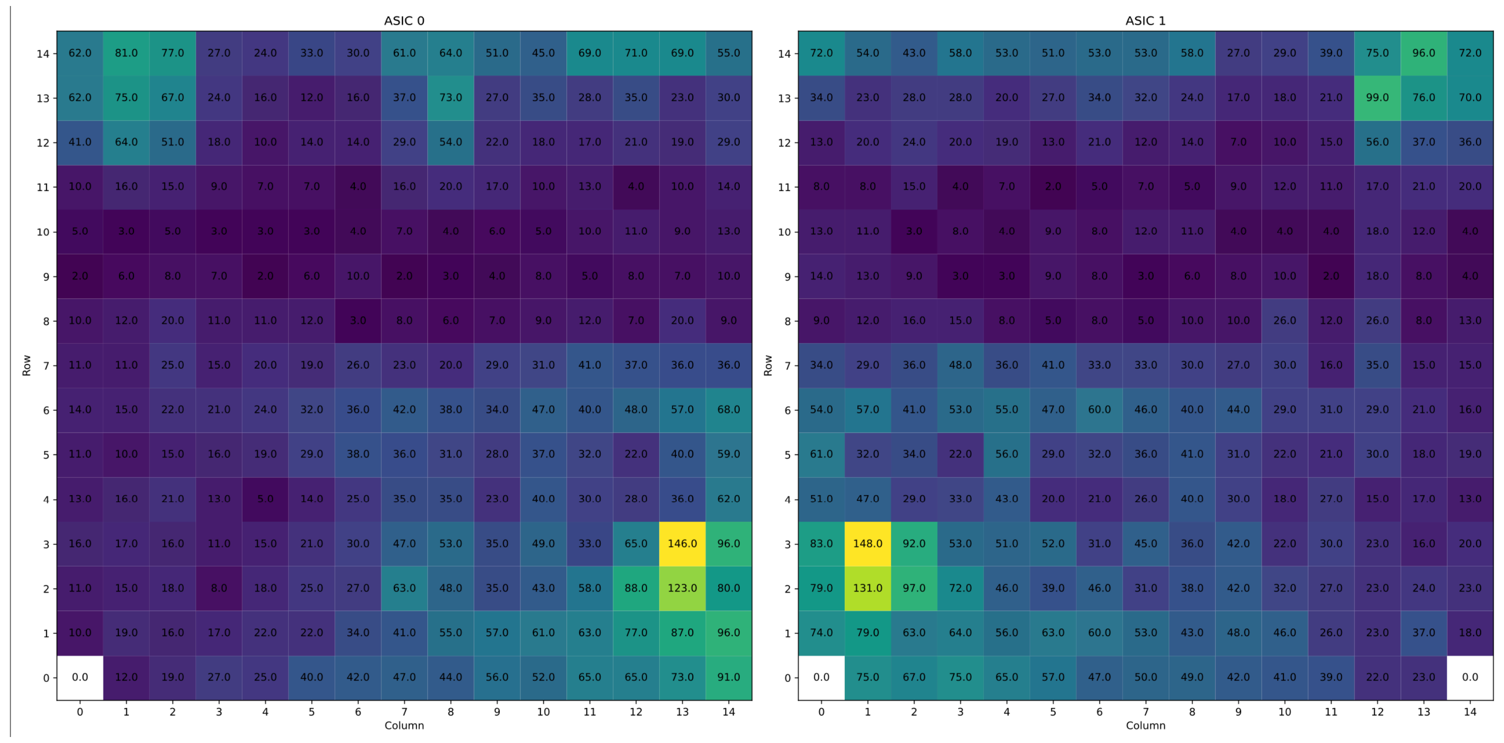


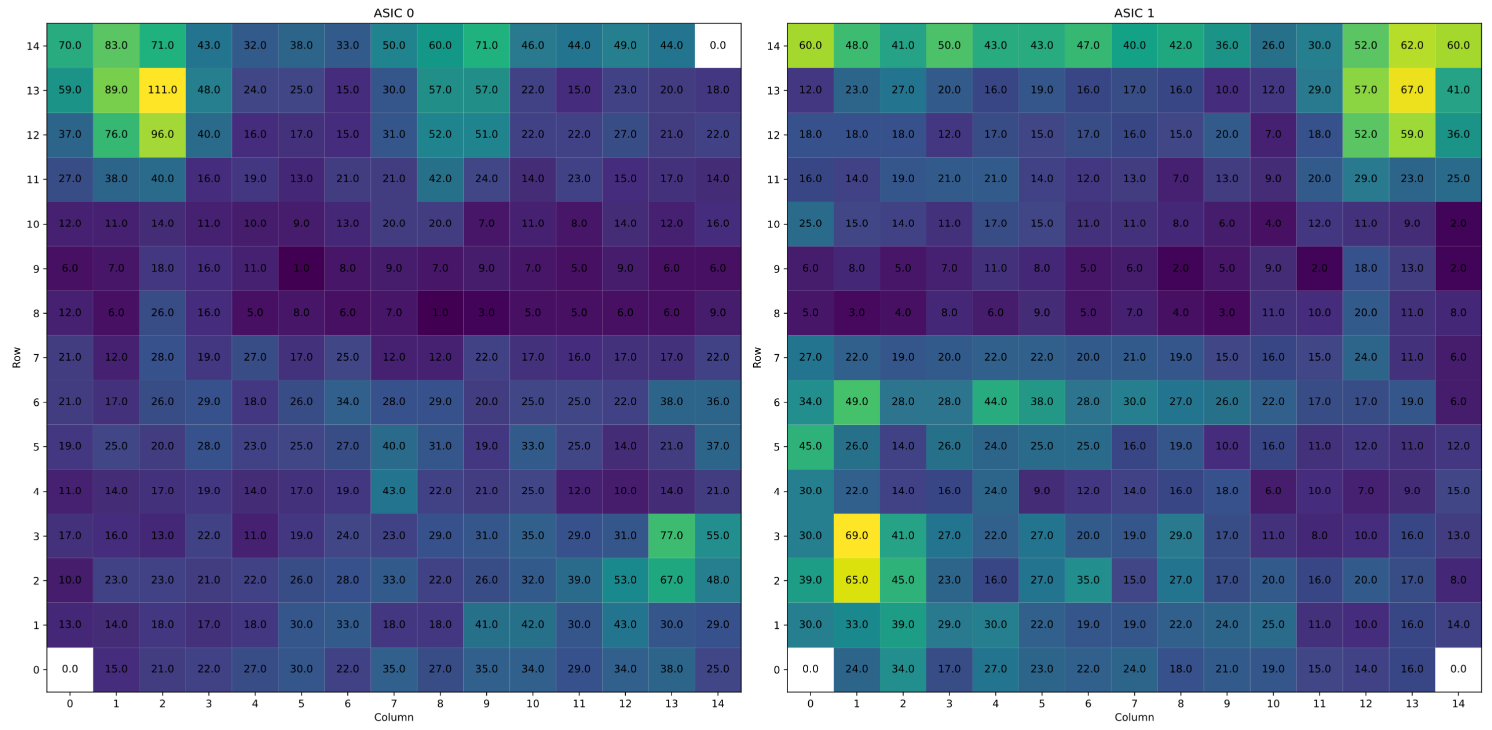
Tot map





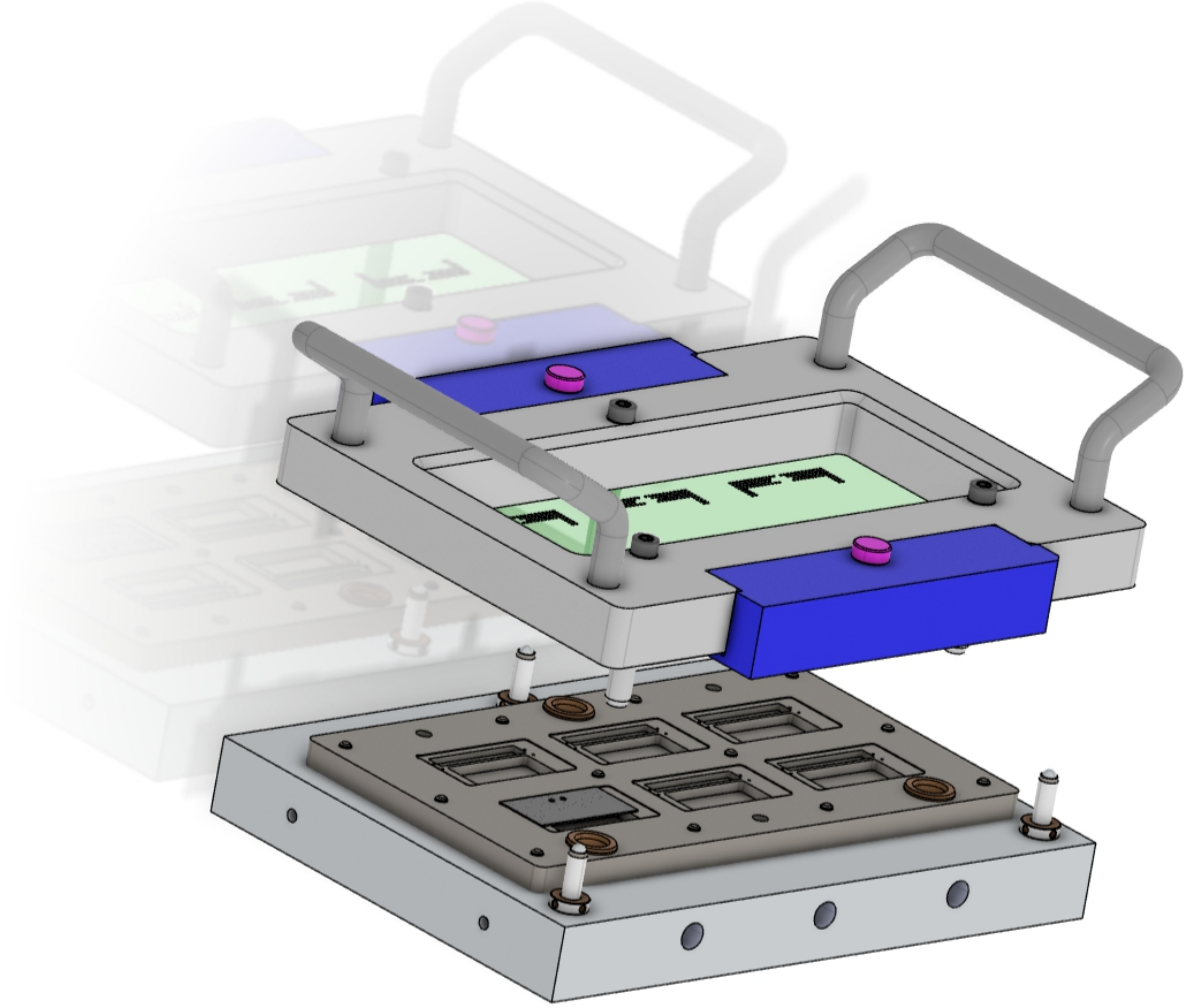
Source scan

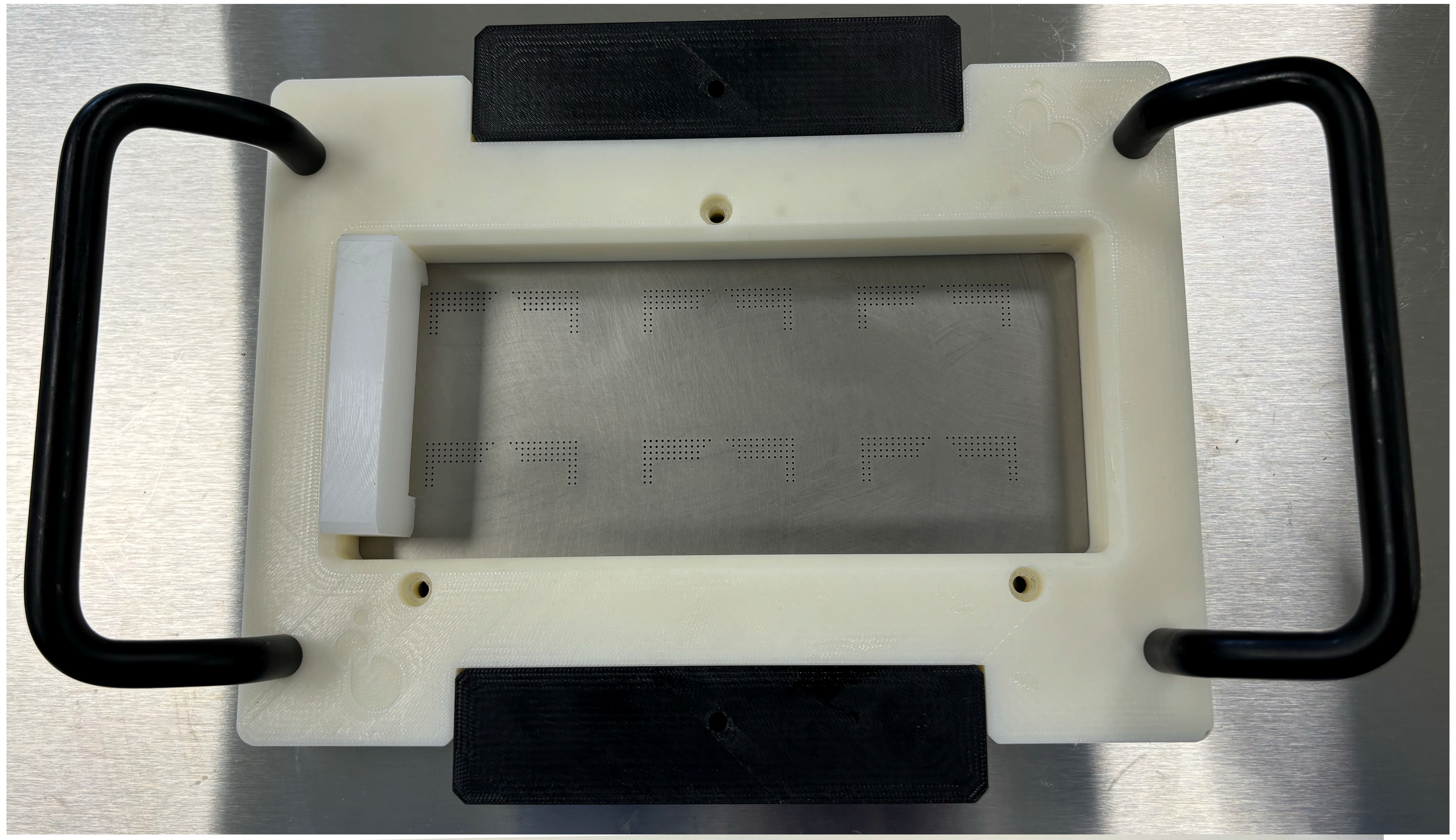




Module assembly - (pre)production

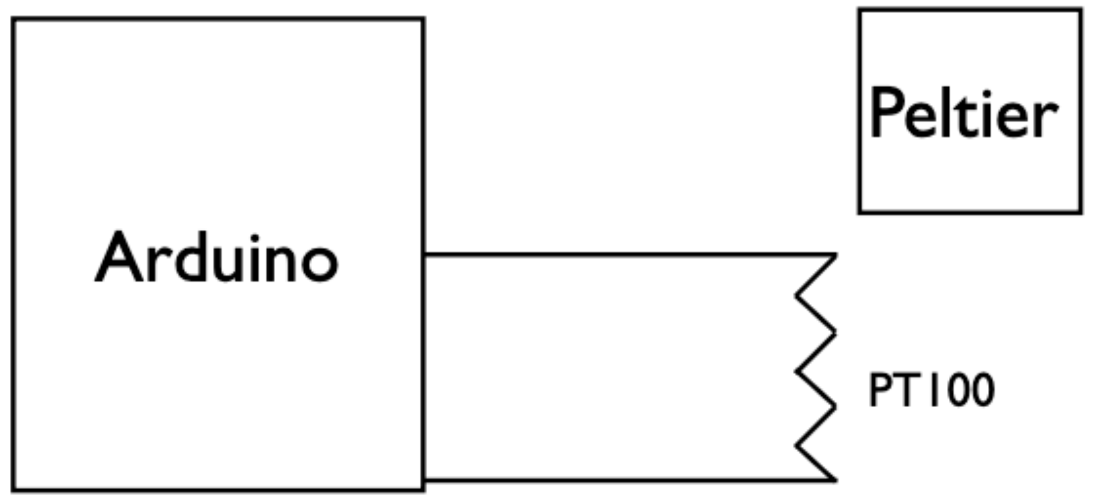
- Plan to move towards 6 module jigs
- Glue will still be deposited over flex using spatula and hole pattern stencils
  - Stencils, the frame for stencils and spatulas manufactured
  - Currently being tested on the inlay-like plate that holds glass with vacuum

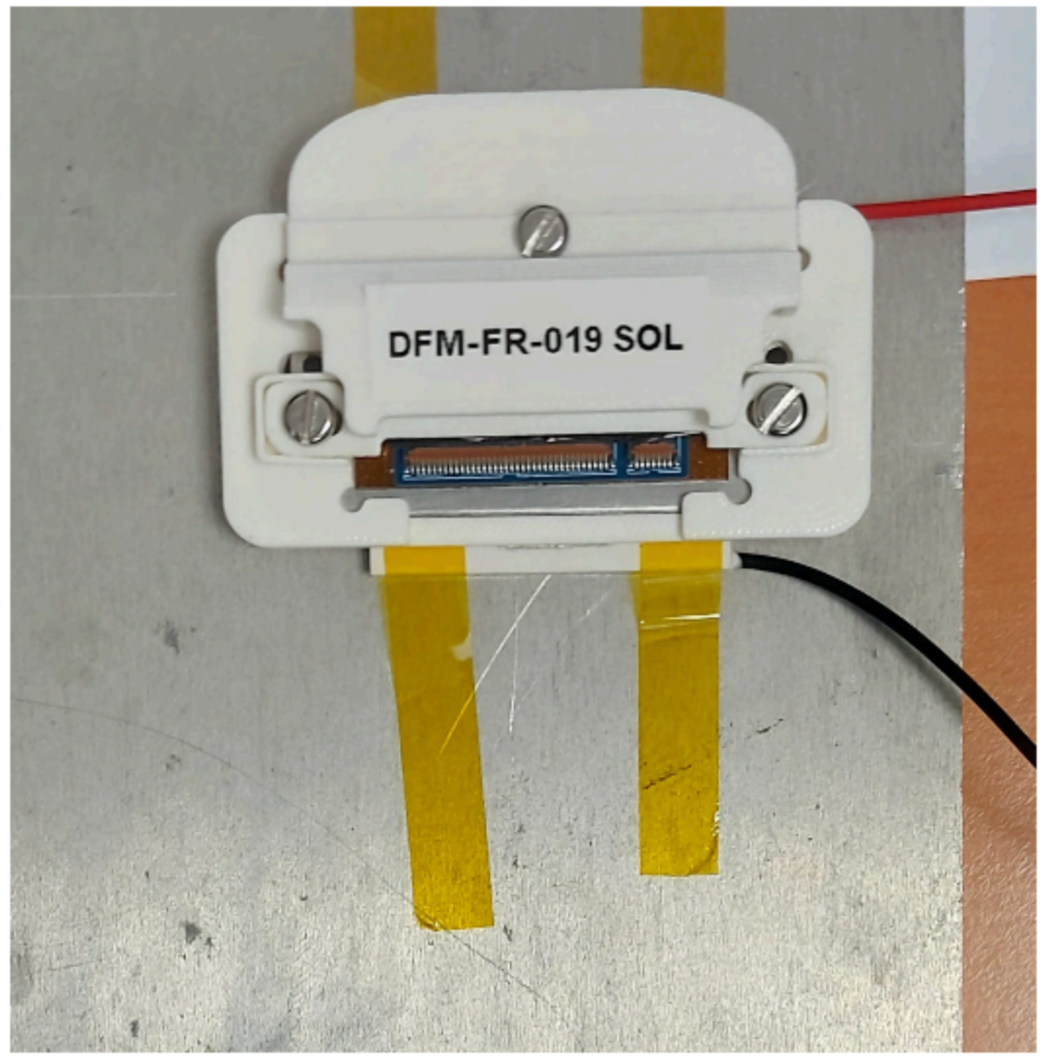


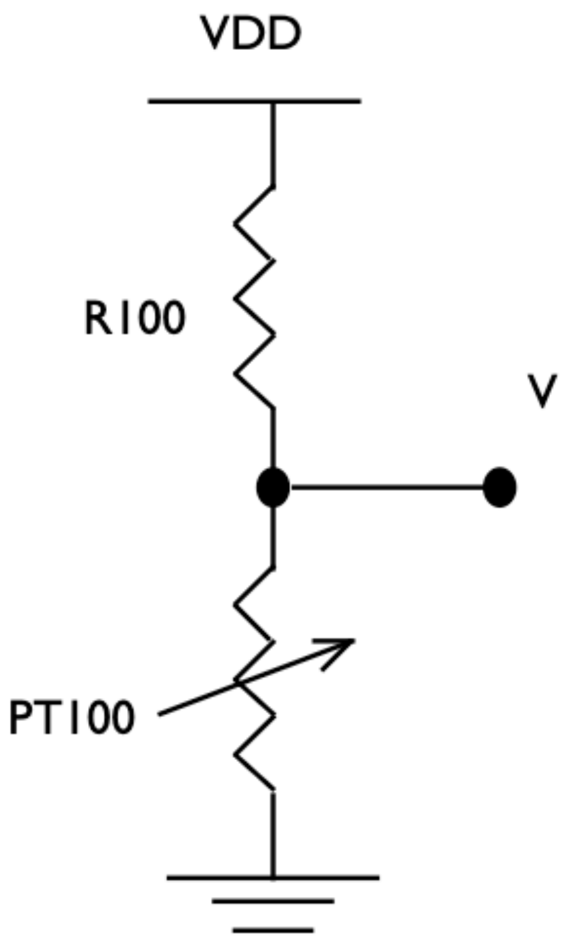


Peltier system

- Defining the setup for future module testing
- Moderating the temperature of the module using Peltier module underneath
- The idea is to have the Peltier element, with a temperature sensor on its surface (Pt100 or Pt1000), and a simple and programmable control system such as an Arduino to do temperature control, by implementing a PID control algorithm and adjusting the current in the Peltier with PWM signal.
- Targeted precision of 1°C







Overall production schedule

- Critical path: Hybrids → module assembly → loading → assembly at CERN
- HGTD A (0-50%):
  - Hybrids:
    - 1st batch (0-12.5%), Aug 2025
    - 50% done by Dec, 2025
  - Module flex: by Oct 2025
  - Detector units : by July 2026
  - Flex tails: by Dec 2025
  - HGTD A ready for install: by Dec 2026
- HGTD C (50-100%):
  - Hybrids: by May 2026
  - Module flex: by March 2026
  - Detector units : by April 2027
  - HGTD C ready for install : by June 2027