

Control, commissioning, operation, and performance of the Phase-I upgrade of the LAr calorimeter electronics of the ATLAS detector

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Doctoral thesis defense

July 11, 2024



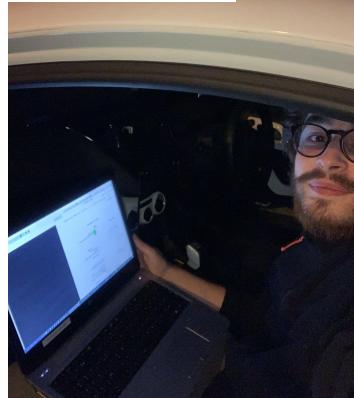
Content

1. Experimental context
2. Improve the stability of the LAr Trigger Digitizer Board
3. Timing shift
4. Digital trigger status
5. Conclusion

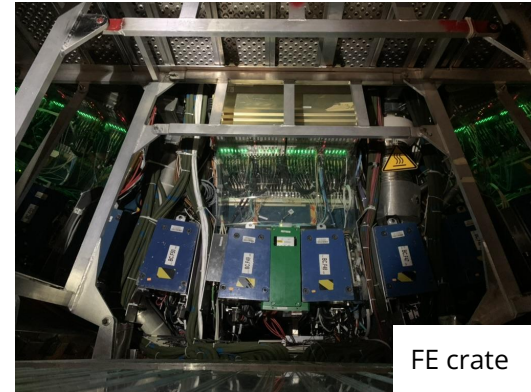
Cleaning of ATLAS cavern



On call expert



Official start of Run 3

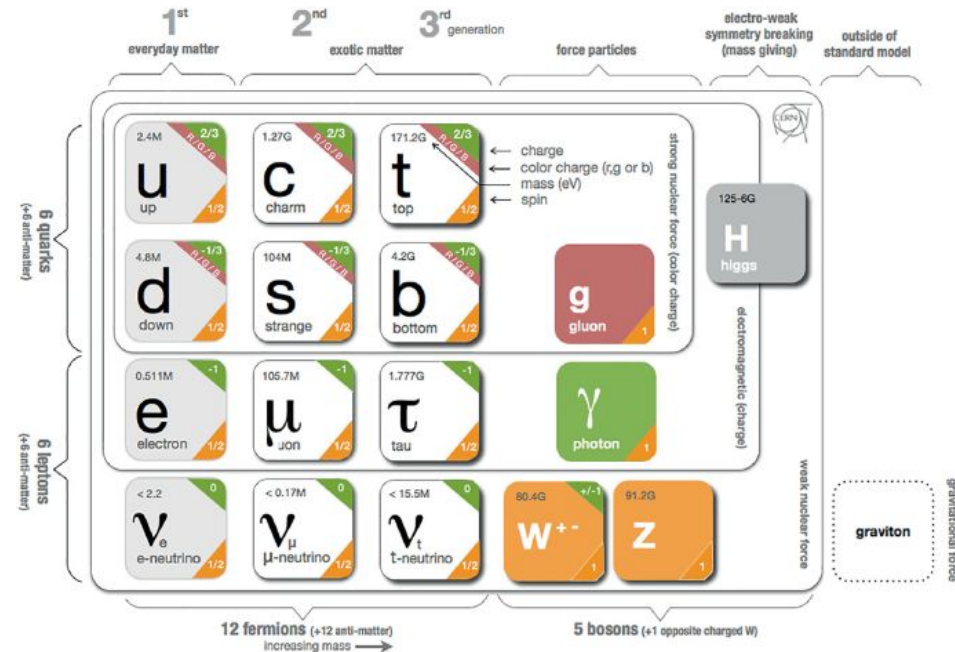


FE crate

Cabling LTDBs control & data fibers

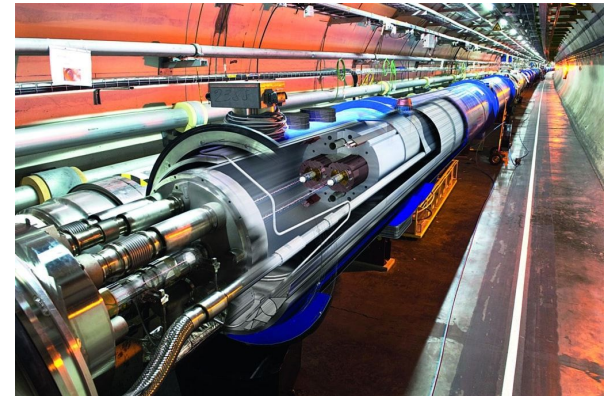
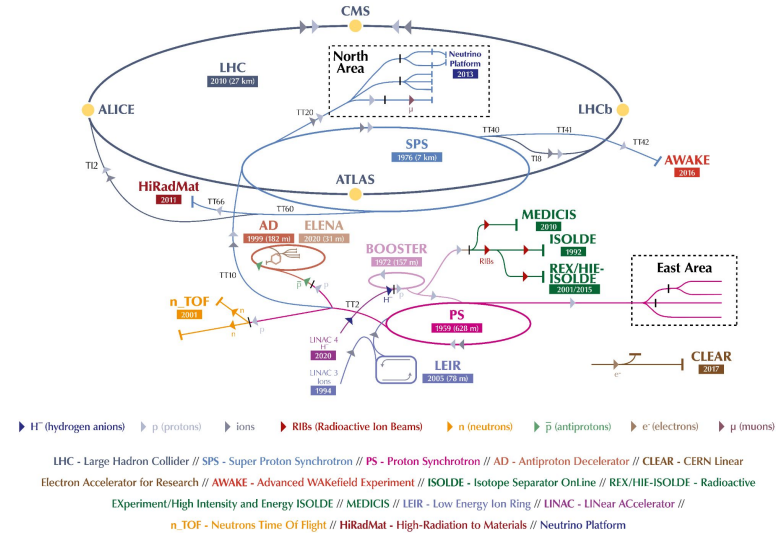
The standard model (SM) of particle physics

- The SM describes the fundamental elements of matter and their interactions
- Composed of 2 types of fundamental particles - *fermions* and *bosons*
 - 12 fermions (6 quarks + 6 leptons)
 - 4 vector-bosons
- Governed by 3 fundamental forces
 - Weak, Electromagnetic, Strong
- The Higgs Boson provides mass to particles
- SM is an incomplete theory
 - *Dark matter* and *dark energy* unexplained
 - *Matter-antimatter asymmetry* unexplained
 - *Gravity* is not included



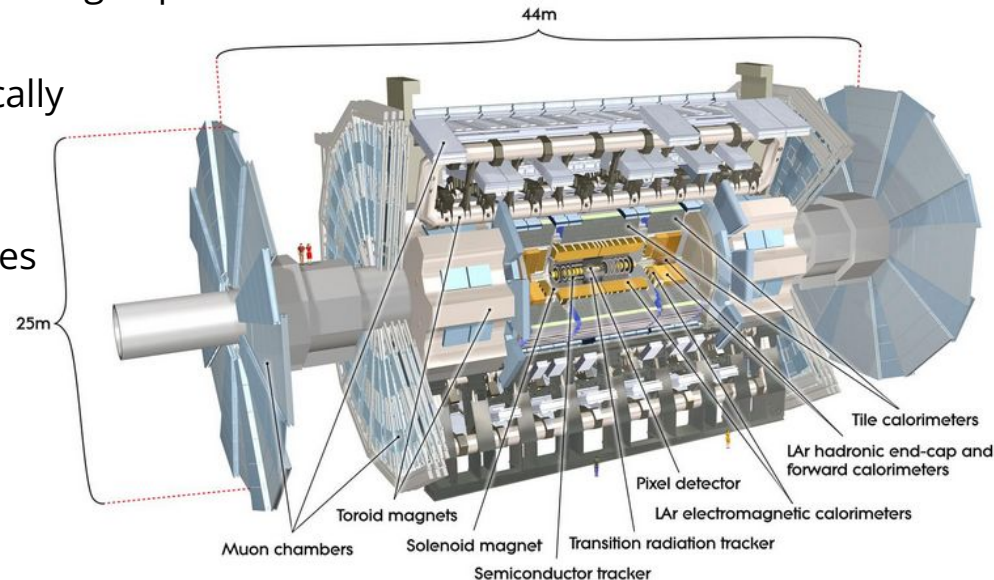
The Large Hadron Collider (LHC)

- Completed at CERN in September 2008
 - In operation since 2010 for physics data taking
- **27 km** circumference accelerator ring with two counter-rotating beams
- Located **100 m** underground
- Center of mass energy up to $\sqrt{s}=14$ TeV
- Proton bunches collide every **25ns** at interaction points
- 40 million bunch crossing per second (**40MHz**)
- Four main experiments:
 - ALICE
 - LHCb
 - CMS
 - **ATLAS**



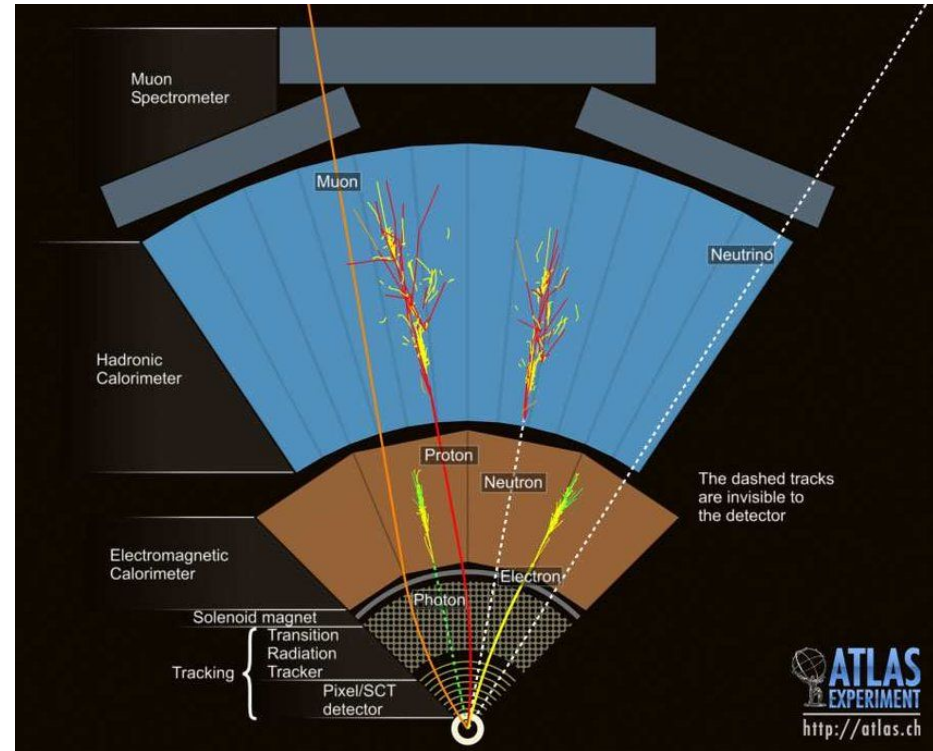
ATLAS detector

- ATLAS is a multi purpose detector
 - Higgs Boson search, SM precision measurements and beyond SM physics searches
- Onion layer detector structure
 - Inner detector
 - Tracks the trajectory and momentum of charged particles
 - Electromagnetic calorimeter
 - Measures the energy of electromagnetically interacting particles
 - Hadronic calorimeter
 - Measures the energy of hadronic particles
 - Muon Spectrometer
 - Measures the momenta of muons
 - Toroid and solenoid magnet
 - Bend the trajectories of charged particles to deduce their momentum



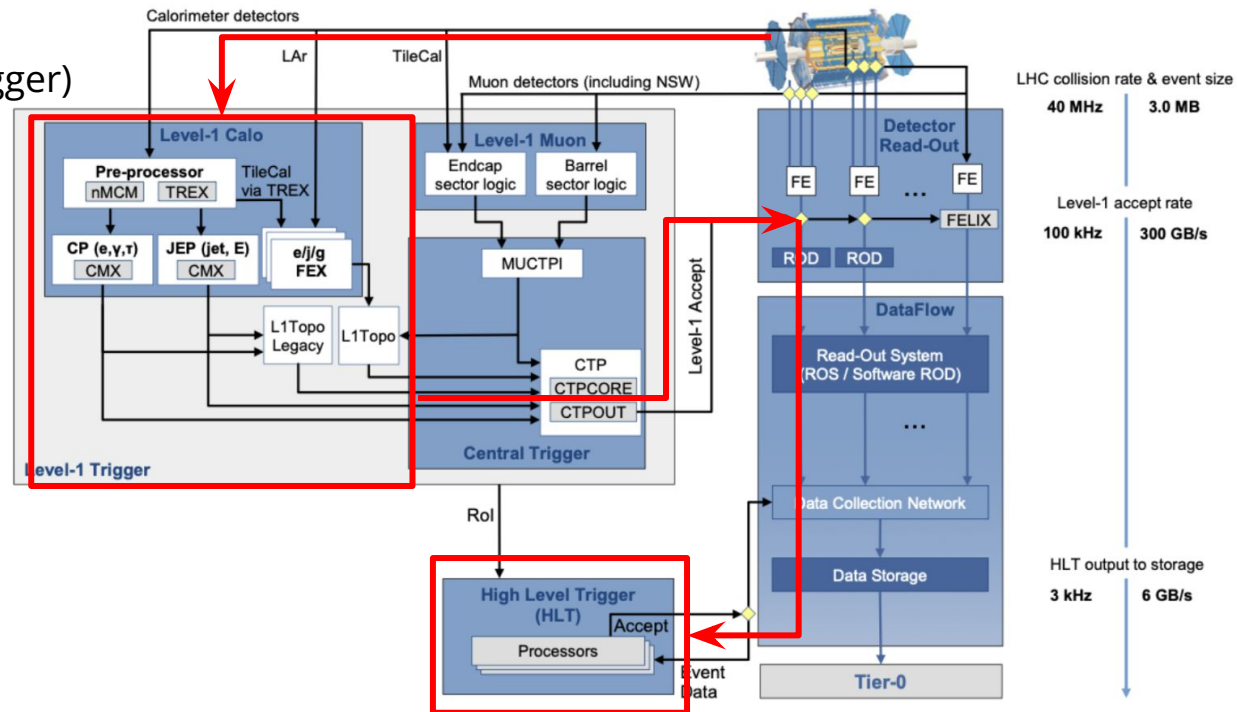
ATLAS detector

- Detector provides position, timing and energy information
- Based on the particle type, interactions occur in different parts of the detector
 - Photons produce showers in the electromagnetic calorimeter
 - Electrons have their trajectory and momentum tracked, and produce showers in the electromagnetic calorimeter



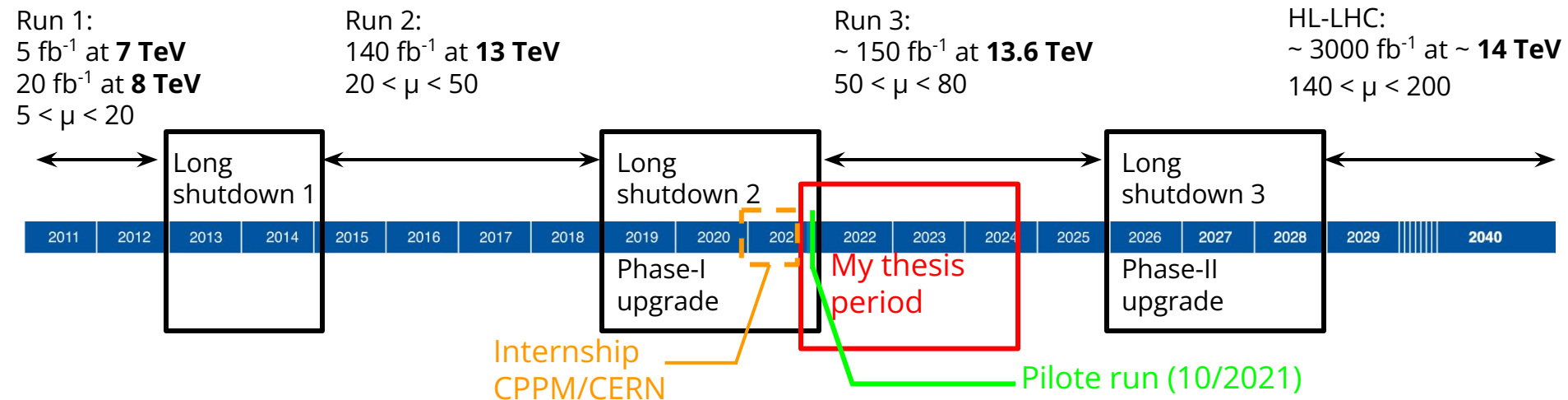
Trigger and readout architecture

- Impossible to record all collisions events at 40 MHz
- ATLAS has 2 levels of trigger
 - Level-1 trigger (Hardware trigger)
 - 40 MHz \rightarrow 100kHz
 - Fixed latency
 - Max latency 2.5 μ s
 - HLT (Software trigger)
 - 100 kHz \rightarrow ~3 kHz



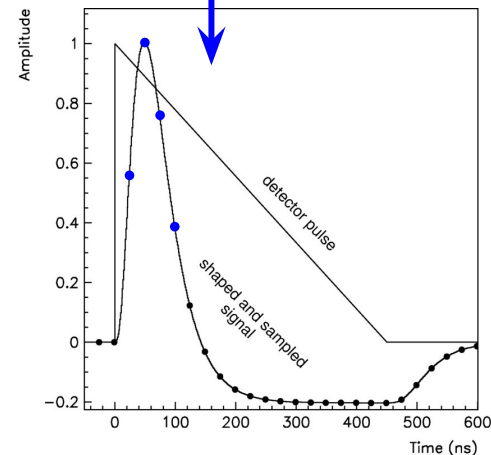
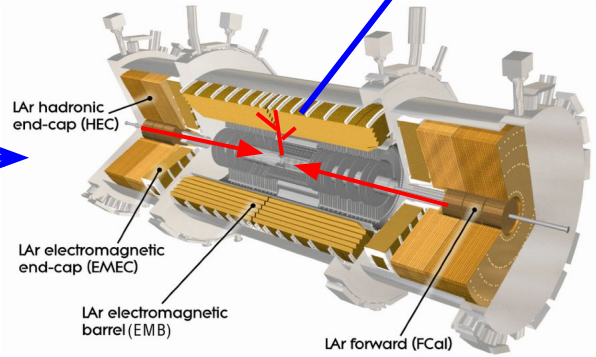
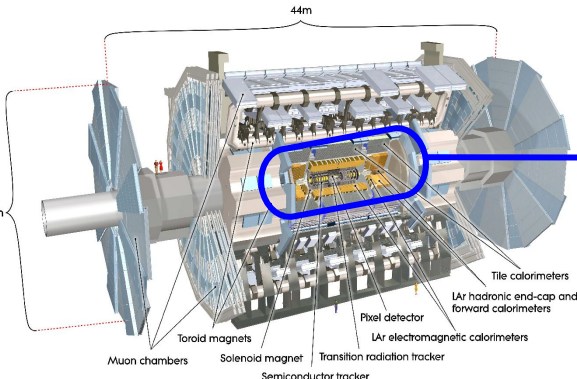
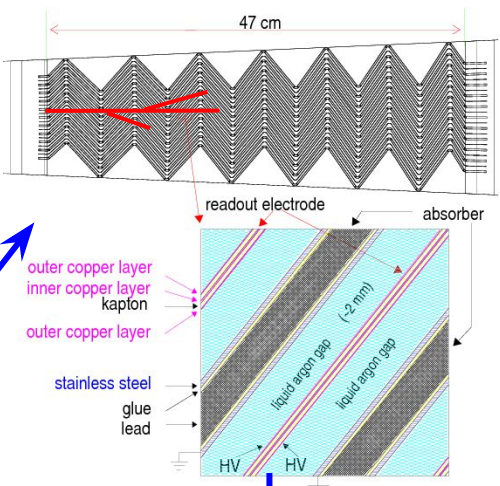
LHC to HL-LHC

- Increase the luminosity in two phases in 2022 and 2029 to reach the HL-LHC
 - Study rare processes
- Trigger degradation
- The detectors will be upgraded to cope with the high pileup at the HL-LHC
 - In particular the ATLAS calorimeter readout electronics will be completely replaced



Liquid Argon Calorimeter

- Used to measure the deposited energy in each of the cell
 - Lead/liquid argon for electromagnetic calorimetry (Barrel/ End-Cap)
 - Copper or Tungsten + liquid argon for hadronic calorimetry (HEC)
 - Ionised the liquid Argon and generate electromagnetic shower
 - Induces triangular electric signal in electrode
 - Amplified/shaped/sampled at 40MHz



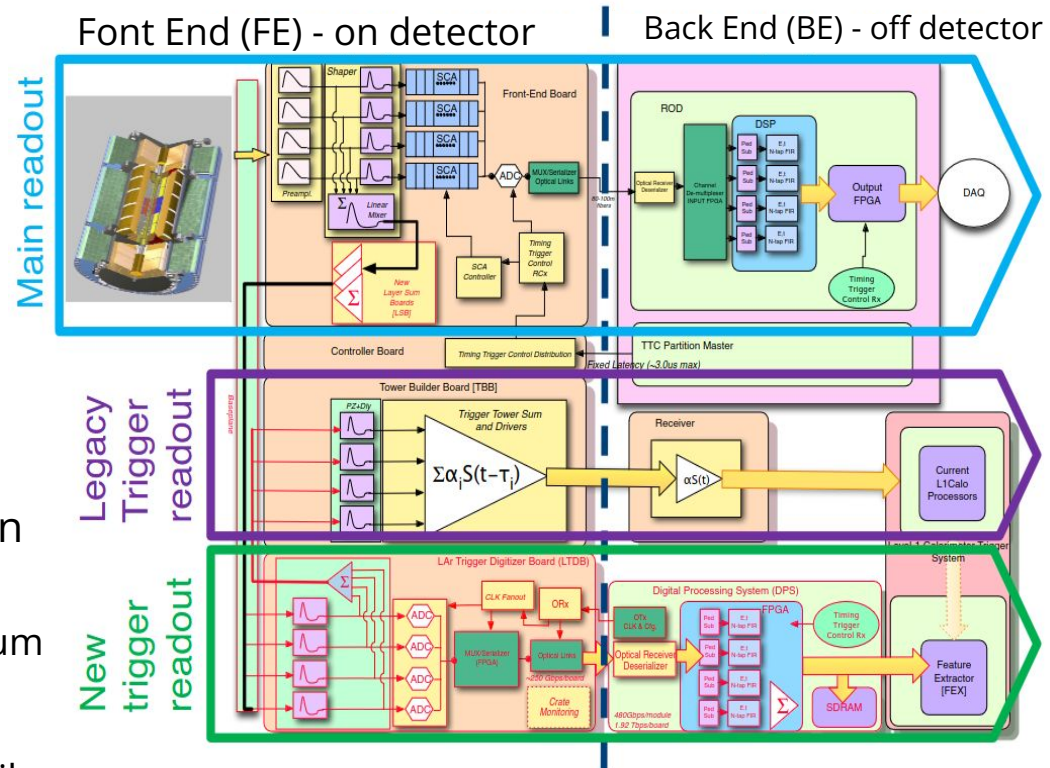
LAr readout

Paths existed during Run 1 & Run 2

- Main readout
 - Record only upon trigger accept
 - Readout of **~180000** Cells
- Analog trigger path
 - Sum channel analogically
 - Uses **~4000** Trigger Towers

Paths during Run 3

- Main readout and analog trigger remain
- Digital trigger path
 - Digital signal from **~34000** Super Cells sum
 - Computes energy for trigger decision
 - Sum signal into trigger tower
 - Trigger decision with analog trigger until end of commissioning

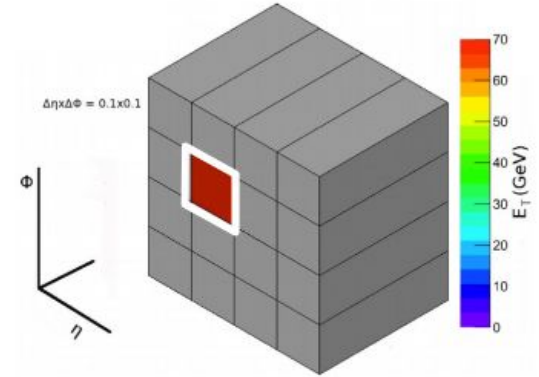


LAr Phase-I upgrade

During Run 1 and Run 2 **Trigger Towers (TT)** were transmitted to Level-1 trigger

- Analog signal
- No longitudinal segmentation
- ~4000 TT from ~180000 Cells
- Fixed size in $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$

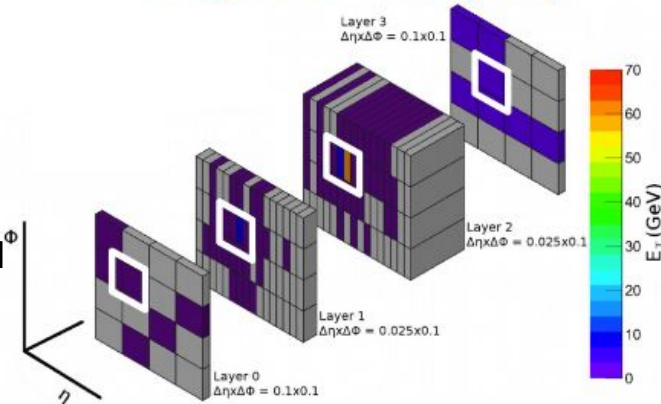
Trigger Towers (TT)



For Run 3 **Super Cells (SC)** energies are sent to Level-1 trigger

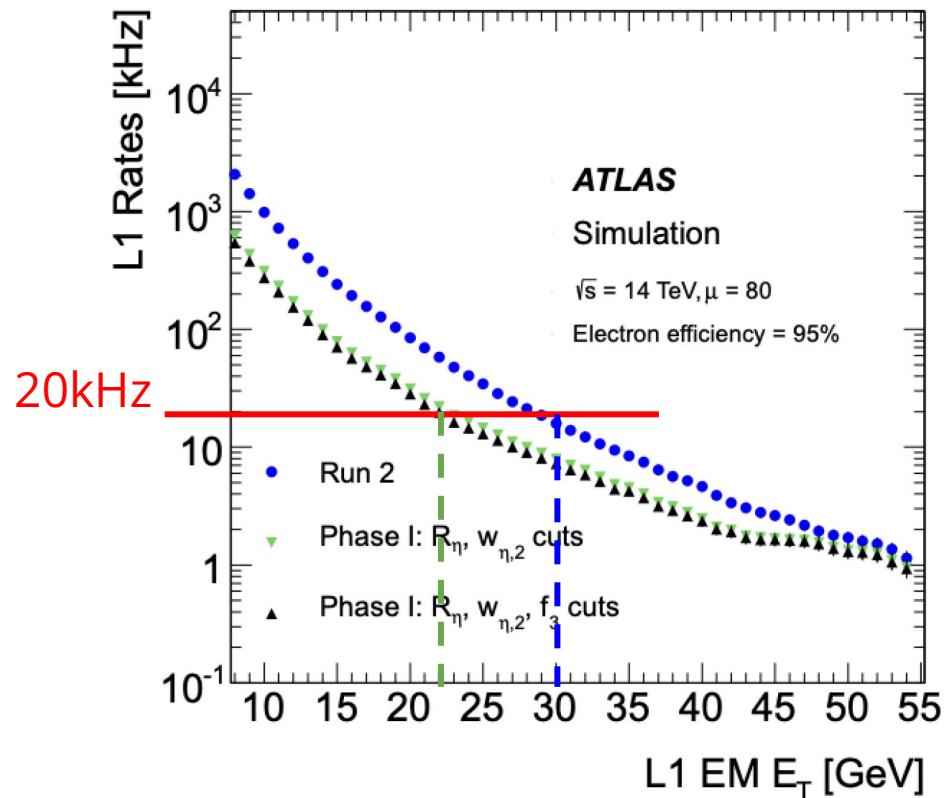
- Digital trigger
- Lateral & longitudinal segmentation
- ~ 34000 SC from ~180000 Cells
- Increased granularity in Front and Middle to $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$
- Increase the precision of the energy measurement (from 10b ADCs to 12b ADCs)

Super Cells (SC)



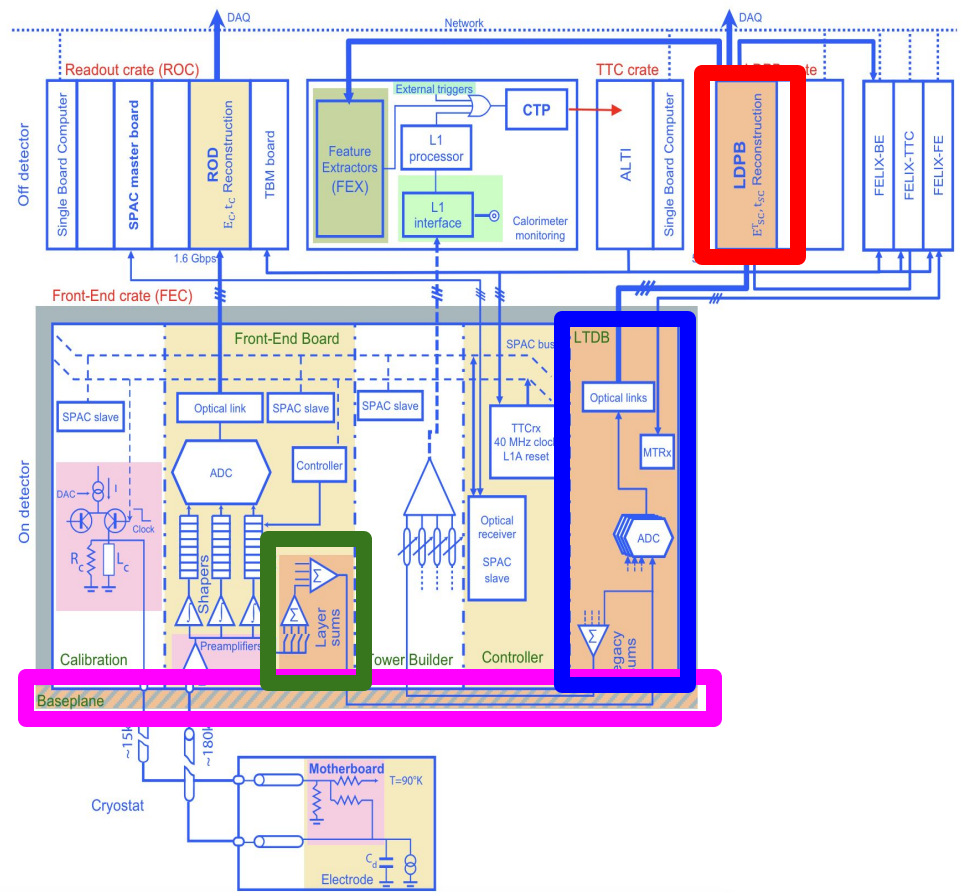
Need a new trigger

- Impossible to record more data
 - Hardware limitation
 - 100kHz for the L1 trigger
- Do a better selection
 - Require a new trigger system
- Simulation of events detect by the electromagnetic trigger (20kHz)
 - With Run 2 trigger → ET cut at **30 GeV**
 - With Run 3 trigger → ET cut at **22 GeV**
- Better selection
 - Significantly increase the scope of research



New LAr electronics for Phase-I

- Layer Sum Board (LSB)
 - Modify summation of cell signals
- Baseplane
 - Re-route SCs signal
- LAr Trigger Digitizer Board (LTDB)
 - Digitize analog signals
 - Send digital signals to the LATOMEs
 - 124 LTDBs are installed
 - **5848** fibers (data and control)
- LAr Trigger prOcessing MEzzanine (LATOME)
 - Receives ADC counts from LTDB
 - Computes energy and pulse timing
 - Sends energy to Feature Extractors
 - 116 LATOMEs are installed
 - **4960** fibers



Phase-I electronic cabling

FELIX LTDB machine (8 in total):

- 3 servers for implementation :
 - **Timing**
 - **Control**
 - **Monitoring**
- 2 FLX-712 board (FPGA)
 - 1 for barrel LTDBs
 - 1 for EMEC, HEC, and FCal LTDBs

Wendy box:

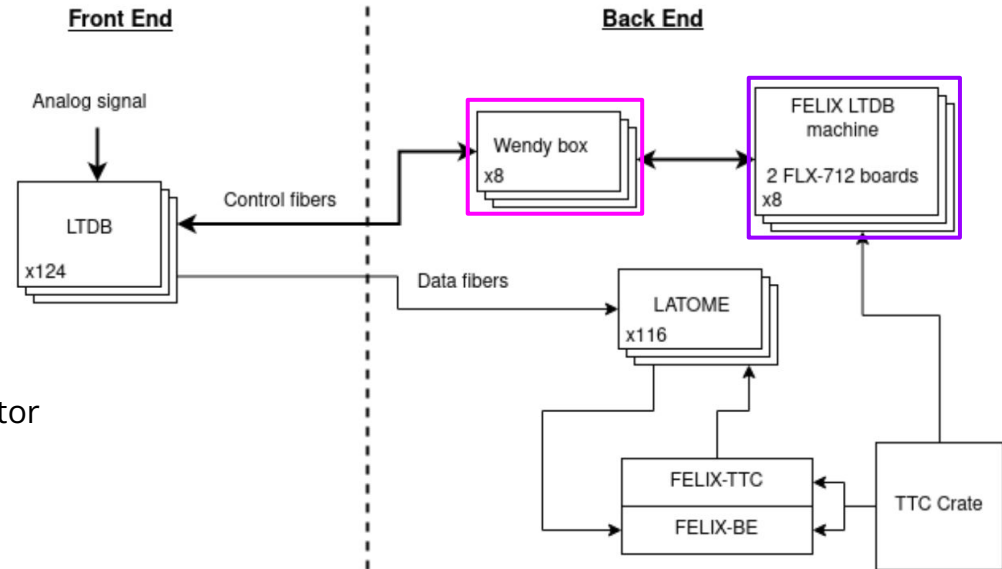
- Map the fiber coming from the LTDB to the FELIX
 - 12 channels connector to a 48 channels connector

Control path:

ATLAS clock → FELIX LTDB ↔ Wendy box ↔ LTDB

Data path:

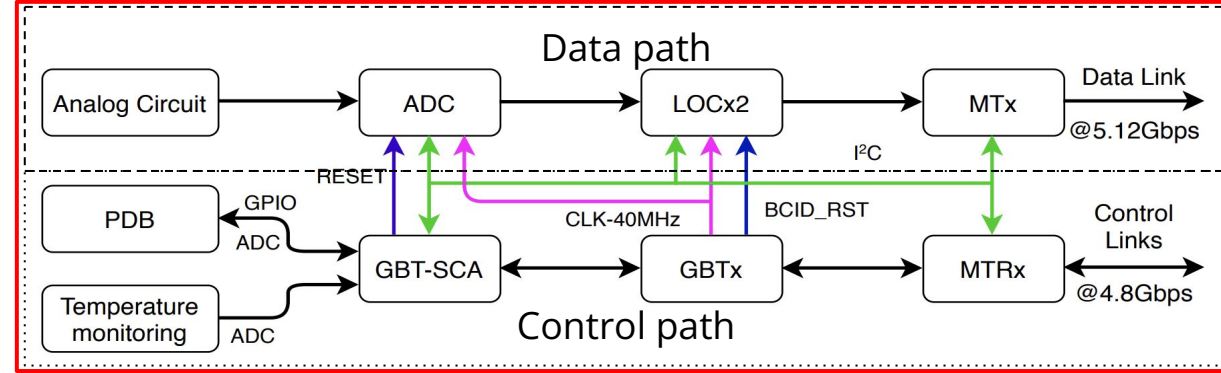
Analog Signal → LTDB → LATOME → L1 trigger



LTDB description

Five identical segments

- 1 control path
- 4 data path

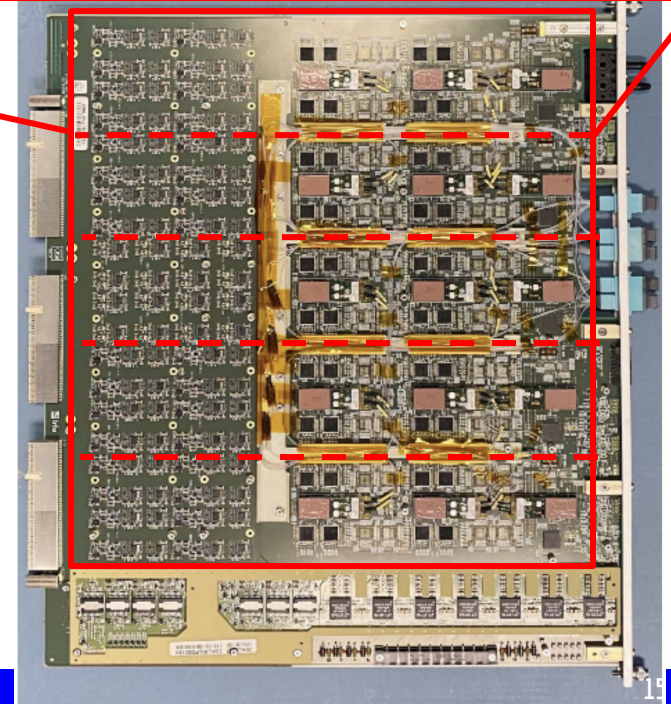


Control path:

- **Miniature Transceiver (MTRx)** optical transceiver for information between the LTDB and the FELIX LTDB
- **GBTx** decode/encode the frame
 - Propagate the clock signal to the LOCx2s and ADCs
- **Slow Control Adapter (GBT-SCA)** will receive information from a custom server to configure the LTDBs
 - Propagate command via I2C bus to the ADCs, LOCx2s, MTxs, and MTRxs

Data path:

- **Analog-to-digital converter (ADCs)** will digitize the signals from the detector
- **LOCx2** receives the serialized ADC data, encodes the digital signal
- **Miniature Transmitter (MTx)** optical transmitter send data to the LATOME



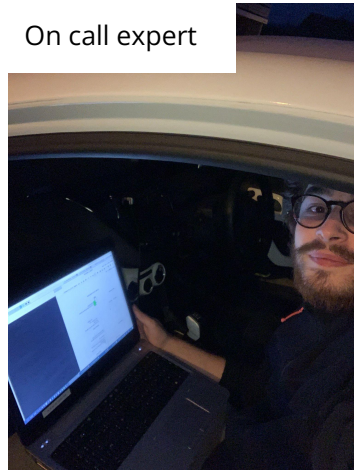
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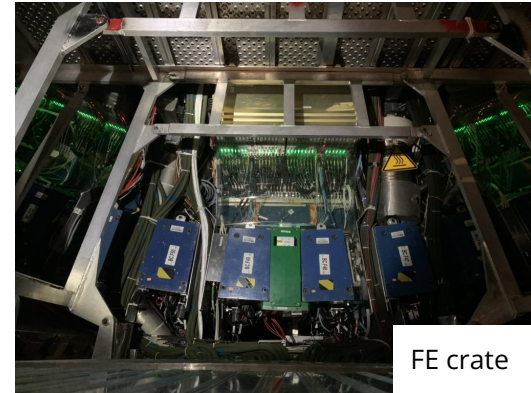
Cleaning of ATLAS cavern



On call expert



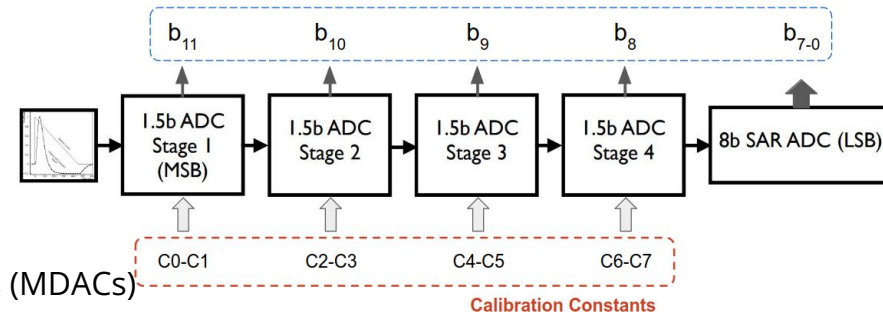
Official start of Run 3



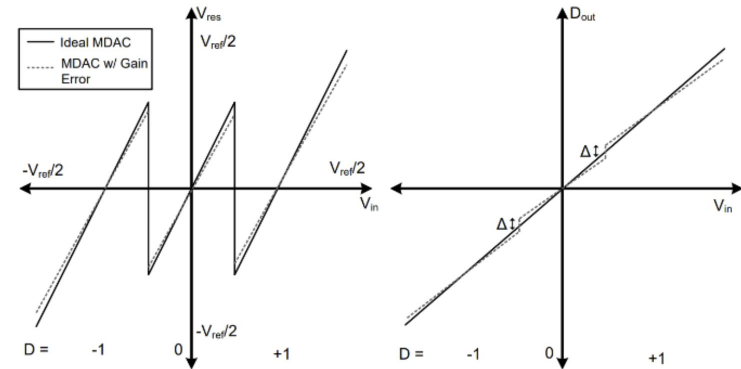
FE crate

Cabling LTDBs control & data fibers

LTDB ADC calibration



- Nevis ADC is a pipeline 12b ADC at 40MHz
 - 4 stage of 1.5 bit Multiplying Digital-to-Analogue Converters (MDACs)
 - 8 bit Successive Approximation Registers (SAR) ADC
- Each MDAC stage will give reference voltage to build the adc response curve
- Constants can be apply to correct the gain error
 - Capacitors at the input and the output of this amplifier
 - Capacitor precision is limited by the CMOS process
- If gain diverges too much from this ideal value
 - discontinuities start to appear in the digital reconstruction

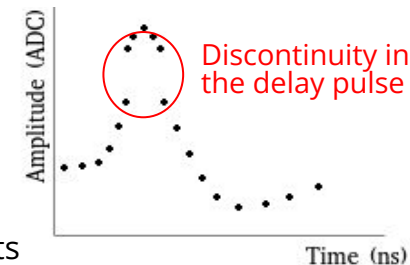


Calibration constants:

- 1st set made during the production of the ADC
- 2nd set made at the validation of the LTDB
- 3rd set made on the detector
- 4th set tuned on the basis of the previous set
 - Fix all ADCs issue related to calibration constants

My contribution:

- I developed a mapping software
 - To identify ADC channel to SC
 - Fix almost all the wrong constants (20 bad channels out of 34048 channels)



LTDB phase selection

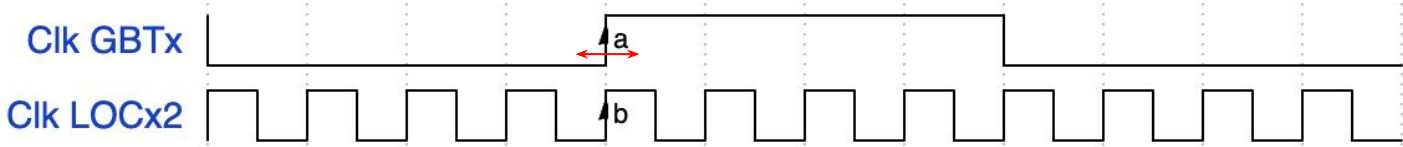
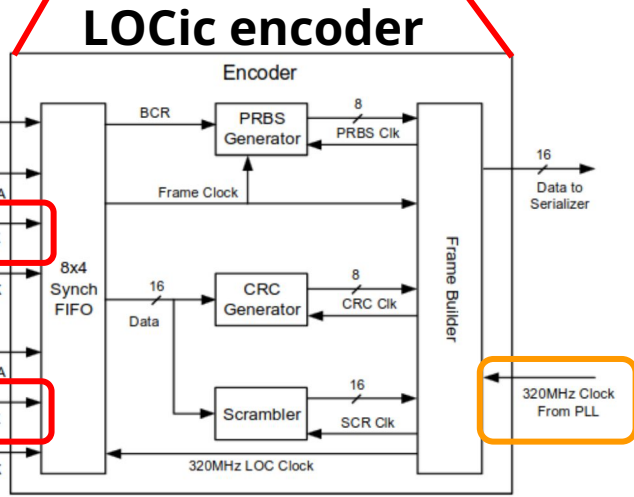
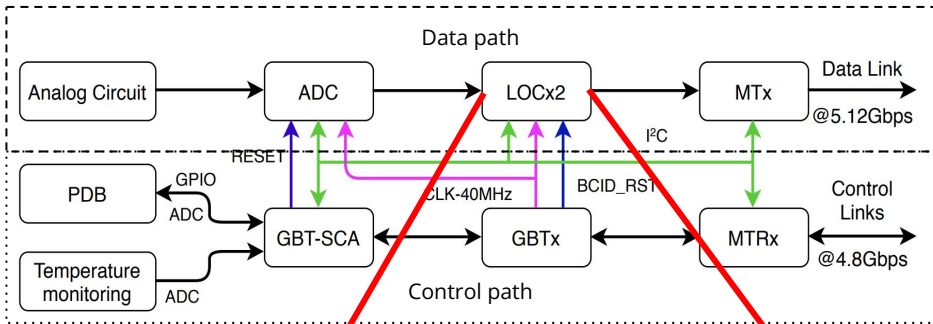
For a proper encoding of the LOCic frame

- Clk from PLL (320MHz) and GBTx clk (40MHz) should not be in phase

Develop a calibration to choose the delay between the 2 phases

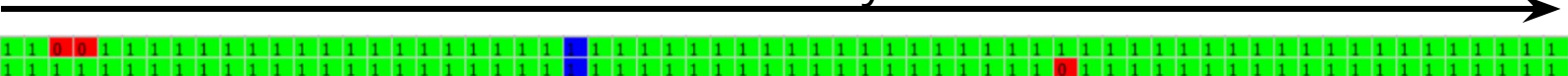
Calibration will induces a delay on the phase of the GBTx clock

Need to be done after each power cycle



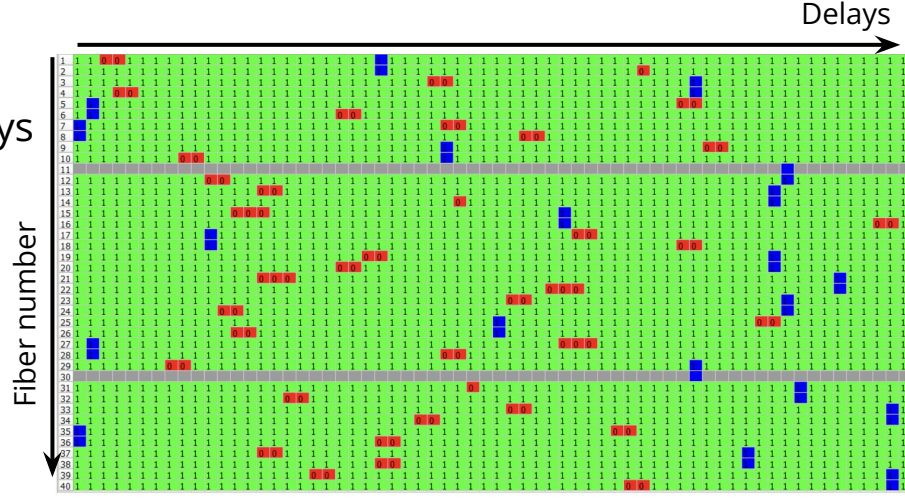
Calibration LTDB phase selection

64 delays



Fibers 1&2

- Works per pair of fibers (1 LOCx2)
- 64 delays in total
- Each delay is scan for the 40 fibers
 - Check the number of errors received by the LATOME
 - If errors → delay is tagged as **bad**
 - If no errors → delay is tagged as **good**
 - **Final delay** is chosen farthest from bad delays



Found not stable

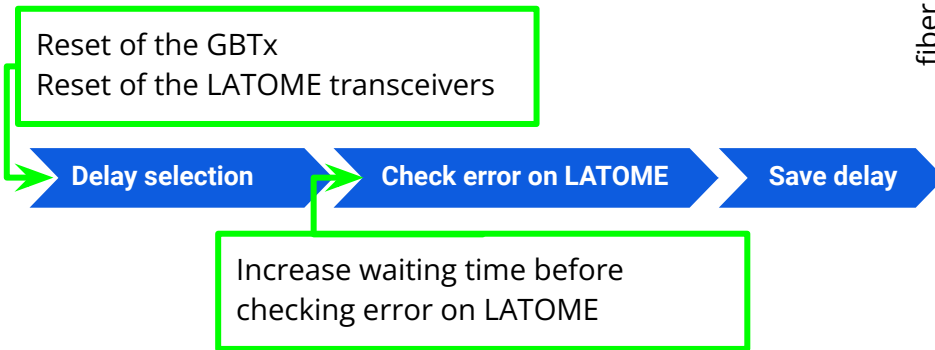
- Need to be done frequently (~1/week)
- Not practical during data taking period

LTDB phase selection

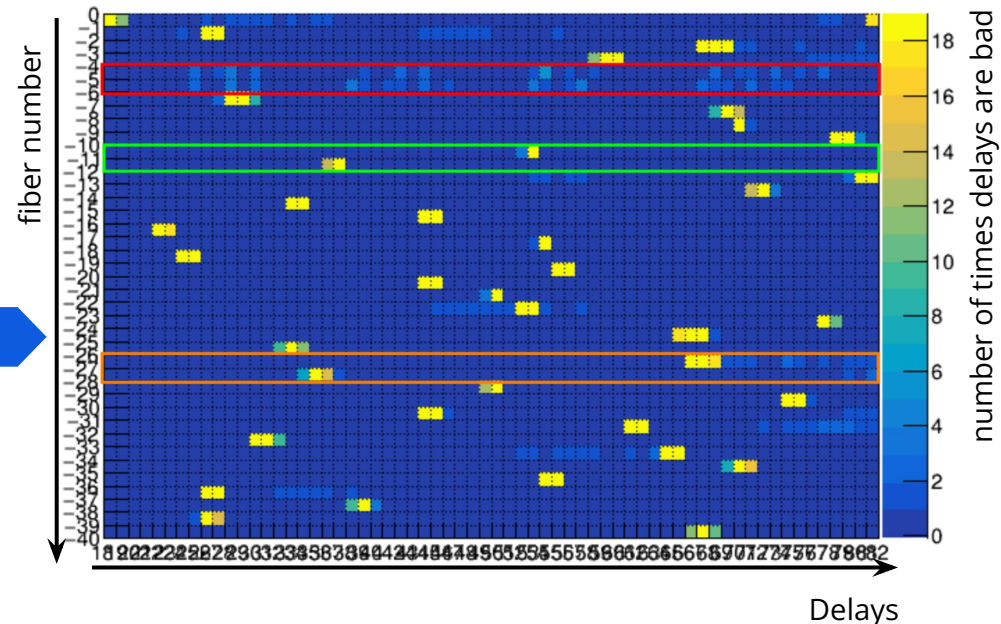
Stacking ClkDes scan of one LTDB during 2022 runs illustrating the evolution of the error rate over time and revealed three patterns:

- **Most** of the fibers are stable
 - **Pattern** with only one area of bad delays
- **Pattern** with a lot of bad delays

Solution found to make it stable:



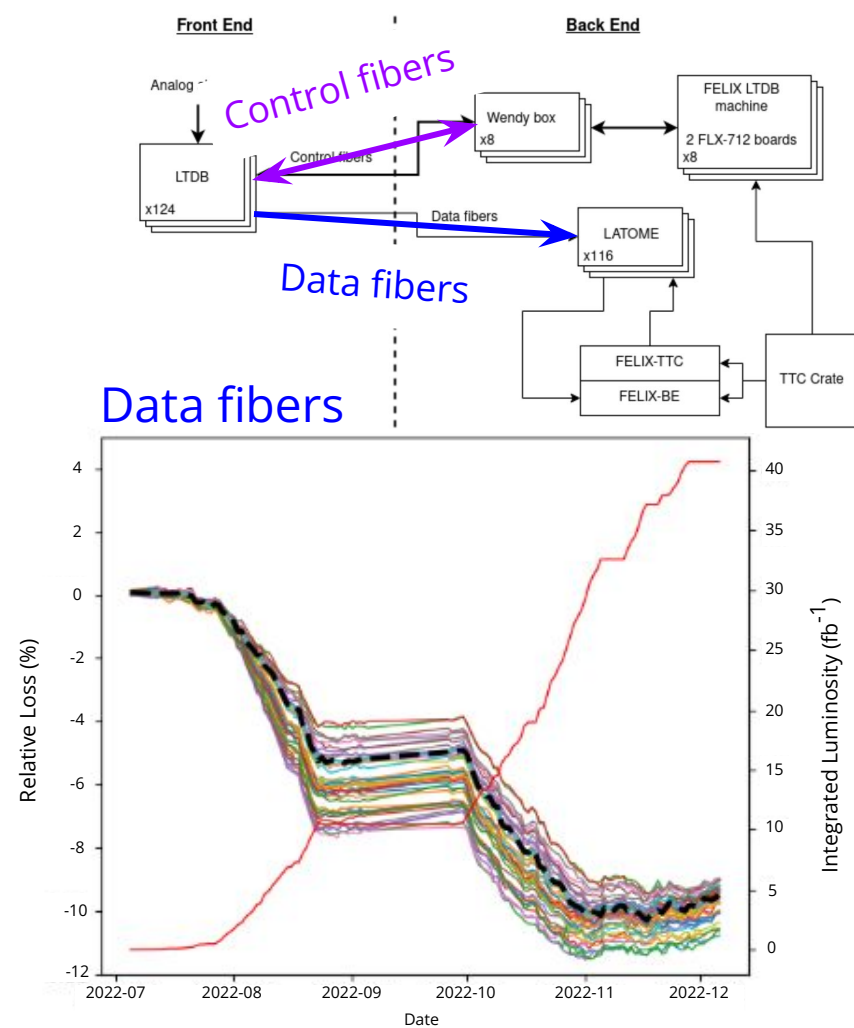
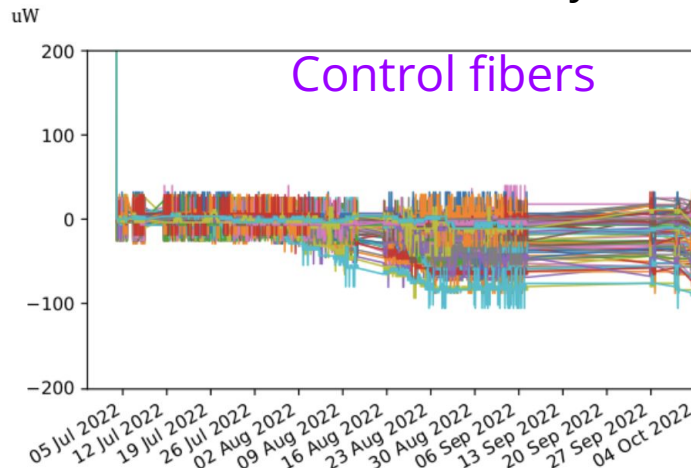
Stable after the implementation of these solutions
Performed only once after the FE power cycle



Loss of light optical power

During 2022 data-taking

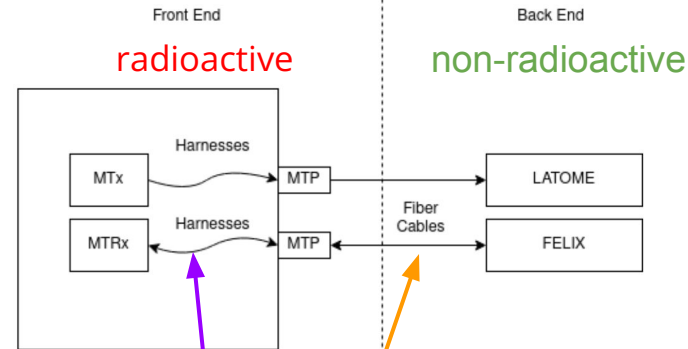
- Most fibers show a **10%** loss of light power
- Seen on **control** and **data** fibers
- Phenomenon observed on EMB (barrel)
- Slight effect on end cap
- Correlated with LHC luminosity



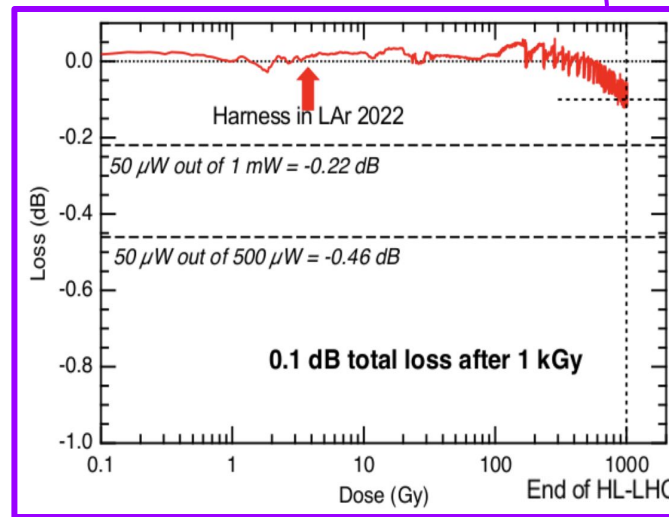
Loss of light optical power

This loss could come from :

- Fiber harnesses inside the LTDB
- Fiber between LTDB and off detector electronics
- MTx
- MTRx



Harness radiation test



Fiber radiation test

Before		After	
dBm	uW	dBm	uW
7,22	5272	7,22	5272
8,93	7816	9,15	8222
7,39	5483	7,63	5794
10,77	11940	10,52	11272
9,09	8110	9,28	8472
6,93	4932	7,51	5636
10,17	10399	10,29	10691
11,2	13183	10,85	12162
7,33	5408	6,9	4898
10,97	12503	10,92	12359
10	10000	9,88	9727
11,85	15311	11,82	15205

Harnesses/Fibers:

- **No phosphor** found
- Irradiated parasitically at Co60
 - **-0.1dB/kGy** on the harness
 - **no effect** seen on fibers after receiving a dose $\sim 25\text{Gy}$

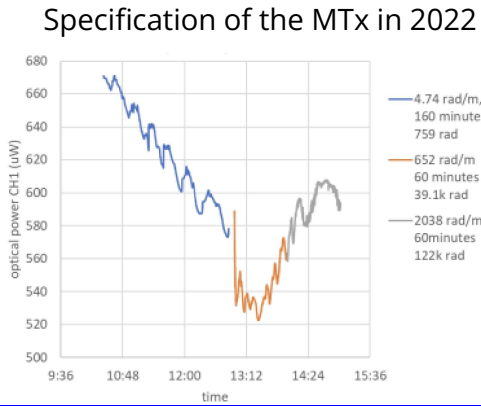
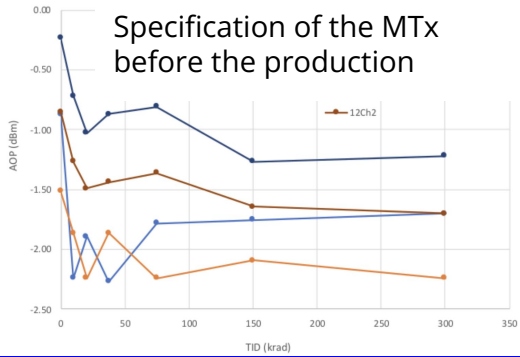
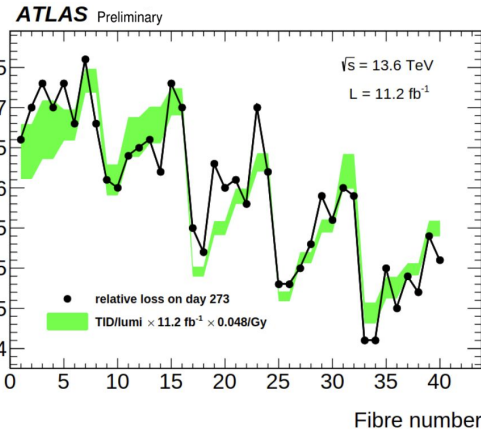
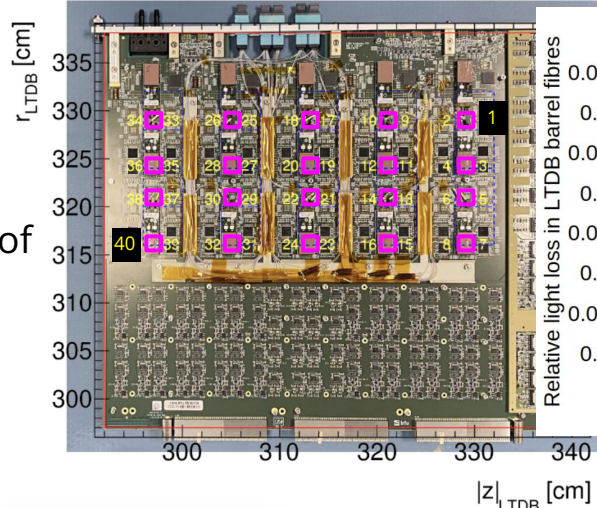
Fiber and harness out of the picture

Loss of light optical power

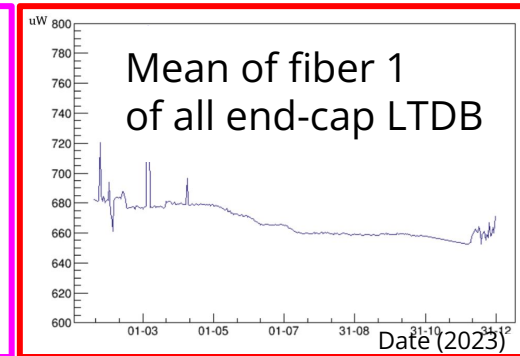
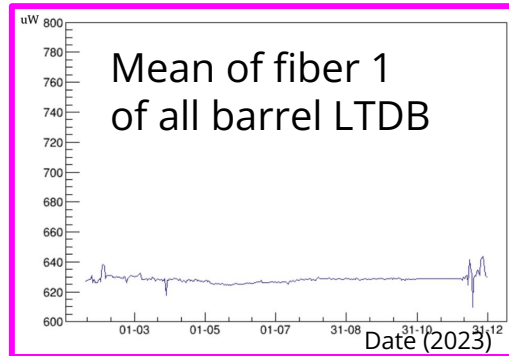
MTx Fiber number

MTx (optical transmitter):

- Measurement of the radiation in function of the MTx position
 - Effect of radiation differs according to position
- Specification of the MTx show:
 - Decrease in light power
 - Stabilization after a high dose of radiation
- Corresponds to the effect observed on the system



Loss of light optical power



This year of data taking

- The **Barrel fibers** are stable
- Effect observed on the **End Cap fibers**
 - Slower decrease due to less radiation

No actions taken:

- Improve the monitoring of those lights
- Setting optical power alarms



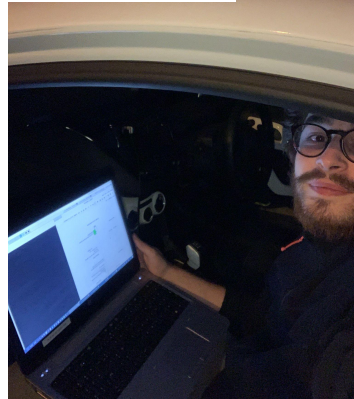
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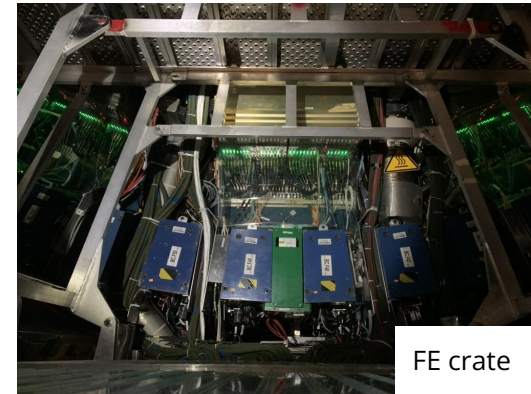
Cleaning of ATLAS cavern



On call expert



Official start of Run 3



FE crate

Cabling LTDBs control & data fibers

Introduction timing shift

Current energy reconstruction uses the Optimal Filtering algorithm (OFC)

- Energy reconstruction from amplitude
- Timing τ from pulse phase changes

$$E_T = \sum_{i=0}^3 A_i (S_i - p - b)$$

$$E_T \tau = \sum_{i=0}^3 B_i (S_i - p - b)$$

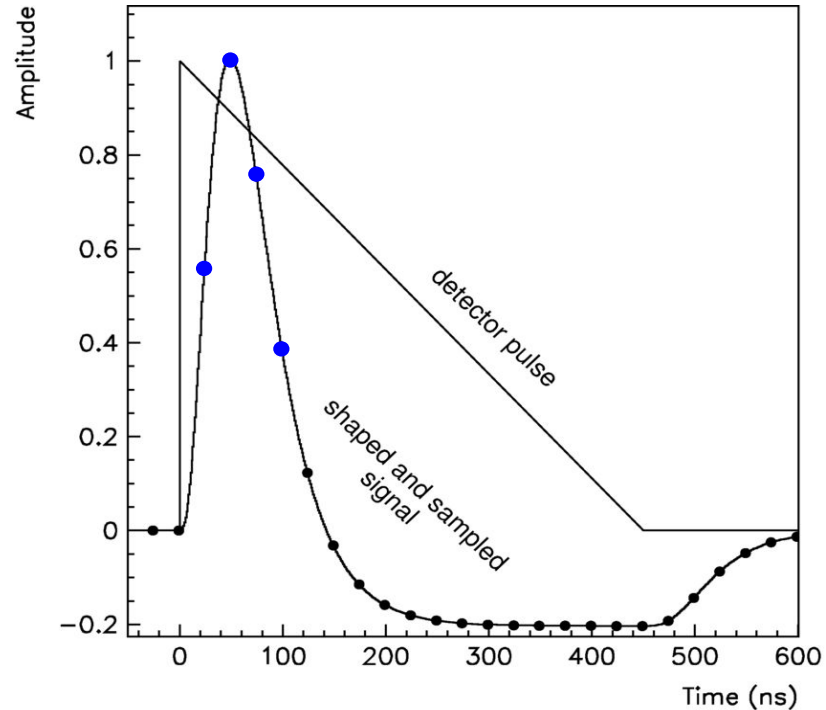
A_i Coefficients for energy reconstruction

S_i Sampled signal

B_i Coefficients for timing

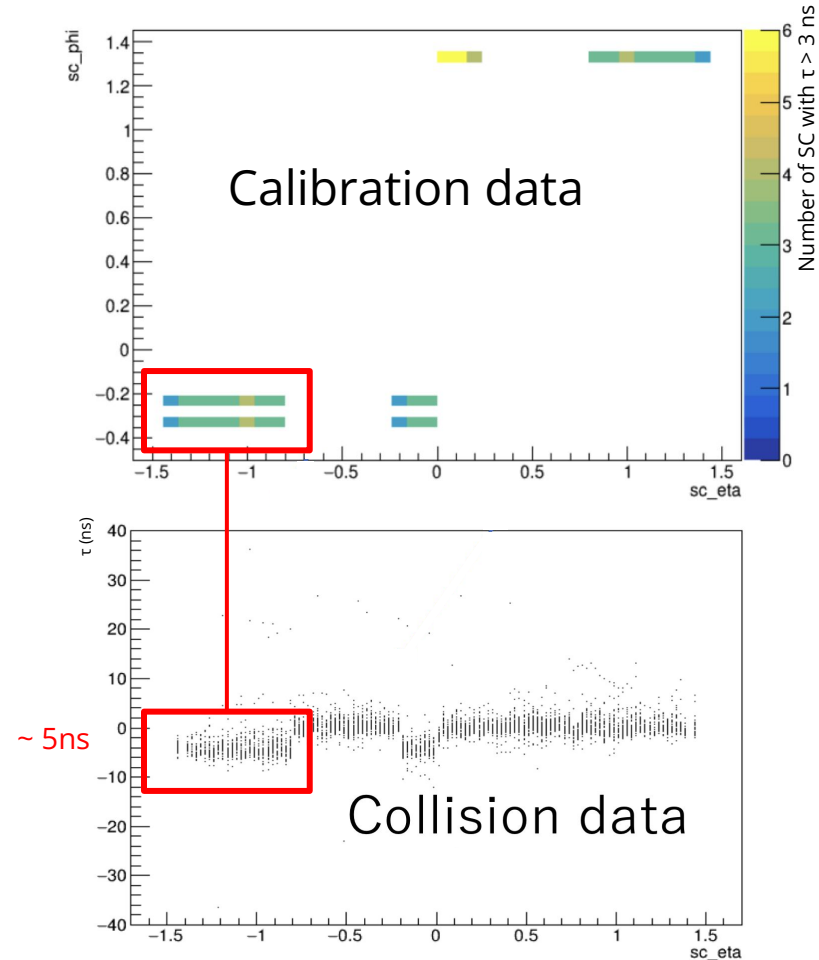
p Pedestal level

b Baseline correction



Introduction timing shift

- After computation of the OFC for all SCs
 - Reference pulse is known for each SC
 - $\tau = 0$ ns \rightarrow max amplitude of the ADC pulse \rightarrow Optimal energy
 - $\tau \neq 0$ ns \rightarrow pulse amplitude is smaller \rightarrow Transmitted energy not optimal
- Issue observed in some region of the detector during:
 - Collision data
 - Calibration data
- Identify the source of the problem
- Quantify the loss in performance caused by this timing shift



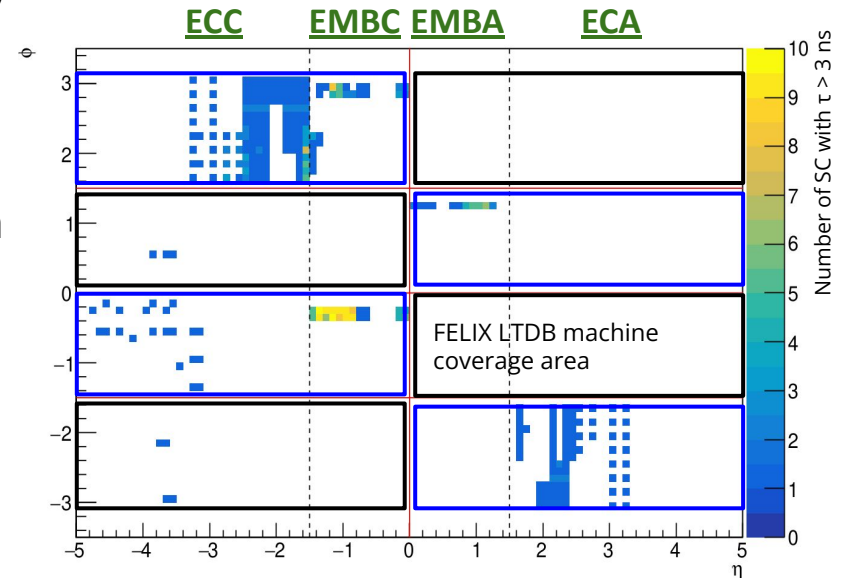
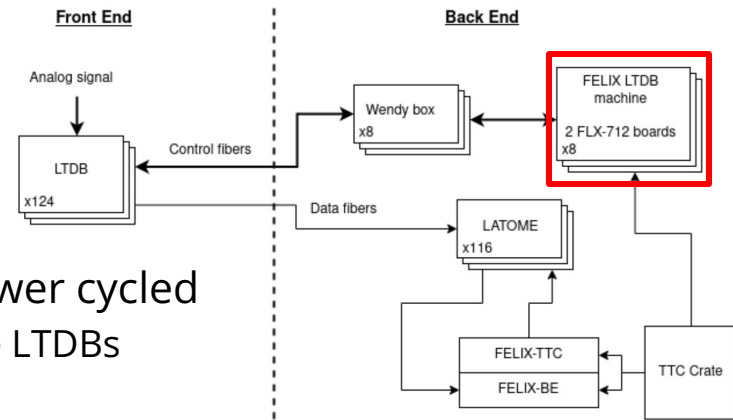
Identify the source

- Timing shift occurs when FELIX LTDB machines are power cycled
 - Used to provide clock signal, configure and monitor the LTDBs
 - 2 FLX-712 board
 - 3 servers (FeliCore, OpcUaSca and OpcUaLarLtdb)

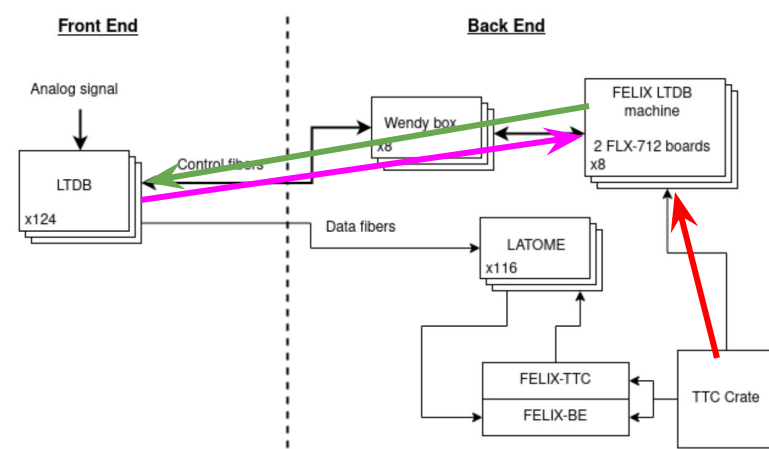
Procedure used:

- Chess pattern used to power cycle machine
- Calibration run → power cycle → calibration run
- Subtraction of timing of the 2 calibration runs

FELIX LTDBs in blue are power-cycled timing shift appears
For the other 4 machines the timing is stable

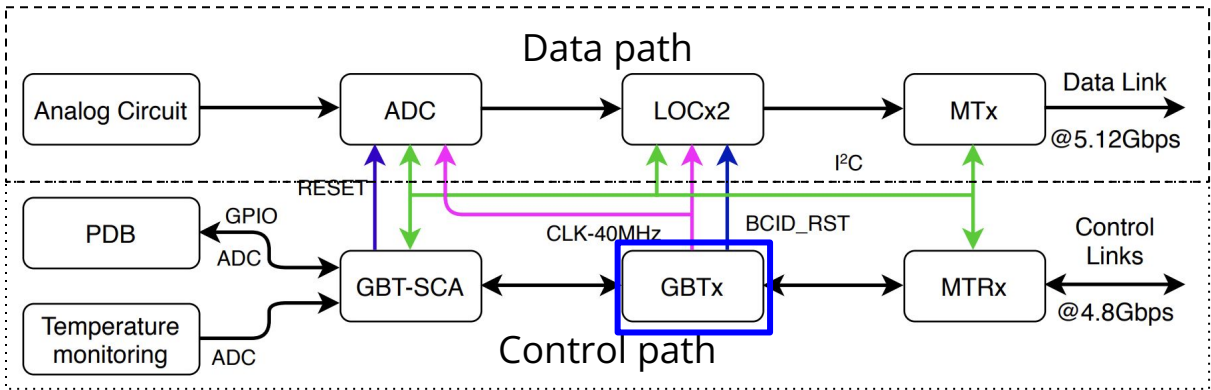


Two hypotheses



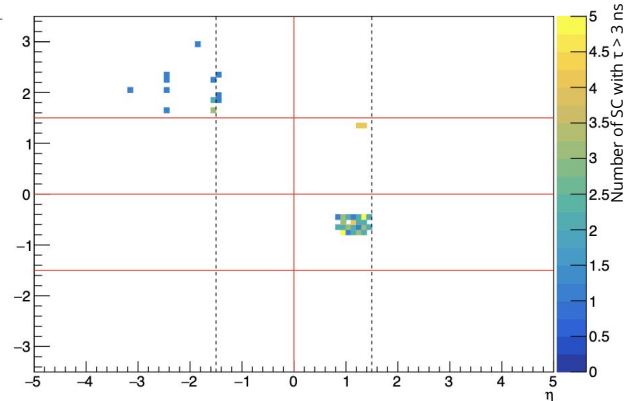
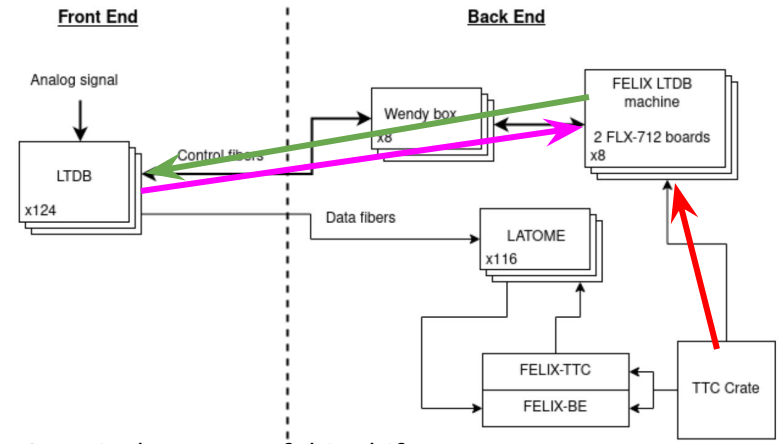
Issue is located on the **LTDB** side or on the **FELIX** side

- **LTDB**
 - Issue on the receiver of the control fibers
 - Issue on the GBTx component
- **FELIX LTDB**
 - Issue of losing the clock signal
 - Issue on the transceiver on the FELIX boards

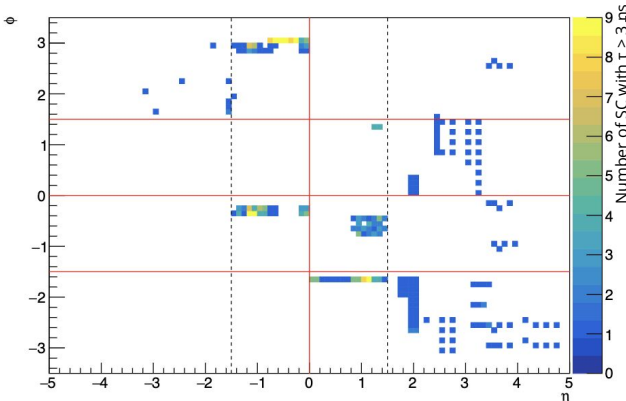


First investigation

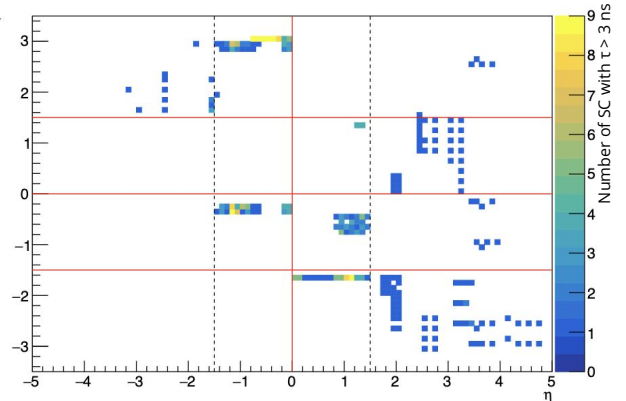
- Turning OFF/ON the **LTDB control signal (LTDB transceiver)**
 - **Does not introduce the timing shift**
- Turning OFF/ON the **LTDB control signal (FELIX transceiver)**
 - **Does not introduce the timing shift**
- Turning OFF/ON the **clock signal (TTC)**
 - **Does not introduce the timing shift**
- Reset of the GBTx
 - If resetting the GBTx after a power cycle clear the timing shift mean the GBTx is the cause of this shift
 - If not it probably on the FELIX side
 - **Does not introduce the timing shift**
 - **Does not fix the problem**



GBTx reset



Power cycle FELIX LTDB

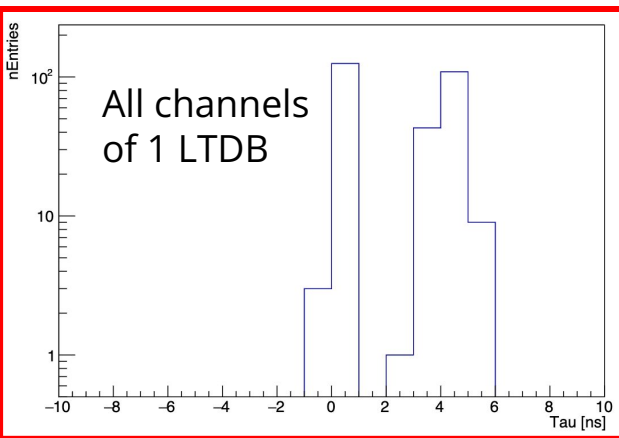
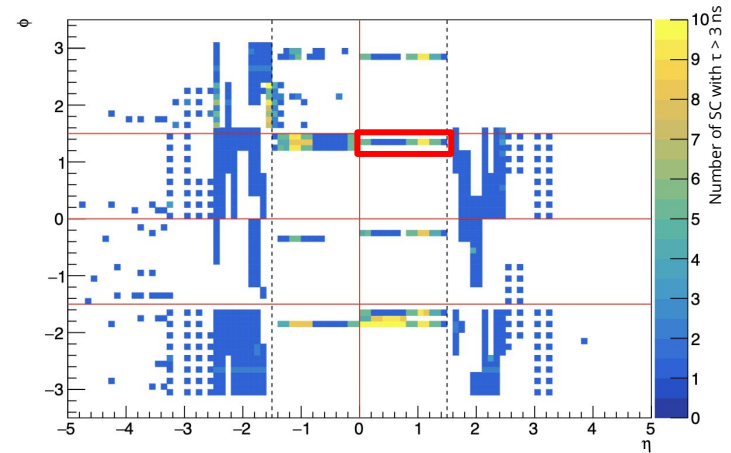


GBTx reset

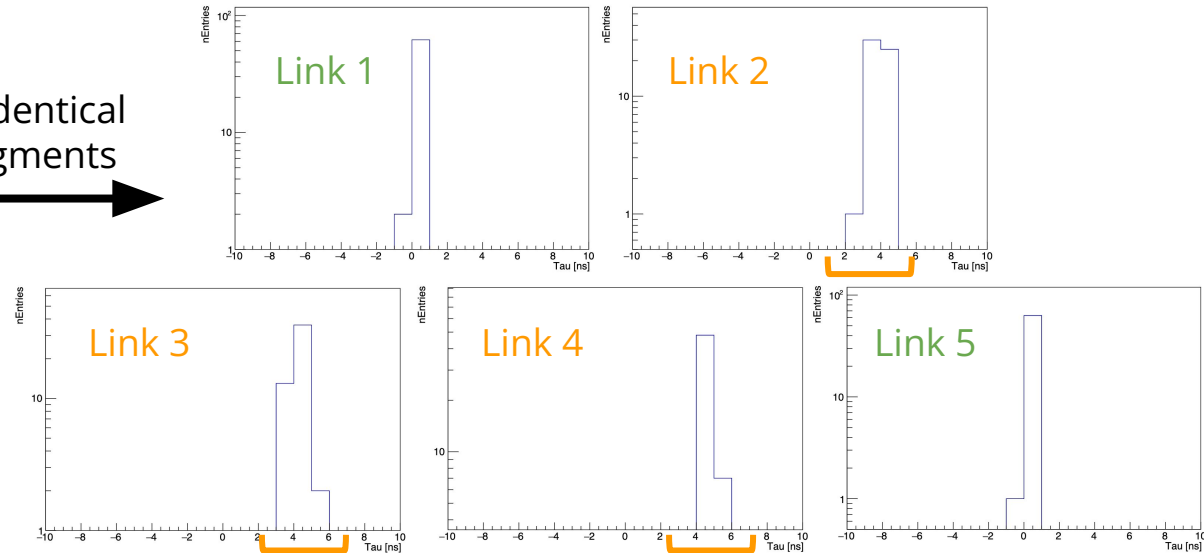
Pattern found

SCs impacted by the power cycle always seems to be the same

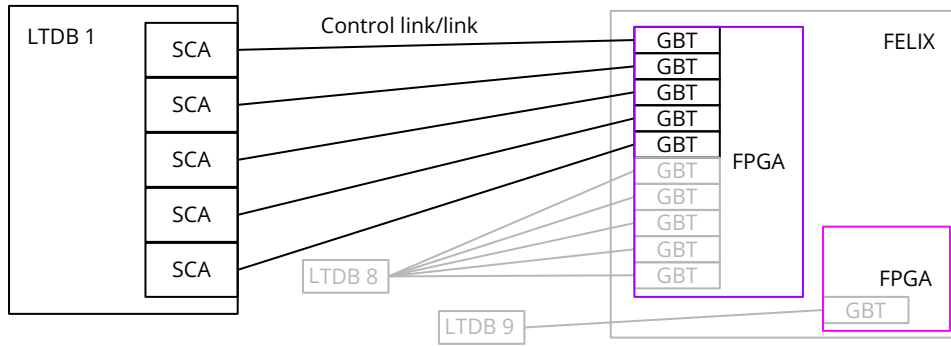
- Timing is stable if no power cycle made
- Timing shift of the order of $\pm 5\text{ns}$
- Appears within an LTDB, but not on the entire LTDB
 - All channels shift in the same way for the same link



5 identical segments



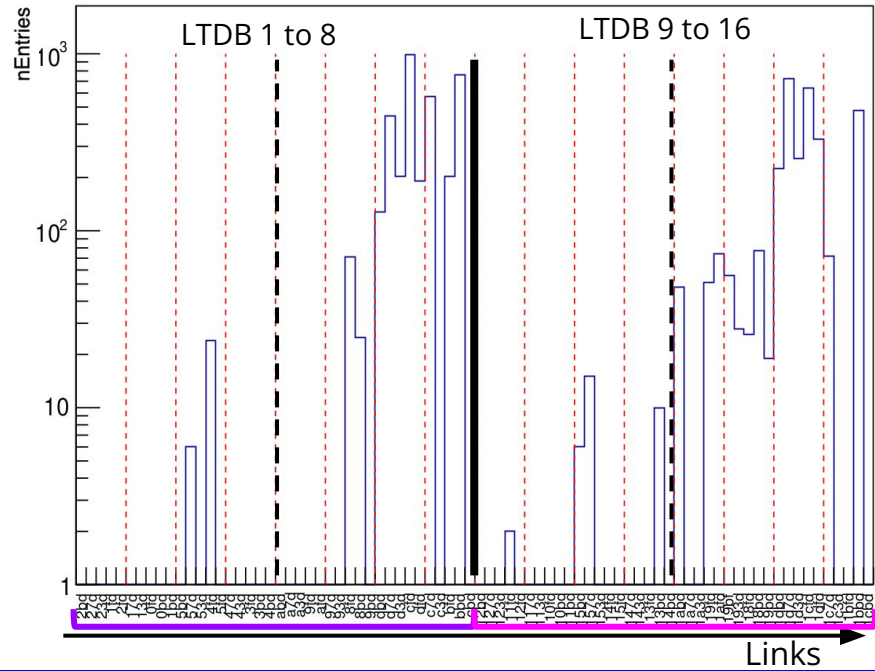
Pattern found



1 LTDB → 5 control links → 5 links

- Control link is bidirectional link between LTDB and the FPGA of the FELIX board
- Mapping made between the SCs and links
- Distribution of timing shift per link for the 8 FELIX LTDB over 12 calibration runs
- power cycle of all FELIX LTDB

- Timing shift appear mainly on the link of the LTDB connected to the last group of GBT of FELIX-712 board



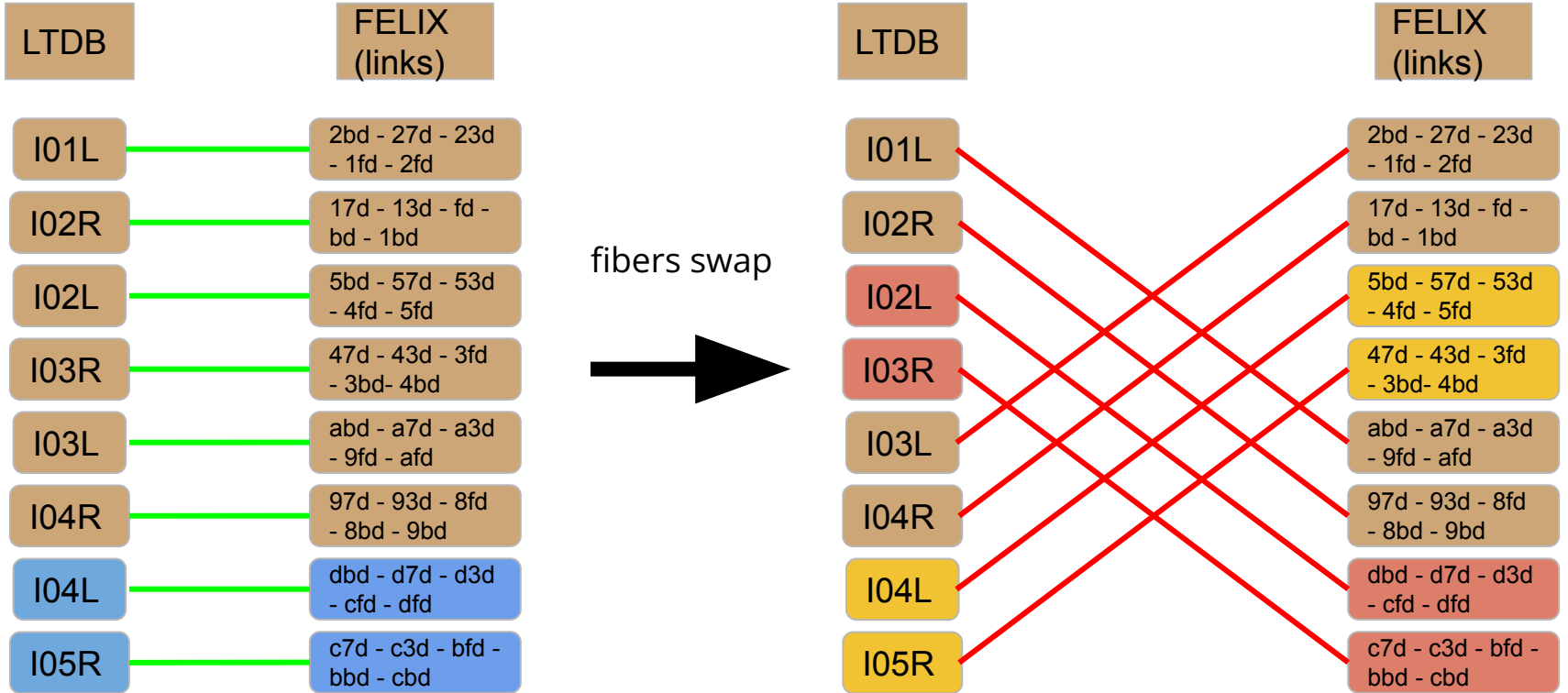
LTDB or FELIX issue ?

FELIX LTDB swap fibers

— Standard cabling
— Swap cabling

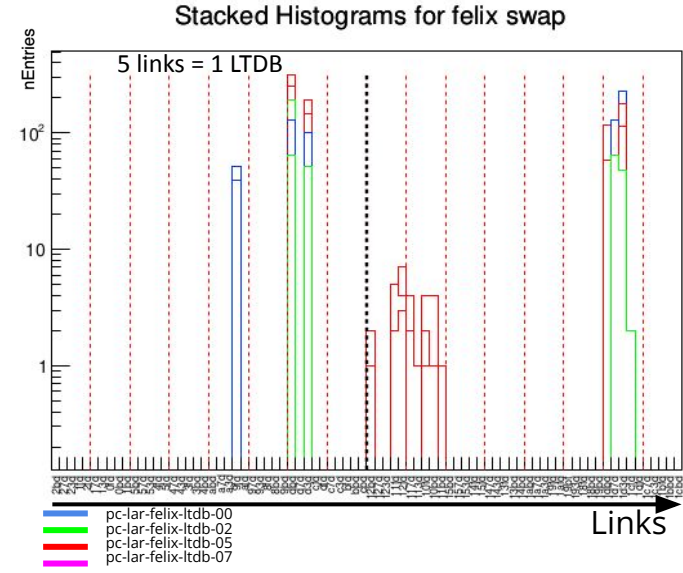
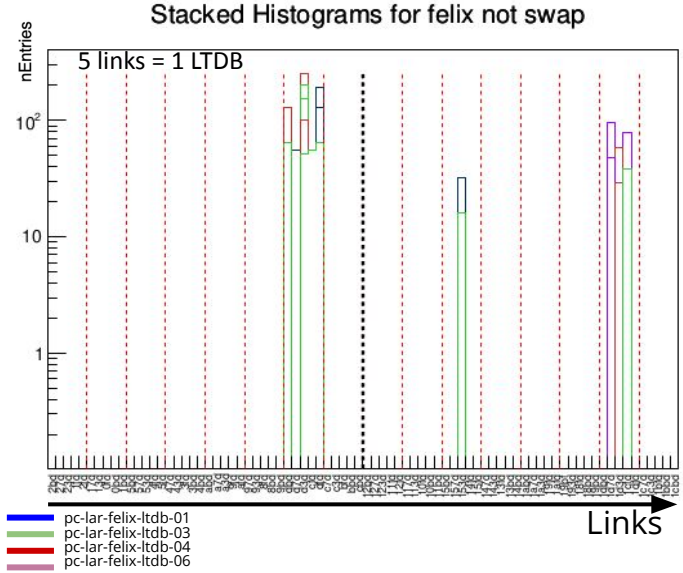
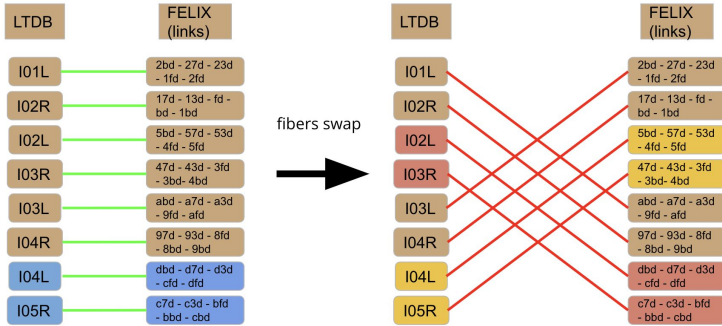
Observed timing shift
 Timing shift if LTDB problem
 Timing shift if FELIX problem

Example for half a FELIX LTDB machine



FELIX LTDB swap fibers

- 4 FELIX LTDB were swapped
- Distribution of timing shift per link for the 8 FELIX LTDB over 6 calibration runs
- Left plot FELIX machine not swap
- Right plot FELIX machine swap

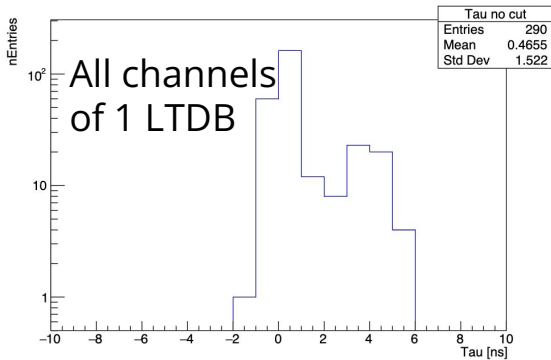
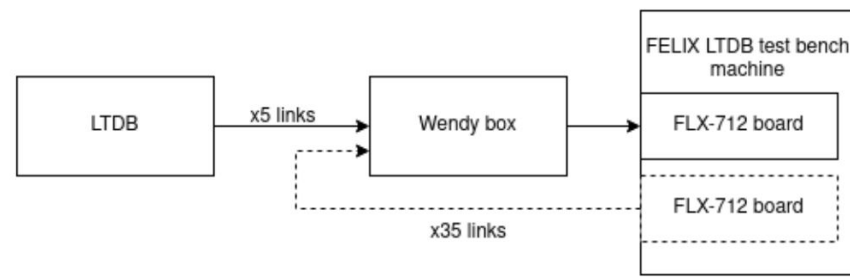


The timing shift persists on the same link despite moving the LTDBs
 Confirming that the problem originates on the FELIX side

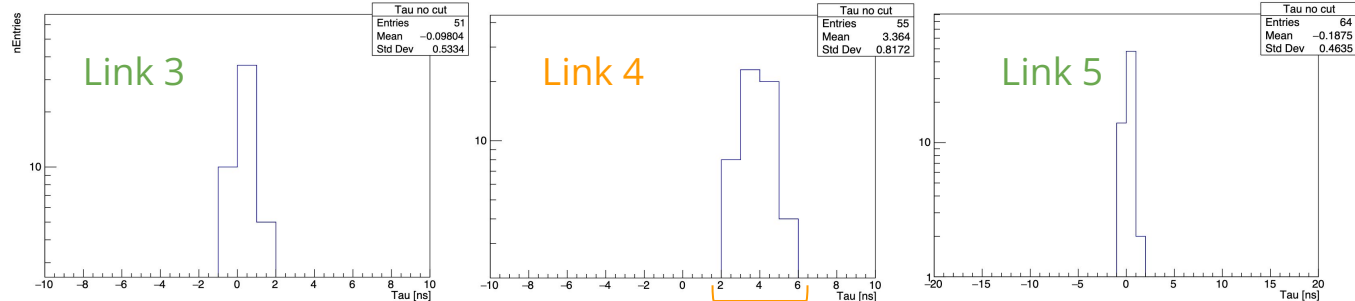
Test on testbench

Reproduce in standalone testbench

- Indication that the issue is on the FELIX side
- Investigation still ongoing with FELIX expert
 - Hardware ?
 - Software ?
 - Firmware?



5 identical segments

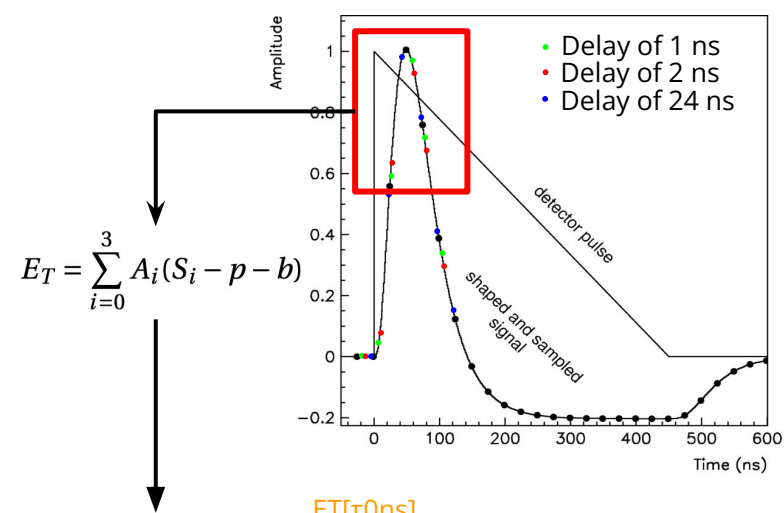


Performance evaluation

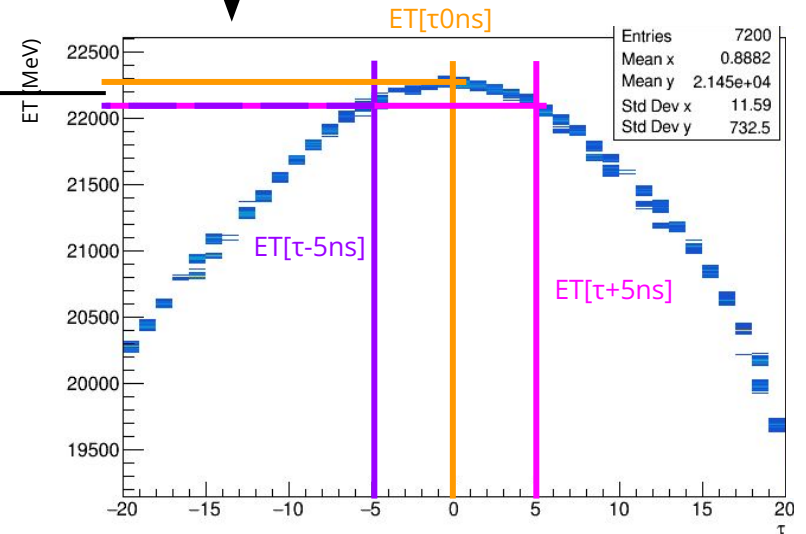
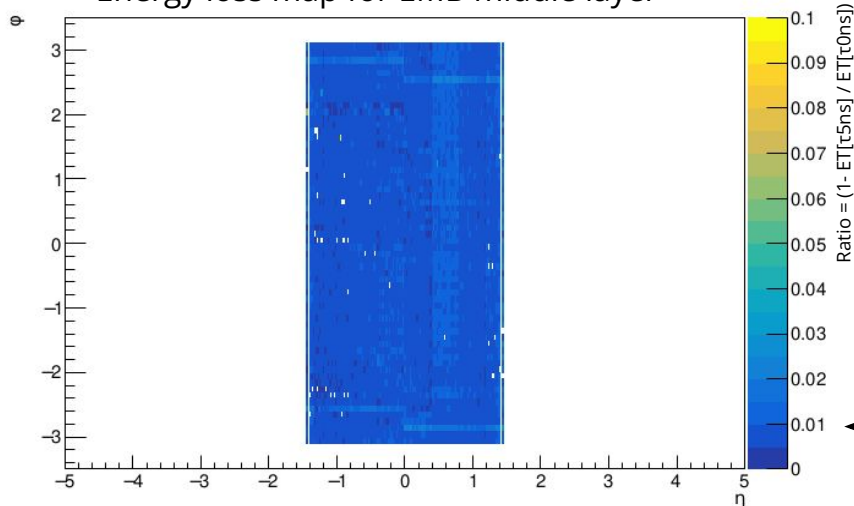
Performance of a specific calibration run:

- Pulse simultaneously on all supercells
- Then shift the 32 samples of the 1ns pulse
- Shift up to +24 ns.

This gives a complete scan of the ADC pulse from 0 ns to 25 ns



Energy loss map for EMB middle layer



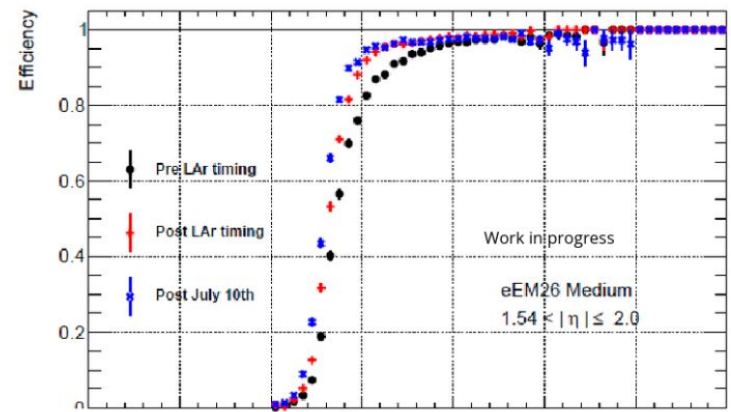
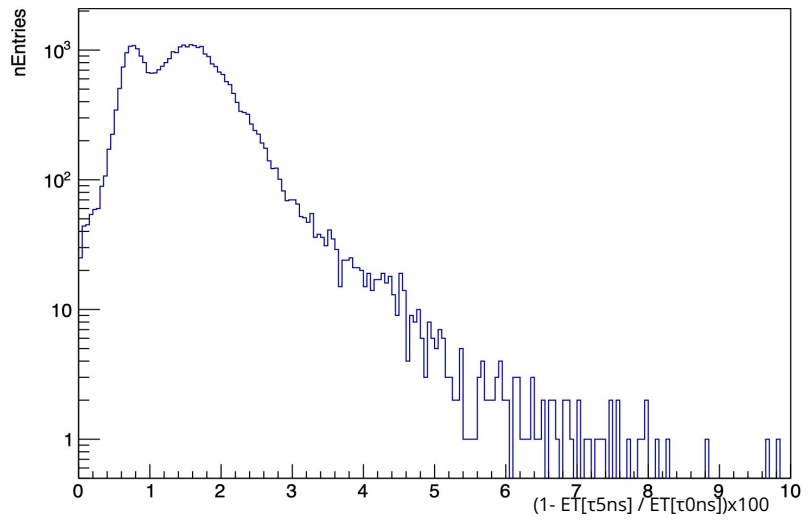
Distribution of energy loss for all SCs

Energy lost when $\tau = \pm 5\text{ns}$

- EMB \rightarrow 1%
- EMEC \rightarrow 1.5%
- HEC \rightarrow 1.1%
- FCAL \rightarrow 3.4%

Timing shift of $\pm 5\text{ns}$ has a small impact on the SCs energy reconstruction

However, much higher impact on trigger efficiency in some regions



Trigger efficiency seen by L1 trigger in the region $1.54 < |\eta| \leq 2.0$

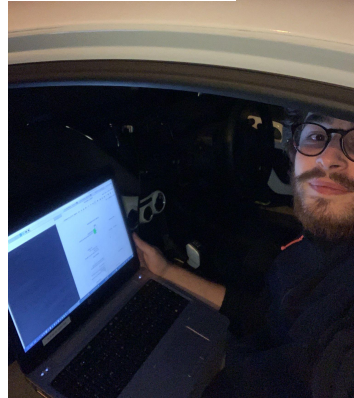
Content

1. Experimental context
2. Improve the stability of the LAr Trigger Digitizer Board
3. Timing shift
4. Digital trigger status
5. Conclusion

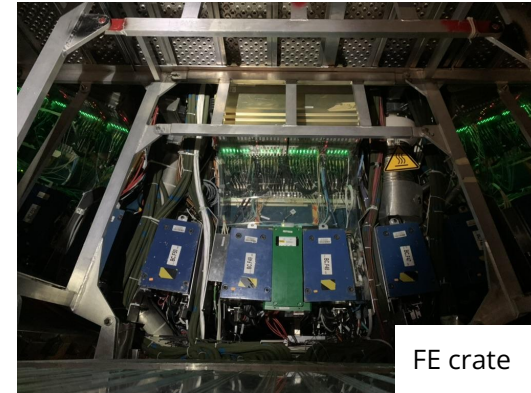
Cleaning of ATLAS cavern



On call expert



Official start of Run 3



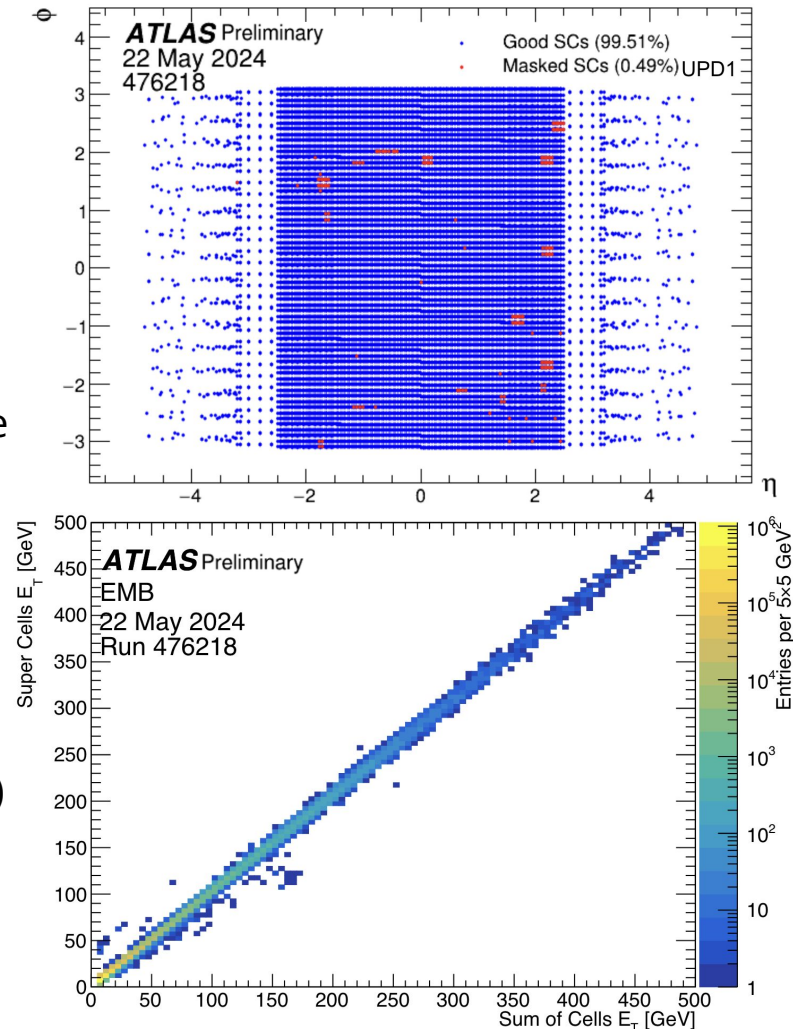
FE crate

Cabling LTDBs control & data fibers

Digital Trigger status

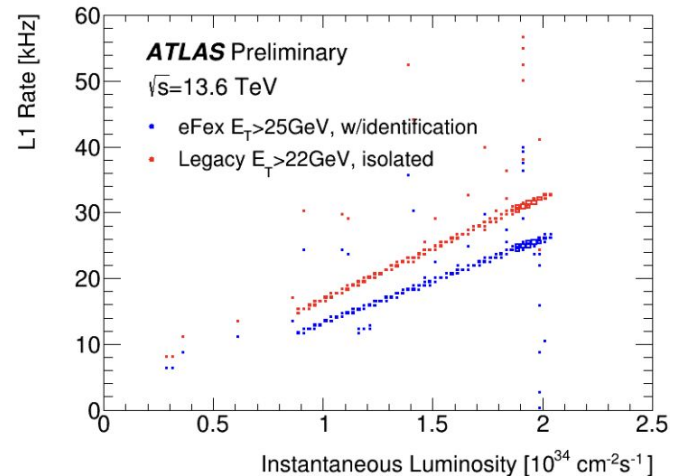
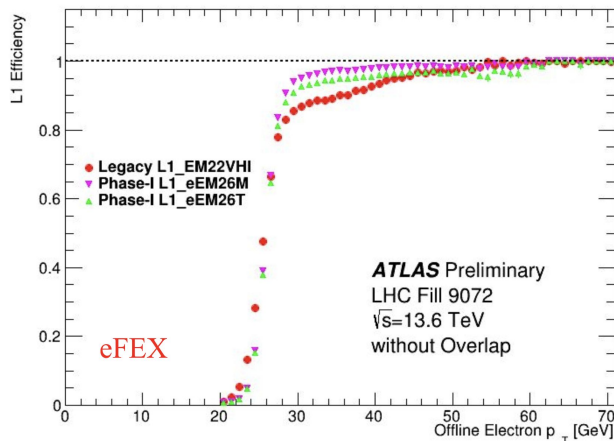
Data from run with the pp collision at $\sqrt{s} = 13.6$ TeV on 22 May 2024

- **99.51%** of SCs (33882 out of 34048) show (in blue) have no issues and return the expected timing and energy
- 166 out of 34048 SCs (in red) are dead, it comes from known problematic Digital Trigger Front End Board channels (LTDBs or with known calibration issues)
- **Good agreement** between the transverse energies (E_T) of SCs and sum of the corresponding LAr cells
 - Bad SCs are not included



Phase-I trigger performance

- **Sharper** efficiency curve on Phase-I based item
 - Show **better** selection of relevant objects at energies just above thresholds
 - Electron (e)-FEX fully enabled in 2023
 - Jet (j)-FEX and global (g)-FEX commissioning being finalized
- Rate reduction by **~5 kHz**
 - Allow ATLAS to run at $\mu = 65$
- Tuning still needed, but in most cases digital trigger **outperforms** the legacy system



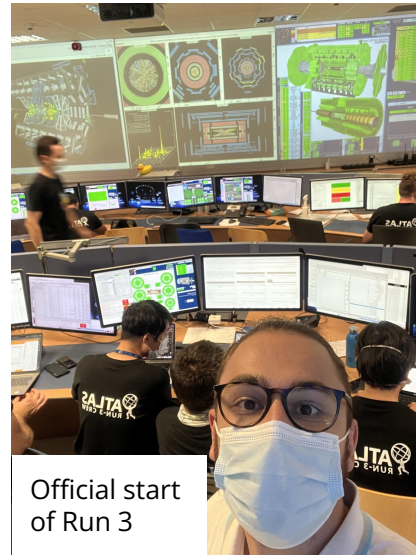
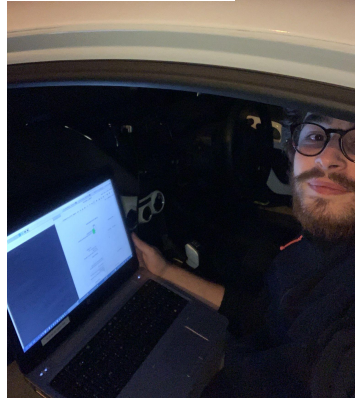
Content

1. Experimental context
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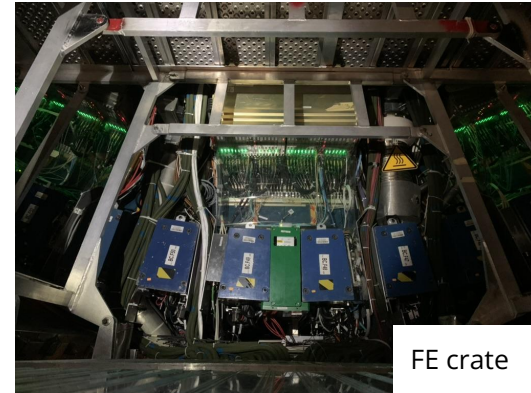
Cleaning of ATLAS cavern



On call expert



Official start of Run 3



FE crate

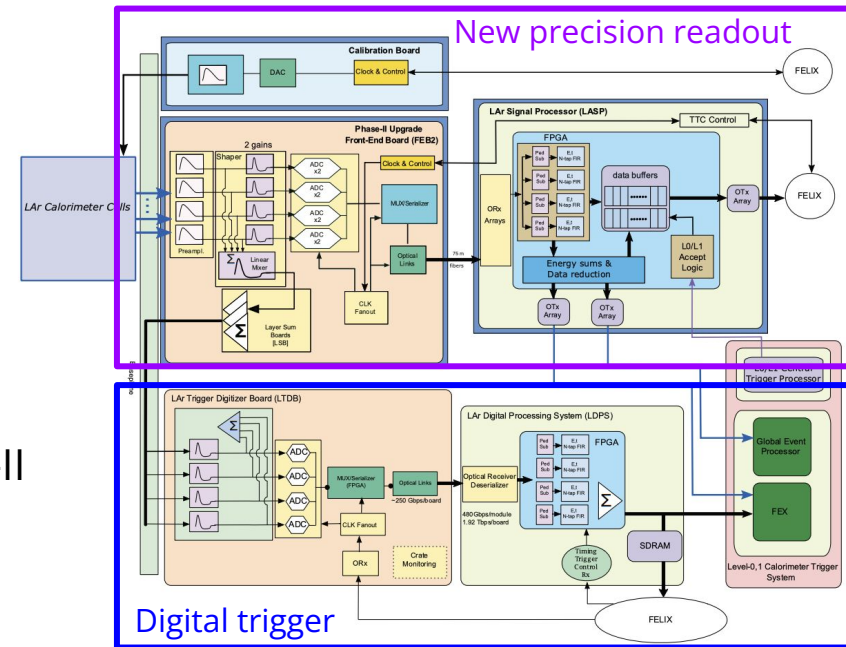
Cabling LTDBs control & data fibers

Conclusion

- Digital trigger commissioning almost finished
 - Sharper efficiency turn-on curve
 - Significant rate reductions (~5 kHz) for electromagnetic object
 - Used as primary trigger system
- Analog trigger ready to be decommissioned
- LTDBs are stable
 - ADC jump due to calibration constant solved
 - Phase selection all fiber stable
 - Robust monitoring and alarm put in place
- LTDBs are cleared of being the source of the timing shift
 - Investigation on going on the FELIX LTDB side

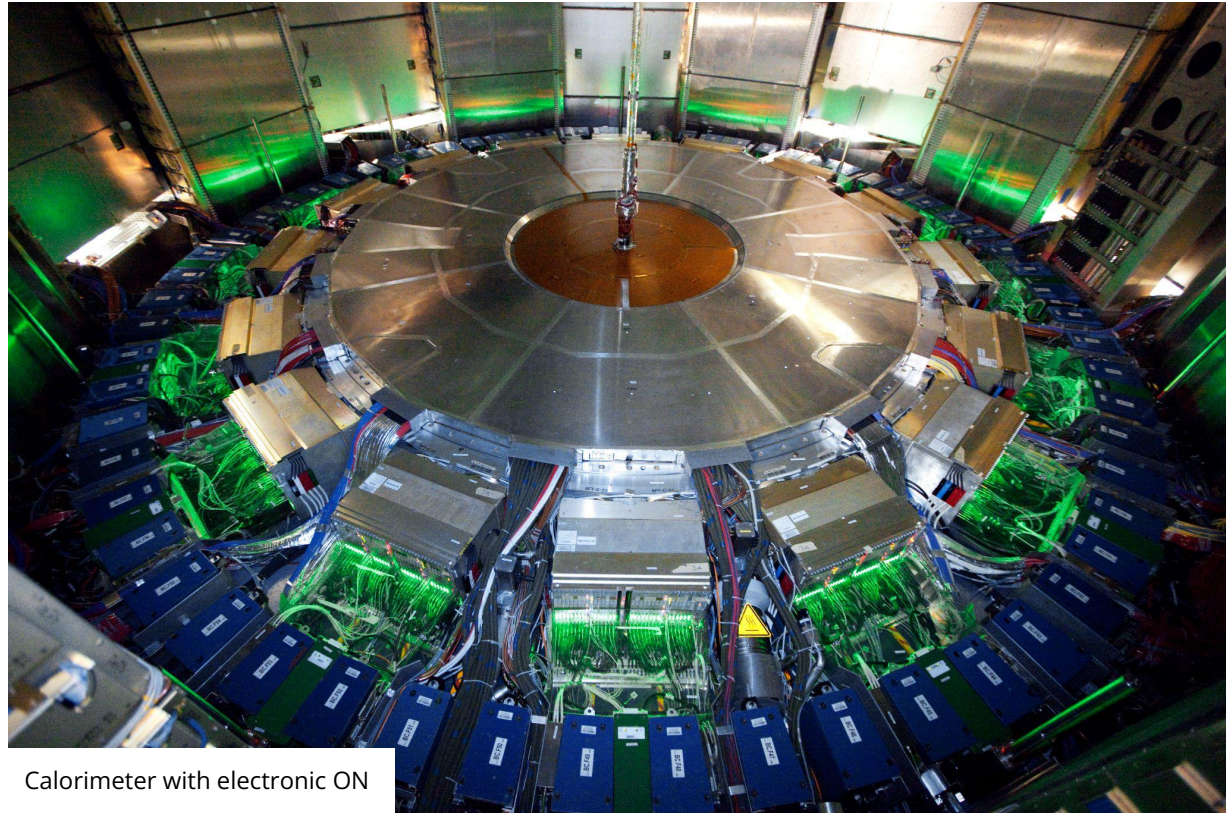
Future Prospects

- Continue to investigate with FELIX expert on the timing shift issue
 - FELIX will remain for Phase-II
 - Mitigation solutions require expert intervention and take time
 - Investigate on the state machine that generates the GBT frame
 - Test new FW
- **Digital Trigger** will remain operational for phase-II
 - Recommissioning of the DT will be mandatory
 - Revalidation of all LTDBs (mapping, ADC calibration, configuration, monitoring, ...)



Thank you for your attention

Any questions ?



Calorimeter with electronic ON

BACKUP



Reference

- ATLAS Liquid Argon Calorimeter Phase-I Upgrade : Technical Design Report
<https://cds.cern.ch/record/1602230/files/ATLAS-TDR-022.pdf>
- The Phase-I trigger readout electronics upgrade of the ATLAS Liquid Argon calorimeters
<https://dx.doi.org/10.1088/1748-0221/17/05/P05024>
- The ATLAS Trigger System for LHC Run 3 and Trigger performance in 2022
<https://arxiv.org/abs/2401.06630>
- The ATLAS Experiment at the CERN Large Hadron Collider: A Description of the Detector Configuration for Run 3
<https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PAPERS/GENR-2019-02/>

Front-end electronics

Baseplane:

New baseplanes provide an additional slot for LTDB and distribute analog signals of SCs from FEBs to LTDB.

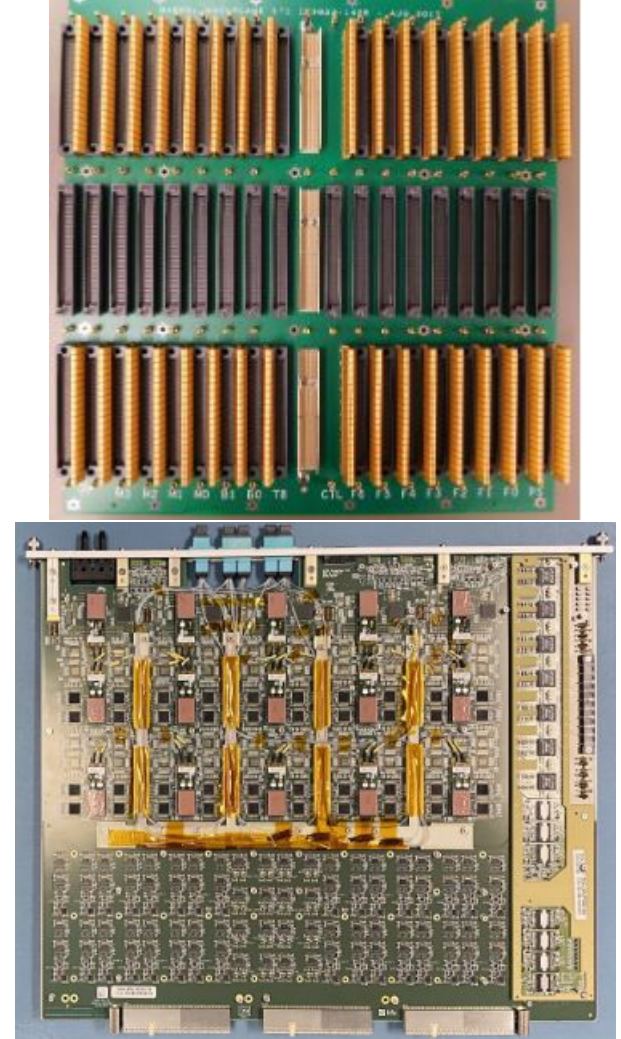
Layer Sum Board (LSB):

A plug-in card of the FEB provides a sum of analog signals for SCs. 2328 LSBs are replaced.



LAr Trigger Digitizer Board (LTDB):

Send analog signals to Tower Builder Board, digitize analog signals, and send digital signals to the back-end. A total of 124 LTDBs are installed



Back-end electronics

Intelligent Platform Management Controller (IMPC):

Manage the power, cooling, and interconnect needs of intelligent devices.



LAr Trigger prOcessing MEzzanine (LATOME):

Receives ADC counts from a LTDB via 40 optical fibers with the speed of 5.12 Gbps for each fiber, computes energy and pulse timing in a FPGA and sends energy to Feature Extractors. 116 LATOMEs are installed.

LAr Carrier (LArC):

Transmit data from LATOMEs to the readout system, distribute clocks and trigger signals synchronized to the LHC beam clock. 30 LArCs are installed.



New electronics for ph-II

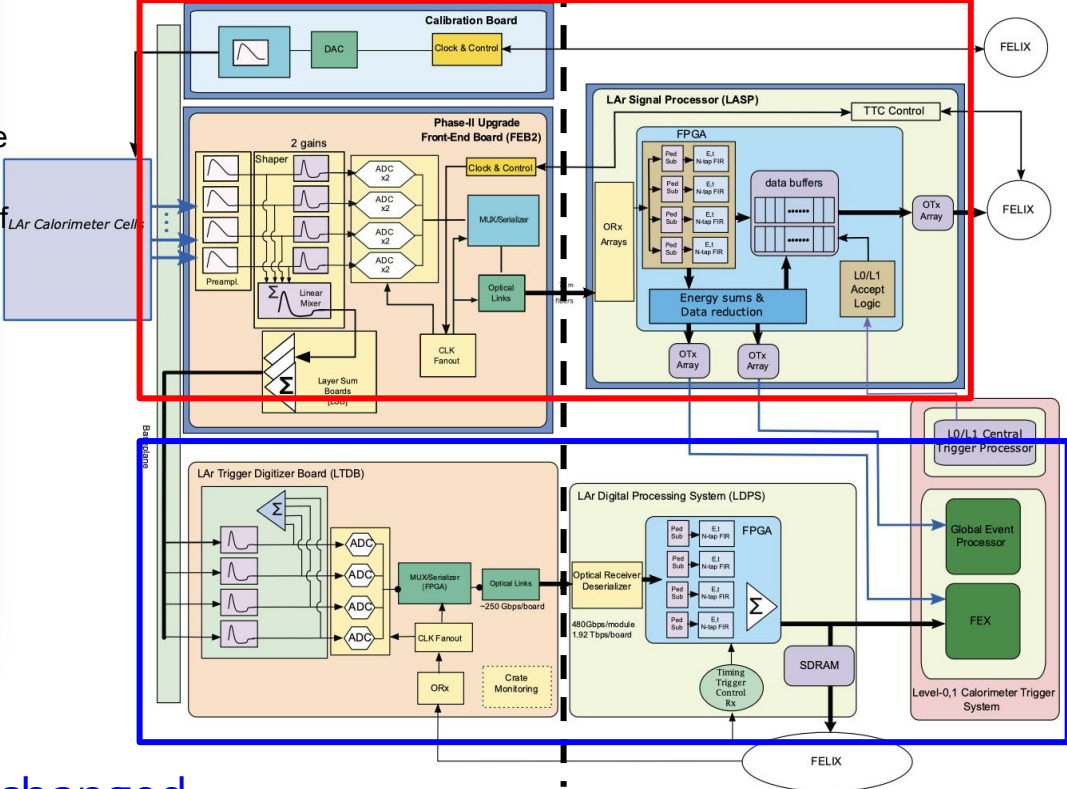
Phase-II electronics:

Calibration Boards: essential for monitoring and calibrating the response of the LAr calorimeter channels. They provide precise calibration signals to the FEBs and allow for in-situ calibration of the detector during data-taking.

Front-End Boards (FEBs): responsible for amplifying and digitizing the analog signals. FEB2 will be developed with improved performance characteristics, such as higher dynamic range, lower noise, and increased radiation tolerance.

LASP: responsible for collecting, digitizing, and transmitting the data from the FEBs to the data acquisition system. Designed to handle higher data rates, incorporate advanced data compression techniques, and improve overall data throughput and efficiency.

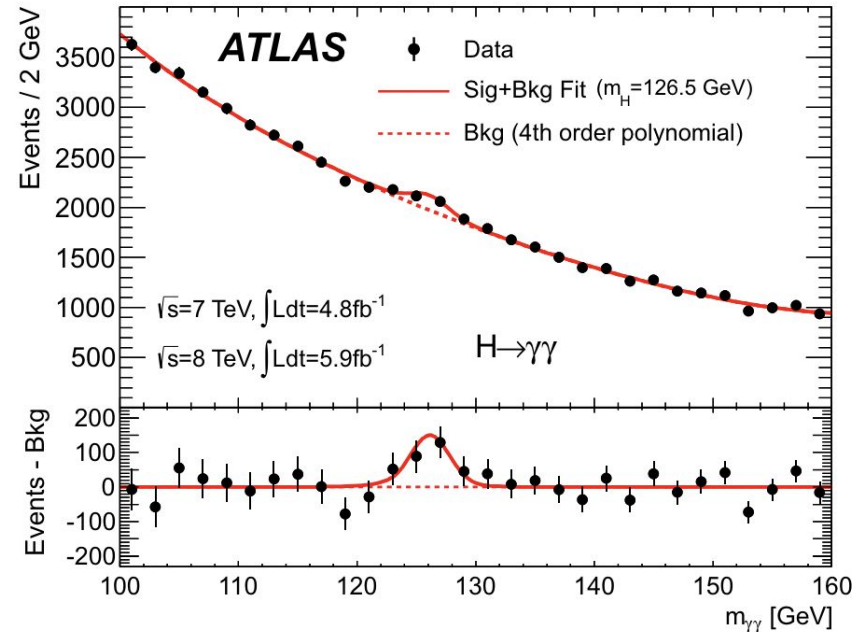
Font End (FE) - on detector Back End (BE) - off detector



Phase-I electronics will remain unchanged

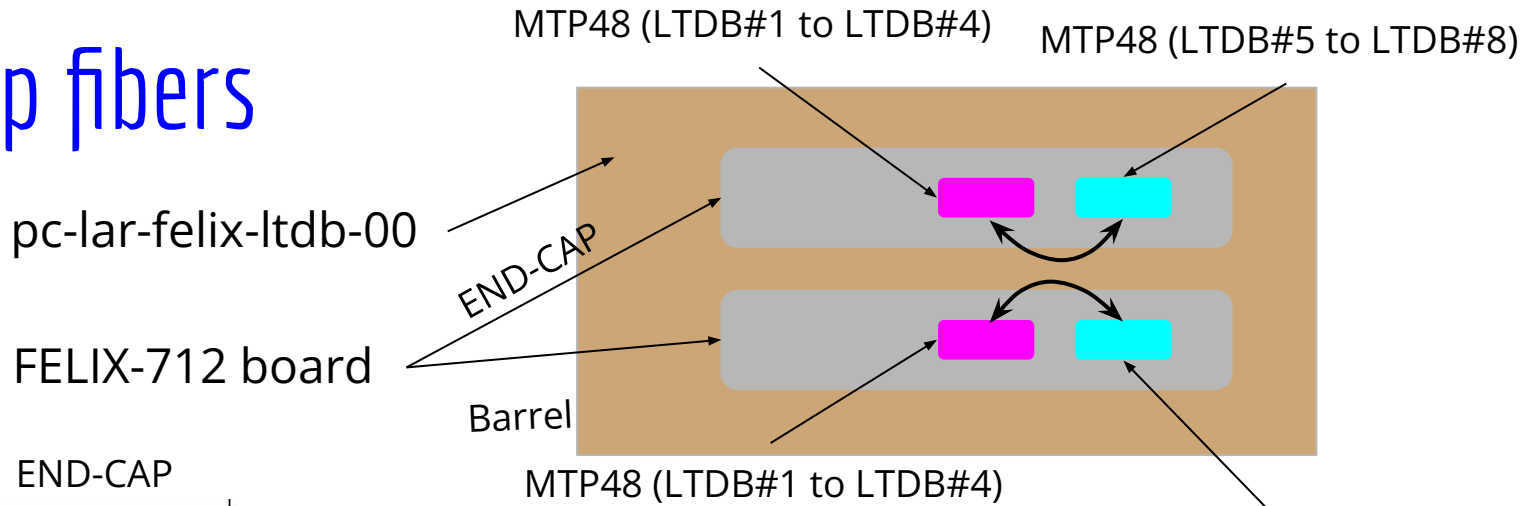
The standard model (SM) of particle physics





- The Higgs Boson discovered in 2012 at the LHC
 - No discoveries of fundamental particles since
- Current and future LHC prospects
 - Precision measurements and search of deviations from the Standard Model
 - Special focus on the Higgs sector
 - Search for Beyond Standard Model particles



- Direct observation of resonances: fundamental way of finding new particles
 - Eg. Higgs Boson discovery in $H \rightarrow \gamma\gamma$ channel
- Fundamental role of energy resolution of the Liquid Argon calorimeter

FELIX swap fibers




	Barrel	END-CAP
	pc-lar-felix-ltodb-00	pc-lar-felix-ltodb-00
1	<u>35(I01L)</u>	<u>132(A01L)</u>
2	<u>31(I02R)</u>	<u>127(A01R)</u>
3	<u>14(I02L)</u>	<u>120(A03L)</u>
4	<u>27(I03R)</u>	<u>116(A03R)</u>
5	<u>23(I03L)</u>	<u>141(A02Spe0)</u>
6	<u>47(I04R)</u>	<u>151(A02Spe1)</u>
7	<u>21(I04L)</u> 	<u>179(A02HEC)</u> 
8	<u>22(I05R)</u> 	<u>187(A04F0)</u> 

- I swap the pink connector with the blue one

Result expected:

- If **LTDB** issue → Timing shift will follow the LTDB
- If **FELIX** issue → Timing shift should stay on the same link


 where the majority of timing shift are observed

DT FE slow control & monitoring

LTDB 124 boards

- Control:
 - Configuration of all the boards
 - Calibration
 - General status
- Monitoring:
 - Optical power of the control fiber
 - Tension/current
 - Fan speed
 - FPGA temperature
 - SCA temperature/register
 - Data fiber status

Run Control



BARREL C BARREL A
 EMEC-C EMEC-A

POWER ON POWER OFF
 IMT SHUTDOWN
 CONFIG UN-CONFIG

Links Status

COPY STATE

Color code

Off	On	Disabled	Error
Unknown	Configured	Unknown	Error

Expert

EN/DESABLE LTDB
 CLK/DES SCAN A SIDE
 CLK/DES SCAN C SIDE

Naming convention

Standard Ltlds:
Crate Name + Position (Left or Right)

FCAL Ltlds:
Crate Name + (F0)/F1
(Follow the standard naming in logs)

EMEC Special Ltlds:
Crate Name + (S0(Spe0))/S1(Spe1)
(In the logs Spe0 is called with crate Name + L and Spe 1 with crate name +R)

HEC Ltlds:
Crate Name +H

Spare Felix

TTC	LOC	TTC	LOC
Clk: LOCAL	Clk: LOCAL	Clk: LOCAL	Clk: LOCAL
Temp 75	Temp 62	Temp 86	Temp 62
Fan 8916	Fan 8470	Fan 8909	Fan 8470

Servers A

FLK-00

FLK-01

FLK-02

FLK-03

Servers C

FLK-04

FLK-05

FLK-06


FLK-07

BARREL C(H)

H01-H16

BARREL A (I)

I01-I16



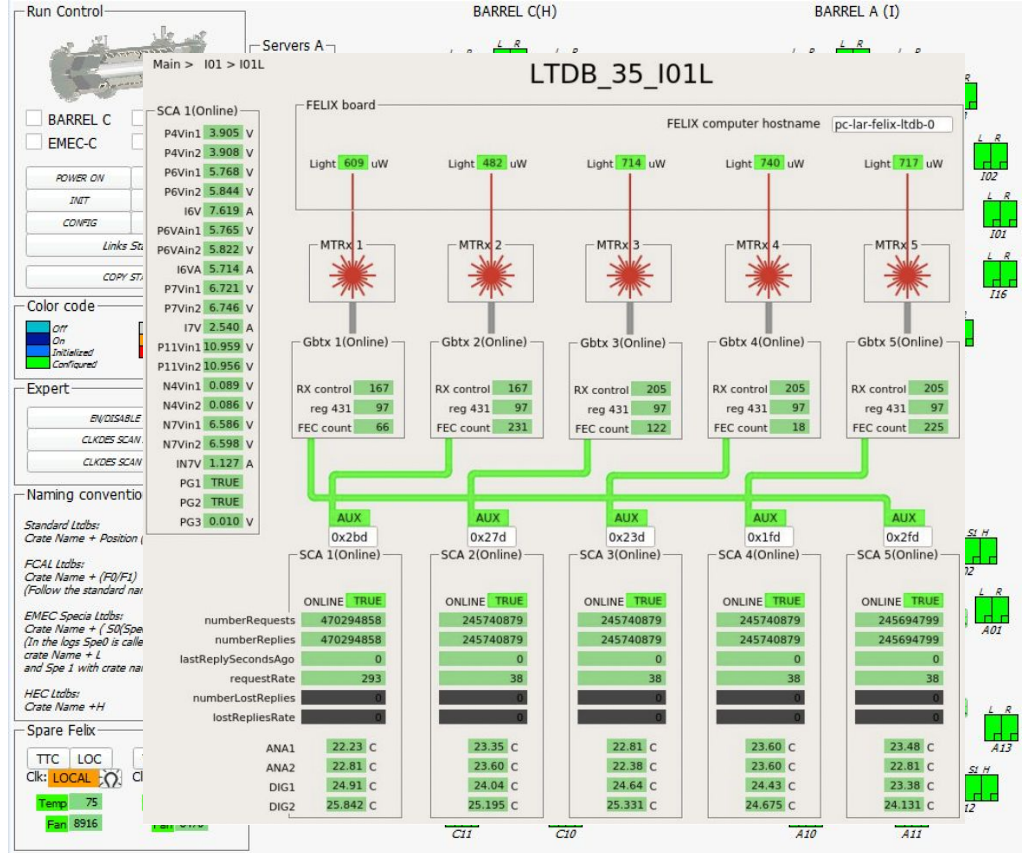
EMEC C(C) EMEC A (A)

The main diagram shows a grid of server racks. Each rack has a status indicator (TTC, LOC, Clk) and a temperature/fan speed readout. The racks are organized into four main sections: Servers A, Servers C, BARREL C(H), and BARREL A (I). Each rack also has a 'COPY STATE' indicator.

DT FE slow control & monitoring

LTDB 124 boards

- Control:
 - Configuration of all the boards
 - Calibration
 - General status
- Monitoring:
 - Optical power of the control fiber
 - Tension/current
 - Fan speed
 - FPGA temperature
 - SCA temperature/register
 - Data fiber status



New electronics of Phase-I

The front end electronics of the **legacy trigger** was dismantled then reassembled, some components replaced:

- Baseplane (to re-route SC signal)
- Layer Sum Board (modify summation of cell)

New cards added for the **digital trigger**

- **LAr Trigger Digitizer Board (LTDB)**
 - Digitize analog signals
 - Send digital signals to the back-end (LDPS).
 - Send summed analog signals to Tower Builder Board
 - 124 LTDBs are installed
- **LAr Digital Processing System (LDPS)**
 - LAr Carrier (LArC)
 - **LAr Trigger prOcessing MEzzanine (LATOME)**
 - Receives ADC counts from LTDB
 - Computes energy and pulse timing
 - Sends energy to Feature Extractors
 - 116 LATOMEs are installed

