



24th AGATA Week, September 2024 - Milano

V2 Electronic data pipeline

O.Stézowski
and the Data Processing Group

Many thanks to the Data Processing Team

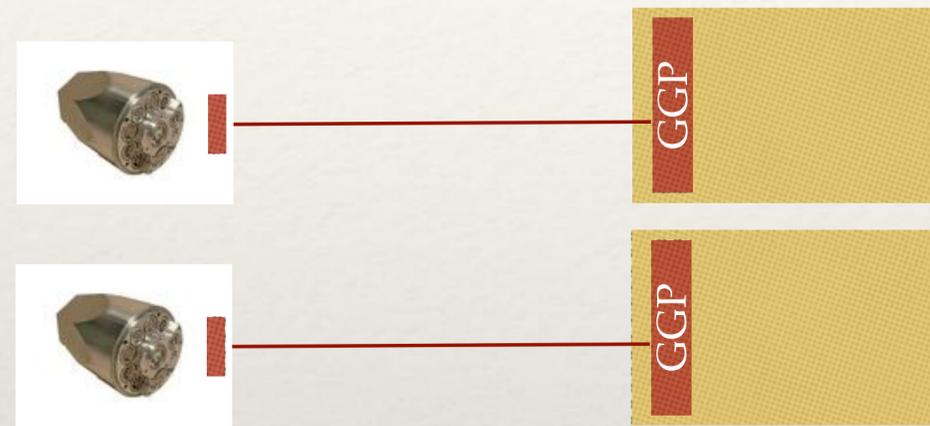
G.Baulieu, Ch. Bonnin, N.Dosme, J.Dudouet, S. Elloumi, Ph. Gauron, A. Goasduff, M.Gulmini,
A. Korichi, J. Jacob, V. Lafage, E. Legay, P. Lejeannic,
J. Ljungvall, G.Philippon, R.Molina, M. Roetto, M. Tauriga-Quere, N.Toniolo

Outlines

- Objectives
- What has been achieved
- What has to be done

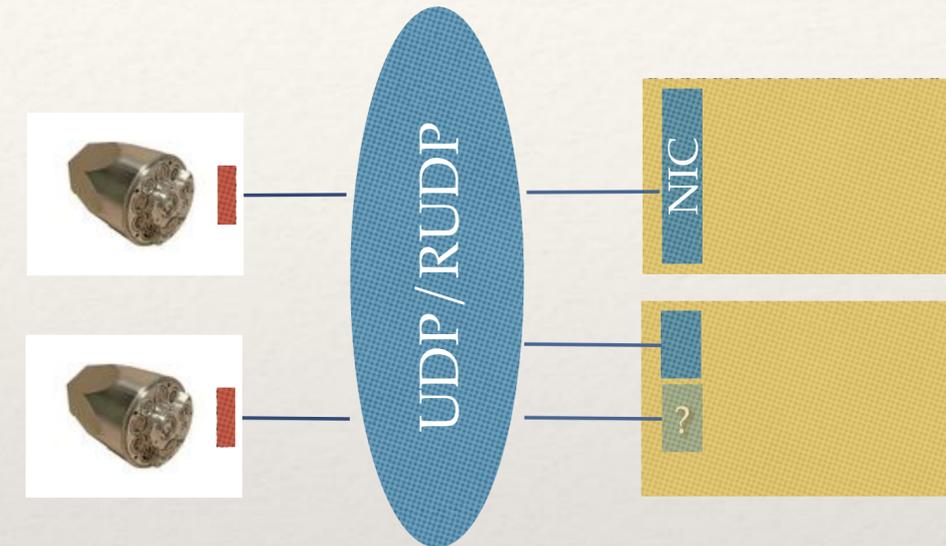
V2 Electronic integration, the new data pipeline

Current situation : GGP (PCI) cards in computers



GGP are 'home made' products

Future situation : NIC Network Interface Card



NIC are standard products

Moving from left to right



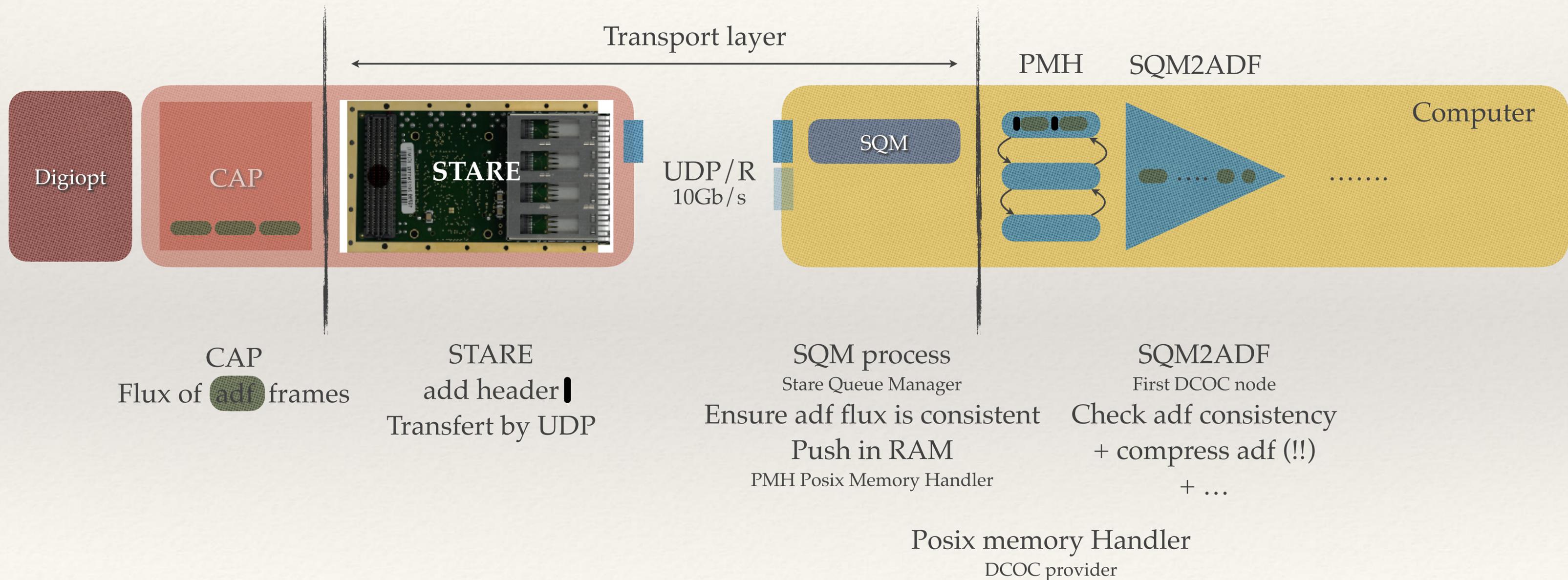
+ cohabitation period !!!
i.e. 'v2 acting like v1'

It does not mean one is better than the other !

Ex : 'Mastering' the Network Card + OS is required for V2

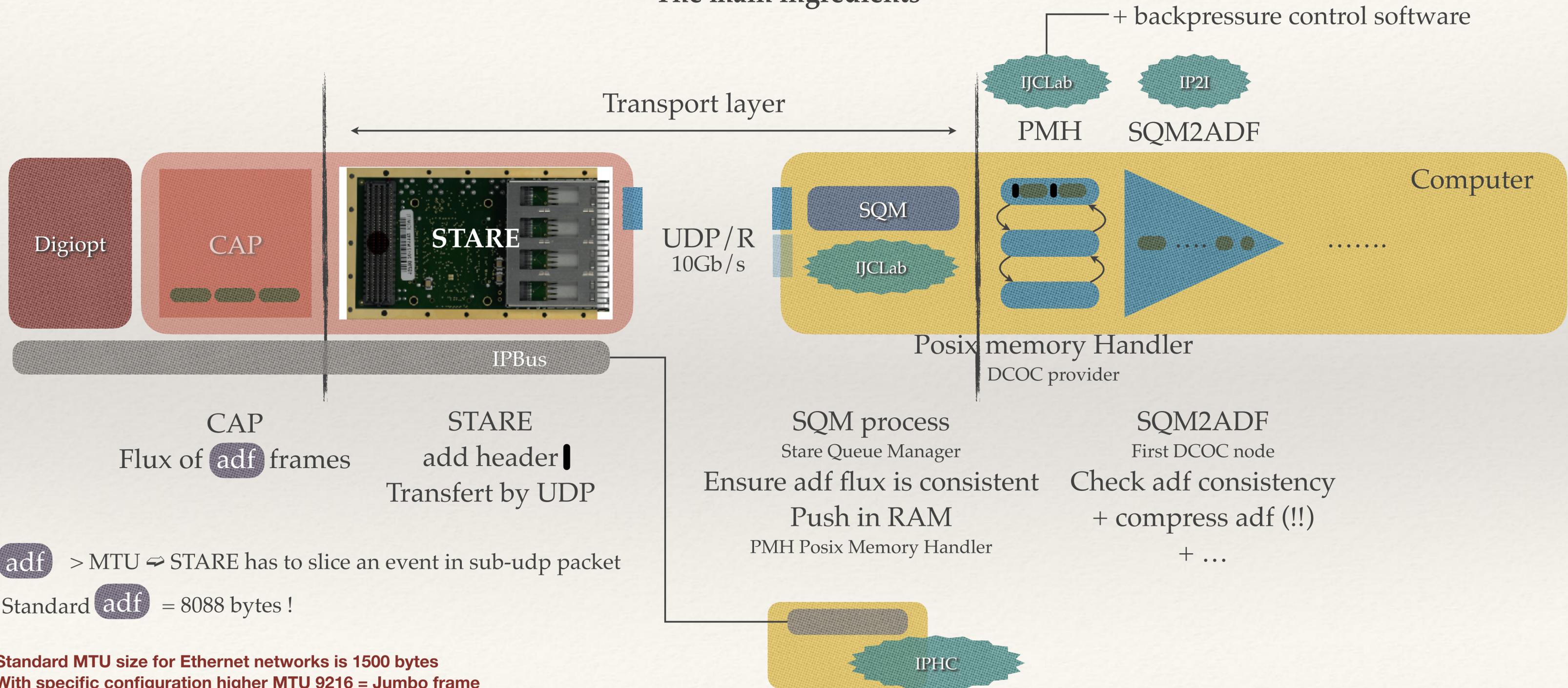
V2 Electronic integration, the new data pipeline

The main ingredients



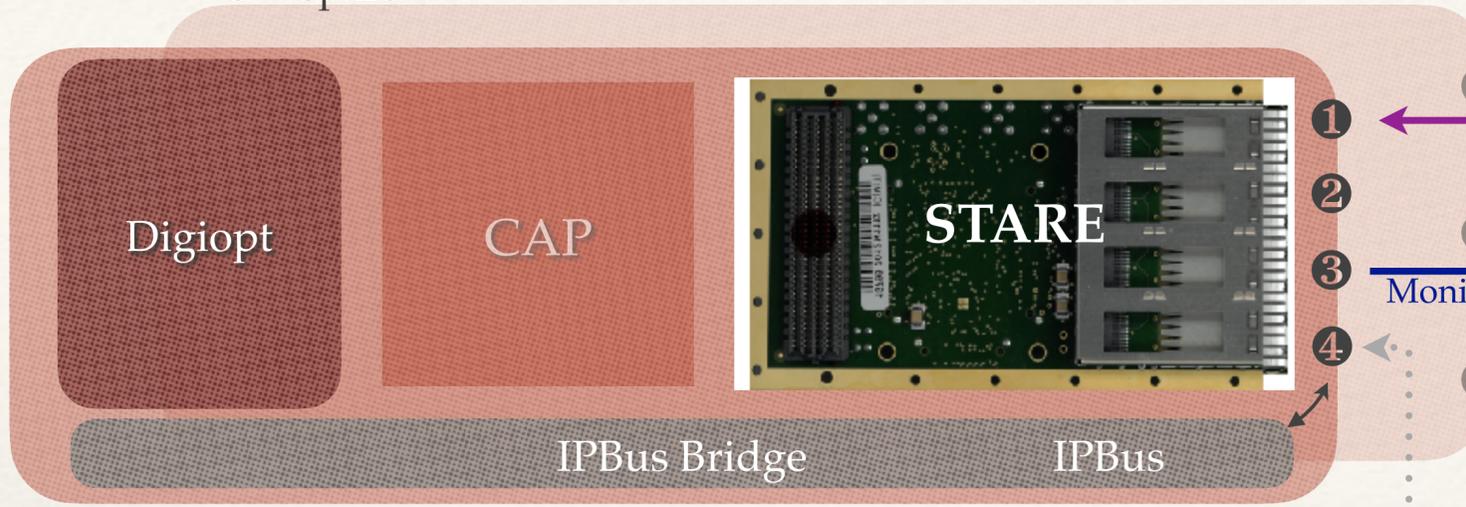
V2 Electronic integration, the new data pipeline

The main ingredients

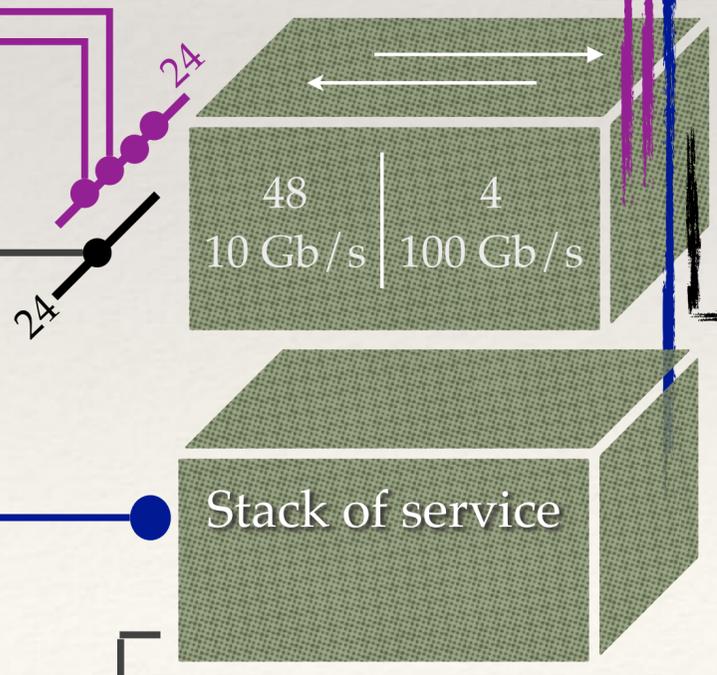
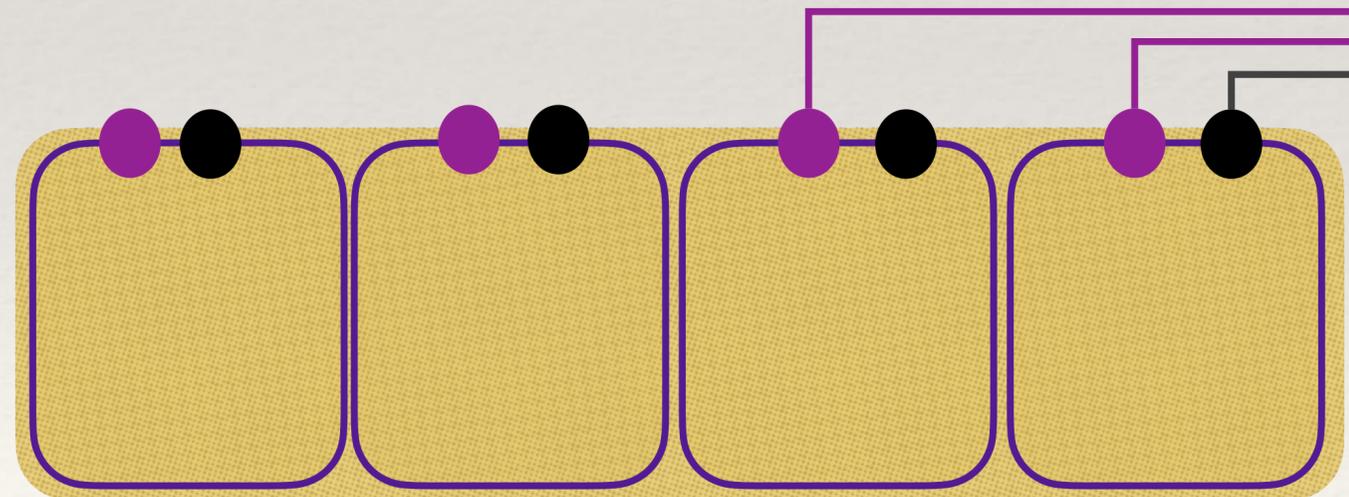
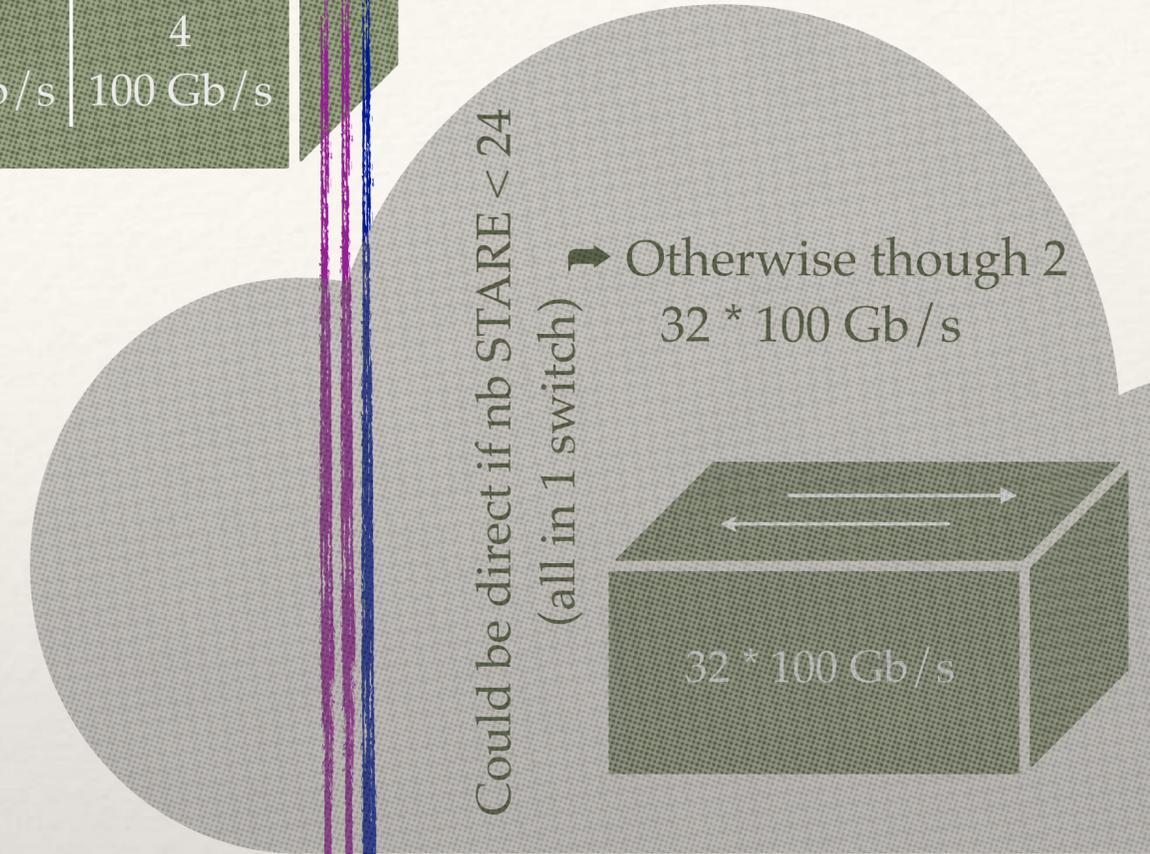
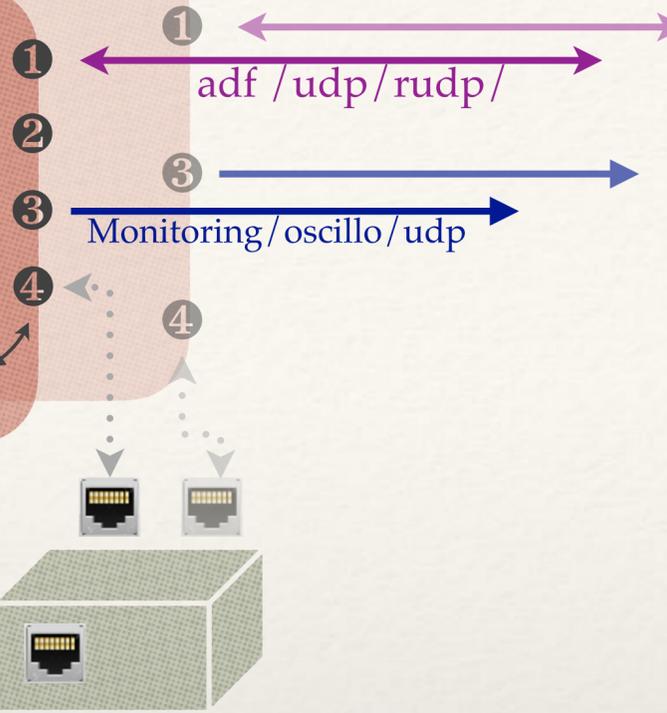
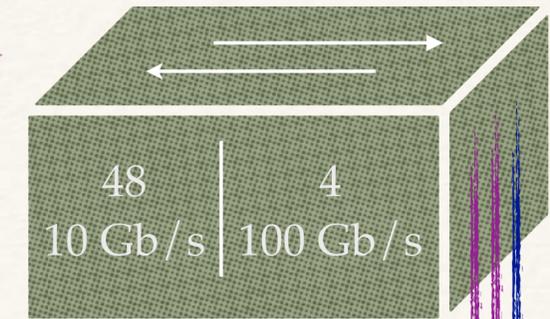


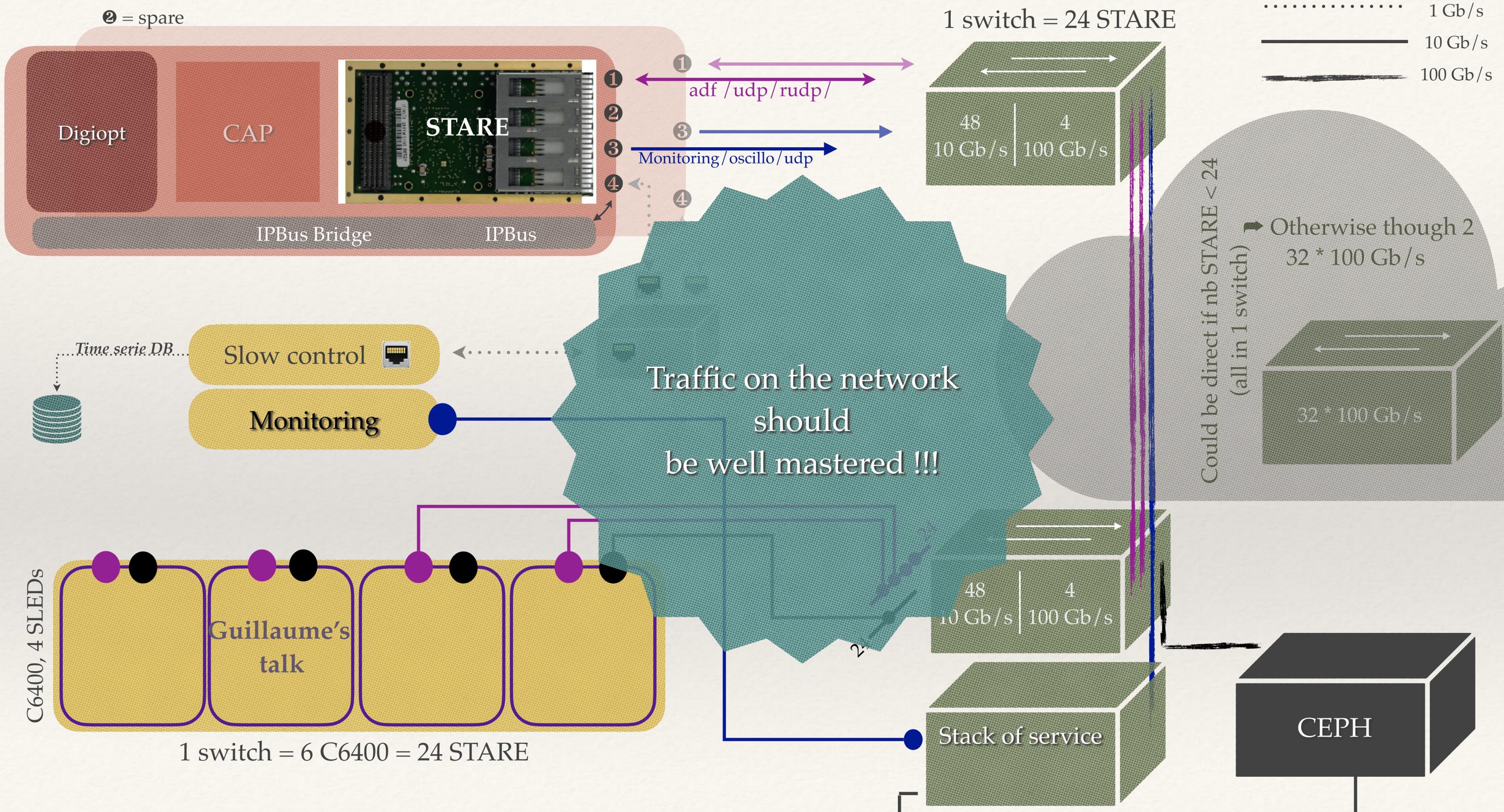
180 Channels

② = spare



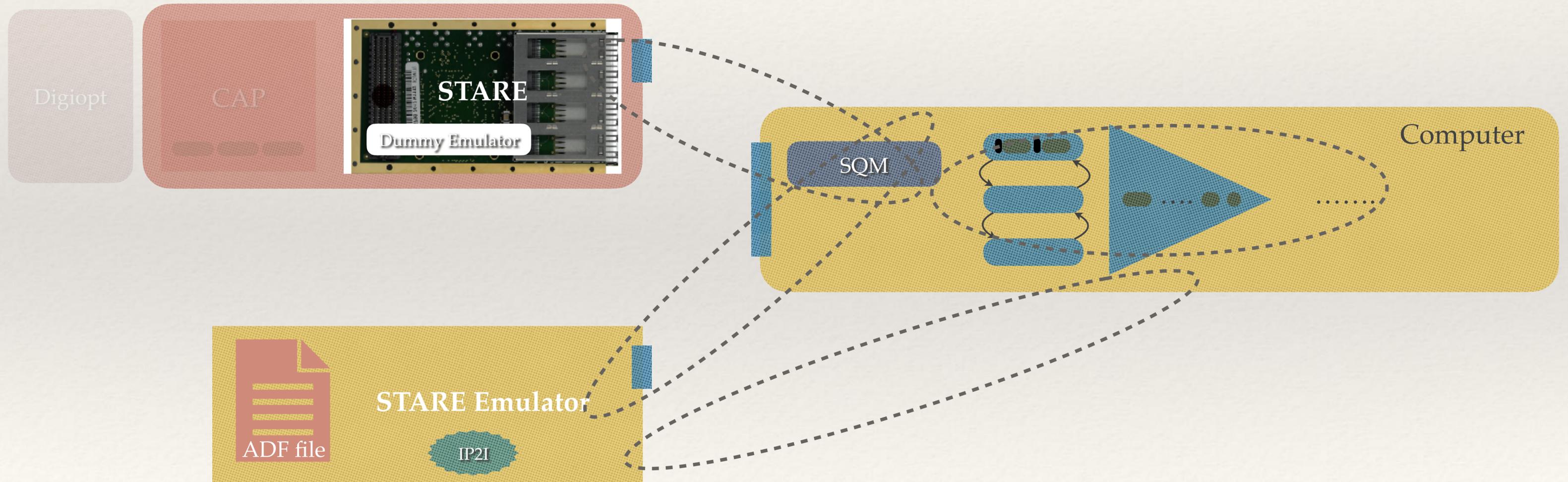
1 switch = 24 STARE





Situation @ previous AGATA Week

First version of the different bricks developed using emulators in specific environments



Situation @ this AGATA Week

Tests realised with the objective of up to 50 kHz PSA

Digiopt

CAP

STARE

ADF Emulator

SQM

... PSA ...

Computer

STARE Emulator

ADF file

IP2I

Full chain tested / benchmarked in emulators

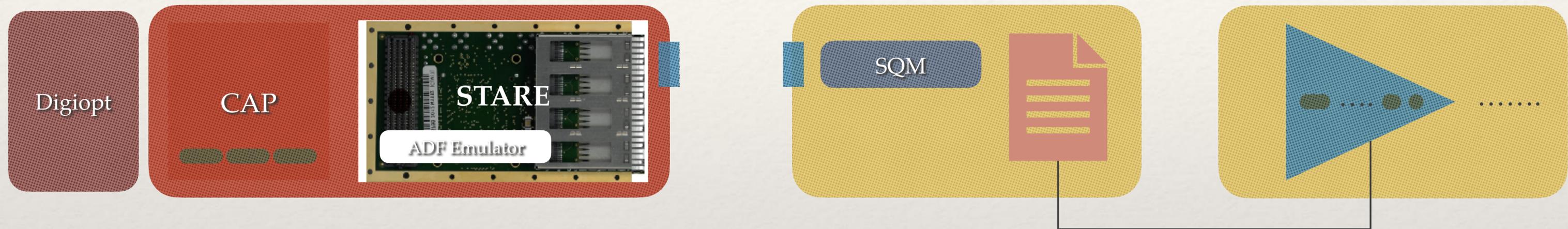
DCOD (online DAQ) integration



➔ Effort to port dcod on last Debian / compiler versions

Situation @ this AGATA Week

We have now data from real detector out of DIGIOPT-CAP-STARE up to SQM then dumped in files



Quality of the data can be checked

Remember

if one 'event'  produced by CAP is < 1 MTU

↳ it is transferred by STARE as one unit = one UDP packet

if one 'event'  produced by CAP is > 1 MTU

↳ it is transferred by STARE split on several UDP packets

PACE can deliver much more than one type of adf !

Module Origin	Name	Crystal Status			AdF		Description	Status
		Mode	Type	Code	Type	Version		
GTS Trigger Match	DATA_100_SC	DA Data	00 Call	DA00	Simple	0	Normal Data 100 samples triggered by slow control call	Impl
	DATA_100_RP	DA Data	01 Time	DA01	Simple	0	Normal Data 100 samples triggered by timer (Fixed datarate)	Impl
	DATA_100_TL	DA LTC	10 Loc	DA10	Simple	0	Normal Data 100 samples triggered by localtrigger data from long traces buffer	Impl
	DATA_100_TG	DA Data	02 Loc	DA02	Simple	0	Normal Data 100 samples triggered by localtrigger (datapath)	Impl
	DATA_100_GT	DA Data	03 GTS	DA03	Simple	0	Normal Data 100 samples triggered by gts validation	Impl
	DATA_200_SC	DA Data	A0 Call	DAA0	Extended	0	Normal Data 200 samples triggered by slow control call	Impl
	DATA_200_RP	DA Data	A1 Time	DAA1	Extended	0	Normal Data 200 samples triggered by timer (Fixed datarate)	Impl
	DATA_200_TG	DA Data	A2 Loc	DAA2	Extended	0	Normal Data 200 samples triggered by localtrigger (datapath)	Impl
	DATA_200_GT	DA Data	AA GTS	DAAA	Extended	0	Normal Data 200 samples triggered by gts validation	Impl
	LT_4k_SC	CE LTC	00 Call	CE00	Simple	0	Long Traces data 4k samples triggered by slow control call	Impl
LT_4k_RP	CE LTC	01 Time	CE01	Simple	0	Long Traces data 4k samples triggered by timer (Fixed datarate)	Impl	
LT_4k_TG	CE LTC	02 Loc	CE02	Simple	0	Long Traces data 4k samples triggered by localtrigger (datapath)	Impl	
LT_4k_GT	CE LTC	03 GTS	CE03	Simple	0	Long Traces data 4k samples triggered by gts validation	Impl	
LTb Long Traces Buffer	LT_4x1k_SC	CE LTC	10 Call	CE10	Extended	0	4 channel Long Traces data 4k samples triggered by slow control call	Impl
	LT_4x1k_RP	CE LTC	11 Time	CE11	Extended	0	4 channel Long Traces data 4k samples triggered by timer (Fixed datarate)	Impl
	LT_4x1k_TG	CE LTC	12 Loc	CE12	Extended	0	4 channel Long Traces data 4k samples triggered by localtrigger (datapath)	Impl
	LT_4x1k_GT	CE LTC	13 GTS	CE13	Extended	0	4 channel Long Traces data 4k samples triggered by gts validation	Impl
	LT_8k_SC	CE LTC	A0 Call	CEA0	Extended	0	Long Traces data 8k samples triggered by slow control call	Impl
	LT_8k_RP	CE LTC	A1 Time	CEA1	Extended	0	Long Traces data 8k samples triggered by timer (Fixed datarate)	Impl
	LT_8k_TG	CE LTC	A2 Loc	CEA2	Extended	0	Long Traces data 8k samples triggered by localtrigger (datapath)	Impl
	LT_8k_GT	CE LTC	A3 GTS	CEA3	Extended	0	Long Traces data 8k samples triggered by gts validation	Impl
vLTb Very Long Traces Buffer	LT_100k_SC	CE LTC	B0 Call	CEB0	Extended	0	Very Long Traces data 8k samples triggered by slow control call	TBD
	LT_100k_RP	CE LTC	B1 Time	CEB1	Extended	0	Very Long Traces data 8k samples triggered by timer (Fixed datarate)	TBD
	LT_100k_TG	CE LTC	B2 Loc	CEB2	Extended	0	Very Long Traces data 8k samples triggered by localtrigger (datapath)	TBD
	LT_100k_GT	CE LTC	B3 GTS	CEB3	Extended	0	Very Long Traces data 8k samples triggered by gts validation	TBD
Spectra Buffer	SPC_100_SC	FA SPC	01 Call	FA01	Simple	0	Short 100 bin spectra for all channel trigger by slow control call	Impl
	SPC_100_RP	FA SPC	02 Call	FA02	Simple	0	Short 100 bin spectra for all channel trigger by timer	Impl
	SPC_4kp_SC	FA SPC	10 Call	FA10	Simple	0	Long 4k bin spectra for one channel trigger by slow control call	Impl
	SPC_8kp_SC	FA SPC	A0 Call	FAA0	Extended	0	Long 8k bin spectra for one channel trigger by slow control call	TBD
System	IDLE			BEDD	Simple	0	IDLE empty message sent each IDLE TIME (set by slow control)	Impl
	ERROR			EEEE	Simple	0	On call (trigger/slow control) system was on error	Impl
	SYSOFF			DEAD	Simple	0	On call (trigger/slow control) system is off (Digitizer/Readout)	Impl

Some are **simple** i.e. coded using < Max MTU

- ➔ requires only one UDP paquet !
- ➔ Just need to be sure we have received it

Other are **extended** i.e. coded using > Max MTU

- ➔ requires more than one UDP paquet !
- ➔ we need to have all received !
- ➔ we need to reconstruct !

} Spectra produced inside the card & sent embedded in the data stream

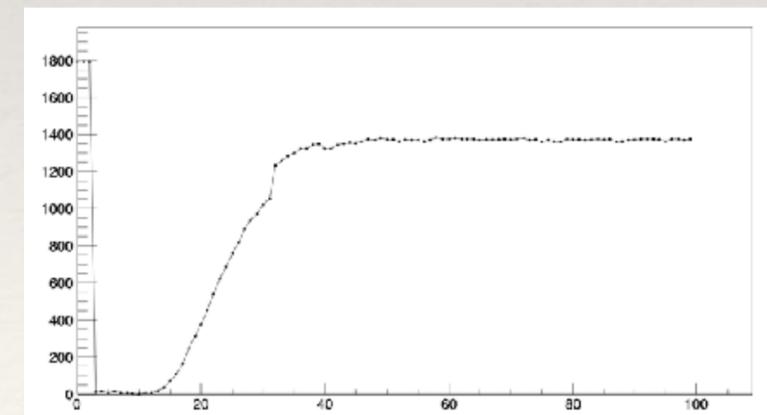
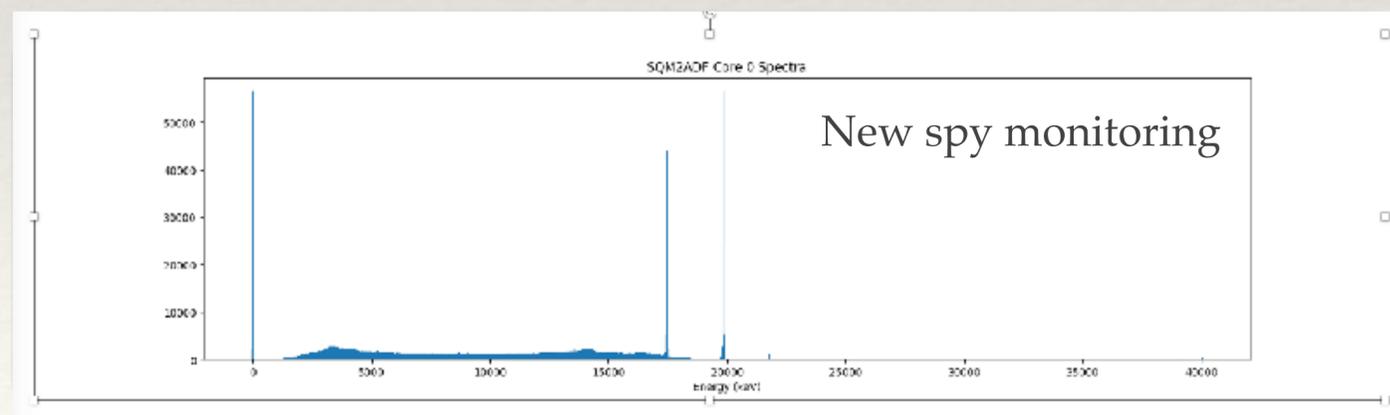
} Information (idles, errors) embedded in an adf frame

Situation @ this AGATA Week

SQM2ADF improved+benchmarked to handle all the situations

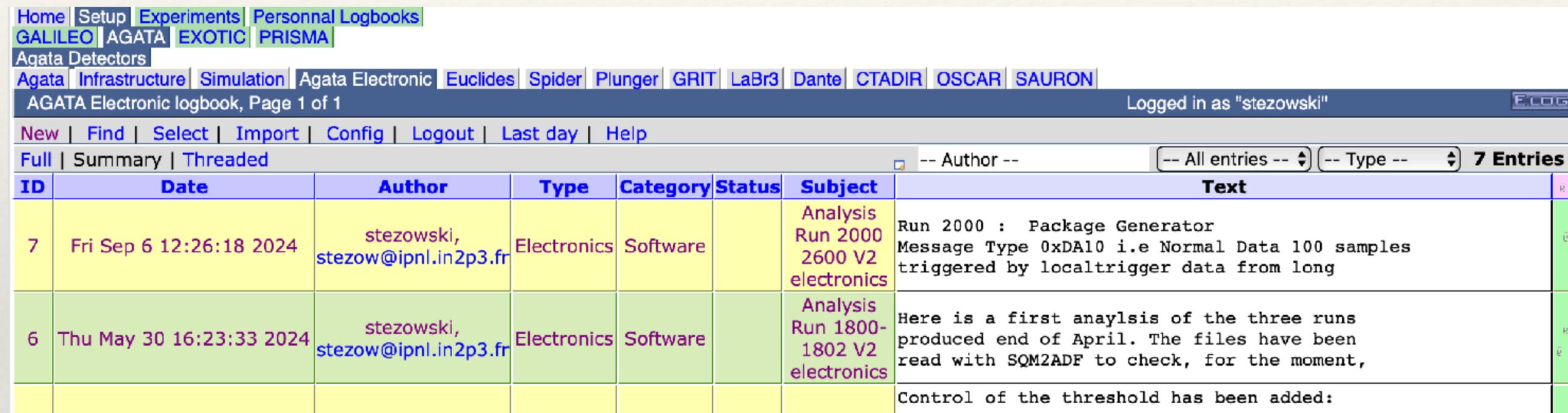


Ex : these pictures are from a real detector through the pipeline @ SQM2ADF level



Work for the coming weeks/months

Data stream NOT YET fully (70-80% ok) under control ➤ interactions with FEE group



The screenshot shows a web-based logbook interface for the AGATA detector. The page title is "AGATA Electronic logbook, Page 1 of 1" and the user is logged in as "stezowski". The interface includes navigation links for various experiments and detectors, and a table of log entries. The table has columns for ID, Date, Author, Type, Category, Status, Subject, and Text. Two entries are visible, both authored by "stezowski, stezow@ipnl.in2p3.fr" and categorized as "Electronics Software".

ID	Date	Author	Type	Category	Status	Subject	Text
7	Fri Sep 6 12:26:18 2024	stezowski, stezow@ipnl.in2p3.fr	Electronics	Software		Analysis Run 2000 2600 V2 electronics	Run 2000 : Package Generator Message Type 0xDA10 i.e Normal Data 100 samples triggered by localtrigger data from long
6	Thu May 30 16:23:33 2024	stezowski, stezow@ipnl.in2p3.fr	Electronics	Software		Analysis Run 1800- 1802 V2 electronics	Here is a first analysis of the three runs produced end of April. The files have been read with SQM2ADF to check, for the moment, Control of the threshold has been added:

Once ok, we can move to data quality, calibrations and PSA

+ handling of many detectors in parallel ... anticipation (see other talks)