LAPP
Laboratoire d'Annecy de Physique des Particules

Retour GTC 2024 : GPU Technical Conference

Pierre Aubert

ESCAPE
cta
cherenkov telescope array
cnrs
UNIVERSITÉ SAVOIE MONT BLANC

Introduction first part

GTC 2024 Presentation Catalog

This is not possible to summarize **1080** talks !

Only focus on :

- **Hardwares** evolution from 2020 to 2023
- **Compilers** evolution
- **Feedback**

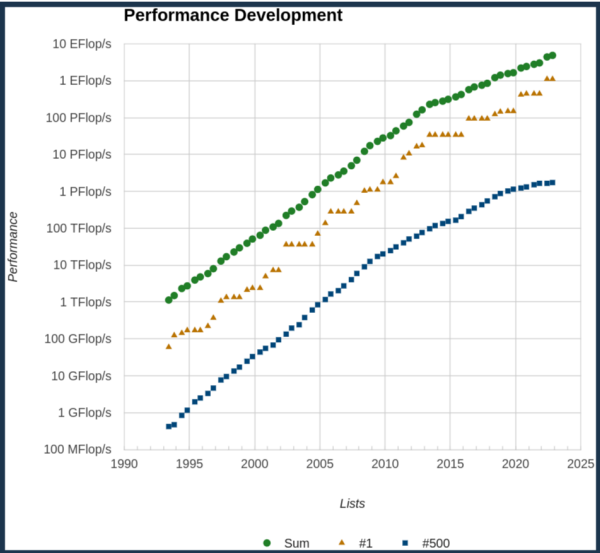
Keynotes video link

Top / Green 500

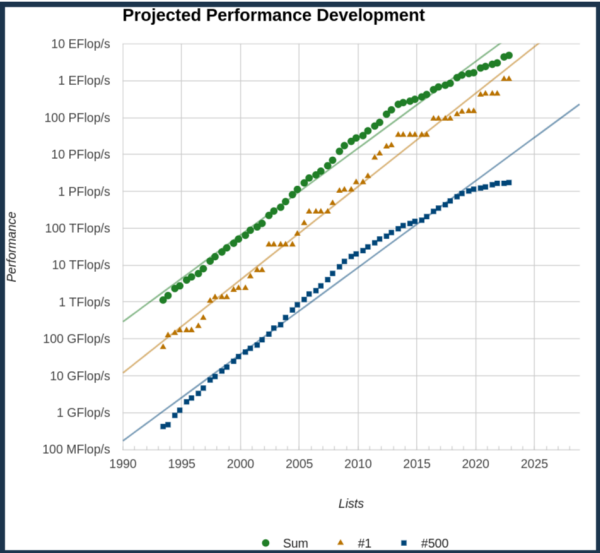
Top 500 :
- Top of the most **powerful** computing center in the world

Green 500 :
- Top of the most **efficient** computing center in the world

Top / Green 500

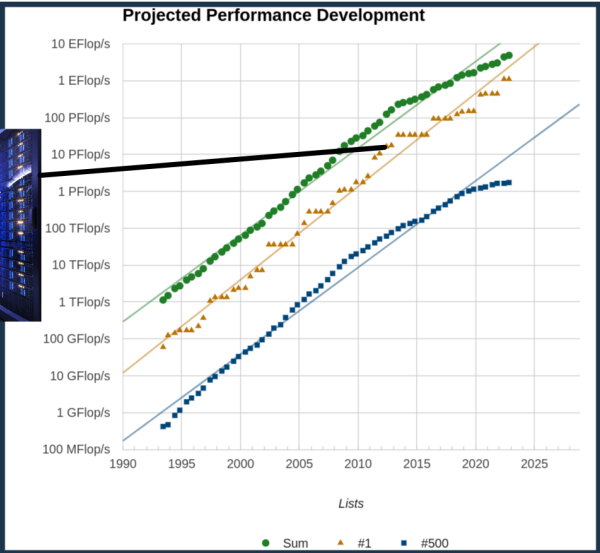


Top / Green 500



Top / Green 500

Titan (2012)
- **20 PFlops**
- **7 MW**



Top / Green 500

Top 500 (11/2022)

Rank	System	Cores	(PFlop/s)	(PFlop/s)	(kW)
1	**Frontier** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** DOE/SC/Oak Ridge National Laboratory United States	8,730,112	1,102.00	1,685.65	21,100
2	**Supercomputer Fugaku** - Supercomputer Fugaku, A64FX 48C 2.2GHz, Tofu interconnect D, **Fujitsu** RIKEN Center for Computational Science Japan	7,630,848	442.01	537.21	29,899
3	**LUMI** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** EuroHPC/CSC Finland	2,220,288	309.10	428.70	6,016
4	**Leonardo** - BullSequana XH2000, Xeon Platinum 8358 32C 2.6GHz, NVIDIA A100 SXM4 64 GB, Quad-rail NVIDIA HDR100 Infiniband, **Atos** EuroHPC/CINECA Italy	1,463,616	174.70	255.75	5,610
5	**Summit** - IBM Power System AC922, IBM POWER9 22C 3.07GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, **IBM** DOE/SC/Oak Ridge National Laboratory United States	2,414,592	148.60	200.79	10,096
6	**Sierra** - IBM Power System AC922, IBM POWER9 22C 3.1GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, **IBM / NVIDIA / Mellanox** DOE/NNSA/LLNL United States	1,572,480	94.64	125.71	7,438
7	**Sunway TaihuLight** - Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway, **NRCPC** National Supercomputing Center in Wuxi China	10,649,600	93.01	125.44	15,371
8	**Perlmutter** - HPE Cray EX235n, AMD EPYC 7763 64C 2.45GHz, NVIDIA A100 SXM4 40 GB, Slingshot-10, **HPE** DOE/SC/LBNL/NERSC United States	761,856	70.87	93.75	2,589
9	**Selene** - NVIDIA DGX A100, AMD EPYC 7742 64C 2.25GHz, NVIDIA A100, Mellanox HDR Infiniband, **Nvidia** NVIDIA Corporation United States	555,520	63.46	79.22	2,646
10	**Tianhe-2A** - TH-IVB-FEP Cluster, Intel Xeon E5-2692v2 12C 2.2GHz, TH Express-2, Matrix-2000, **NUDT** National Super Computer Center in Guangzhou China	4,981,760	61.44	100.68	18,482

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Green 500 (11/2022)

Rank	TOP500 Rank	System	Cores	Rmax (PFlop/s)	Power (kW)	Energy Efficiency (GFlops/watts)
1	405	**Henri** - Lenovo ThinkSystem SR670 V2, Intel Xeon Platinum 8362 32C 2.80GHz, [3X]L NVIDIA H100 80GB PCIe, Infiniband HDR, **Lenovo** Flatiron Institute United States	5,920	2.04	31	65.091
2	32	**Frontier TDS** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** DOE/SC/Oak Ridge National Laboratory United States	120,832	19.20	309	62.684
3	11	**Adastra** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** Grand Equipement National de Calcul Intensif - Centre Informatique National de l'Enseignement Superieur (GENCI-CINES) France	319,072	46.10	921	58.021
4	15	**Setonix - GPU** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** Pawsey Supercomputing Centre, Kensington, Western Australia Australia	181,248	27.16	477	56.983
5	68	**Dardel-GPU** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** KTH - Royal Institute of Technology Sweden	52,864	8.26	146	56.491
6	1	**Frontier** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** DOE/SC/Oak Ridge National Laboratory United States	8,730,112	1,102.00	21,100	52.227
7	3	**LUMI** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, **HPE** EuroHPC/CSC Finland	2,220,288	309.10	6,016	51.382
8	159	**ATOS THX.A.B** - BullSequana XH2000, Xeon Platinum 8358 32C 2.6GHz, NVIDIA A100 SXM4 64 GB, Quad-rail NVIDIA HDR100 Infiniband, **Atos** Atos France	25,056	3.50	86	41.411
9	359	**MN-3** - MN-Core Server, Xeon Platinum 8260M 24C 2.40Hz, Preferred Networks MN-Core, MN-Core DirectConnect, **Preferred Networks** Preferred Networks Japan	1,664	2.18	53	40.901
10	331	**Champollion** - Apollo 6500, AMD EPYC 7763 64C 2.45GHz, NVIDIA A100 SXM4 80 GB, Mellanox HDR Infiniband, **HPE** Hewlett Packard Enterprise France	19,840	2.32	60	38.555

Top / Green 500

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2020 - Ampere GPU

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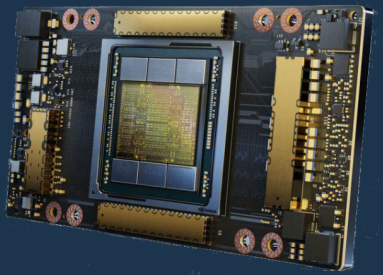
A100 (Ampere)



A100 SXM

2020 - Ampere GPU

7 nm

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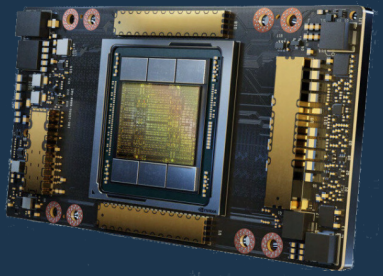

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Compute Capabilites **8.0**

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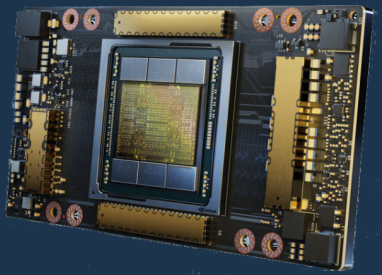

A100 SXM

2020 - Ampere GPU

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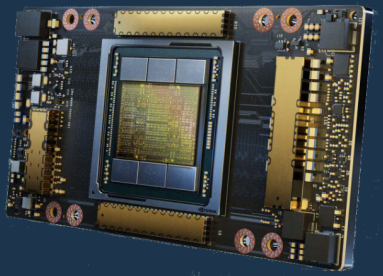

A100 SXM

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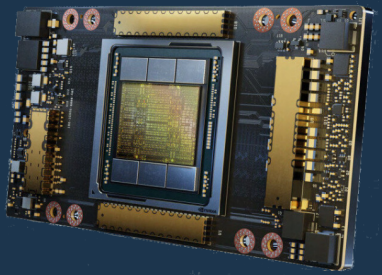
Compute Capabilites **8.0**

108 SMs **6912** Cores

2020 - Ampere GPU

A100 (Ampere)



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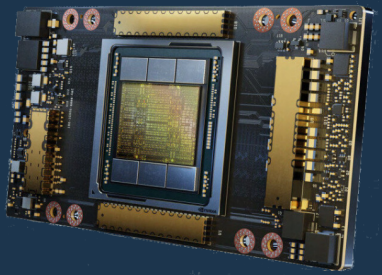

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2020 - Ampere GPU

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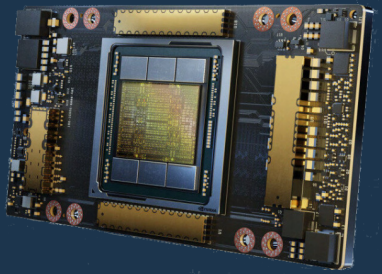

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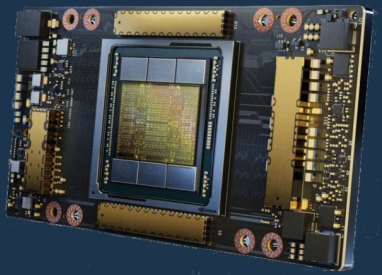
1.3 TB/s Bandwidth (**HBM2**)

2020 - Ampere GPU

A100 (Ampere)



A100 SXM

7 nm

Compute Capabilites **8.0**

108 SMs **6912** Cores

Peak **19.5 TFlops** (without tensor cores)

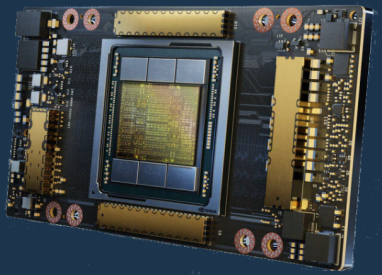
40 - **80** GB DRAM

1.3 TB/s Bandwidth (**HBM2**)

NVLink 600 GB/s

2020 - Ampere GPU

A100 (Ampere)



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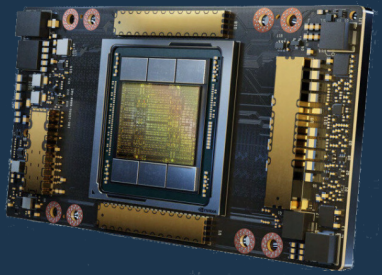

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MIG : **Multiple Instance GPU**

Too much for **PCIe** ?

2021 - Hardware evolution

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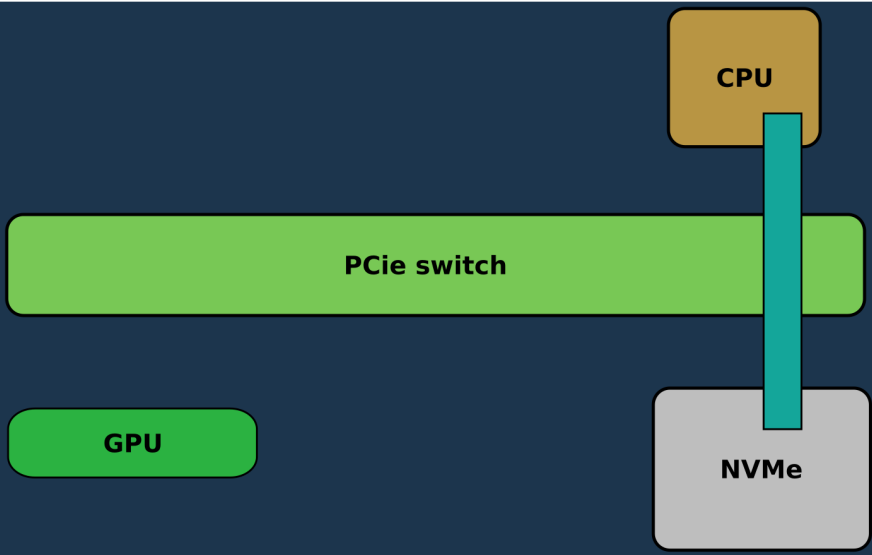
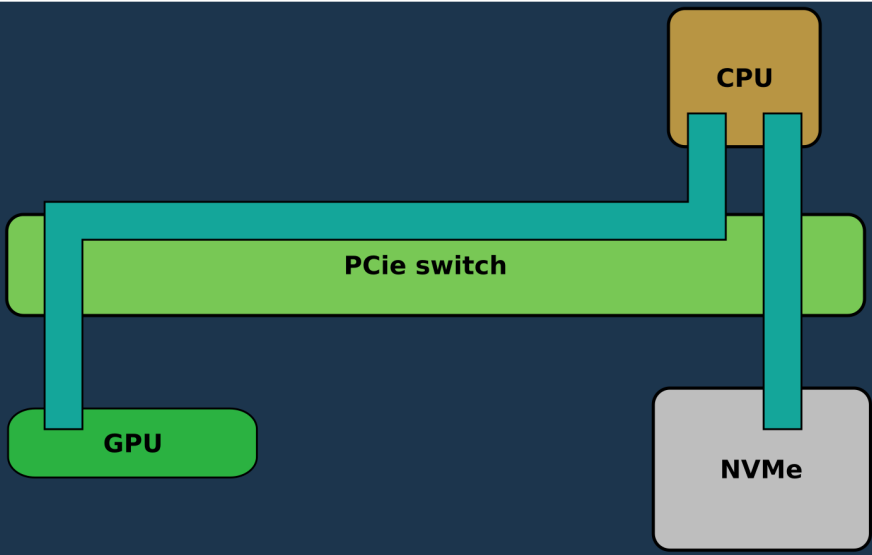


2021 - Hardware evolution



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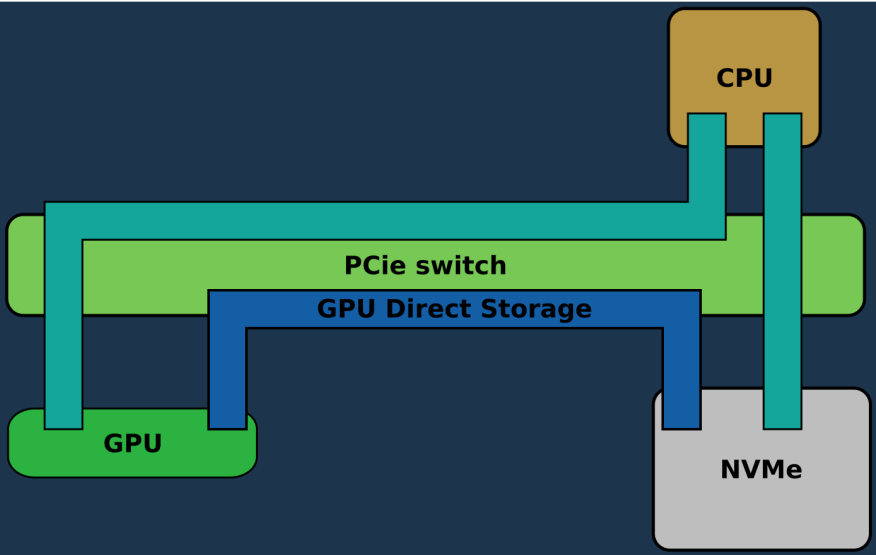
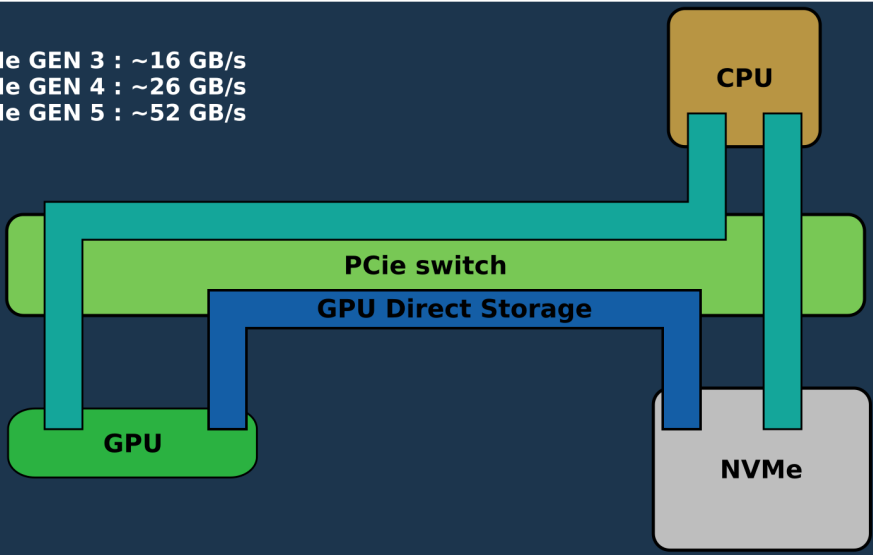


2021 - Hardware evolution

- PCIe GEN 3 : ~16 GB/s
- PCIe GEN 4 : ~26 GB/s
- PCIe GEN 5 : ~52 GB/s



NVCC, NVC++ evolution (NVidia)

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Today (2021)

NVCC, NVC++ evolution (NVidia)

Today (2021)

nvc++

C++17 : **std::transform**
Fortran : **do concurent**

NVCC, NVC++ evolution (NVidia)

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-stdpart
target GPU

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Compute Capabilities :
- Ampere : 8
- Turing : 7
- Volta : 7
- Pascal : 6

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nvcc

CUDA_ARCH

__host__
__device__
__global__

NVCC, NVC++ evolution (NVidia)

Today (2021)

Future (2022-2023)

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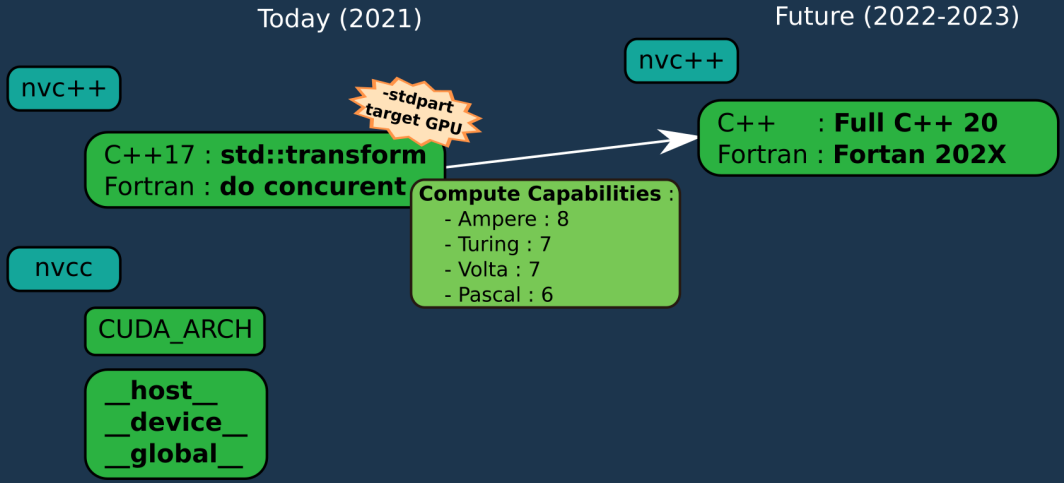
NVCC, NVC++ evolution (NVidia)



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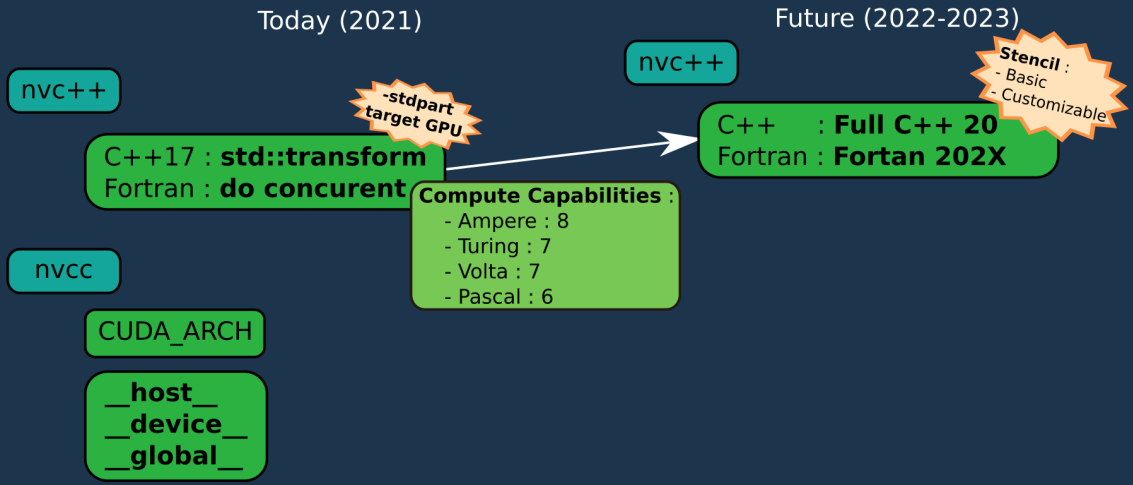

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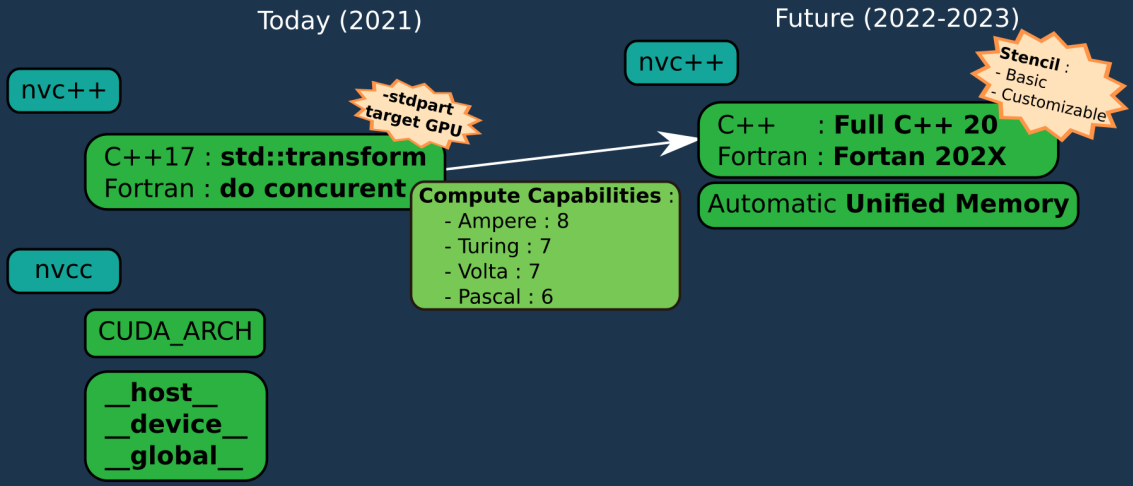

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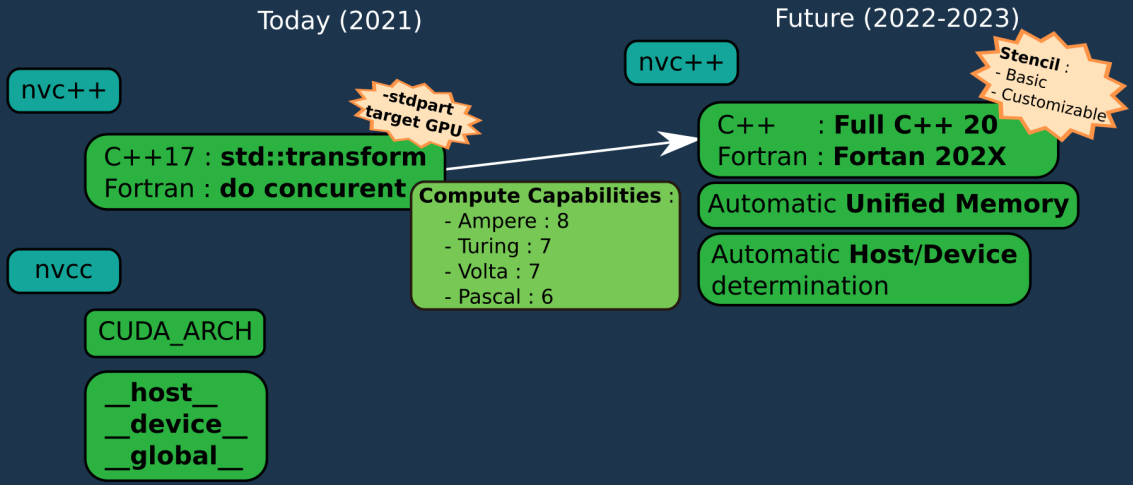

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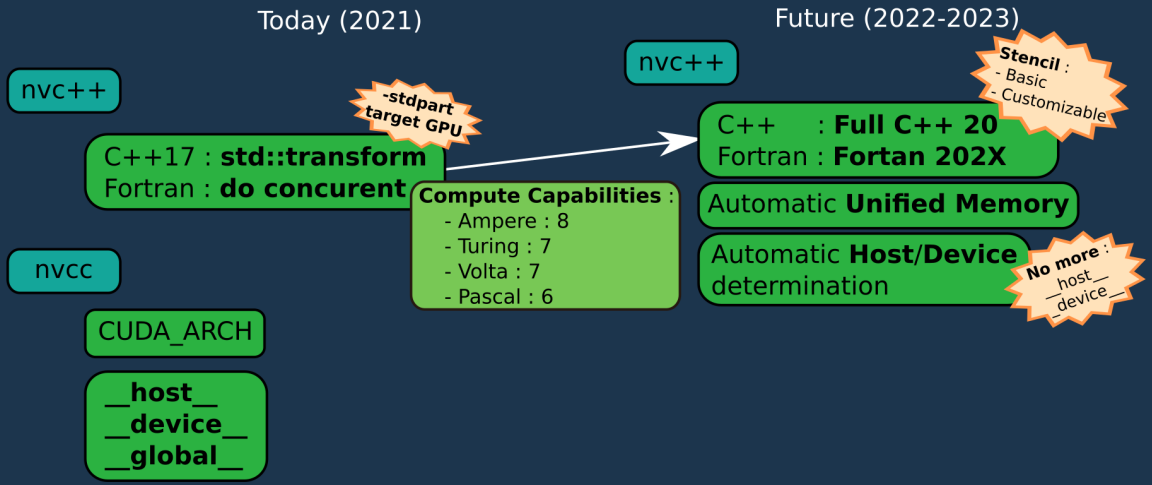

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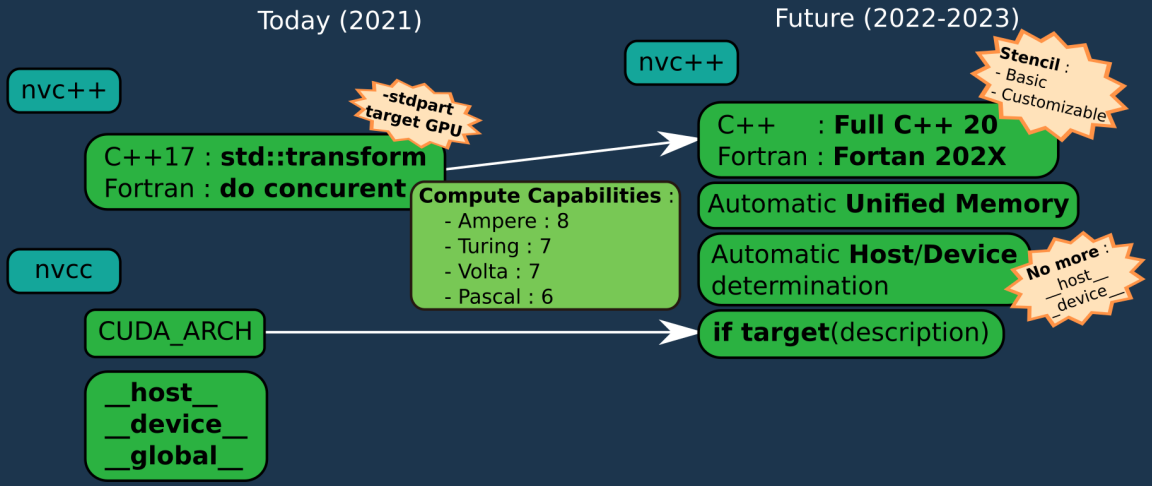

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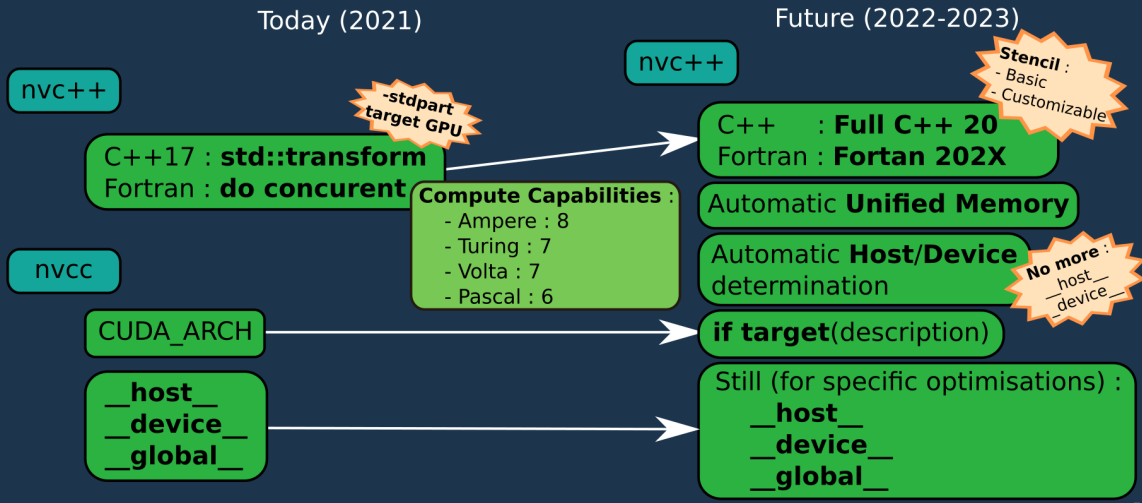


GPU and FORTRAN (NVFortran)

```
d = 2.5 * ceil(transpose(a)) + 3.0 * abs(transpose(b))
d = 2.5 * ceil(transpose(a)) + 3.0 * abs(b)
d = reshape(a,shape=[ni,nj,nk])
d = reshape(a,shape=[ni,nk,nj])
d = 2.5 * sqrt(reshape(a,shape=[ni,nk,nj],order=[1,3,2]))
d = alpha * conjg(reshape(a,shape=[ni,nk,nj],order=[1,3,2]))
d = reshape(a,shape=[ni,nk,nj],order=[1,3,2])
d = reshape(a,shape=[nk,ni,nj],order=[2,3,1])
d = reshape(a,shape=[ni*nj,nk])
d = reshape(a,shape=[nk,ni*nj],order=[2,1])
d = reshape(a,shape=[64,2,16,16,64],order=[5,2,3,4,1])
d = abs(reshape(a,shape=[64,2,16,16,64],order=[5,2,3,4,1]))
c = matmul(a,b)
c = matmul(transpose(a),b)
c = matmul(reshape(a,shape=[m,k],order=[2,1]),b)
c = matmul(a,transpose(b))
c = matmul(a,reshape(b,shape=[k,n],order=[2,1]))
```

```
c = matmul(transpose(a),transpose(b))
c = matmul(transpose(a),reshape(b,shape=[k,n],order=[2,1]))
d = spread(a,dim=3,ncopies=nk)
d = spread(a,dim=1,ncopies=ni)
d = spread(a,dim=2,ncopies=nx)
d = alpha * abs(spread(a,dim=2,ncopies=nx))
d = alpha * spread(a,dim=2,ncopies=nx)
d = abs(spread(a,dim=2,ncopies=nx))
d = transpose(a)
d = alpha * transpose(a)
d = alpha * ceil(transpose(a))
d = alpha * conjg(transpose(a))
c = c + matmul(a,b)
c = c - matmul(a,b)
c = c + alpha * matmul(a,b)
d = alpha * matmul(a,b) + c
d = alpha * matmul(a,b) + beta * c
```

Paradigms evolution

Current default situation

New default situation

Paradigms evolution

Current default situation

Scalar

New default situation

Paradigms evolution

Current default situation

Scalar

Single-threaded

New default situation

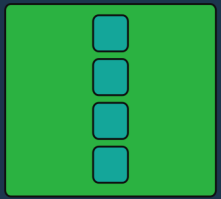
Paradigms evolution

Current default situation

Scalar

Single-threaded

Execution **in order**



New default situation

Paradigms evolution

Current default situation

Scalar

Single-threaded

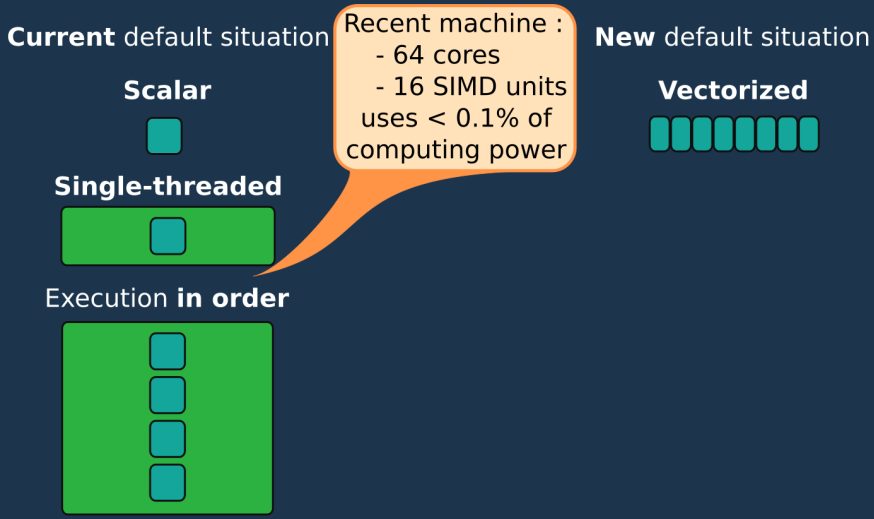
Execution **in order**

Recent machine :
- 64 cores
- 16 SIMD units

uses < 0.1% of computing power

New default situation

Paradigms evolution



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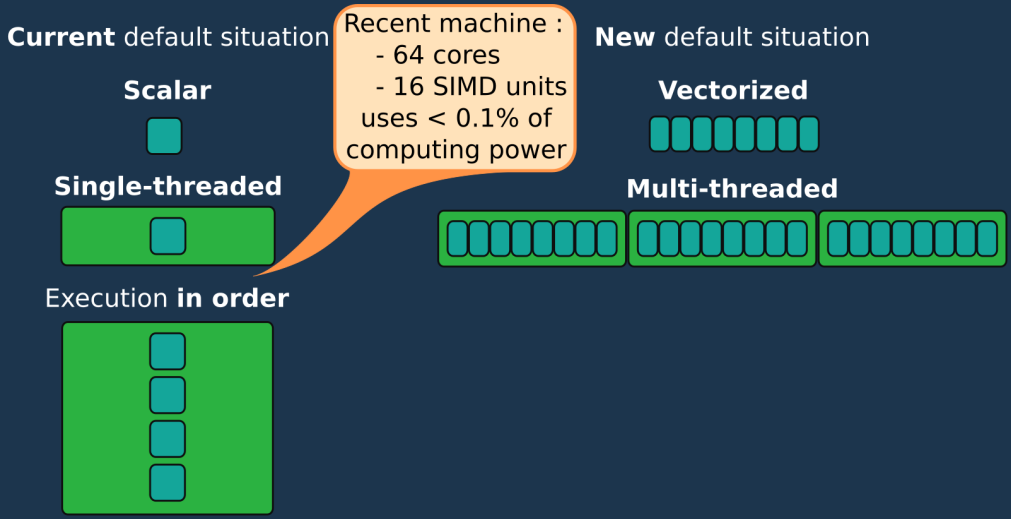

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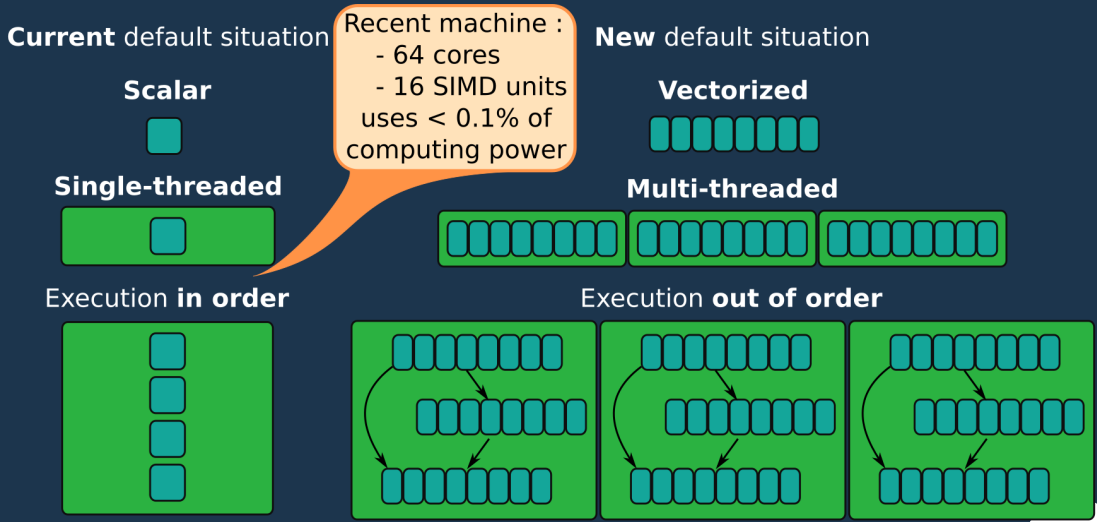

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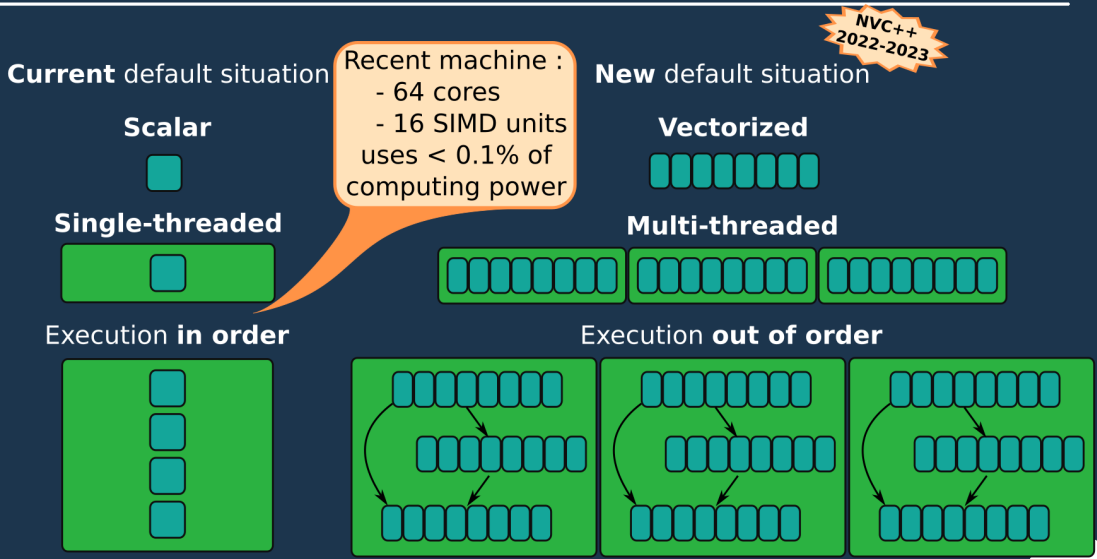
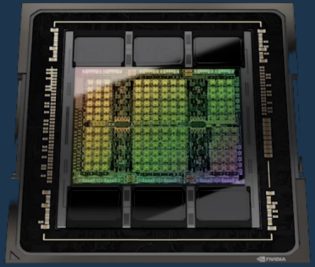


2022 - Hopper GPU

2022 - Hopper GPU

H100 (Hopper)



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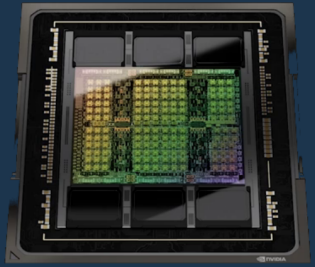
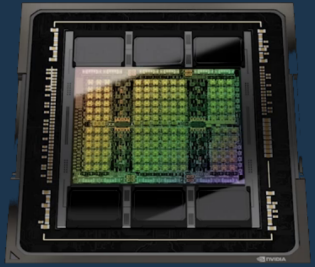


H100 SXM5 and PCie

2022 - Hopper GPU

4 nm (A100 7 nm)

H100 (Hopper)



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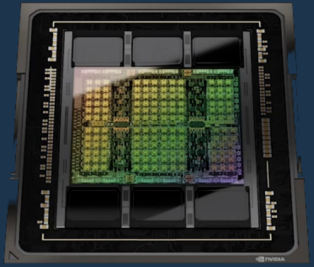


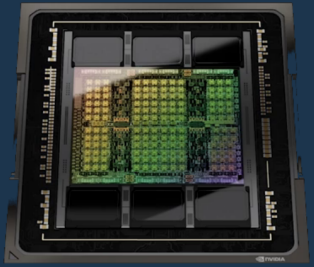
H100 SXM5 and PCie

4 nm (A100 7 nm)

Compute Capabilites 9.0

2022 - Hopper GPU

H100 (Hopper)



H100 SXM5 and PCie

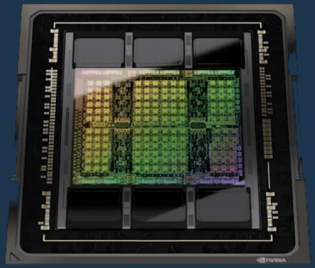
4 nm (A100 7 nm)

Compute Capabilites 9.0

132 SMs (tensor core Gen4) 8448 Cores

2022 - Hopper GPU

H100 (Hopper)



H100 SXM5 and PCie

4 nm (A100 7 nm)

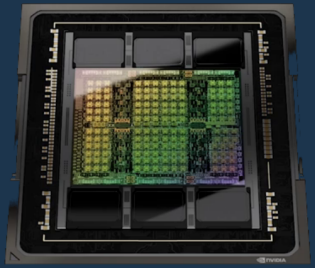
Compute Capabilites 9.0

132 SMs (tensor core Gen4) 8448 Cores

80 GB DRAM

2022 - Hopper GPU

H100 (Hopper)



H100 SXM5 and PCie

4 nm (A100 7 nm)

Compute Capabilites 9.0

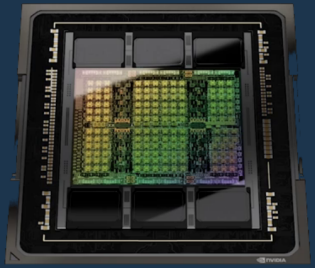
132 SMs (tensor core Gen4) 8448 Cores

80 GB DRAM

3 TB/s Bandwidth (HBM3)

2022 - Hopper GPU

H100 (Hopper)



H100 SXM5 and PCie

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Compute Capabilites 9.0

132 SMs (tensor core Gen4) 8448 Cores

80 GB DRAM

3 TB/s Bandwidth (HBM3)

NVLink Gen 4 (900 GB/s)

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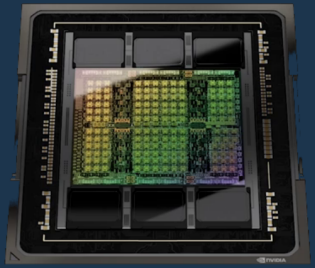

H100 SXM5 and PCie

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- MIG Gen 2 with confidential computing
  (all instances have Image/Video decoding)

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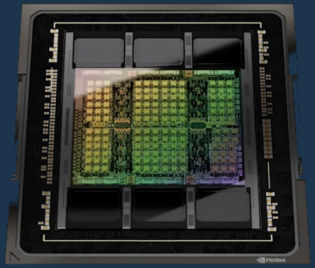

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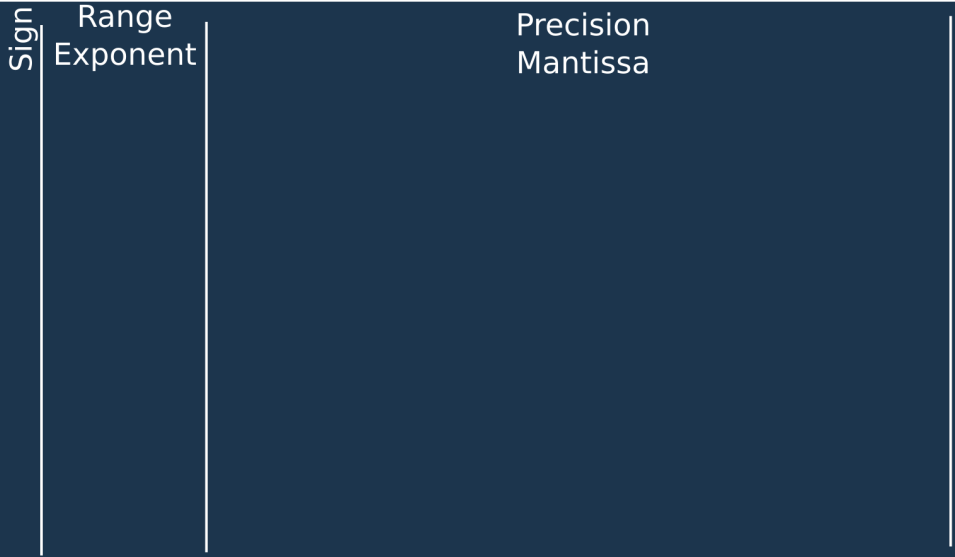
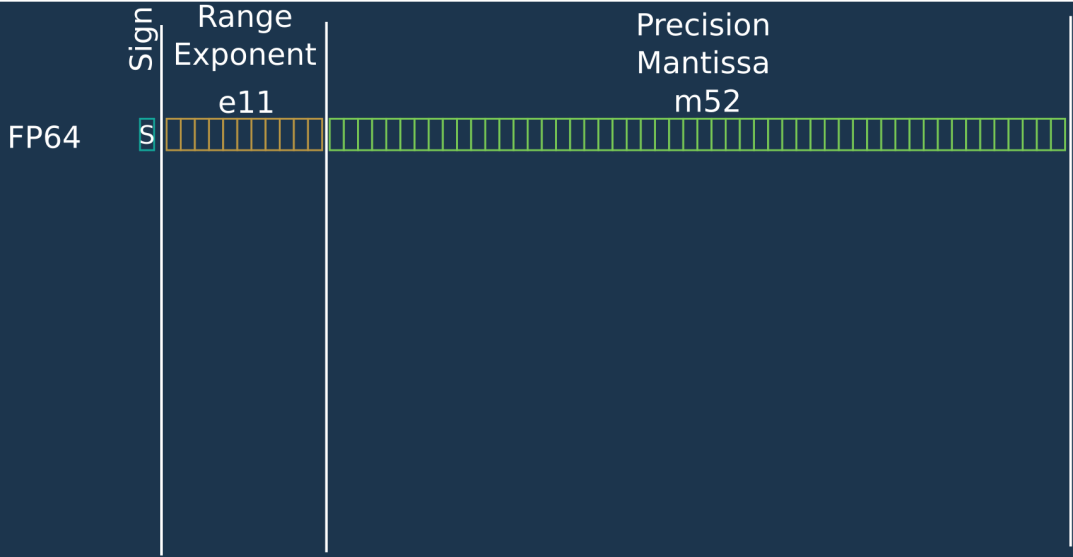
- A lot a computing precisions

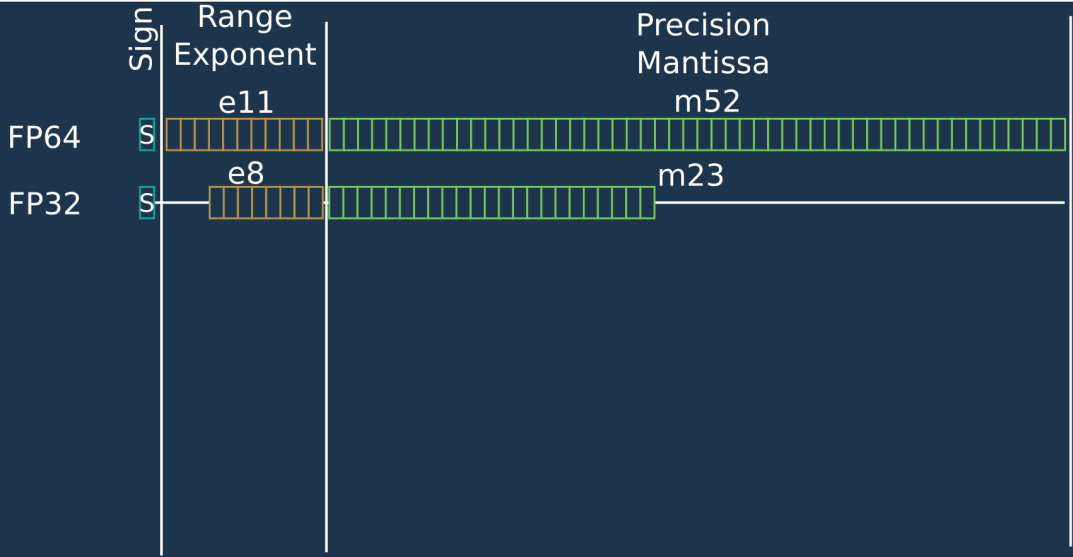
Computing Precision



Computing Precision



Computing Precision



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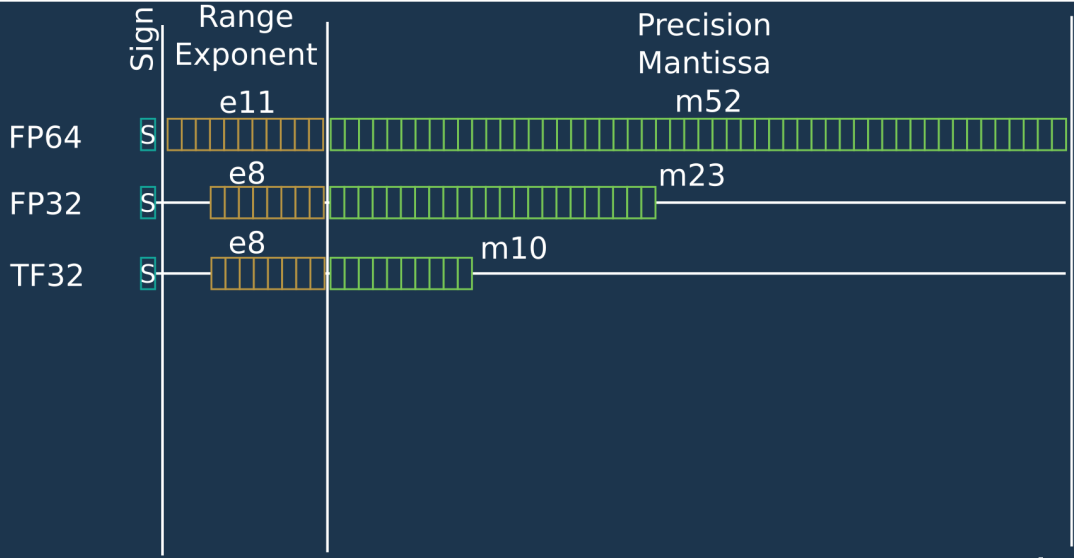

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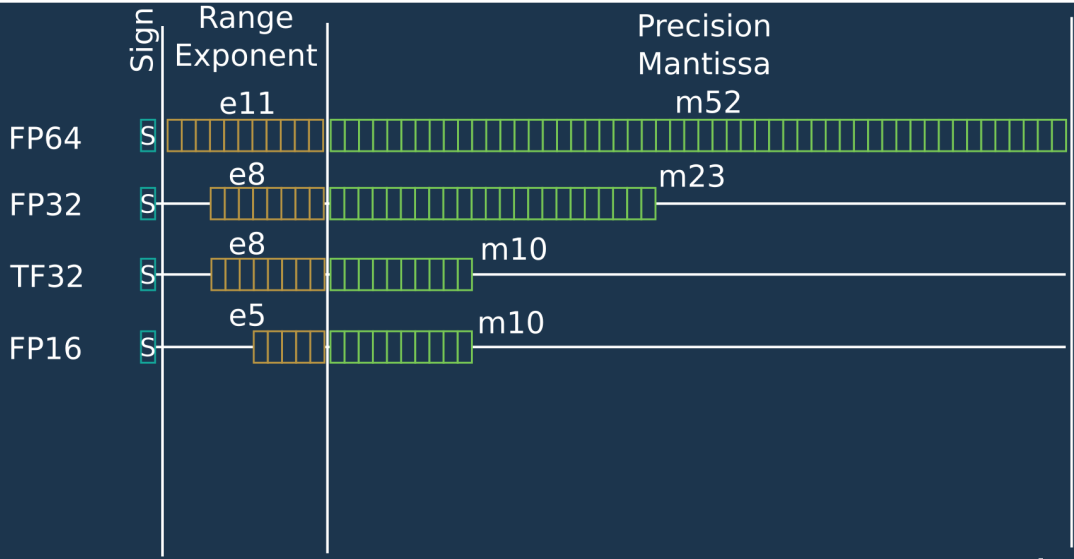
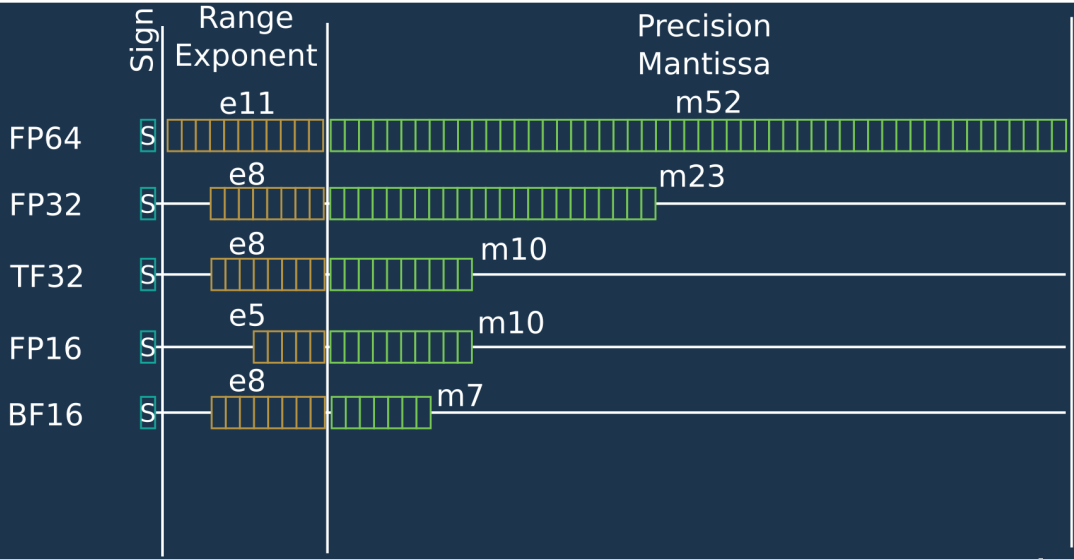
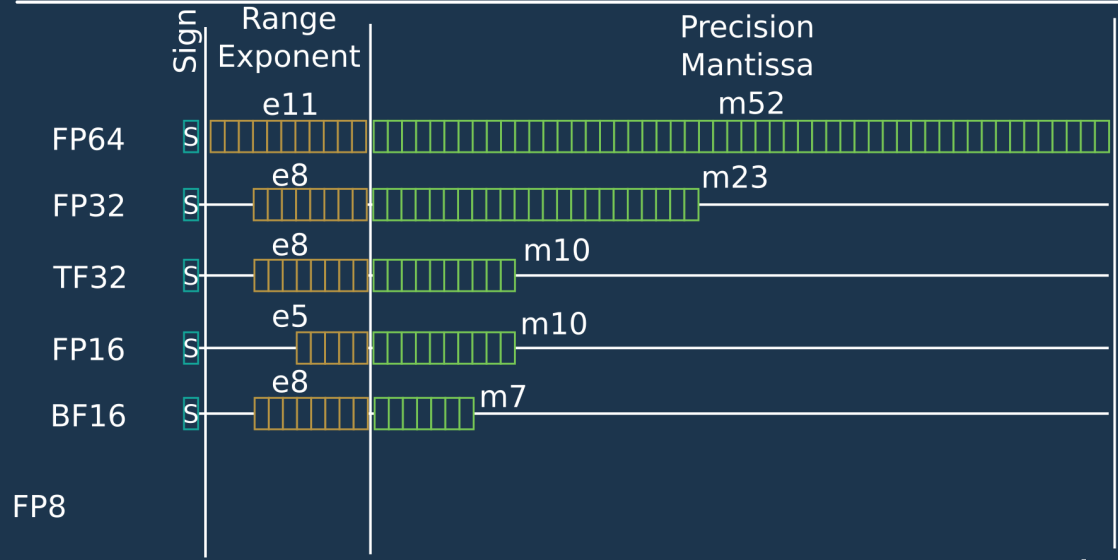


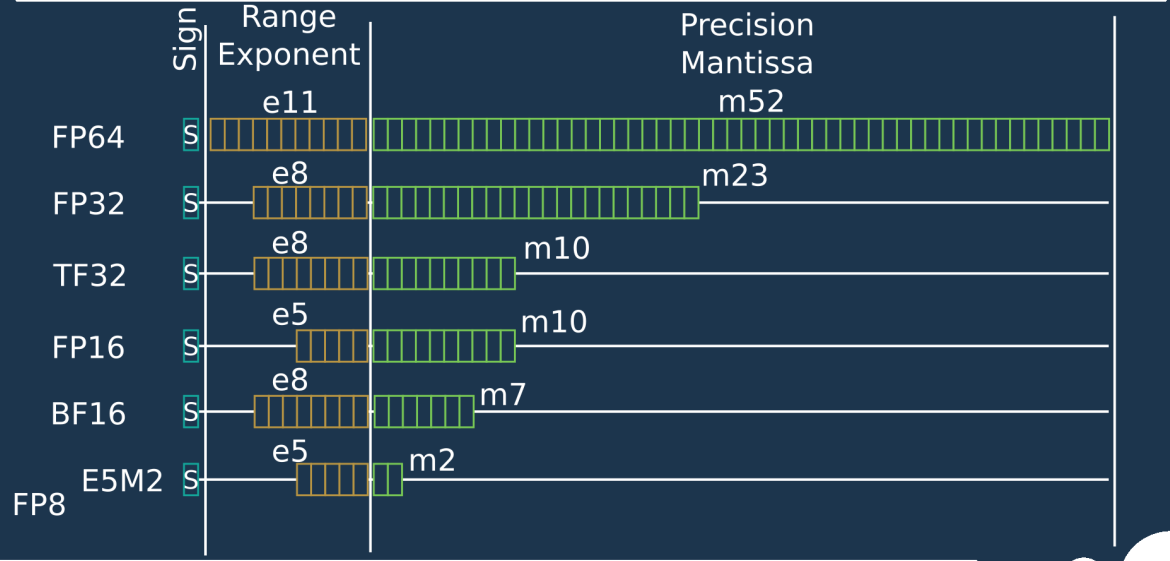
Computing Precision



Computing Precision



Computing Precision



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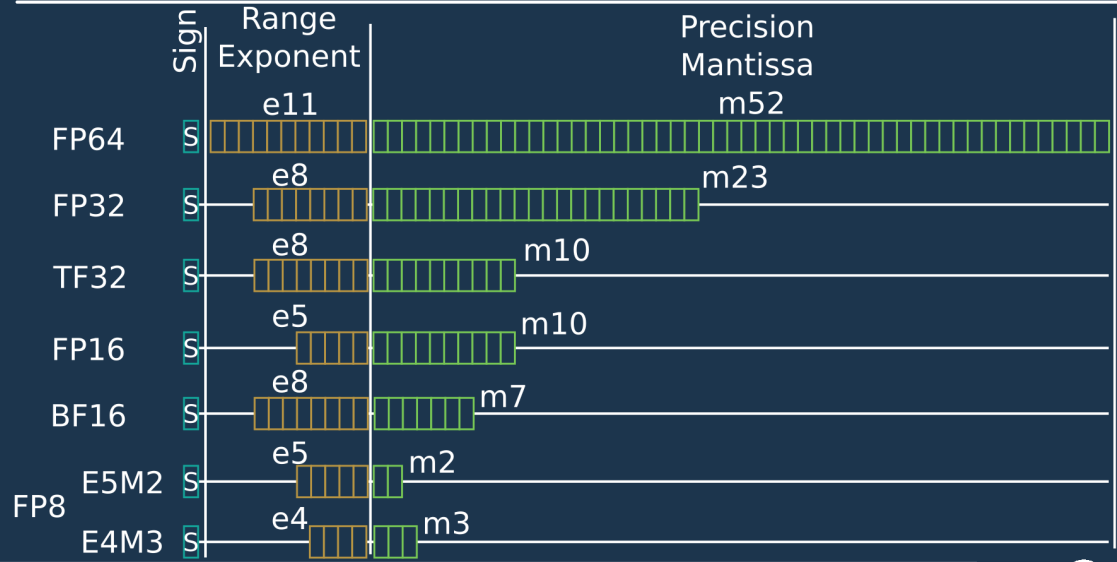

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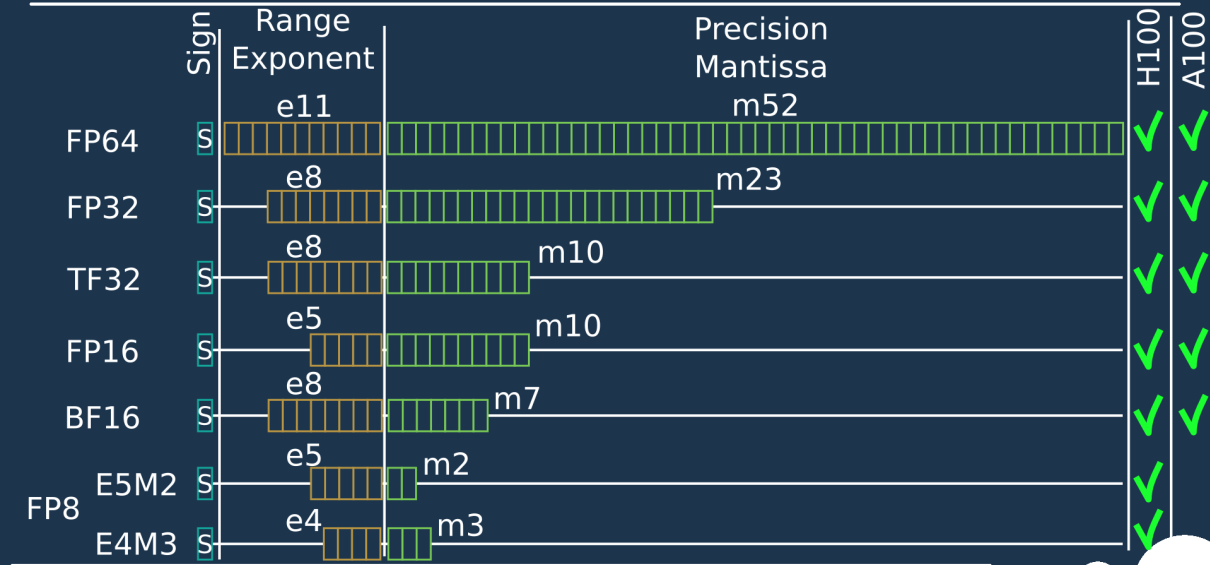
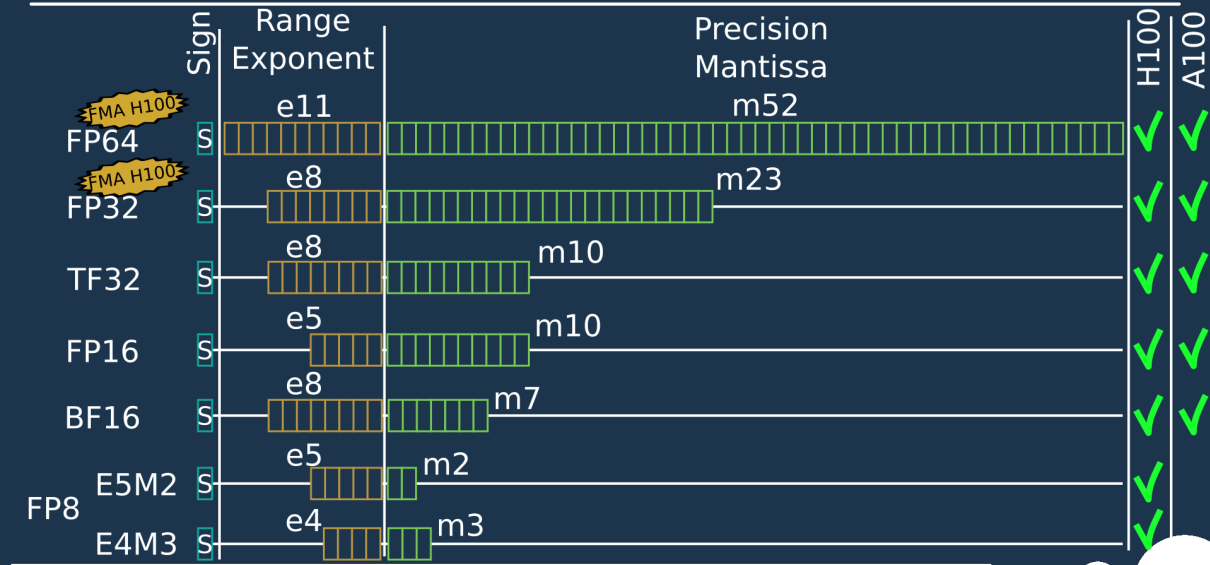
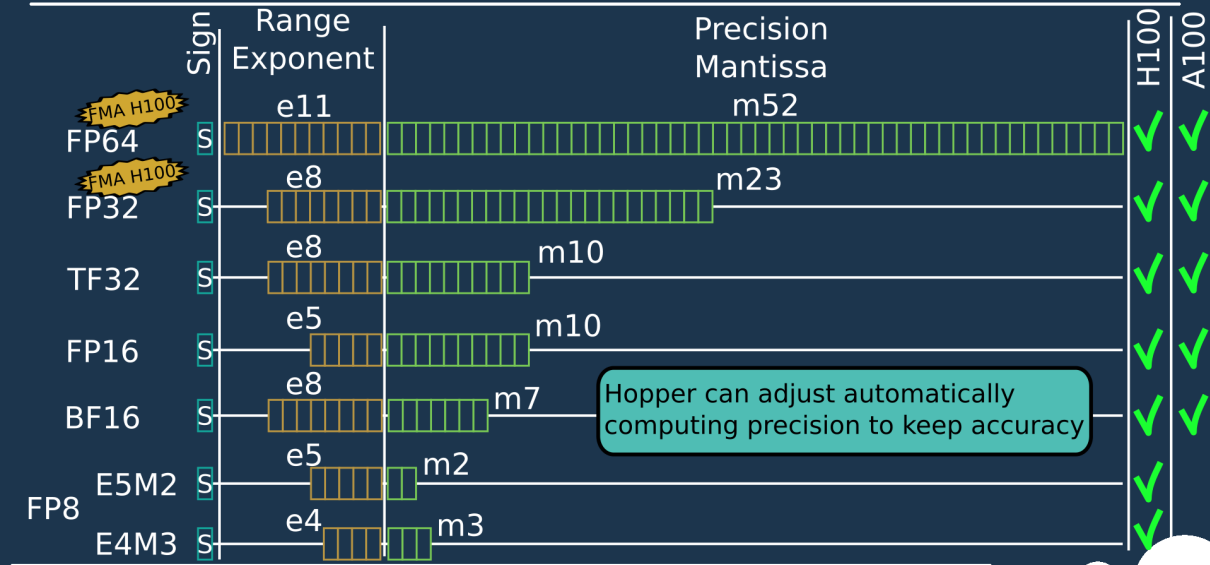


Computing Precision



Computing Precision



Why all these computing precisions ?

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Lower precision are **fast** to compute

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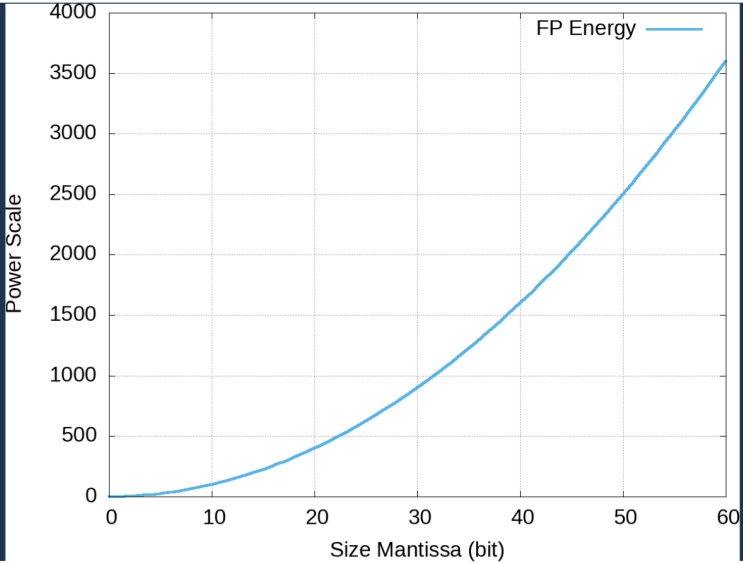

Lower precision are **fast** to compute

Consuption is mostly **proportional** to the **square** of **mantissa** size

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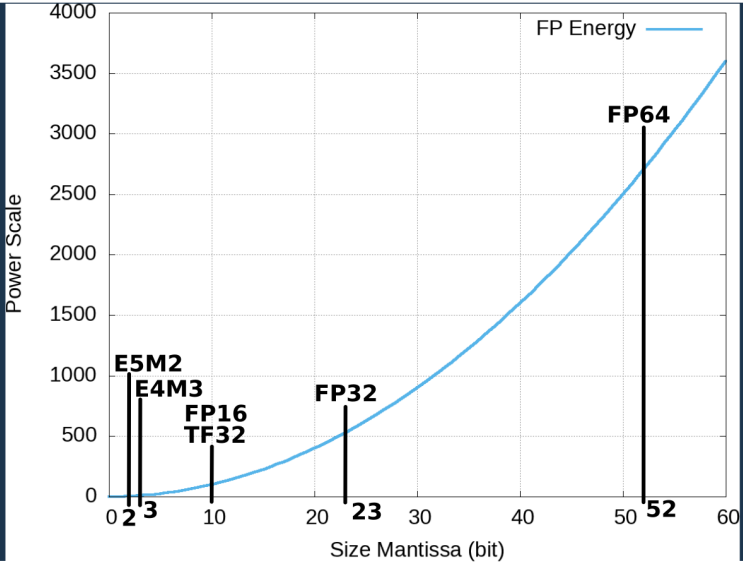

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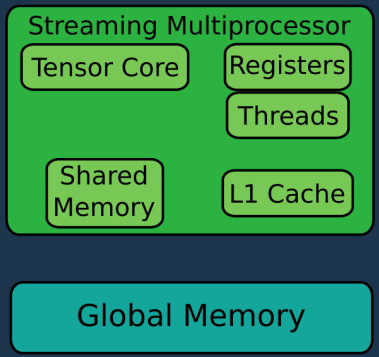
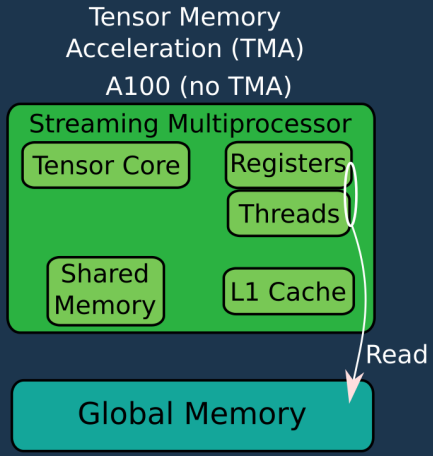
Thread acceleration

Thread acceleration

Tensor Memory Acceleration (TMA)



Thread acceleration



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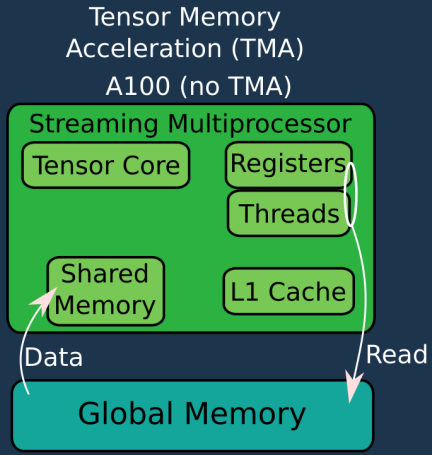

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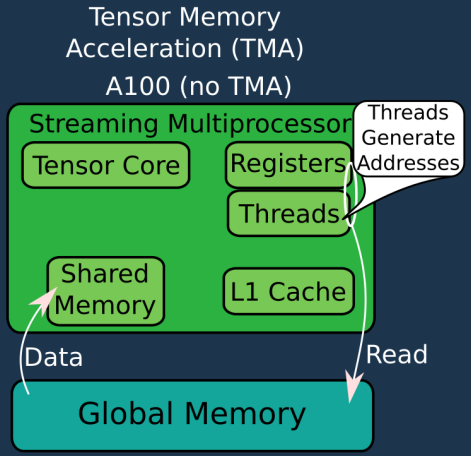

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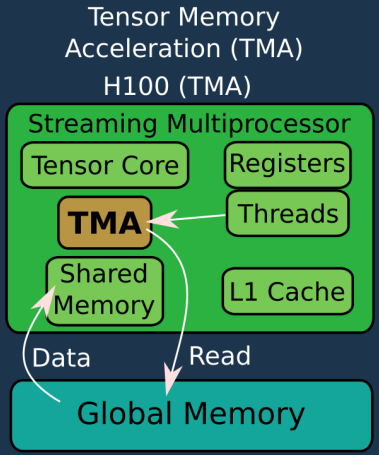
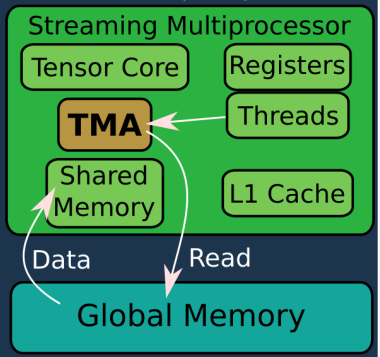


Thread acceleration

Tensor Memory Acceleration (TMA)

H100 (TMA)

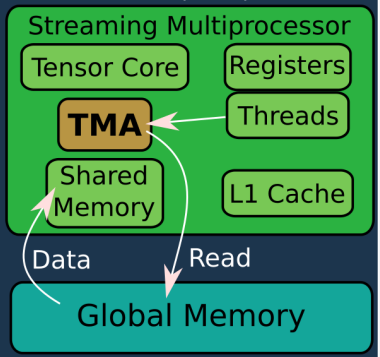


Distributed shared memory

Thread acceleration

Tensor Memory Acceleration (TMA)

H100 (TMA)



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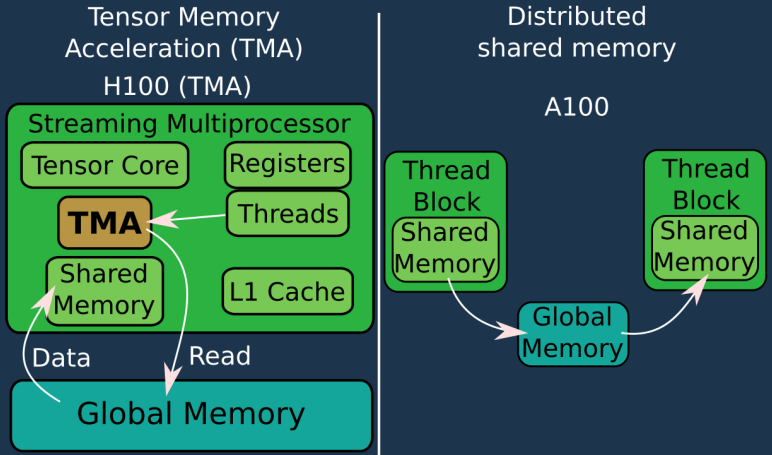

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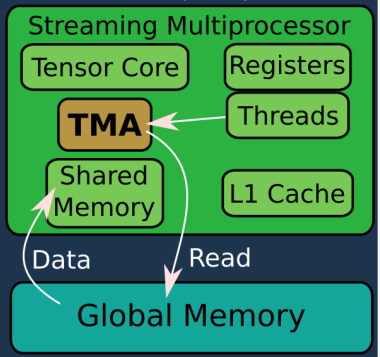

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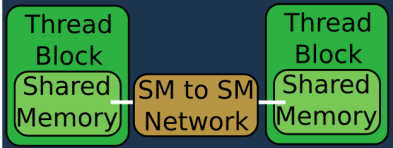
H100



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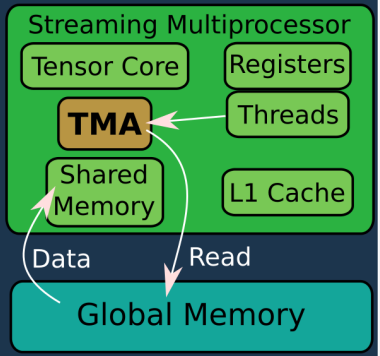

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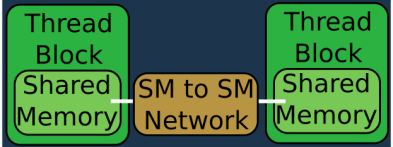
H100



Asynchronous Transaction Barrier

Thread acceleration

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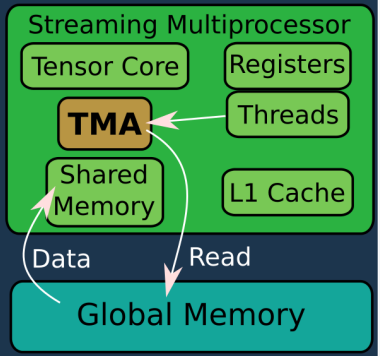

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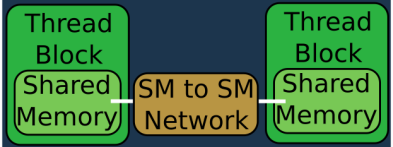

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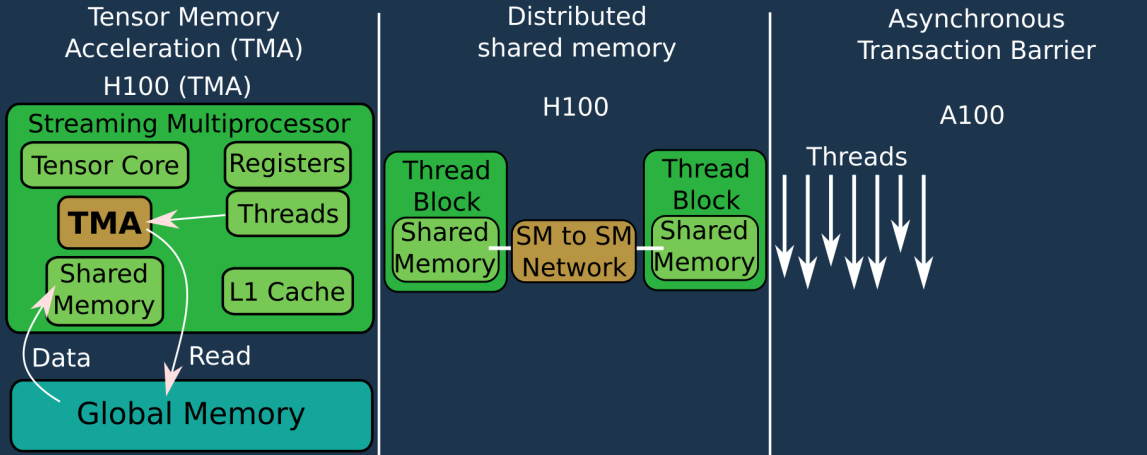

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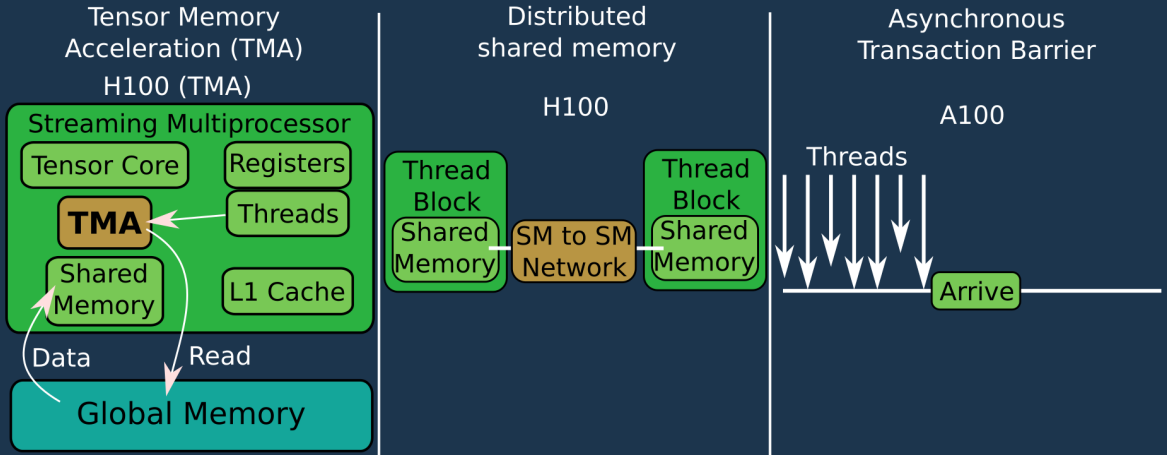

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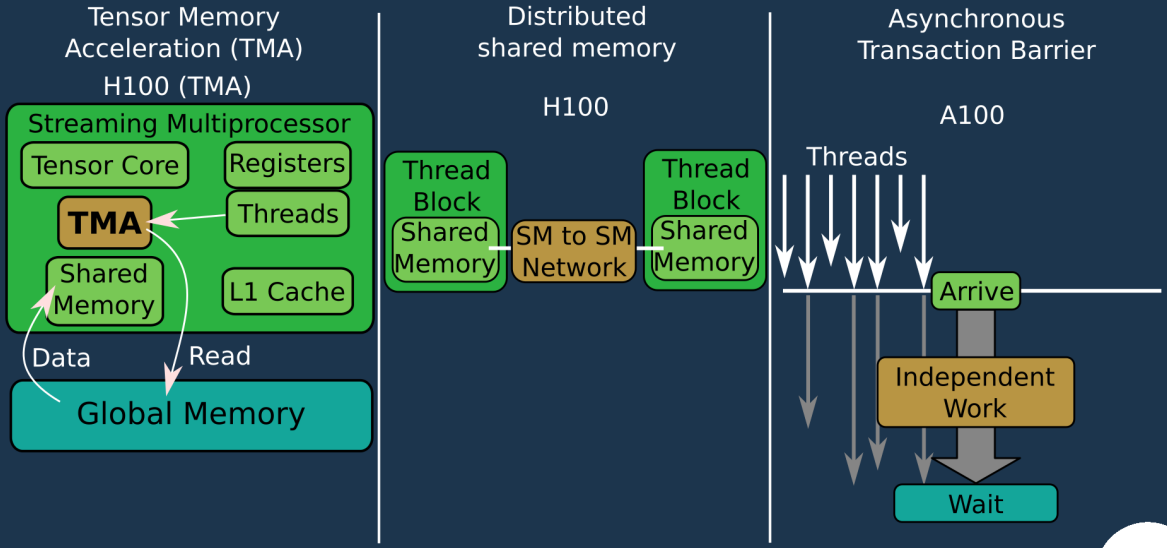

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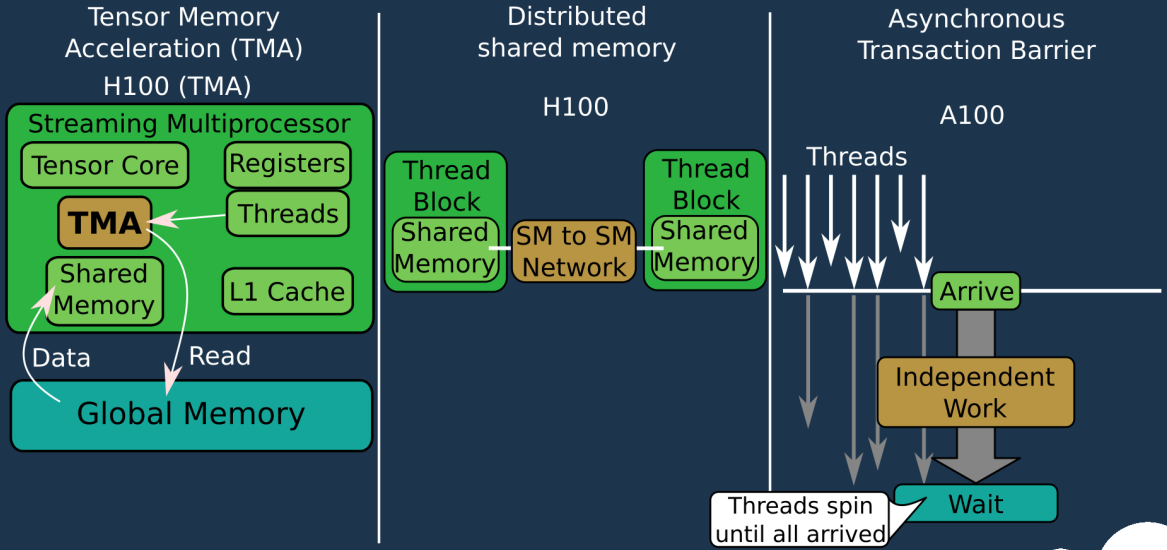

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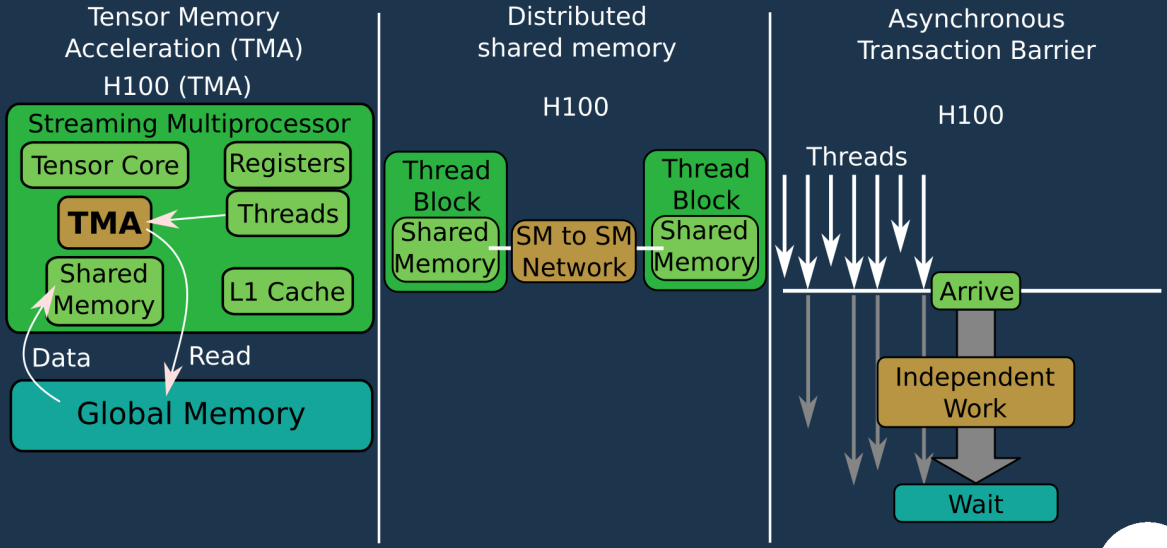

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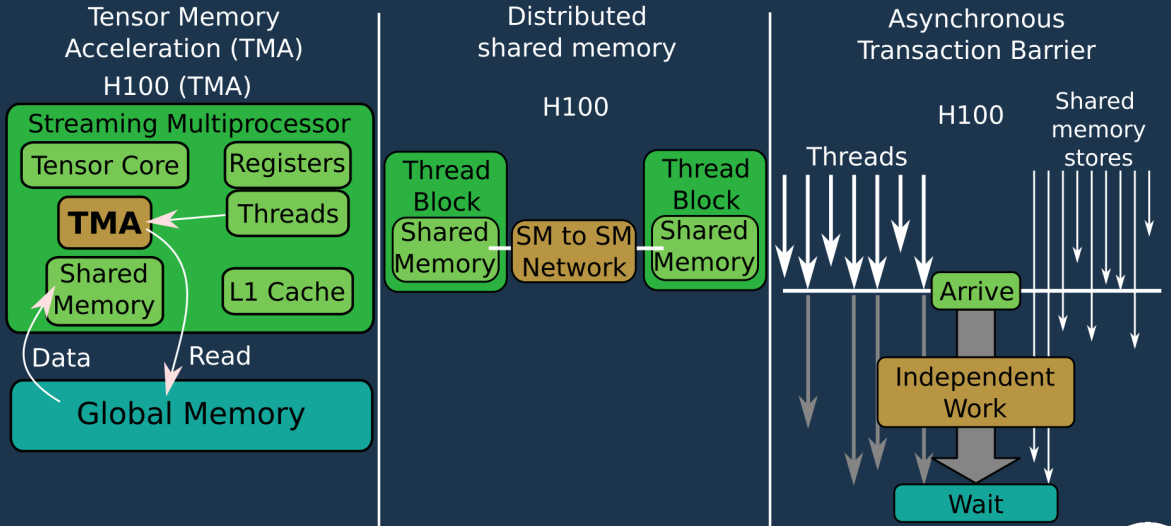

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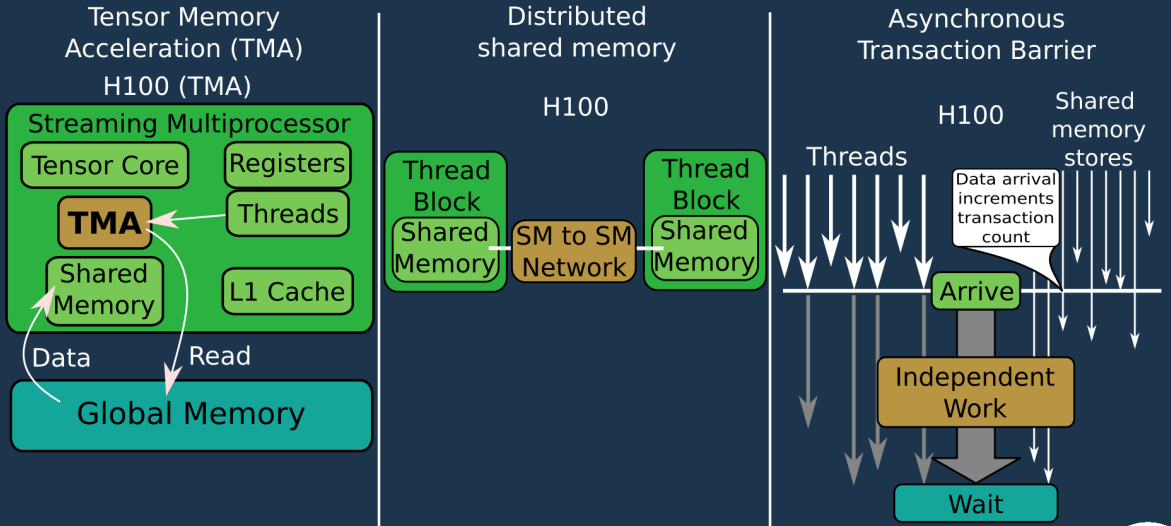

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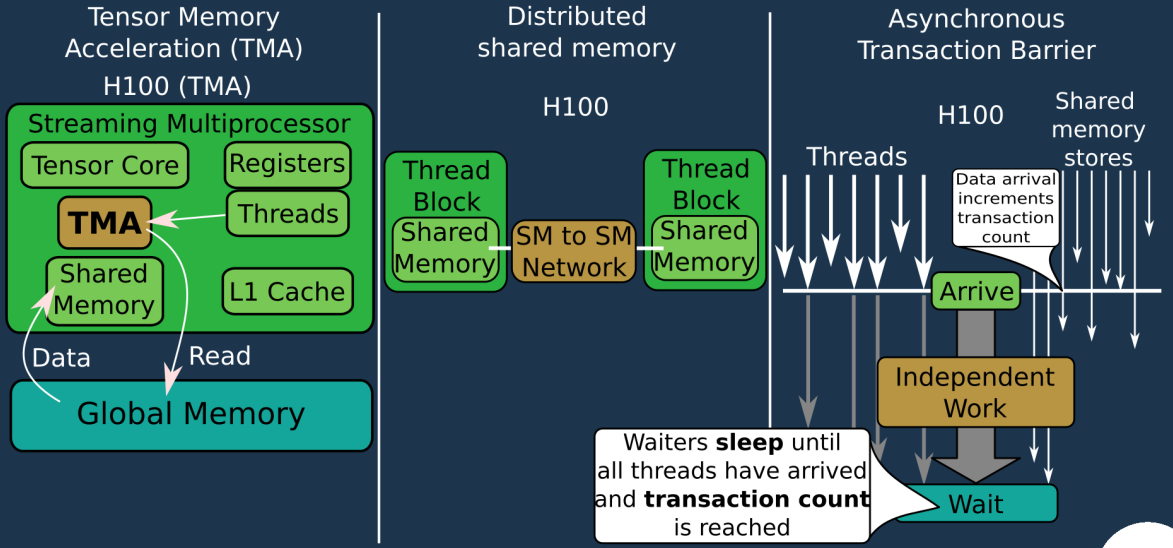

New intrinsic functions

New intrinsic functions

Dynamic Programming Acceleration (DPX) : recursive algorithms

New intrinsic functions

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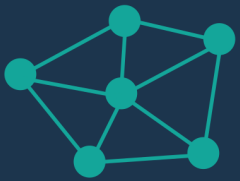
Floyd-Warshall Algorithm

Route optimization



New intrinsic functions

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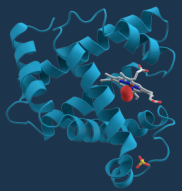
Smith-Waterman and **Needleman-Wunsch** Algorithm

Pattern Matching

- DNA sequence alignment
- Protein classification
- Protein folding



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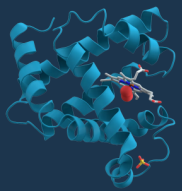
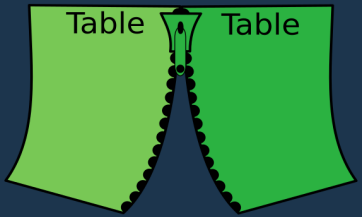


SQL Query optimisation

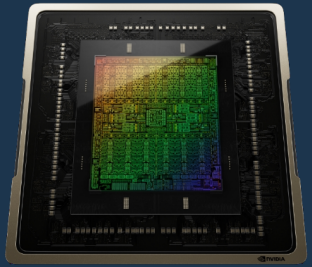
Join in optimal order



Hardware evolution

Hardware evolution

GeForce 4090
(Ada Lovelace)



Hardware evolution

4 nm (A100 7 nm)

GeForce 4090
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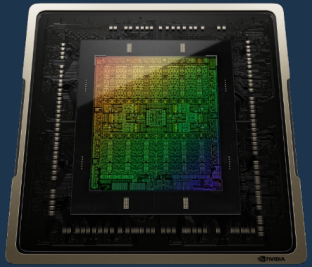

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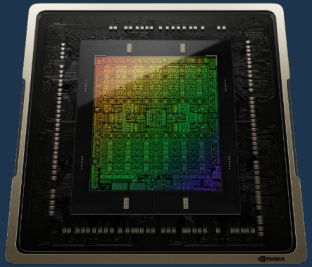

4 nm (A100 7 nm)

128 SMs (tensor core Gen4) 16384 Cuda Cores

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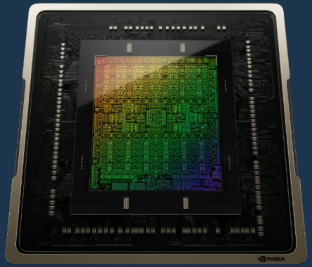

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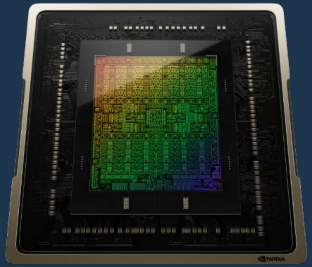

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1 TB/s Bandwidth

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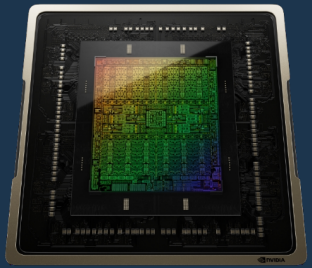

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Peak 82 TFlops (FP32 without tensor cores)

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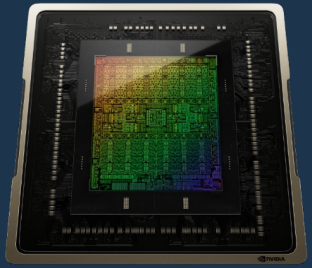

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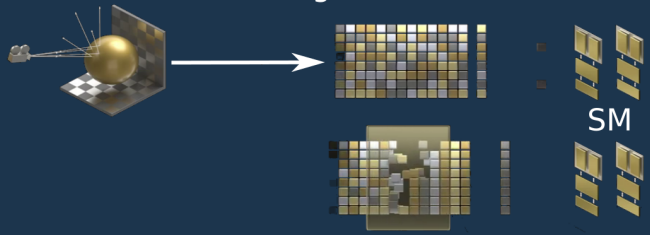
Shader Reordering



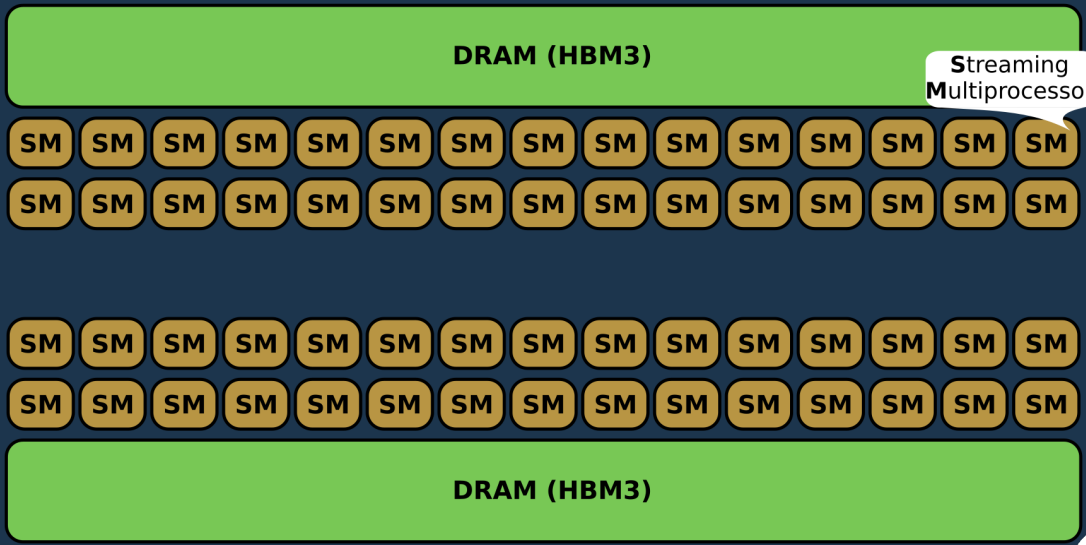
GPU Architecture

GPU Architecture

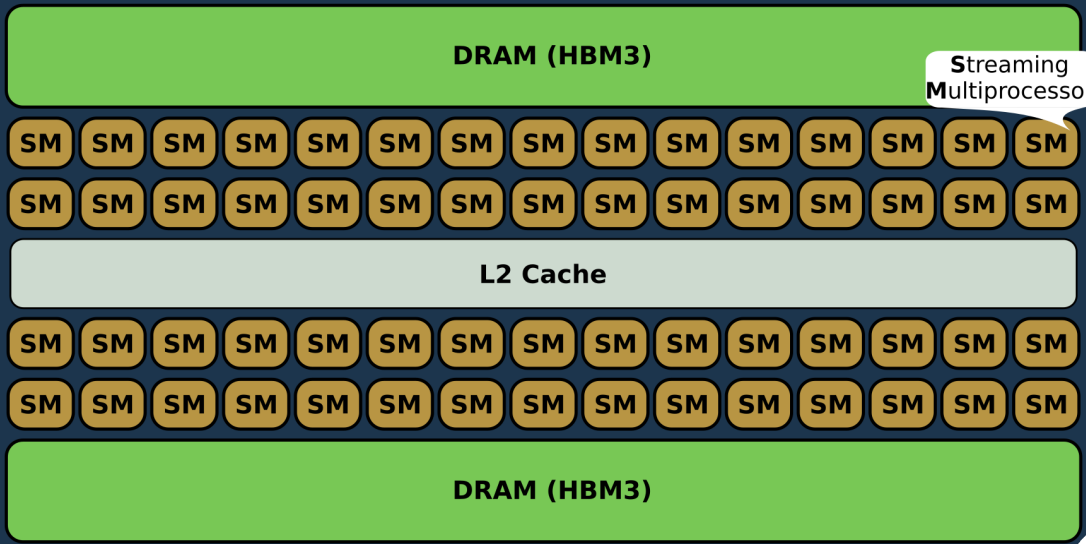
DRAM (HBM3)

DRAM (HBM3)

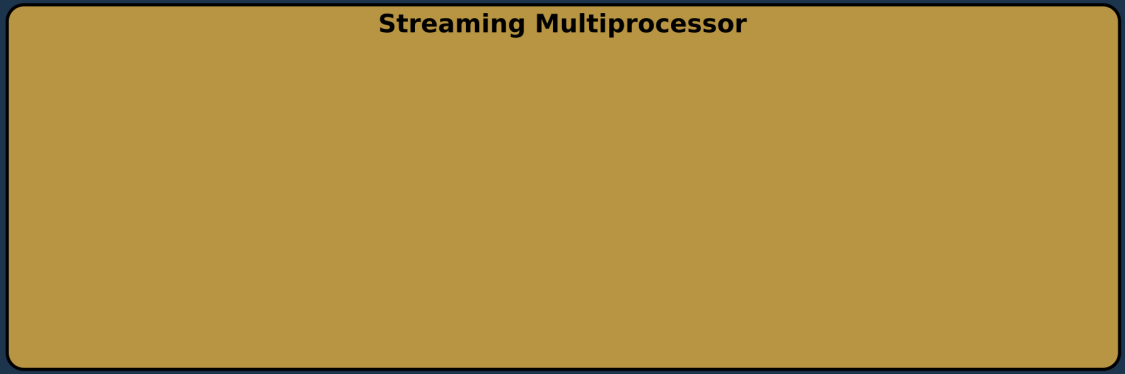
GPU Architecture



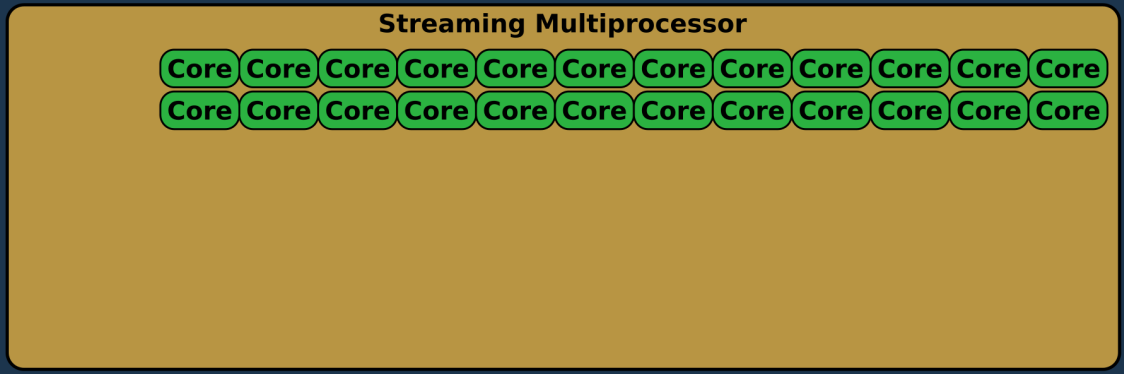
GPU Architecture



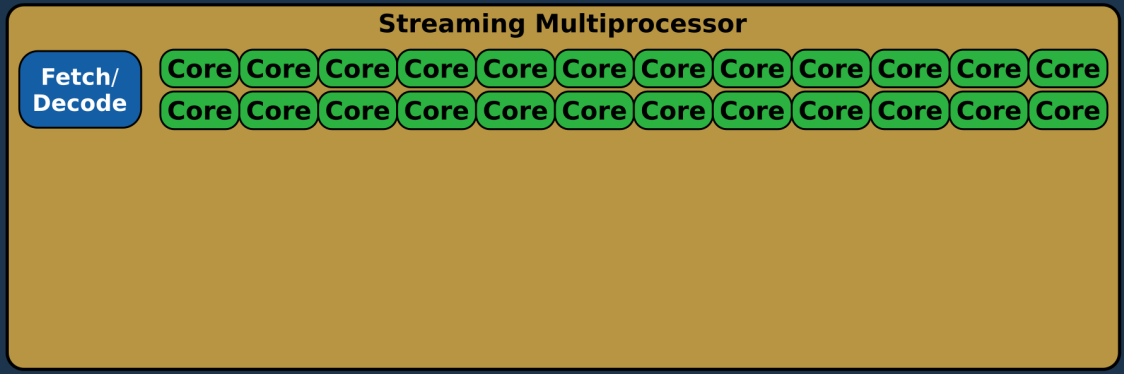
Streaming Multiprocessor



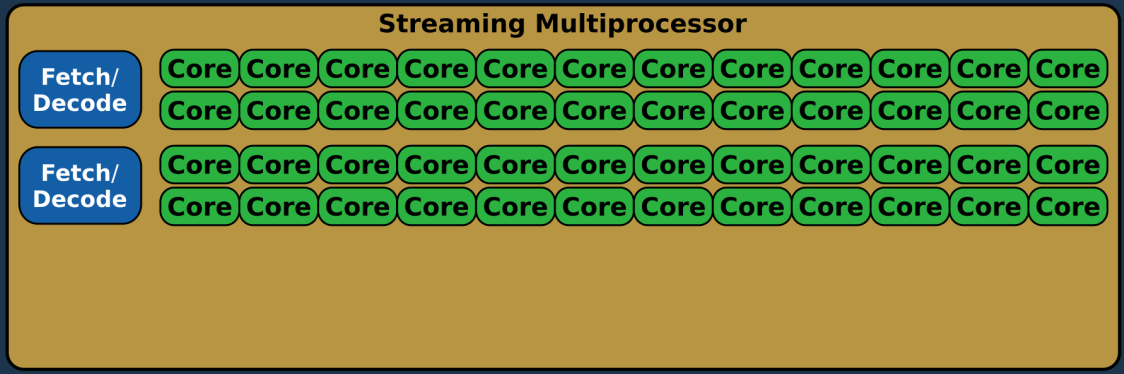
Streaming Multiprocessor



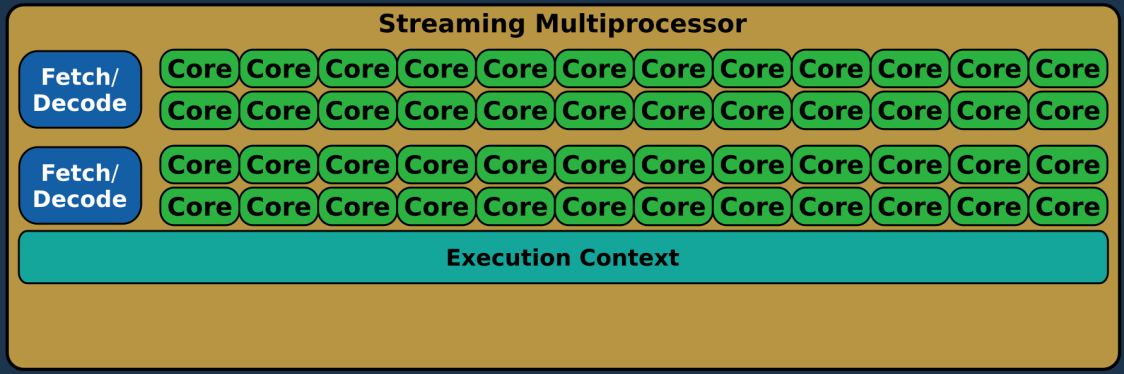
Streaming Multiprocessor



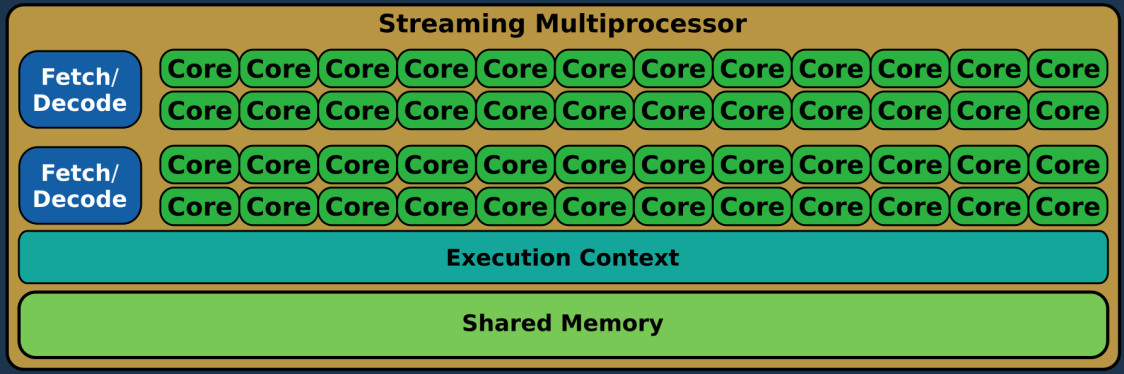
Streaming Multiprocessor



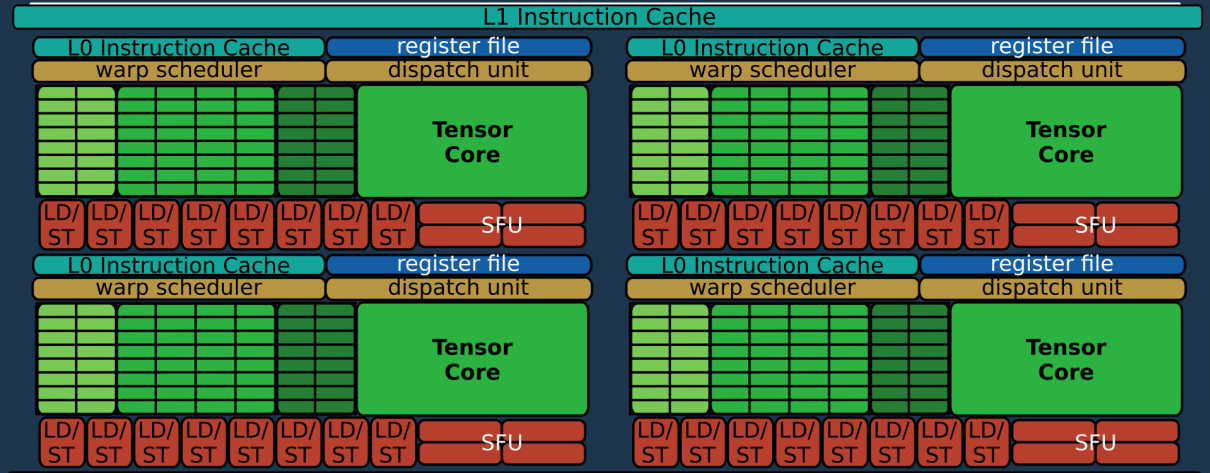
Streaming Multiprocessor



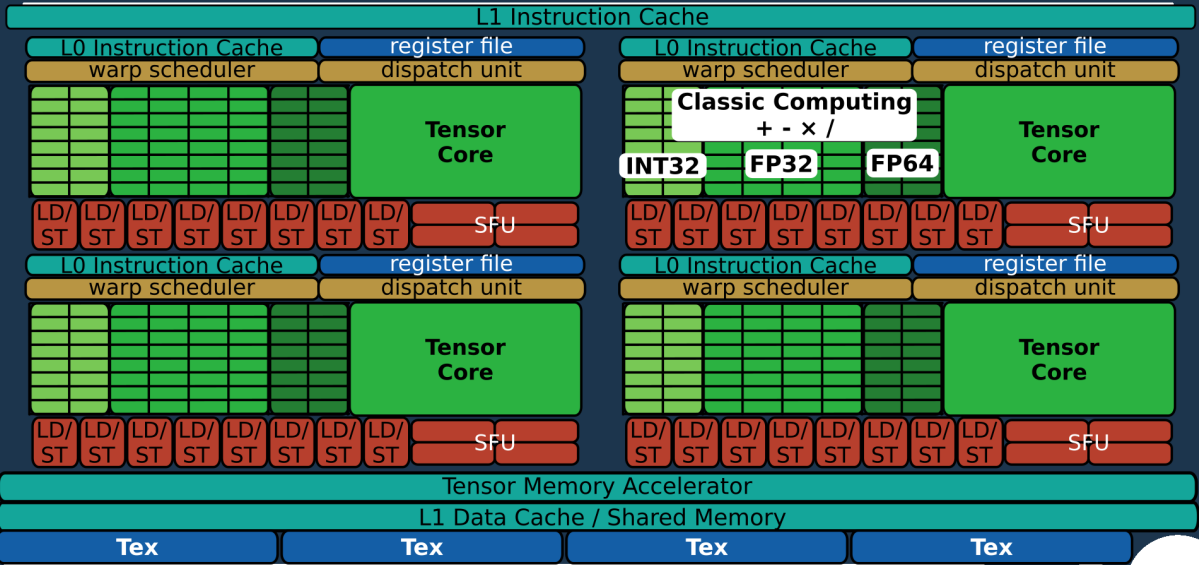
Streaming Multiprocessor



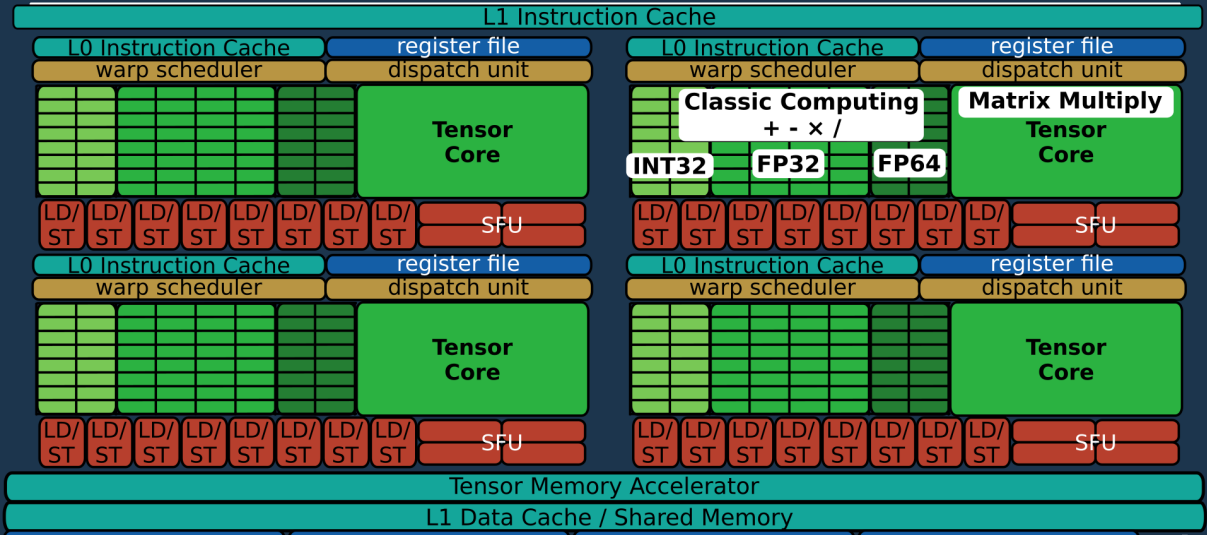
Streaming Multiprocessor H100



Streaming Multiprocessor H100

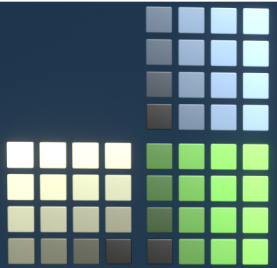


Streaming Multiprocessor H100

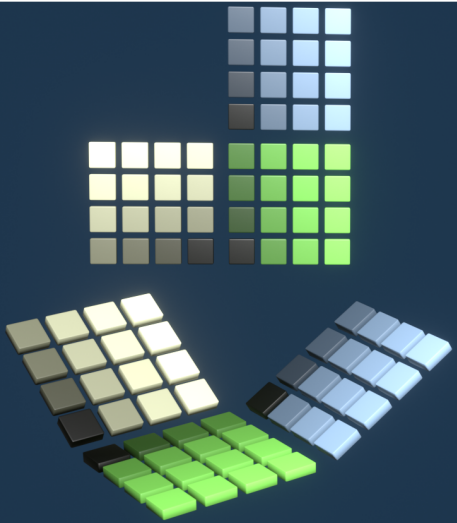


Tensor Core

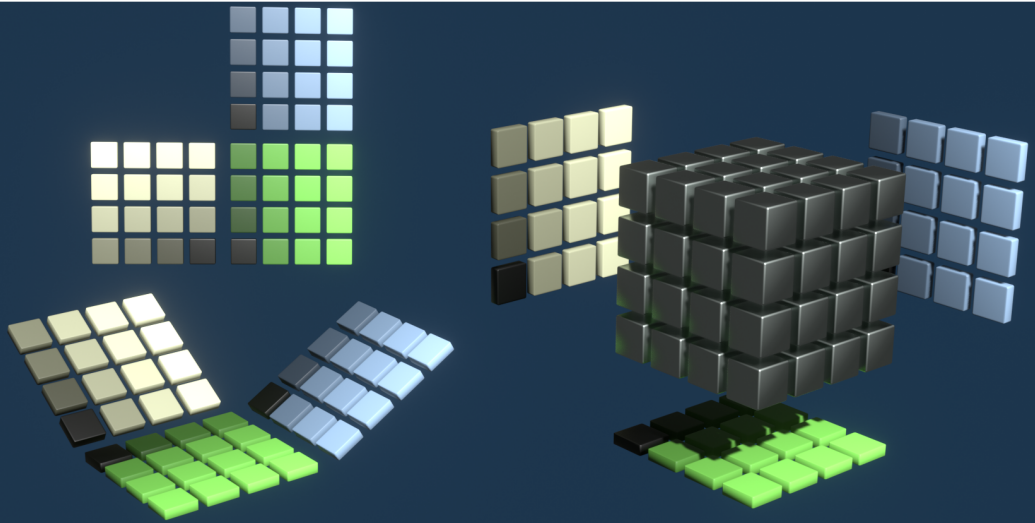
Tensor Core



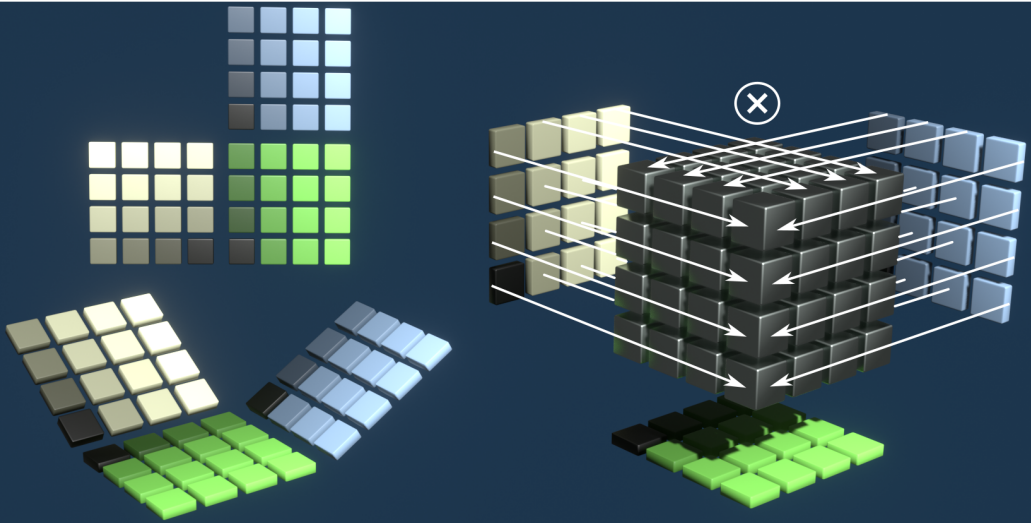
Tensor Core



Tensor Core



Tensor Core



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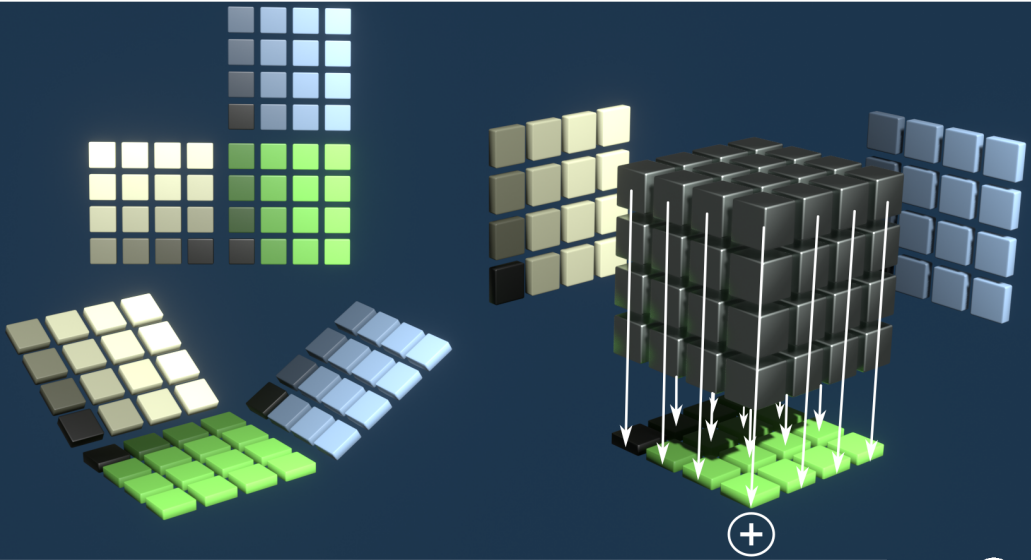

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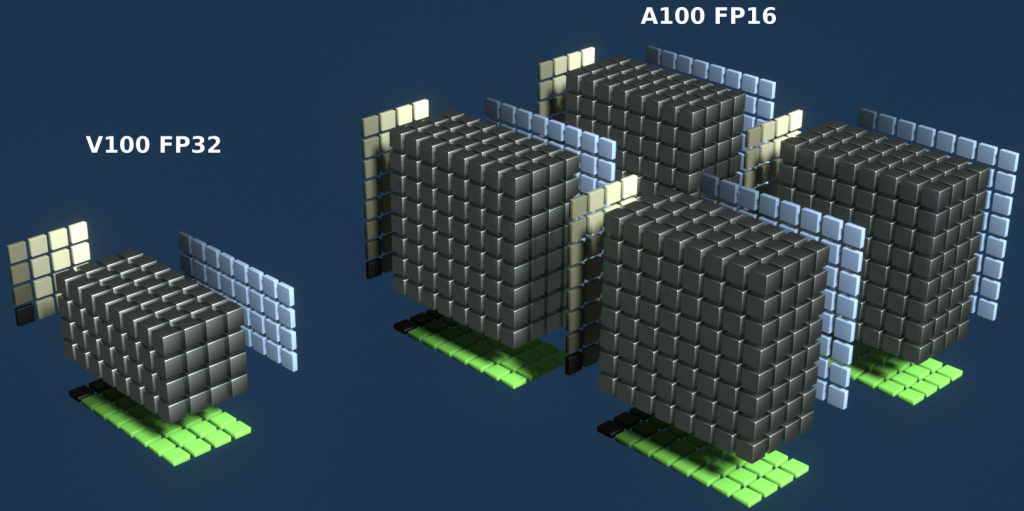

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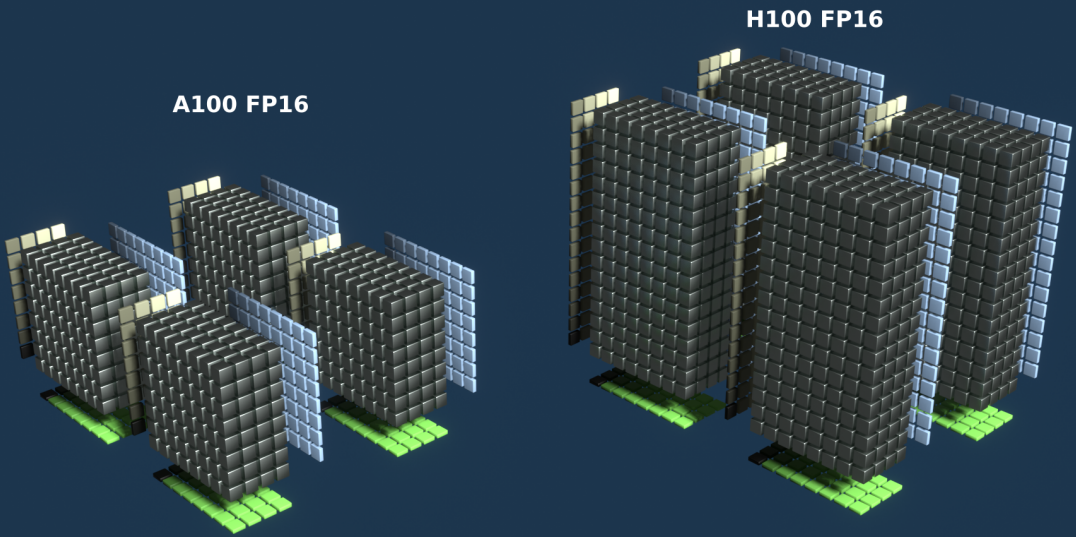
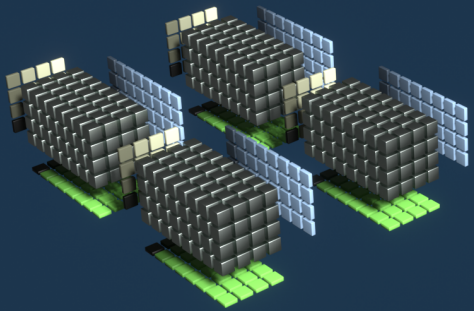
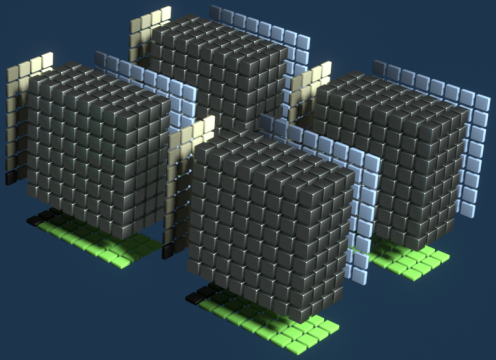


Tensor Core

A100 TF32



H100 TF32



Tensor Core

Tensor Core

Turring FP16

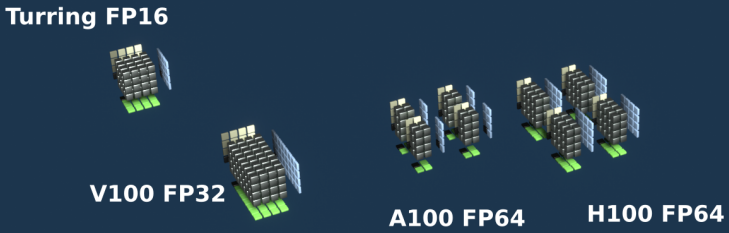
Tensor Core

Turring FP16

V100 FP32

Tensor Core

Tensor Core

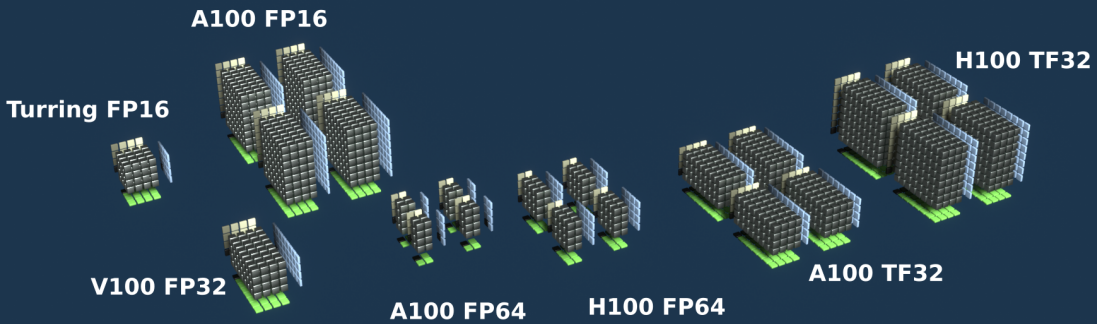


Tensor Core

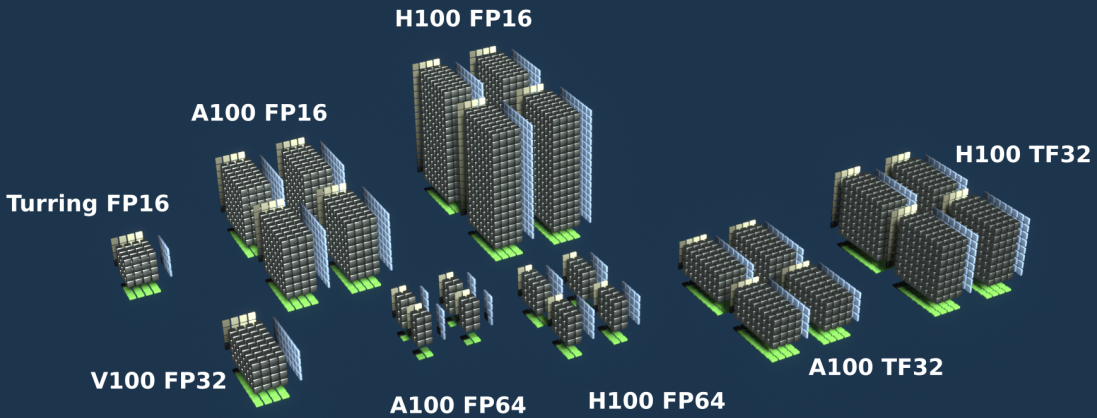
Tensor Core


Turring FP16
V100 FP32
A100 FP64
H100 FP64
A100 TF32
H100 TF32

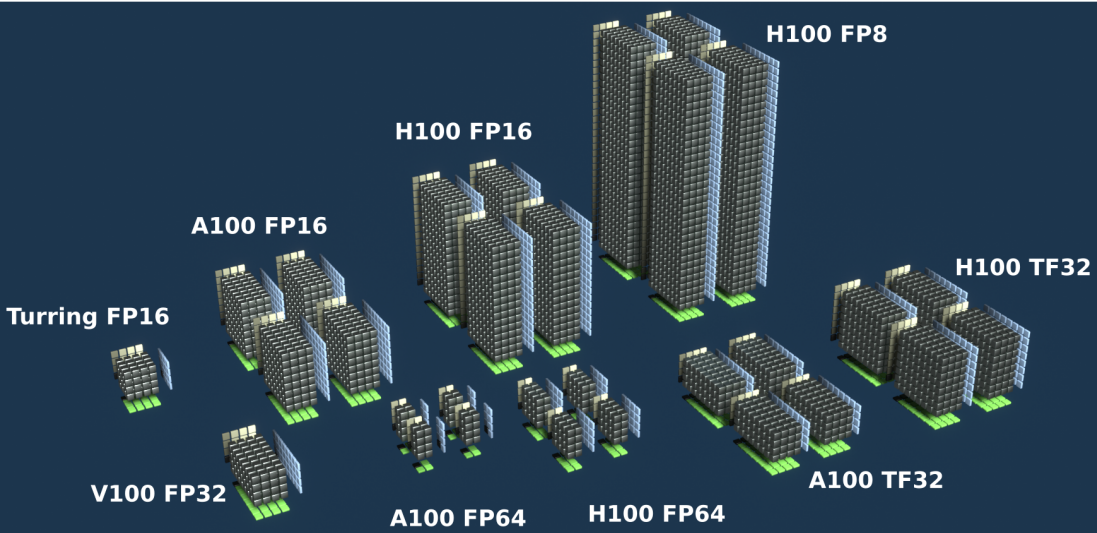
Tensor Core


A100 FP16
Turring FP16
H100 TF32
V100 FP32
A100 FP64
H100 FP64
A100 TF32

Tensor Core


H100 FP16
A100 FP16
H100 TF32
Turring FP16
V100 FP32
A100 FP64
H100 FP64
A100 TF32

Tensor Core


H100 FP8
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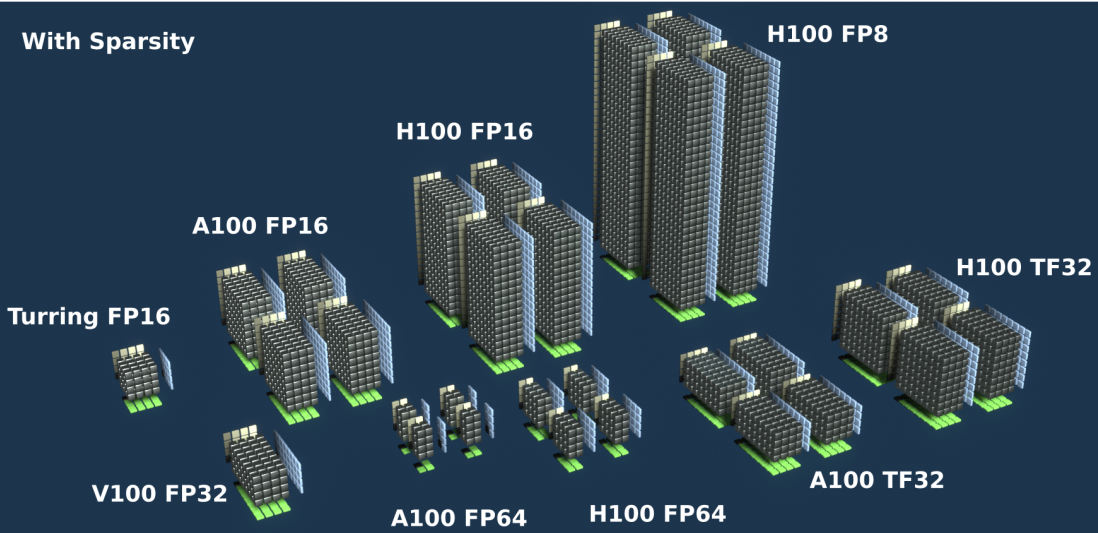
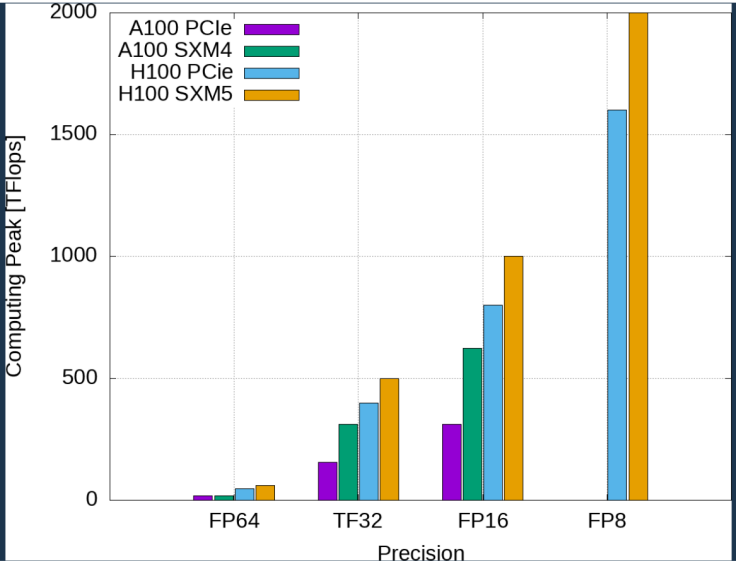
A100 FP64
H100 FP64
A100 TF32

Tensor Core


With Sparsity
H100 FP8
H100 FP16
A100 FP16
H100 TF32
Turring FP16
V100 FP32
A100 FP64
H100 FP64
A100 TF32

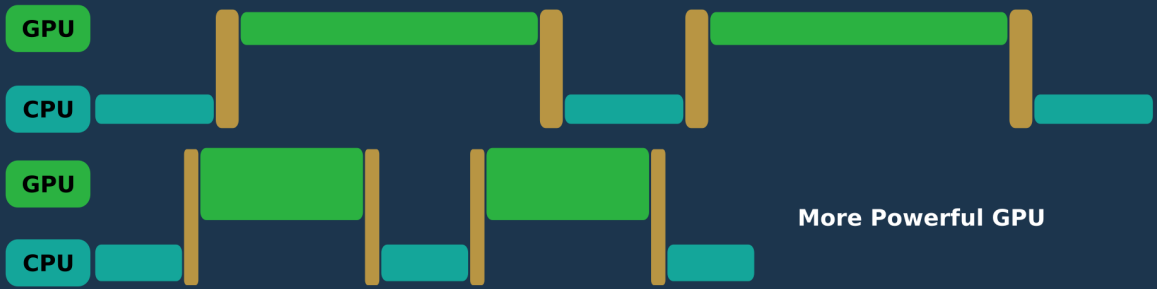
Tensor Core


A100 PCIe
A100 SXM4
H100 PCIe
H100 SXM5
Computing Peak [TFlops]
2000
1500
1000
500
0
FP64
TF32
FP16
FP8
Precision

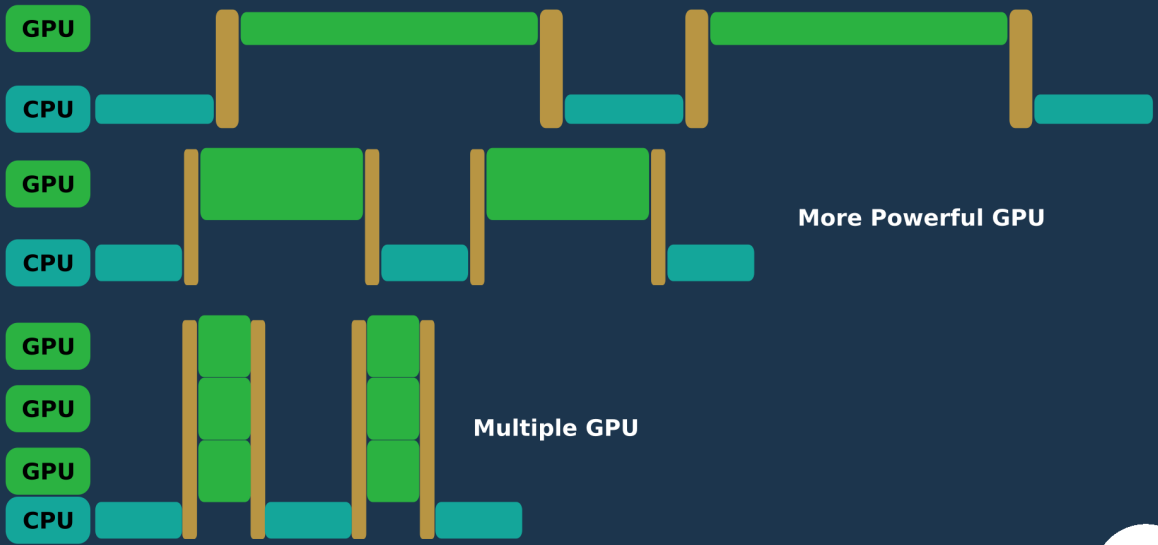
CPU + GPU Computing

CPU + GPU Computing

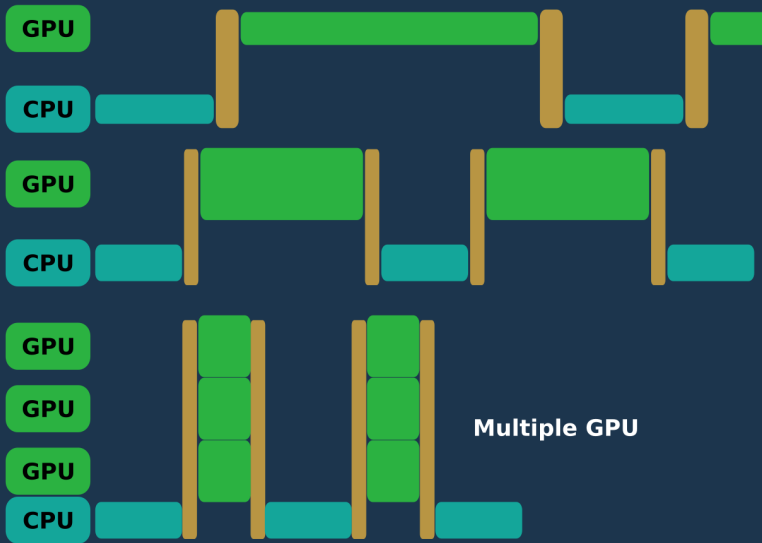
CPU + GPU Computing



CPU + GPU Computing



CPU + GPU Computing



More Powerful GPU

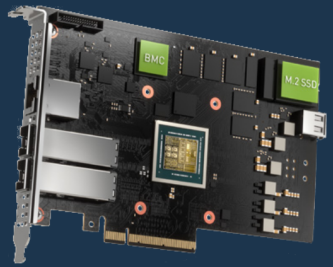
Stay on GPU as much as possible

Multiple GPU

Make less transfers as possible

Bluefield 3

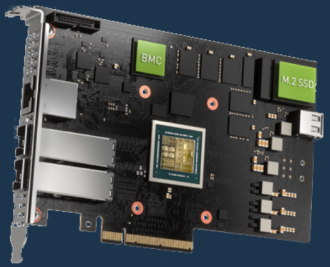
DPU : Data Processing Unit



Bluefield 3 DPU – 2x 200Gb/s
FHHL form factor

Bluefield 3

DPU : Data Processing Unit

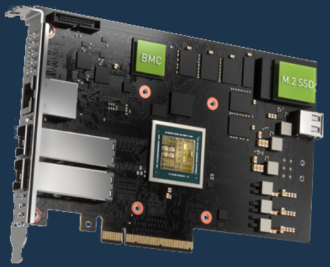


Bluefield 3 DPU – 2x 200Gb/s
FHHL form factor

1, 2, 4 ports with up to 400Gb/s connectivity
(Ethernet or NDR InfiniBand)

Bluefield 3

DPU : Data Processing Unit



Bluefield 3 DPU – 2x 200Gb/s
FHHL form factor

1, 2, 4 ports with up to 400Gb/s connectivity
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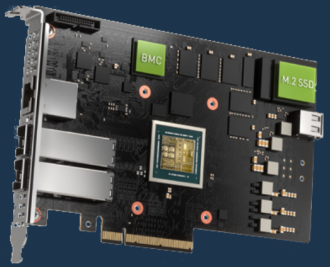
16 GB on-board DDR5 memory

Bluefield 3

DPU : Data Processing Unit



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FHHL form factor

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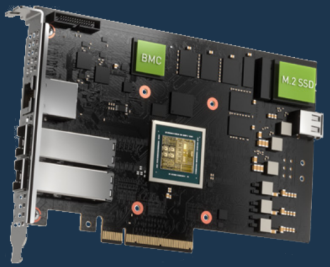
16 GB on-board DDR5 memory

1 GbE out-of-band management port

Bluefield 3

DPU : Data Processing Unit



Bluefield 3 DPU – 2x 200Gb/s
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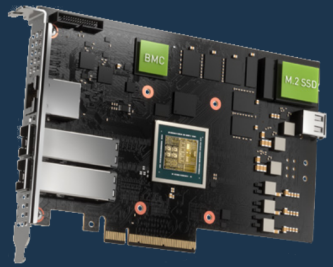
16 GB on-board DDR5 memory

1 GbE out-of-band management port

M.2 / U.2 connectors options for
direct attached storage

Bluefield 3

DPU : Data Processing Unit



Bluefield 3 DPU – 2x 200Gb/s
FHHL form factor

1, 2, 4 ports with up to 400Gb/s connectivity
(Ethernet or NDR InfiniBand)

16 GB on-board DDR5 memory

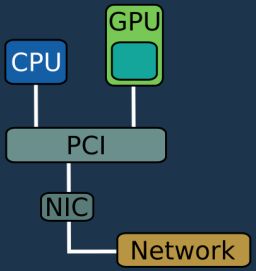
1 GbE out-of-band management port

M.2 / U.2 connectors options for
direct attached storage

Form factors: HHHL, FHHL

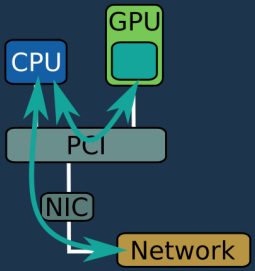
2022 - Hardware evolution

< 2022



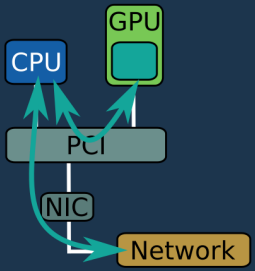
2022 - Hardware evolution

< 2022

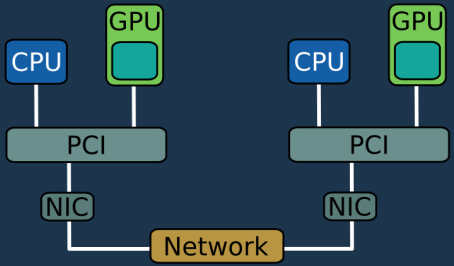


2022 - Hardware evolution

< 2022

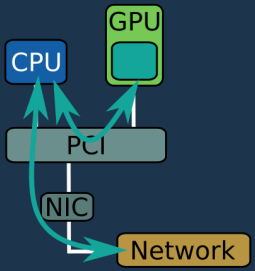


2022 and after

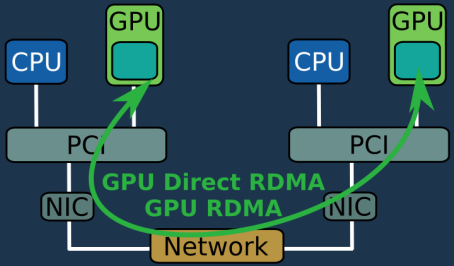


2022 - Hardware evolution

< 2022

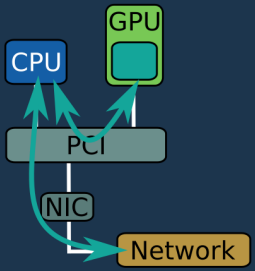


2022 and after

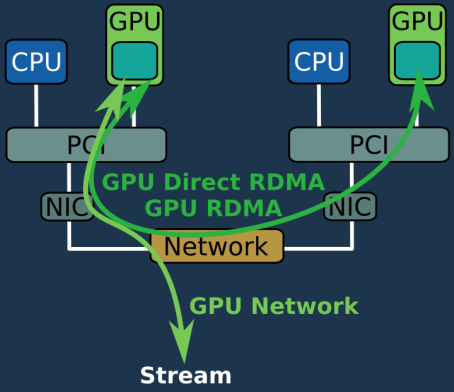


2022 - Hardware evolution

< 2022

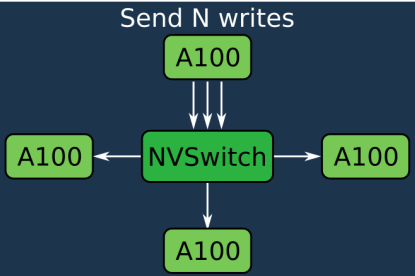


2022 and after

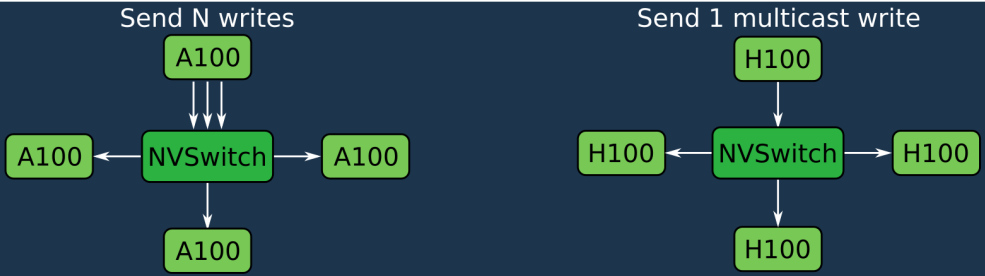


NVLink/NVSwitch acceleration

NVLink/NVSwitch acceleration



NVLink/NVSwitch acceleration



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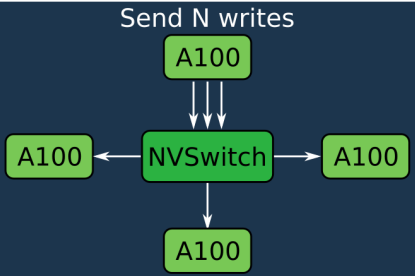

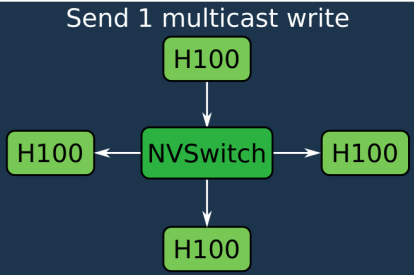

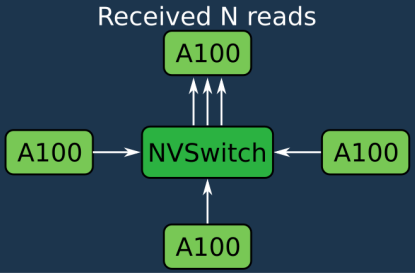

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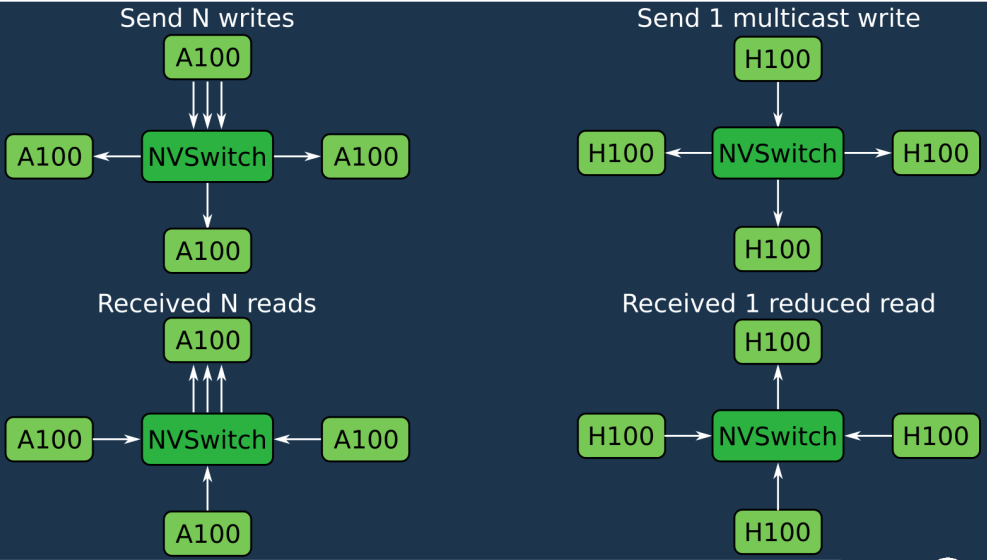

DGX H100 / DGX POD H100

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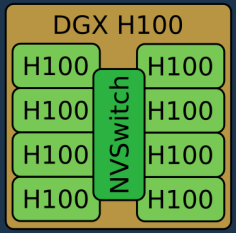

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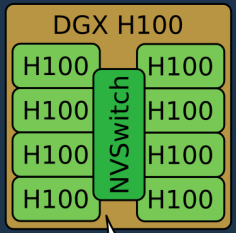

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- 32 PFlop (AI performance)
- 640 GB HBM3 Memory
- 24 TB/s memory Bandwidth

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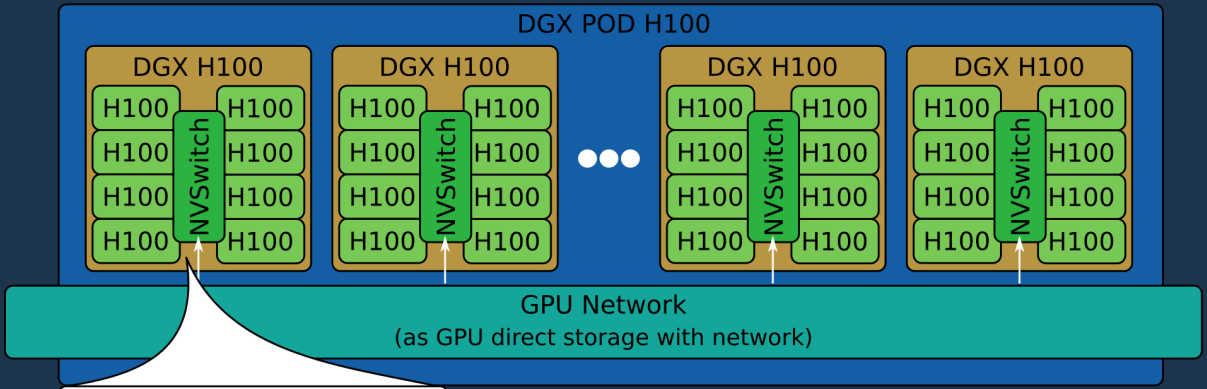

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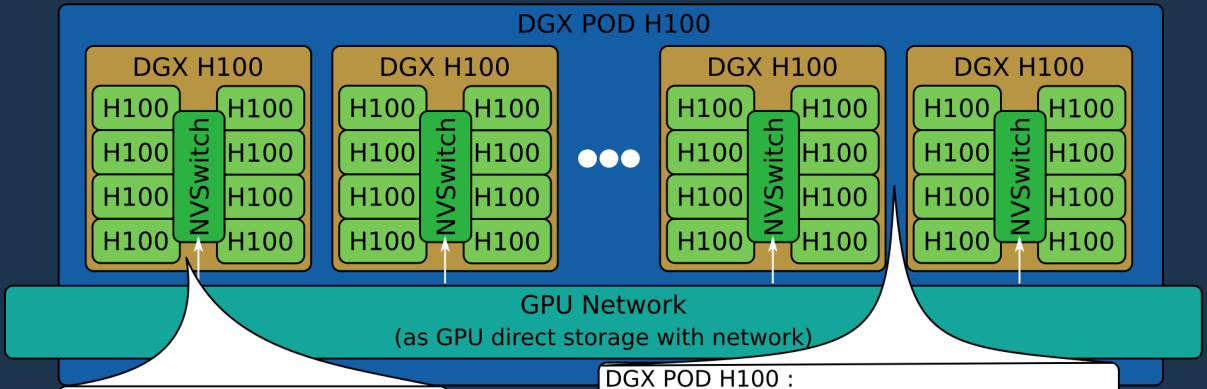

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DGX POD H100 :
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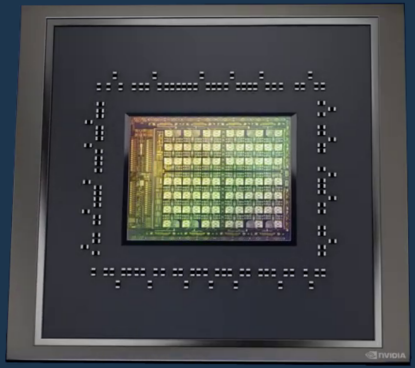
- 1 EFlop (AI performance)
- 20 TB HBM3 Memory
- 70 TB/s memory Bandwidth
- 192 TFlops of Sharp in-Network compute

2023 Grace CPU

Grace



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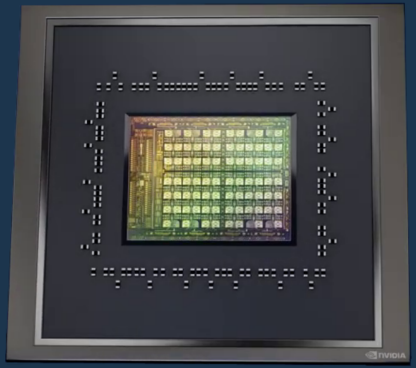

72 Neoverse V2 cores, Armv9
SVE2 with 4x128b

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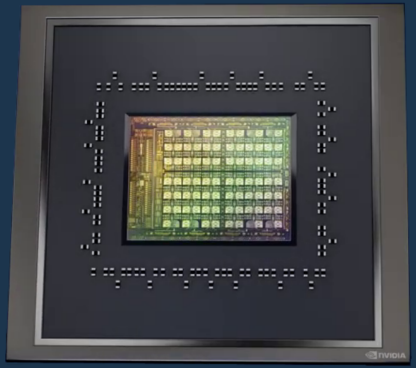

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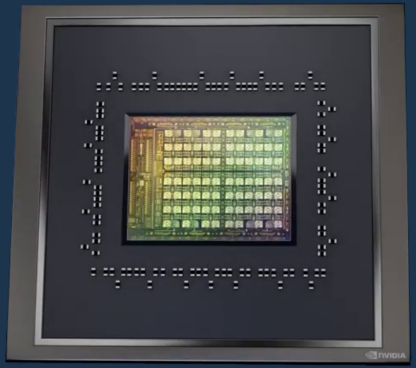

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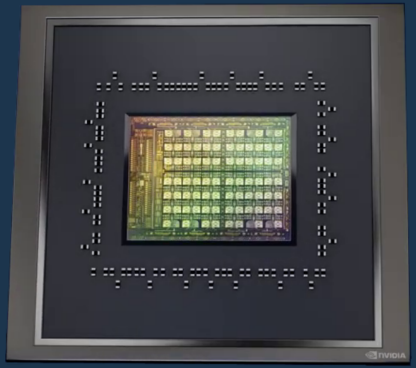

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2023 Grace CPU

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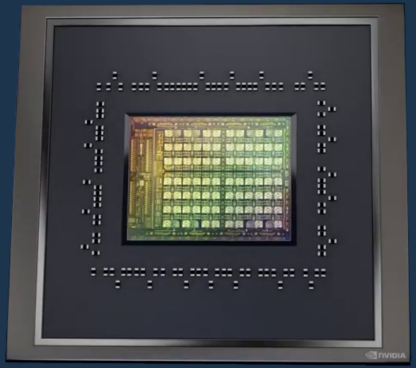

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Supports up to 4 chip coherency over Coherent NVLINK

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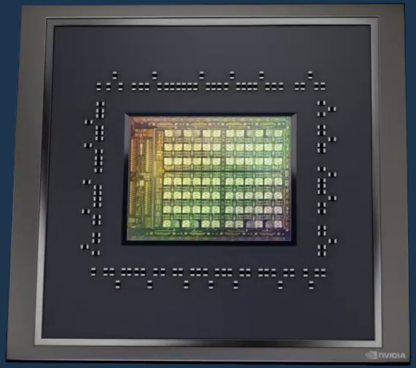

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NVLink C2C (900 GB/s)

2023 - Grace Superchip

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Grace Superchip

Neoverse V2 Cores: Armv9 with 4x128b SVE2

2023 - Grace Superchip

Grace Superchip

Neoverse V2 Cores: Armv9 with 4x128b SVE2

144 Cores

2023 - Grace Superchip

Grace Superchip

Neoverse V2 Cores: Armv9 with 4x128b SVE2

144 Cores

1 TB/s Bandwidth (HBM3)

2023 - Grace Superchip

Grace Superchip

Neoverse V2 Cores: Armv9 with 4x128b SVE2

144 Cores

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960 GB RAM (LPDDR5X)

2023 - Grace Superchip

Grace Superchip

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960 GB RAM (LPDDR5X)

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2023 - Grace Superchip

Grace Superchip

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NVLink Gen 4 (900 GB/s)

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NVLink Gen 4 (900 GB/s)

7.1 TFlops (FP64 computing peak)

2023 - Grace Superchip

Grace Superchip

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2023 - Grace Superchip

Grace Superchip

Passive air colling

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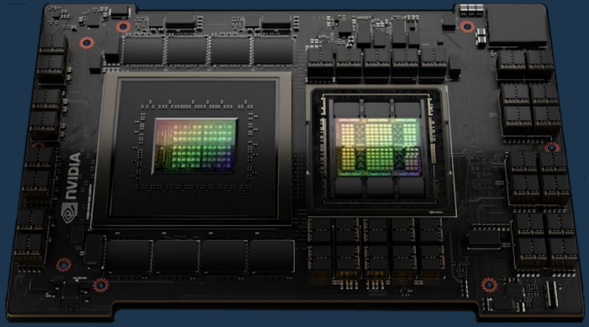
2023 - Grace Hopper

Grace Hopper Superchip



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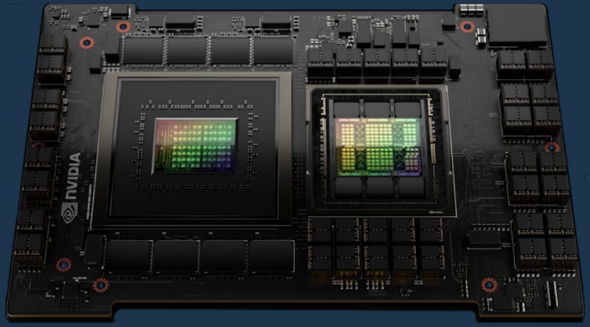
Grace Hopper Superchip



4 TB/s Bandwidth

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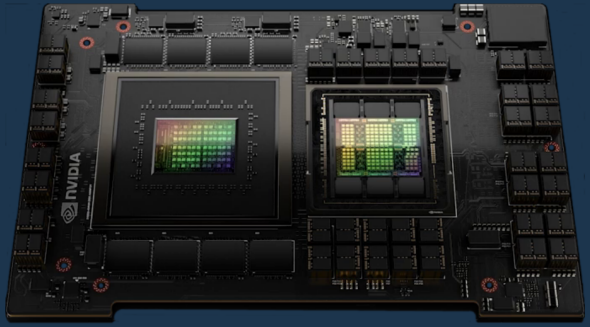

4 TB/s Bandwidth

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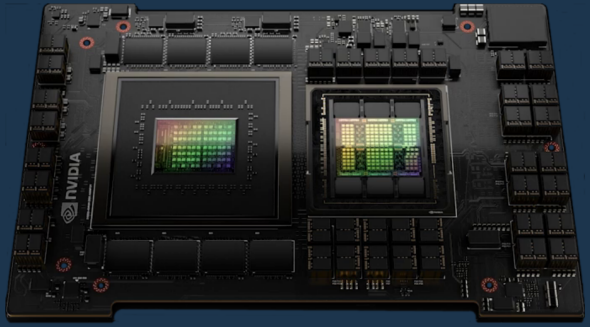

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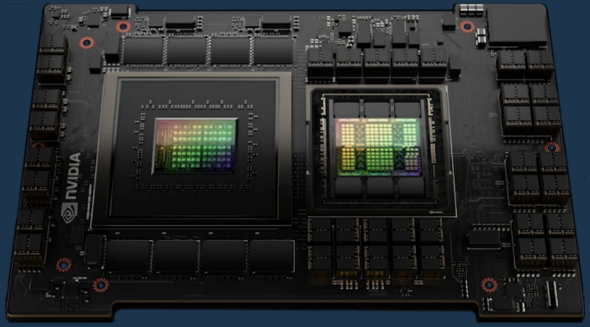
NVLink C2C (900 GB/s)

2023 - Grace Hopper

Grace Hopper Superchip



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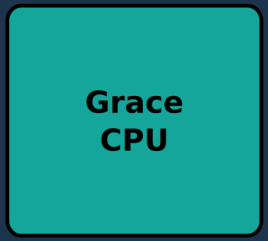
Unified Memory

Grace Hopper Superchip

Grace Hopper Superchip



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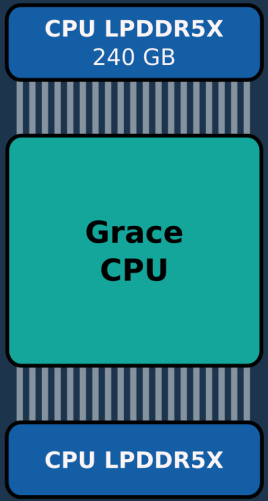

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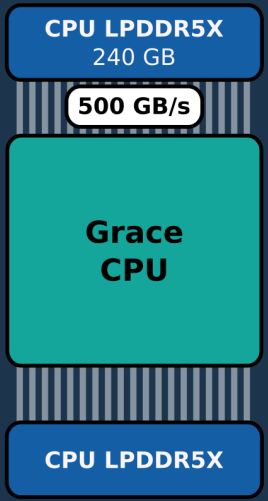

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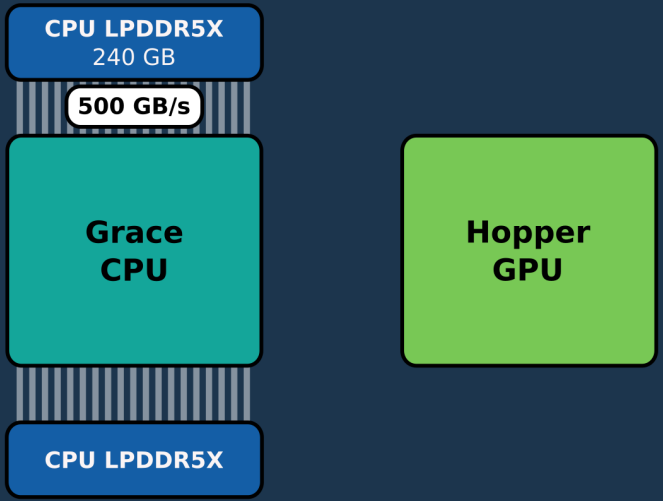

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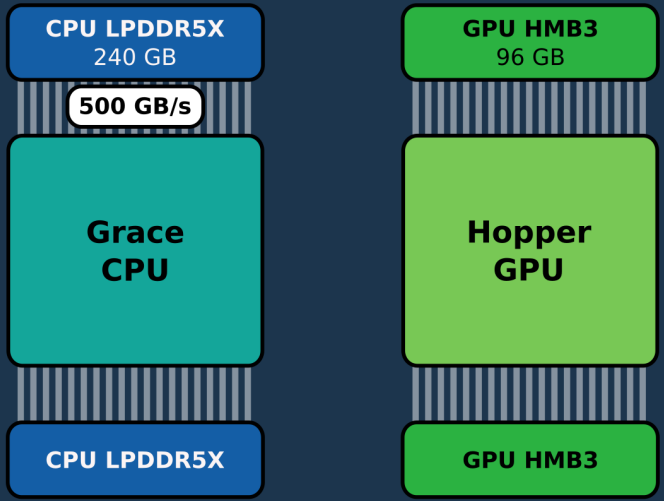

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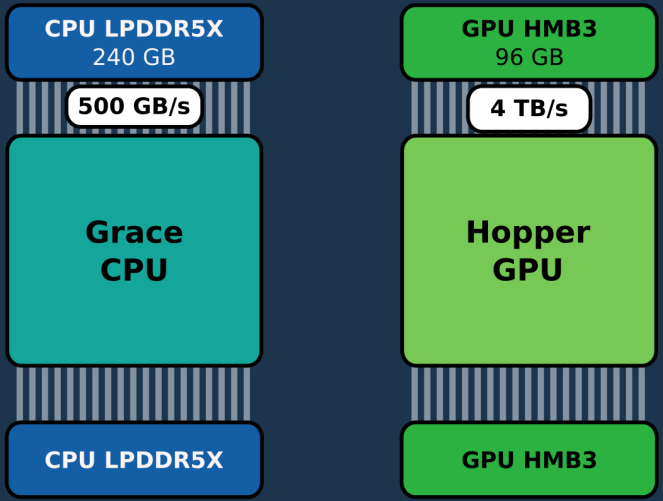

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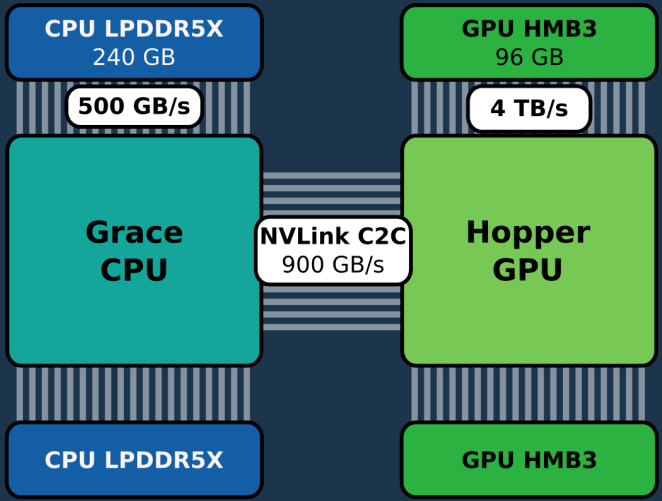

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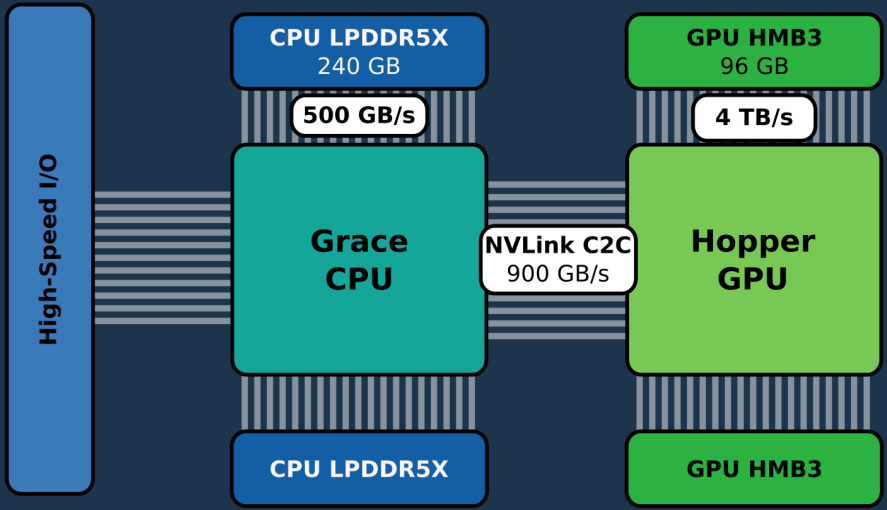

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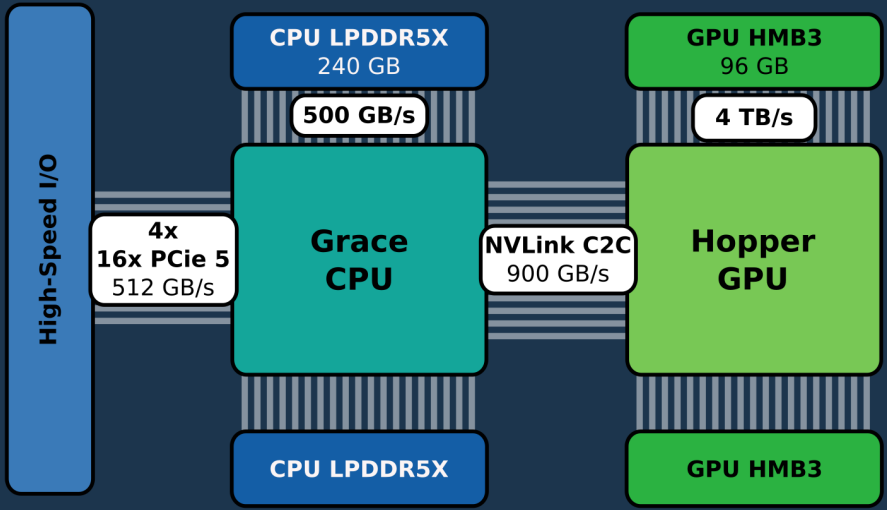

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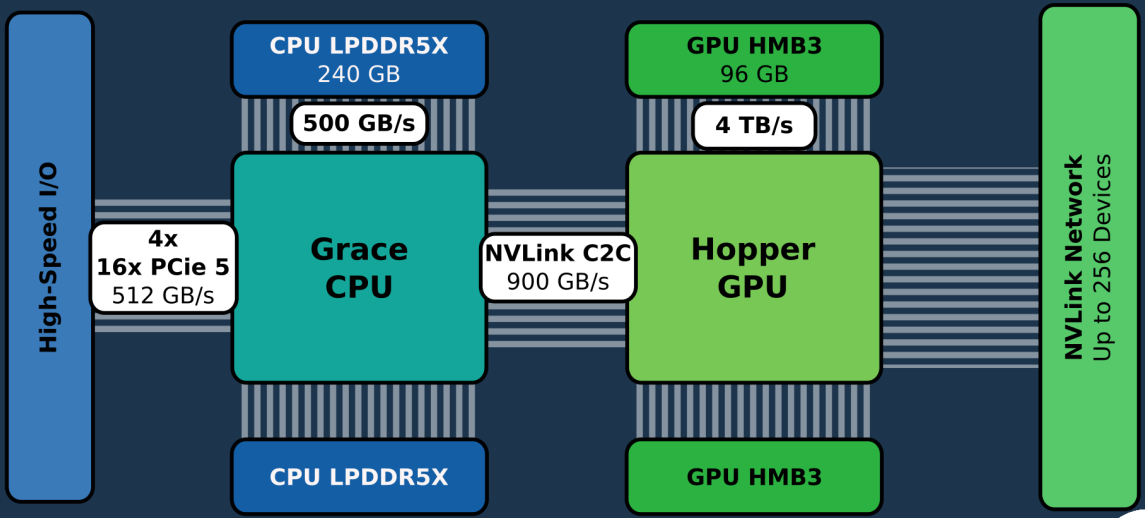

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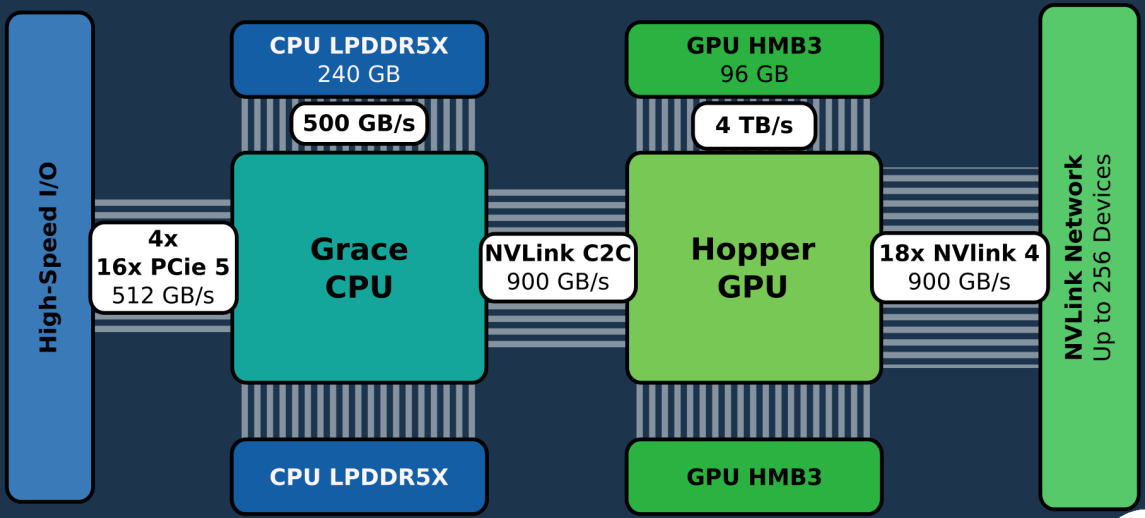
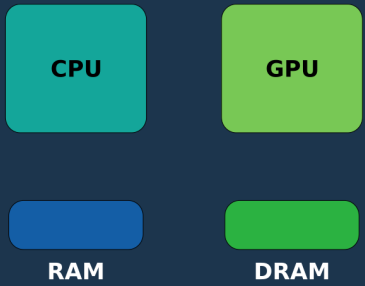


Memory Management

Memory Management

CUDA

< 2020



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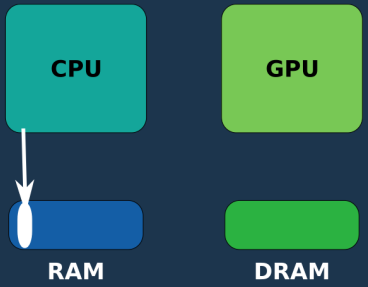

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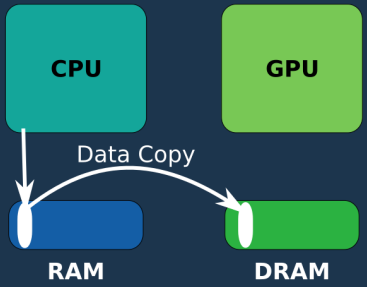

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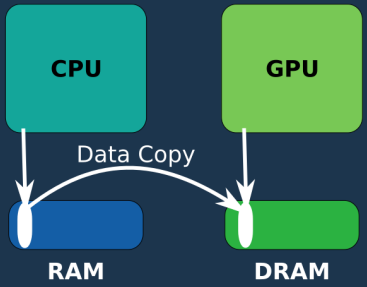

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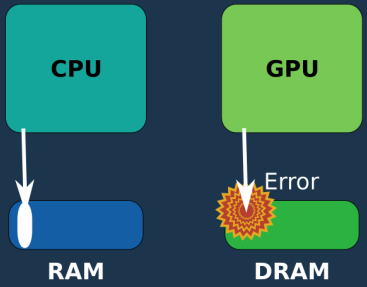

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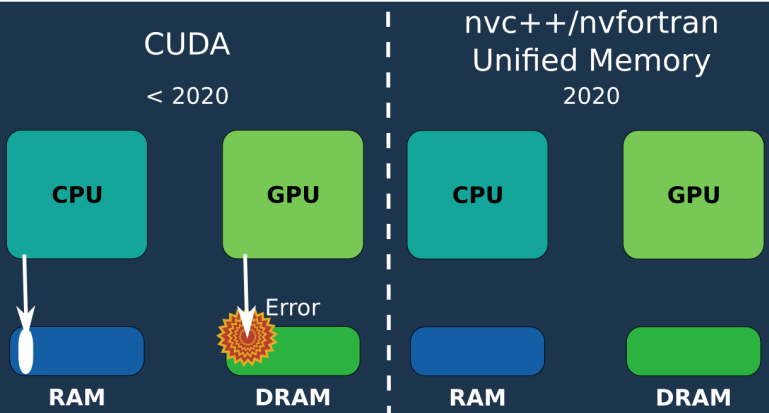
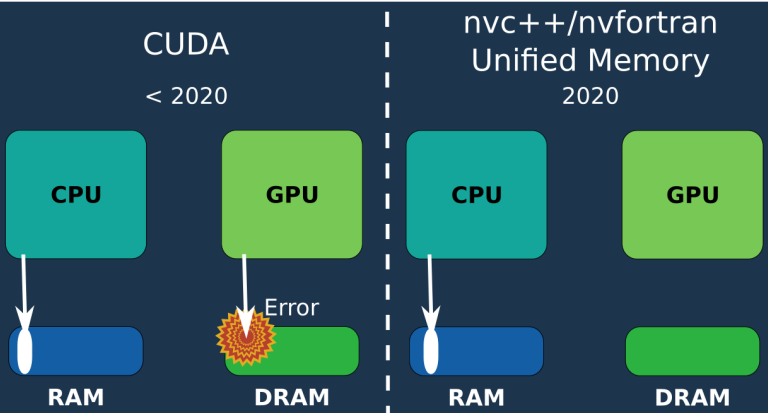


Memory Management



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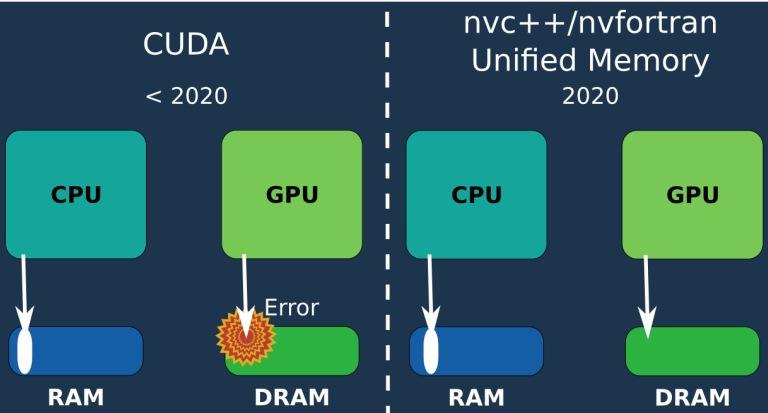

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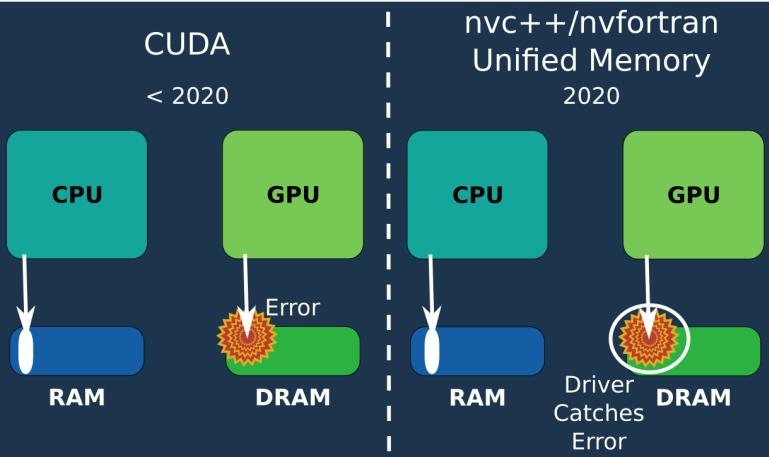

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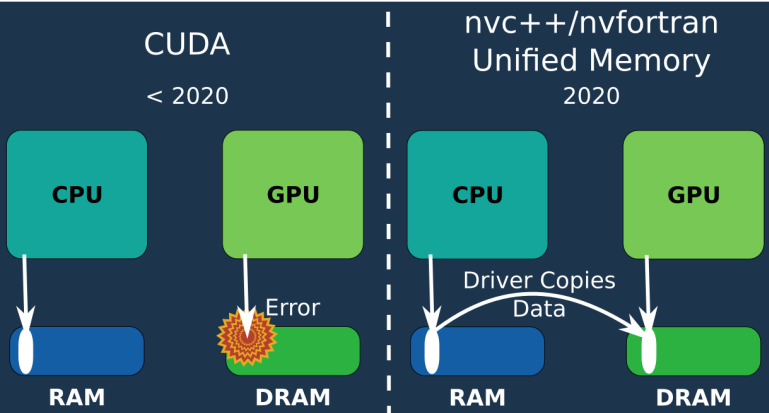

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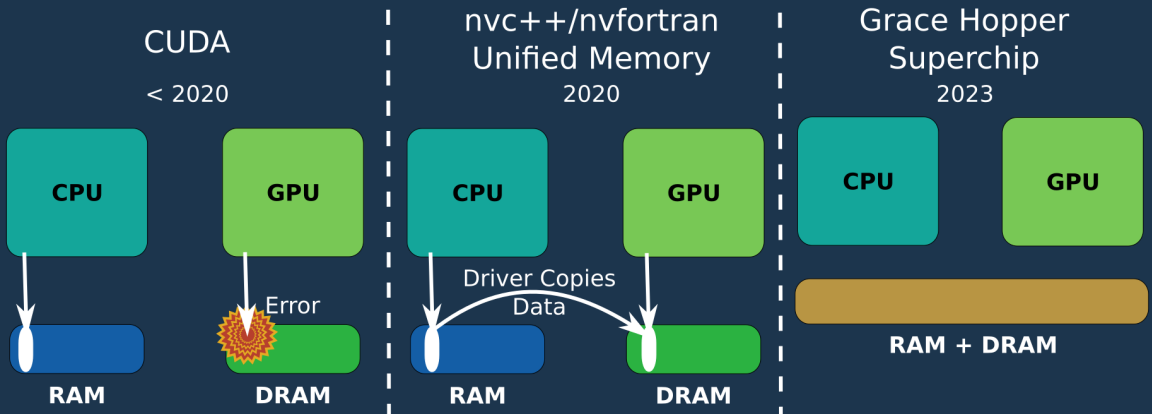

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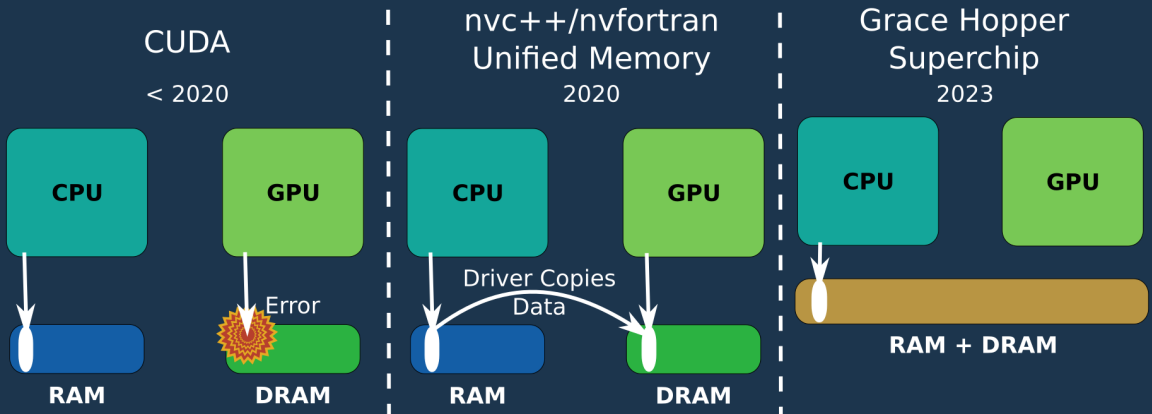

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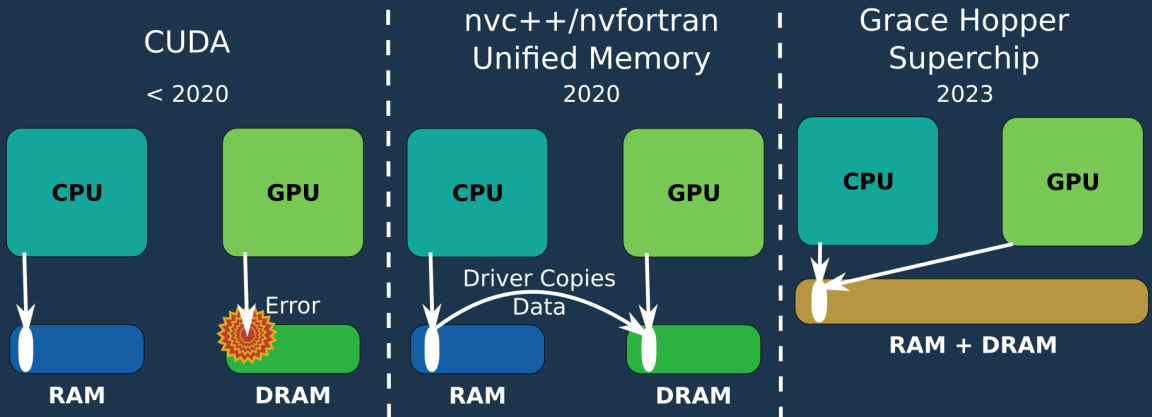

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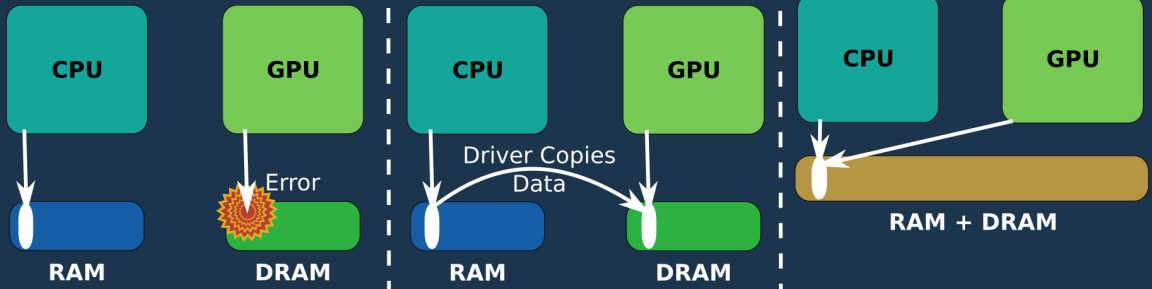
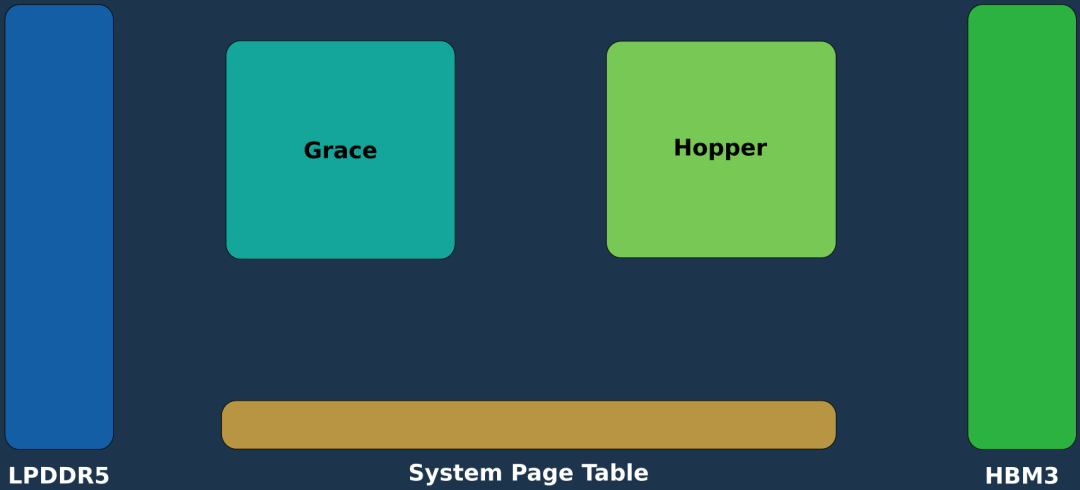


Yes but **RAM** and **DRAM** are **physically different**

Memory Management Grace Hopper



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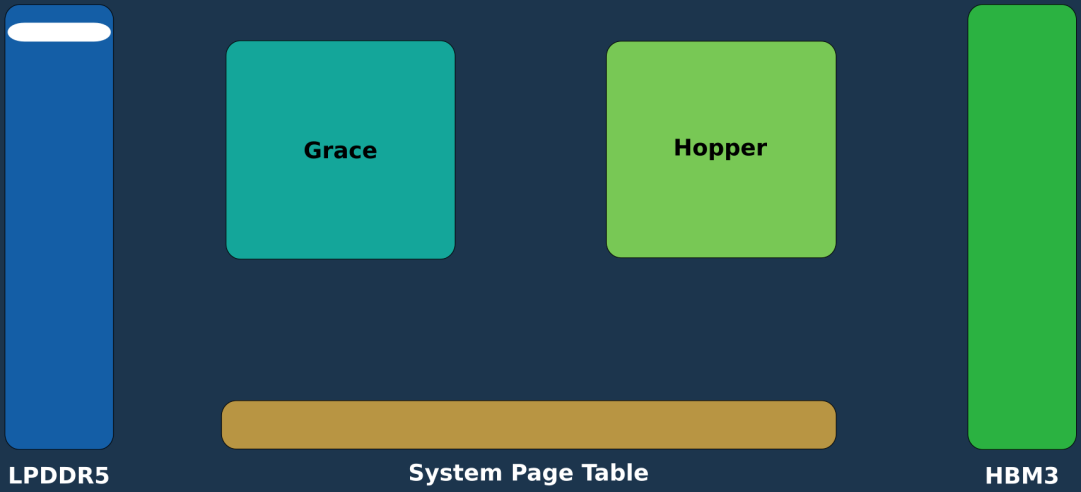

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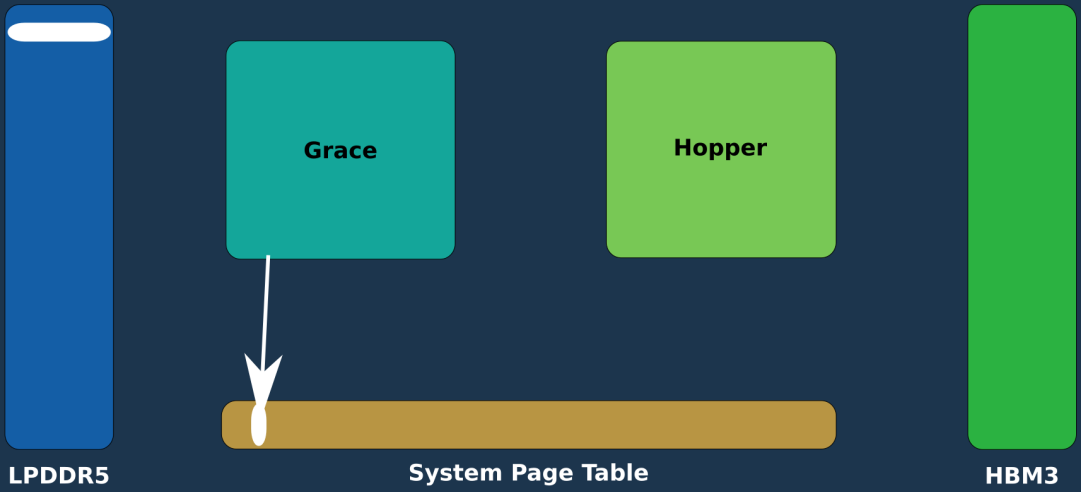

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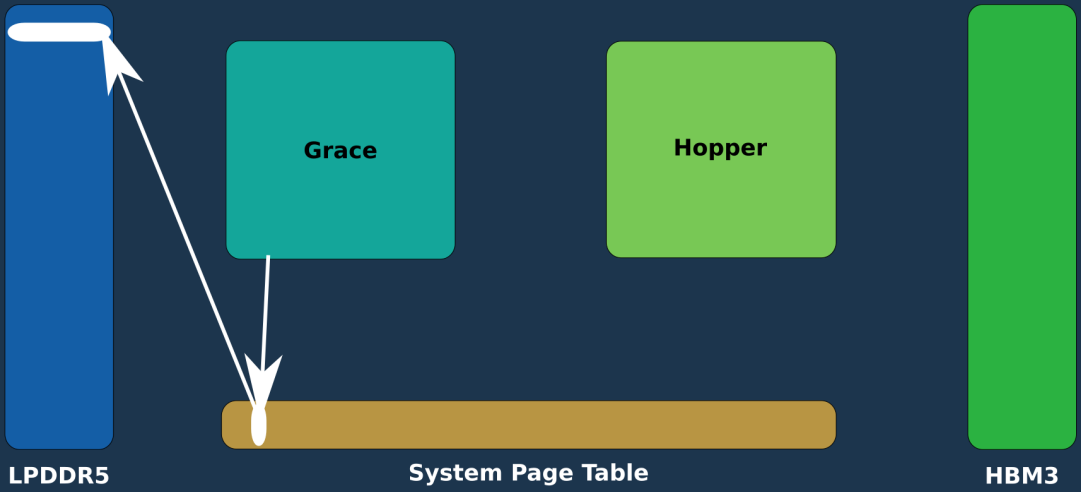

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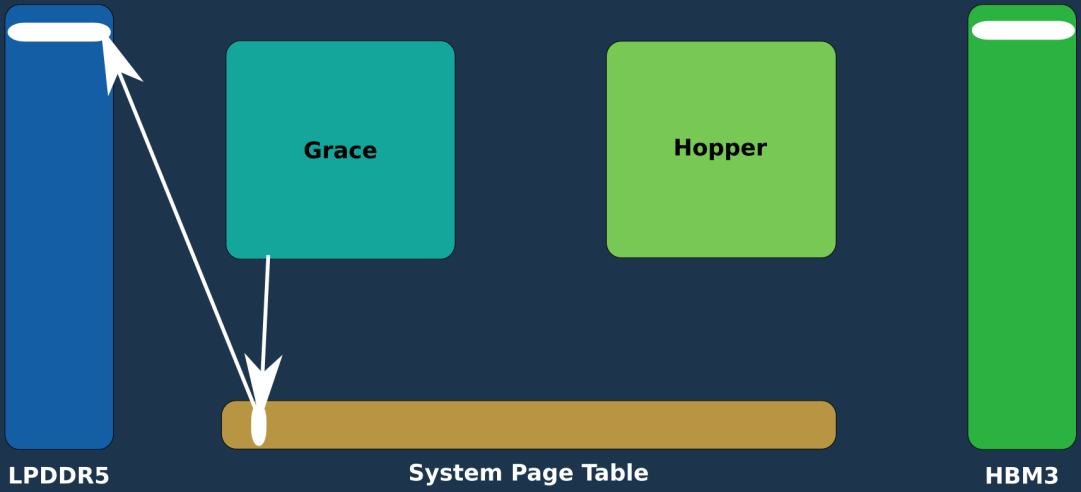

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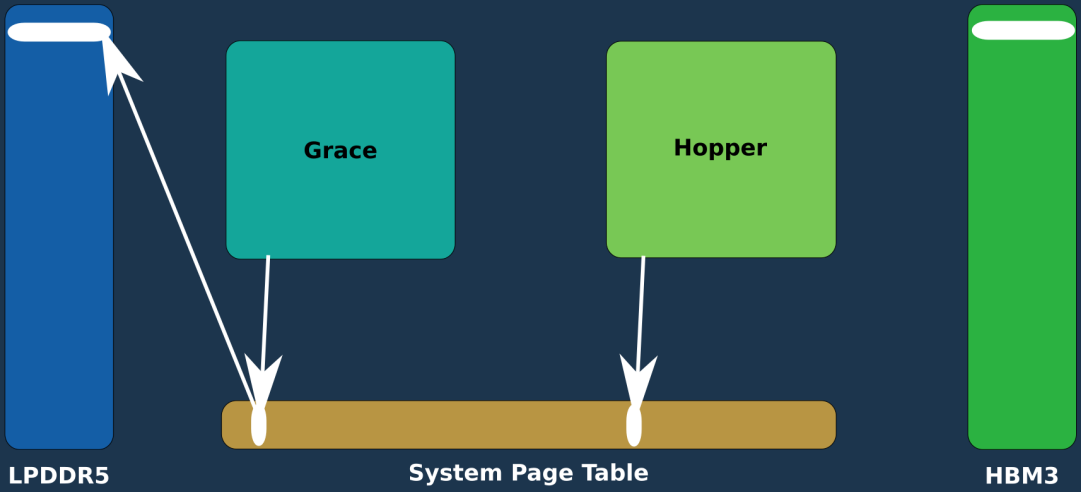

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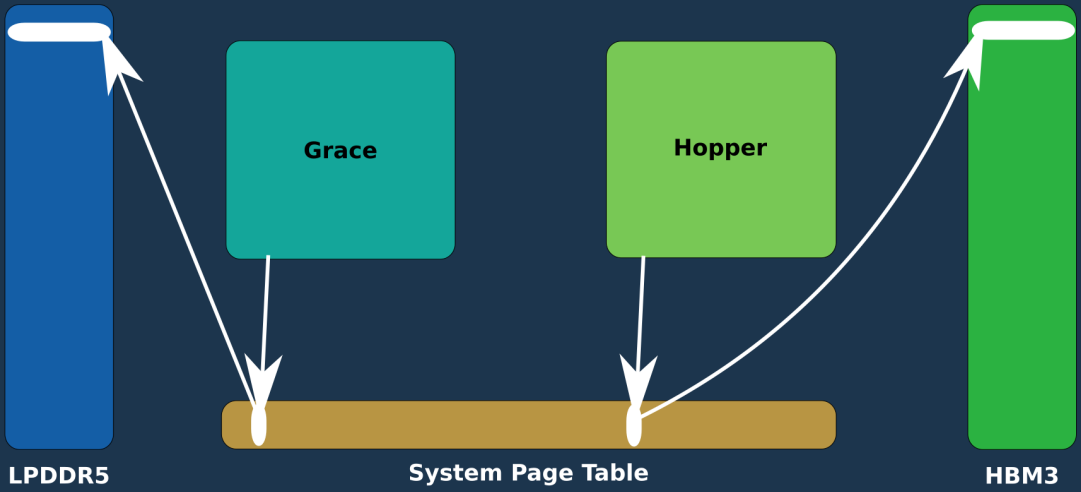

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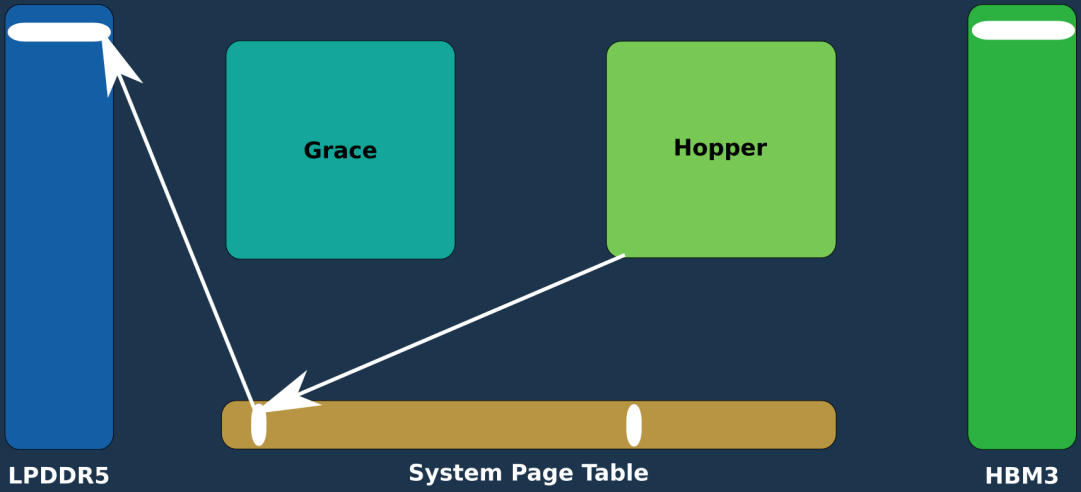

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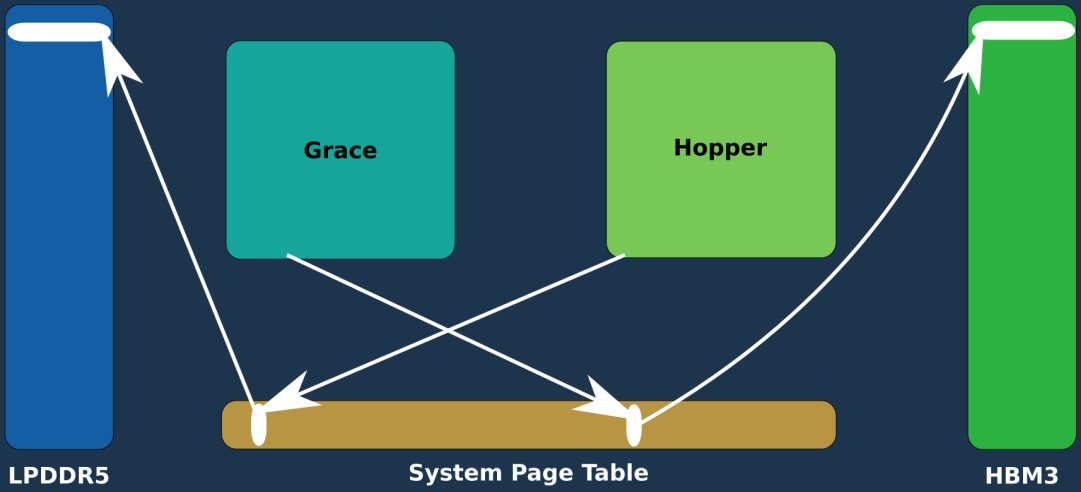

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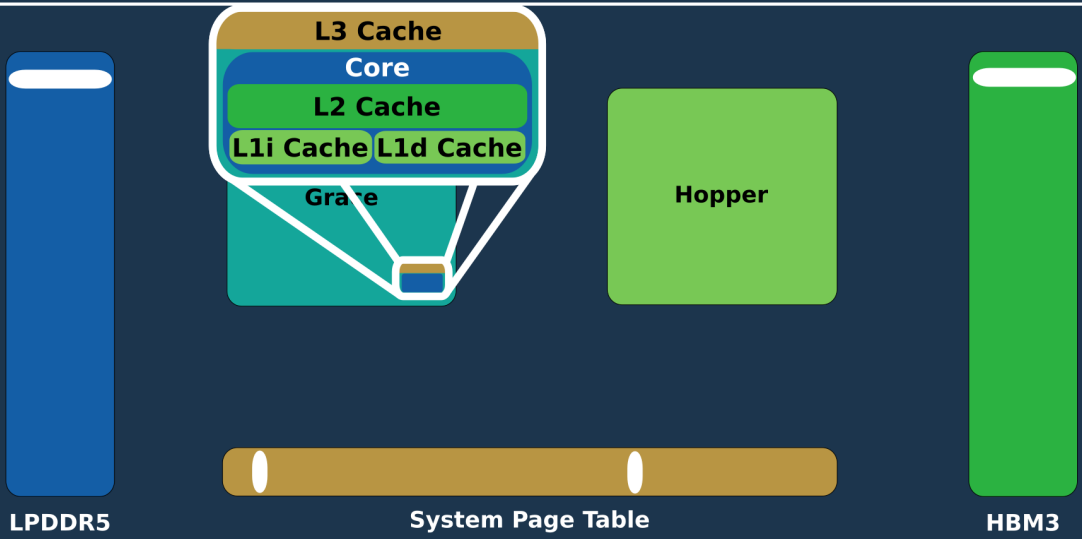

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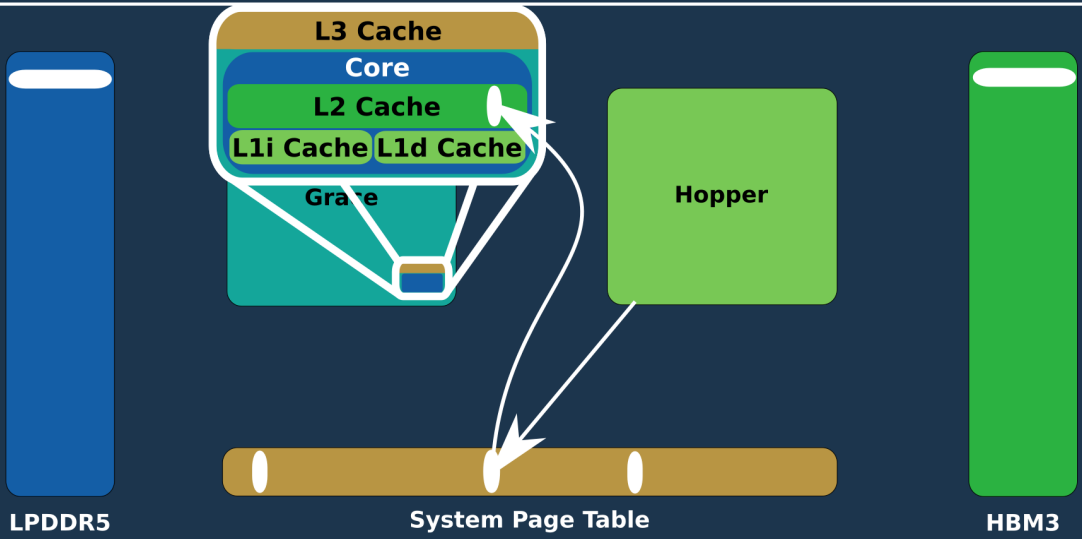


Grace Software Ecosystem

Grace Software Ecosystem

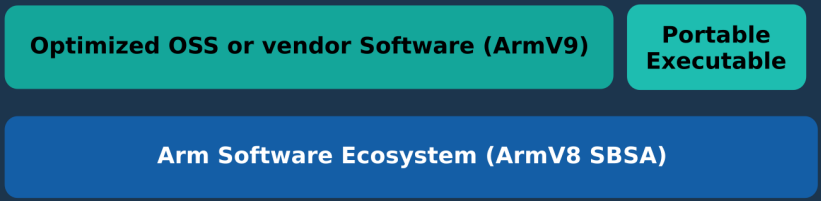
Arm Software Ecosystem (ArmV8 SBSA)

Grace Software Ecosystem

Optimized OSS or vendor Software (ArmV9)

Arm Software Ecosystem (ArmV8 SBSA)

Grace Software Ecosystem



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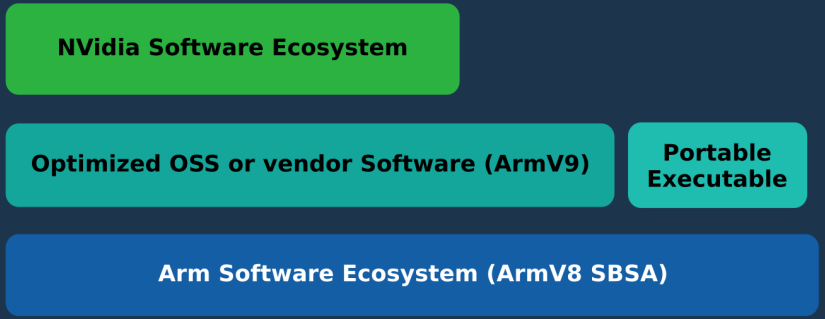

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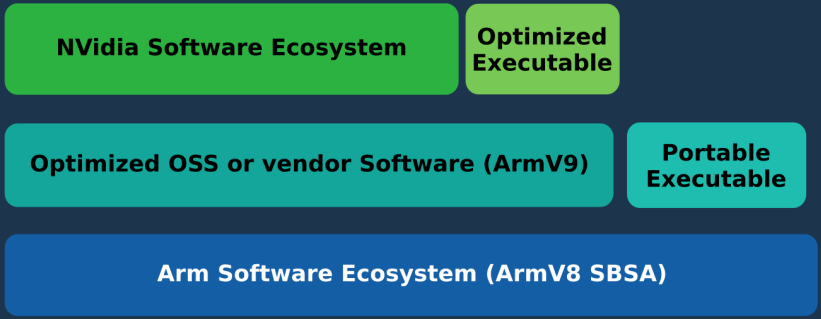

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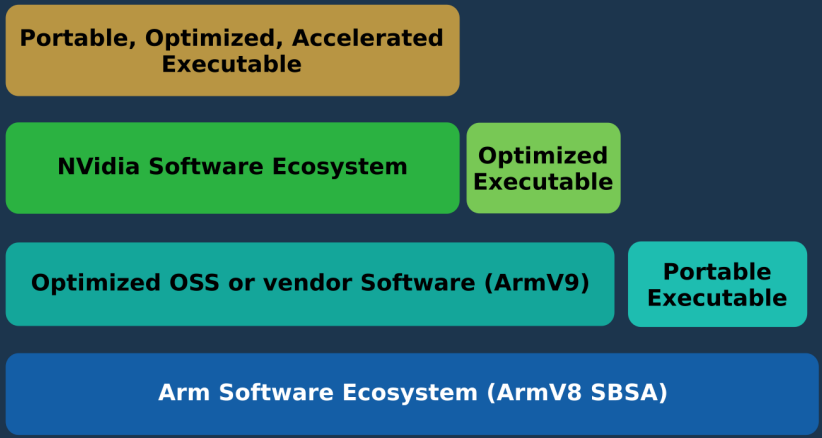
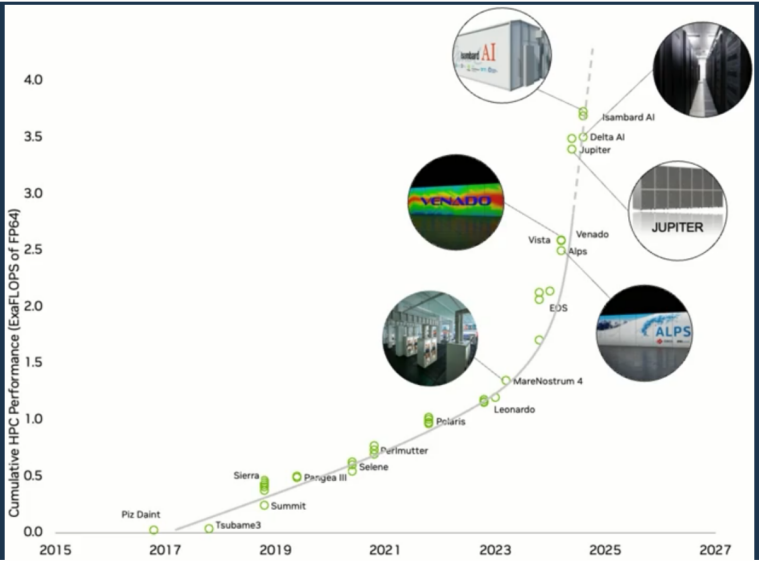


Supercomputers



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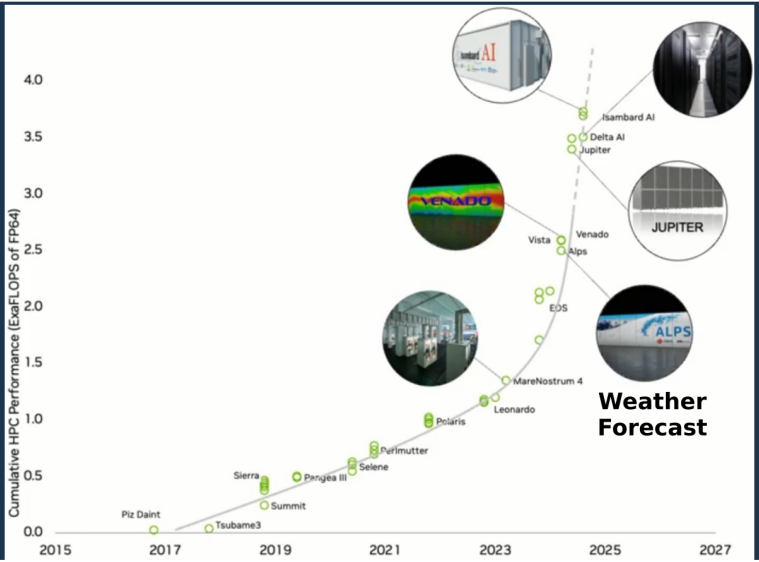

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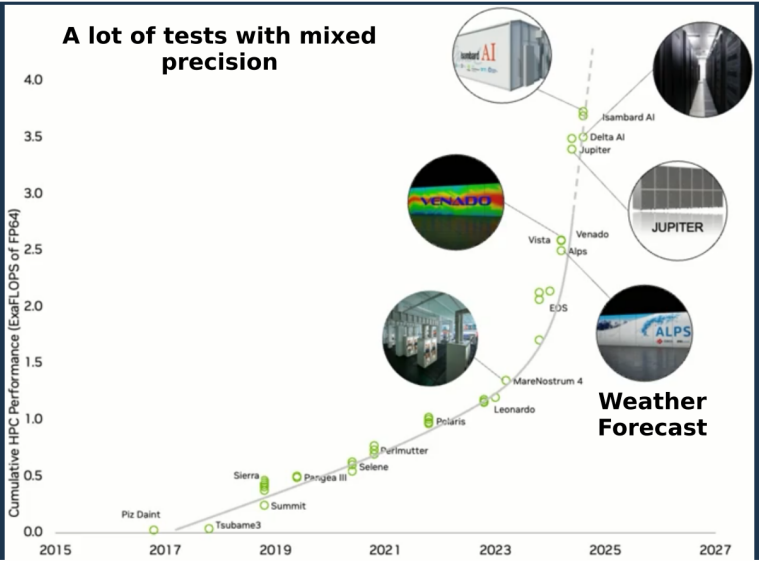

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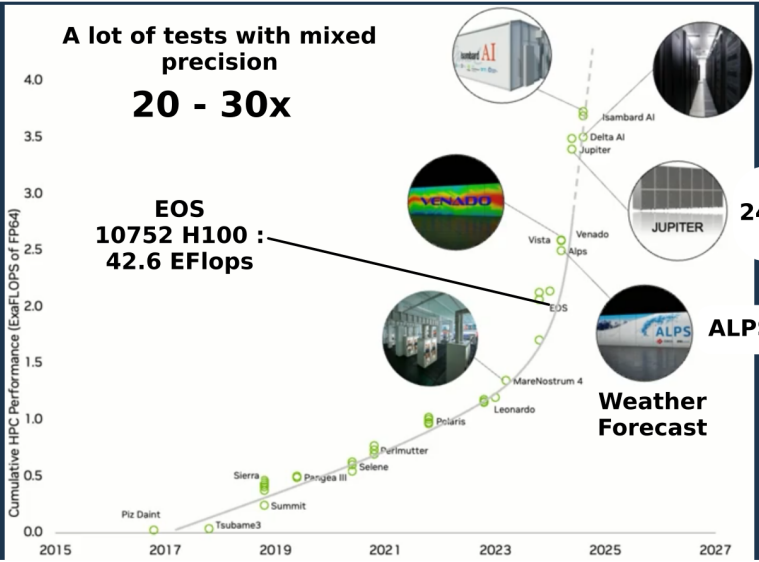

Feedback from ALPS

Thomas Schulthess : Director, ETH Zurich/The Swiss National Supercomputing Center (CSCS)

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Forecasting weather simulation

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Forecasting weather simulation

CUDA implementation (ICON)
Weather Simulation of **60 days per day**
without coupling

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Forecasting weather simulation

For now : 4719 PFlops (330x efficiency than Titan)

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Stream tests with **1 Grace** : **375 GB/s**

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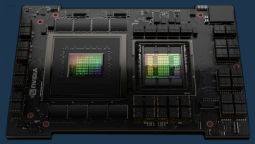
Will be **archieved** :
Upgrade with
64 Grace Hopper
ready for **summer 2024**



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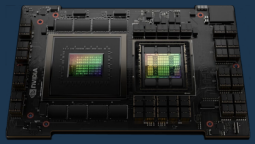

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They already investigate **mix precision** to **gain an other order of magnitude**

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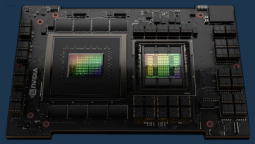

Stream tests with **1 Grace** : **375 GB/s**

They already investigate **mix precision** to **gain an other order of magnitude**

Next Upgrade : **40 EFlops**
2800x efficiency than **Titan**

Feedback from LOFAR

John Romein : Researcher, ASTRON (Netherlands Institute for Radio Astronomy)

LOFAR : LRw Frequency ARray Radioastronomy (Fast radio burst, dark matter)

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LOFAR : 100s antenna => 13 Tb/s

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Group of Antenna

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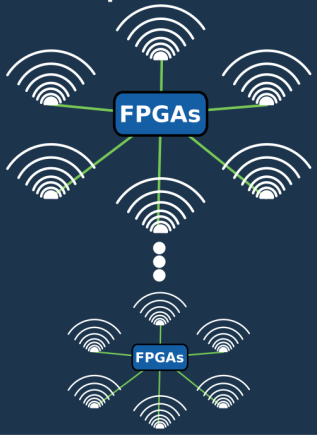

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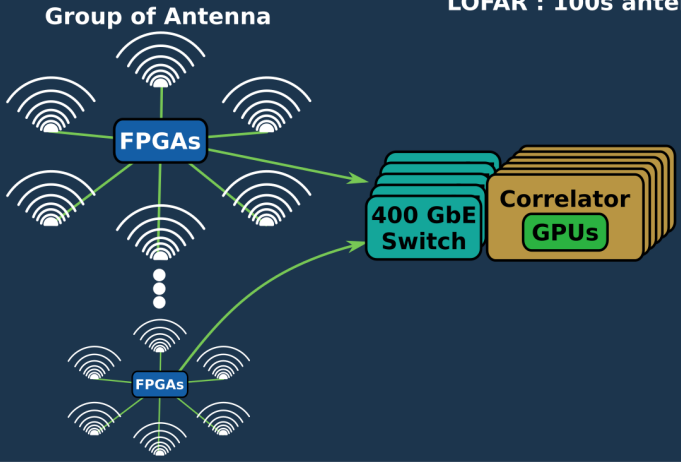

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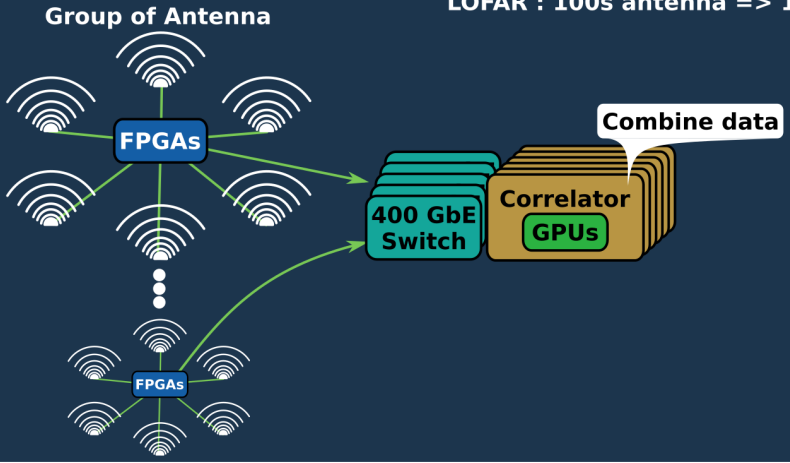

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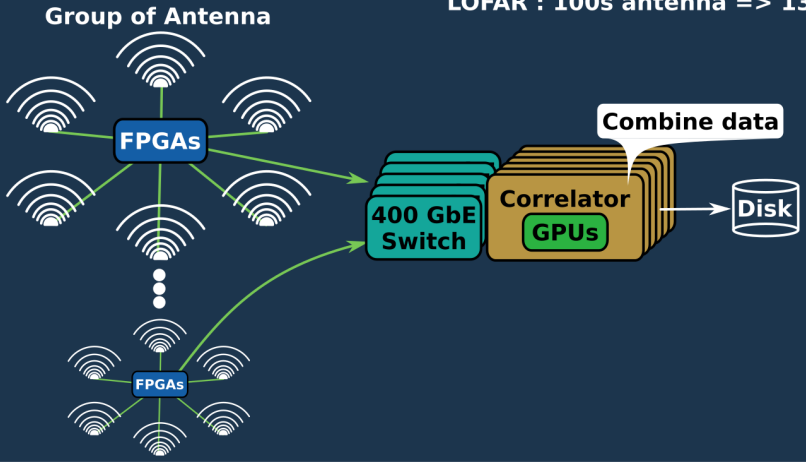

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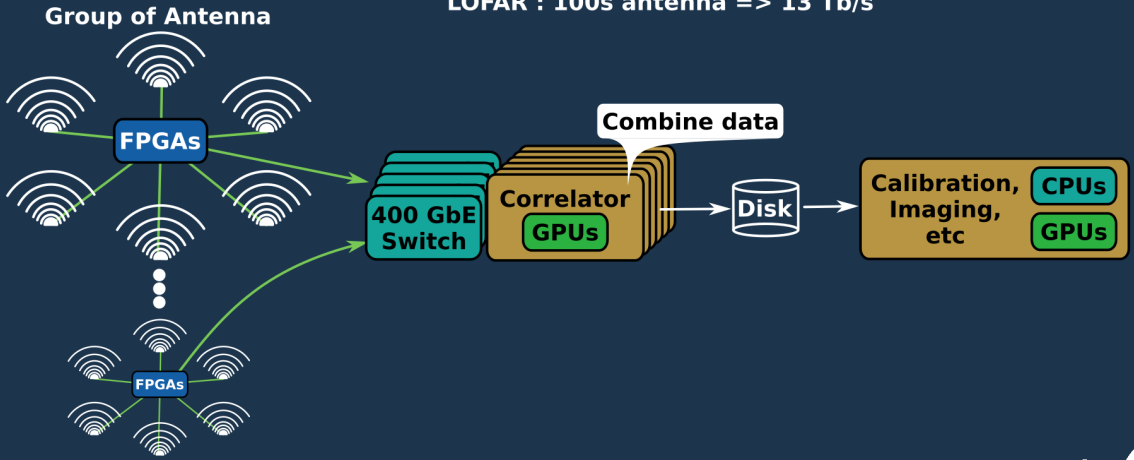

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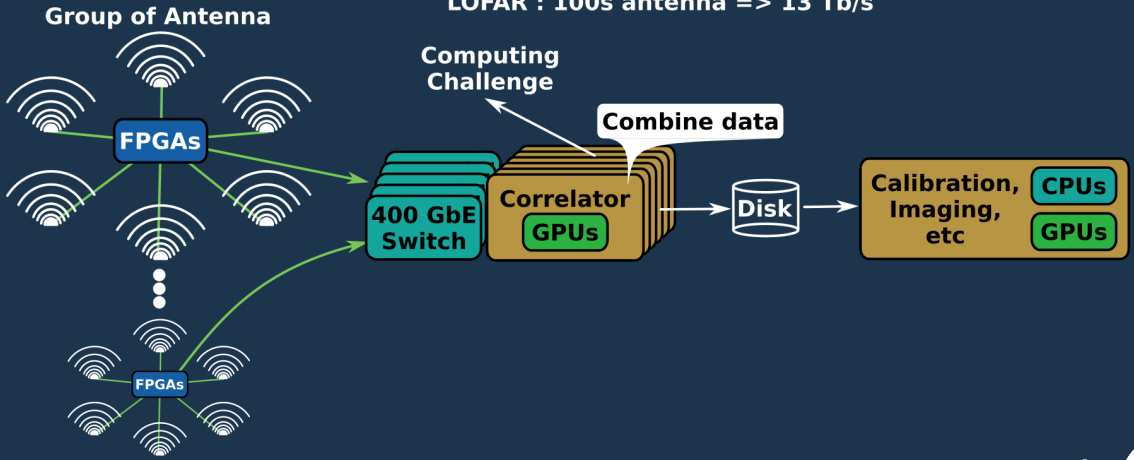

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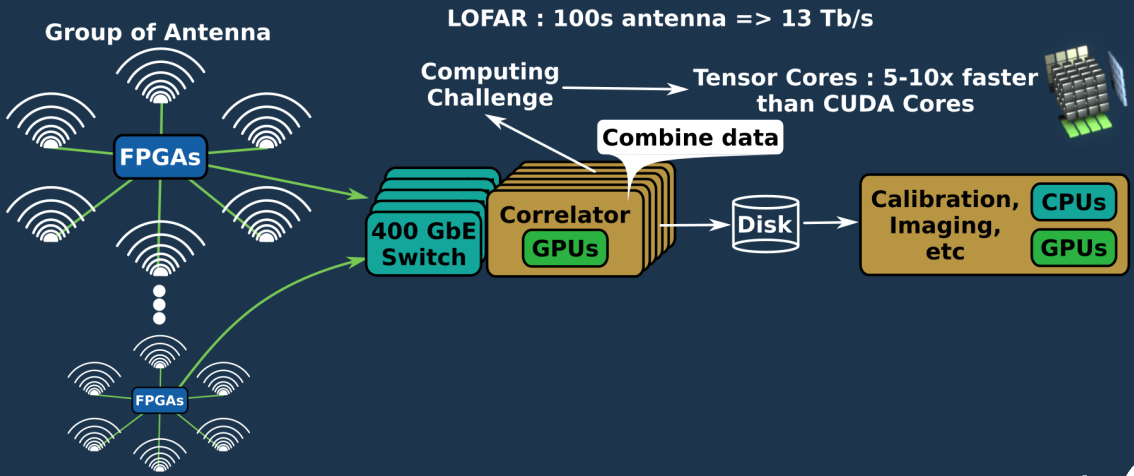

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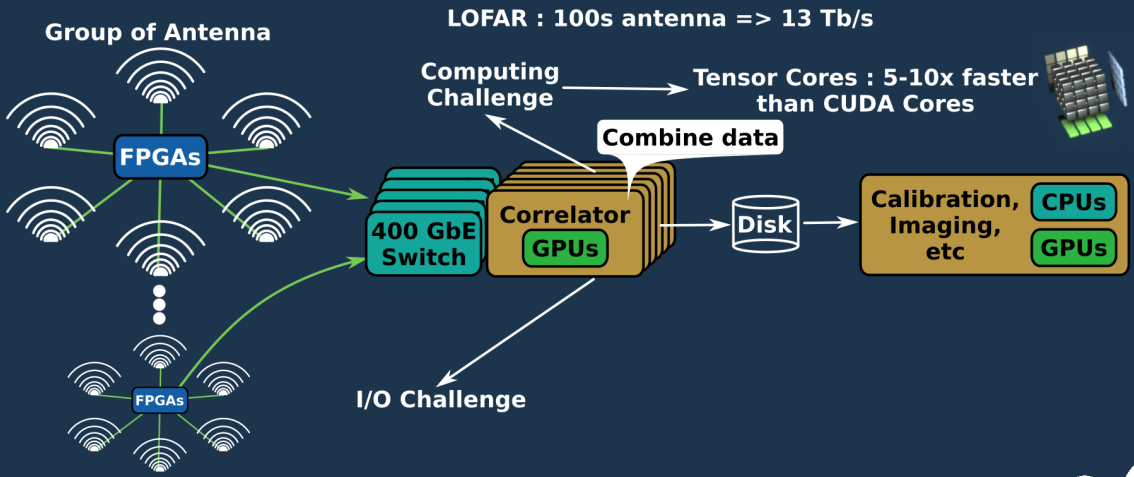

Feedback from LOFAR

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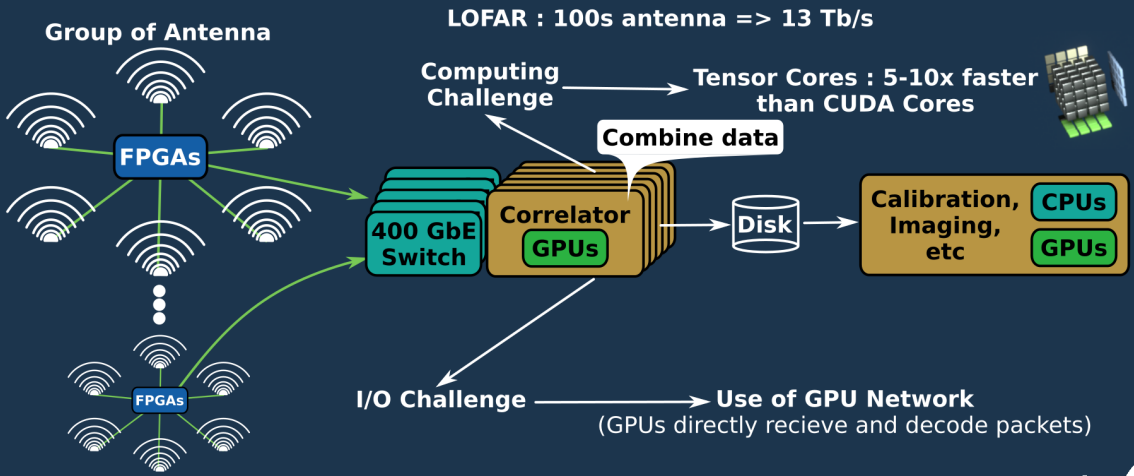
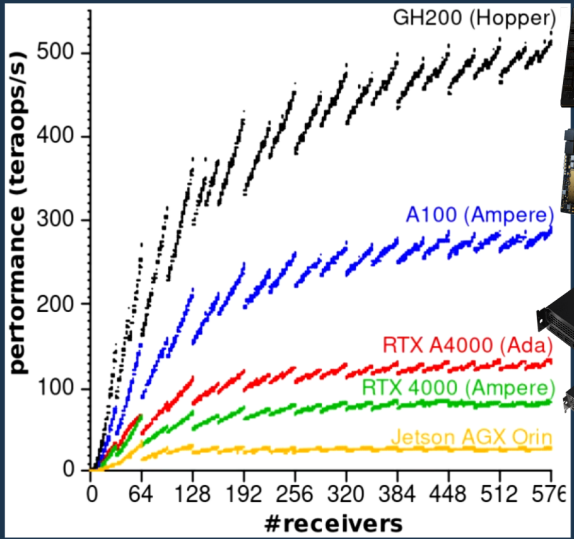
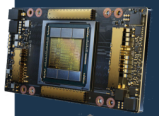


Feedback from LOFAR



(**TMA** not yet used)



Computing Challenge

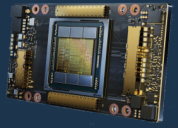
8-bit samples :
- 4-bit : ~2x faster
- 16-bit : ~2x slower

Feedback from LOFAR

I/O Challenge ⟶ Use of GPU Network

Feedback from LOFAR

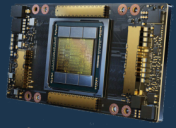
I/O Challenge → **Use of GPU Network**



A100 : (on 2 x 100Gb/s lines) get 198.6 Gb/s into A100
=> carefull tunning to avoid packet loss

Feedback from LOFAR

I/O Challenge → Use of GPU Network



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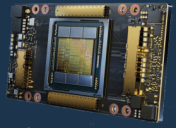
Feedback from LOFAR

I/O Challenge ⟶ Use of GPU Network



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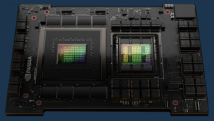
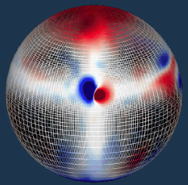


GH200 : 398.6 Gb/s on line at 400 Gb/s
=> eventual goal 1200 Gb/s

Full Site :
13000 Gb/s

Solar Storms Simulation



Ron Caplan : Computational Scientist, Predictive Science Inc.

Solar Storms Simulation

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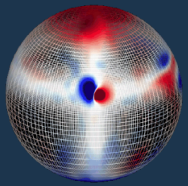

Fortran

OPEN MPI

Solar Storms Simulation

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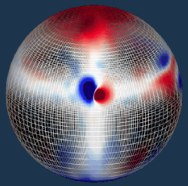

do concurrent

nvfortran

Fortran

Solar Storms Simulation

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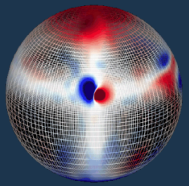

do concurrent

nvfortran

Fortran

Smaller code base
CPU/GPU parallelism

Solar Storms Simulation

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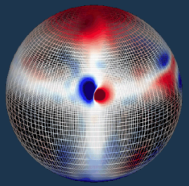

do concurrent

NVIDIA HPC DEV

nvfortran

Fortran

Smaller code base
CPU/GPU parallelism

OPEN MPI

GCC

gfortran

Solar Storms Simulation

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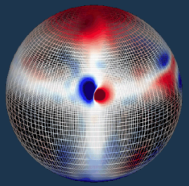

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No reduction in
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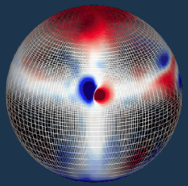

do concurrent

NVIDIA HPC DEV

nvfortran

Fortran

Smaller code base
CPU/GPU parallelism

OPEN MPI

OpenACC
More Science, Less Programming

Data Movement
Directives

GCC

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gfortran

Solar Storms Simulation

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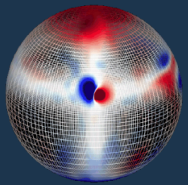

do concurrent

nvfortran

V100

×8

34.3 h

Fortran

Smaller code base
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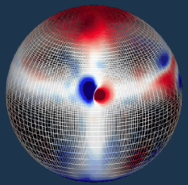

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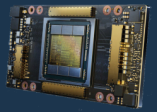
34.3 h

A100 40GB

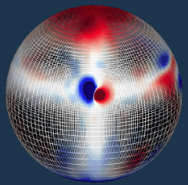


×8

23.7 h

Solar Storms Simulation

Ron Caplan : Computational Scientist, Predictive Science Inc.



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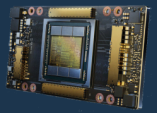
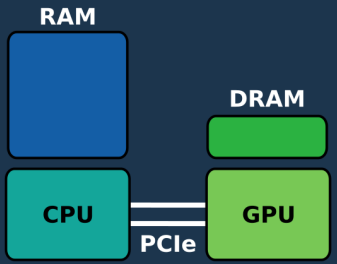


×8

23.7 h

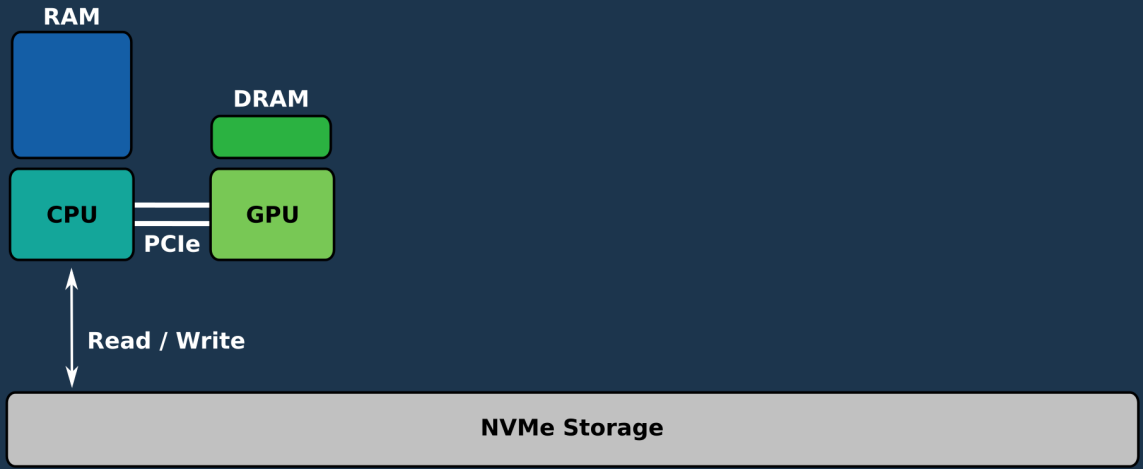
Computing needs went from
4 nodes to only
1 single node

Training with Grace Hopper



NVMe Storage

Training with Grace Hopper



Training with Grace Hopper

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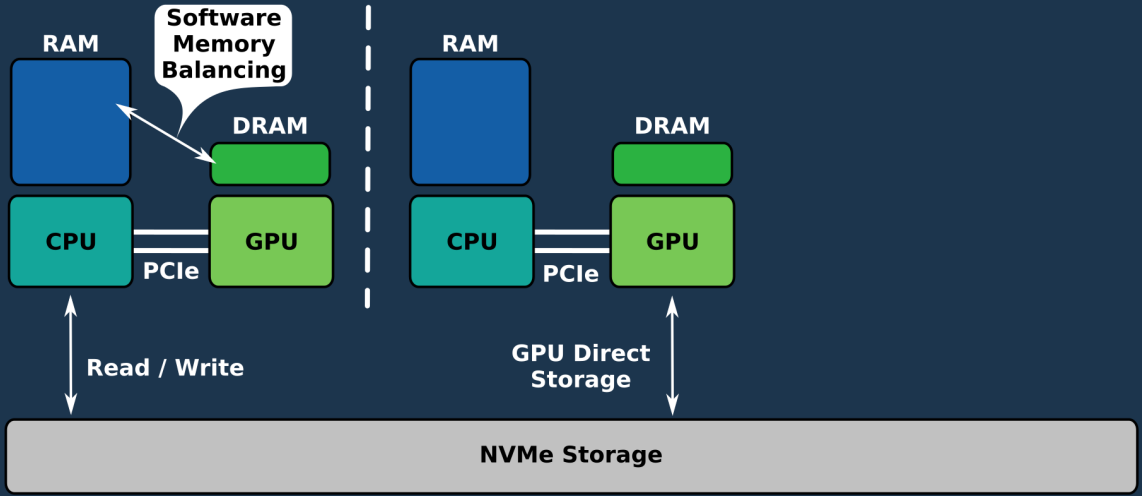

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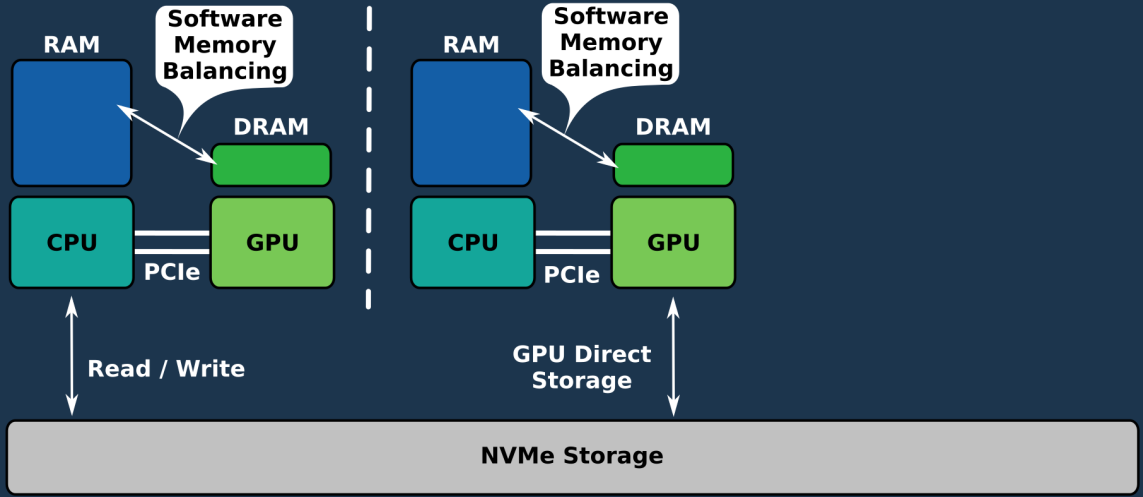

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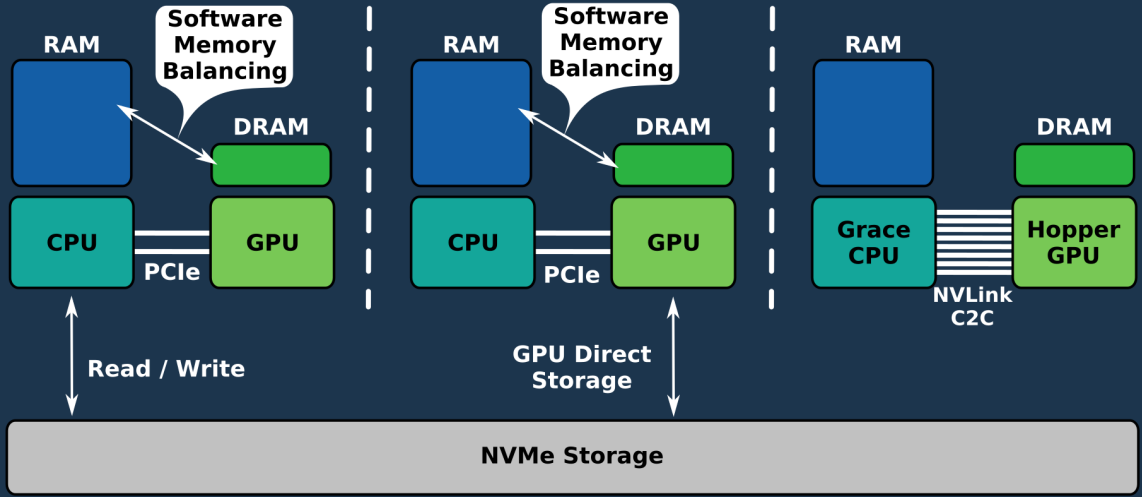

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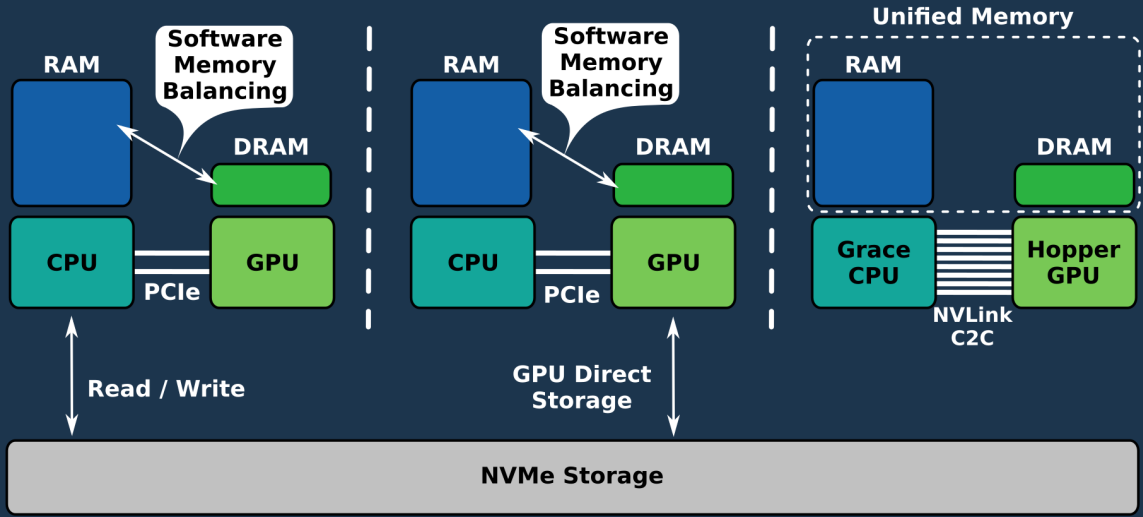

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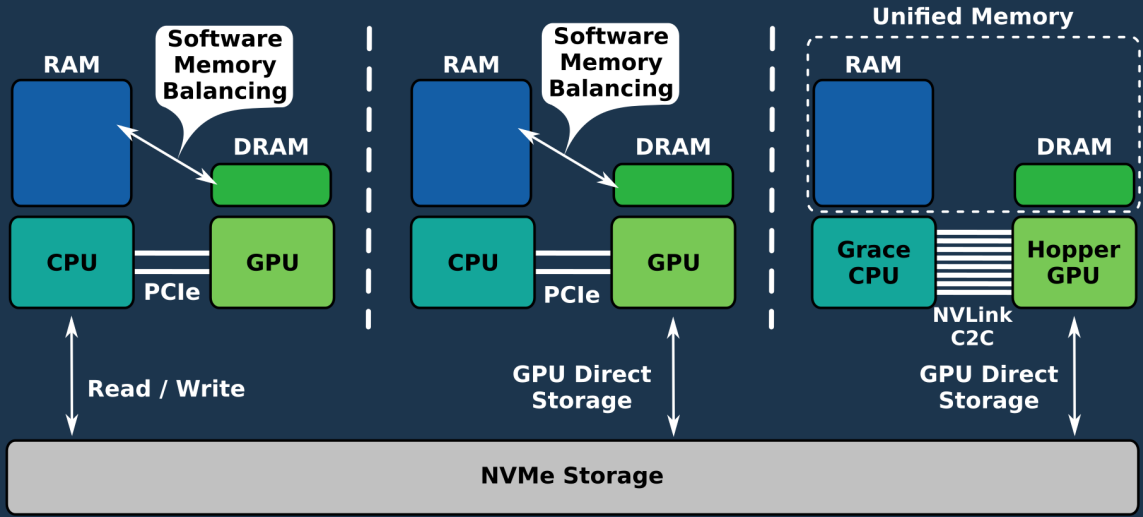

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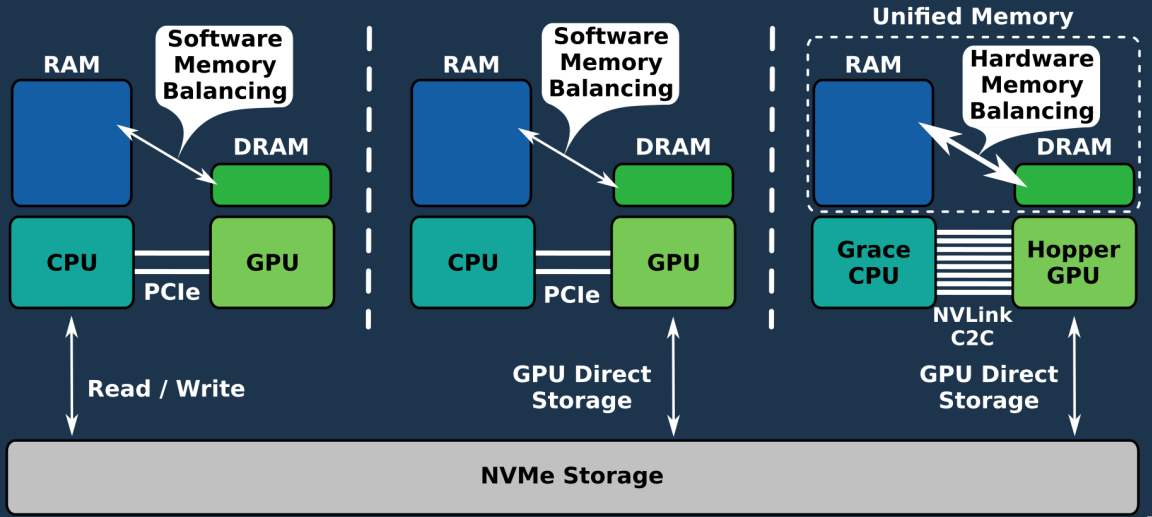

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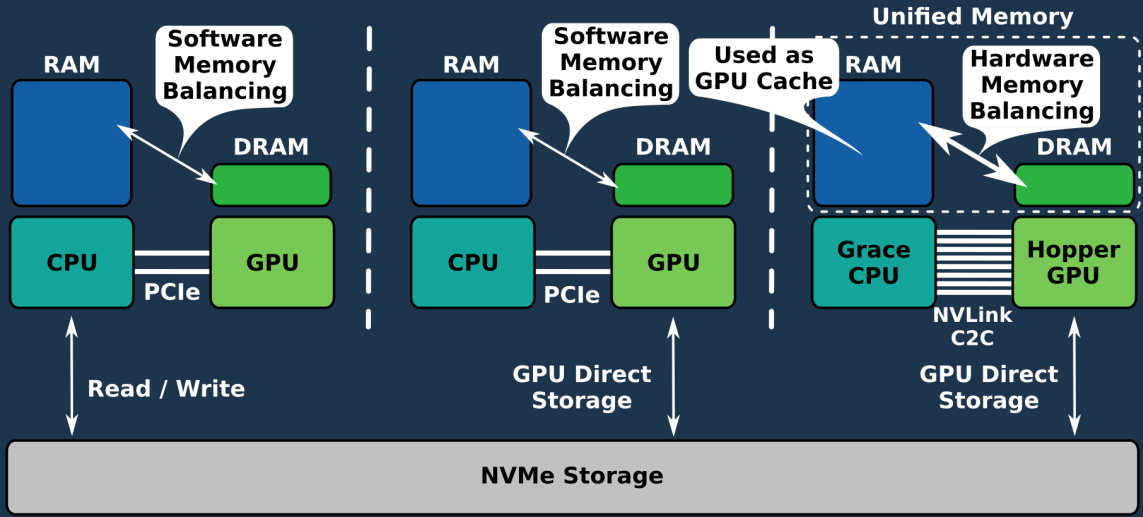

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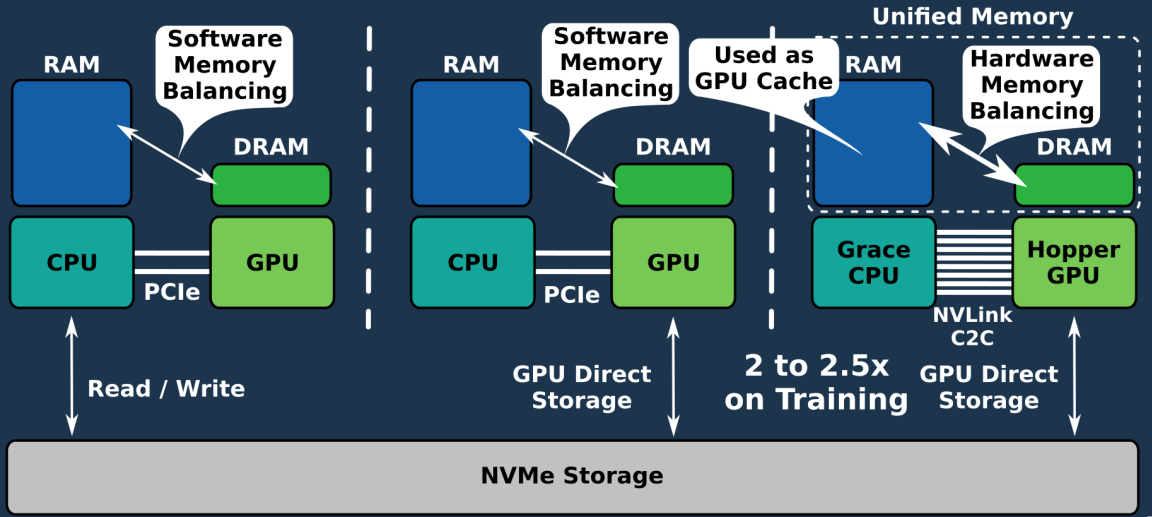
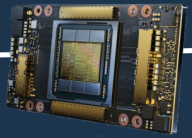


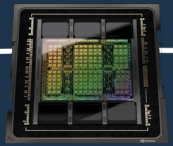
End of the first part

End of the first part

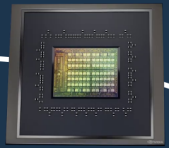
A100



H100



Grace CPU



Grace Superchip

Grace Hopper Superchip

Introduction Second Part

GTC 2024 Presentation Catalog

This is not possible to summarize **1080** talks !

Only focus on :

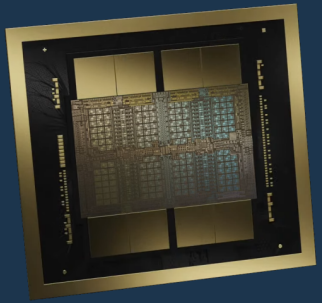
- **Hardwares** evolution
- **Frameworks** evolution :
  - **Computing**
  - **Data Formats**
  - **Machine Learning** / **Deep Learning**
- **Photolithography**

Keynotes video link

2024 - Blackwell GPU

2024 - Blackwell GPU

B100 (Blackwell)



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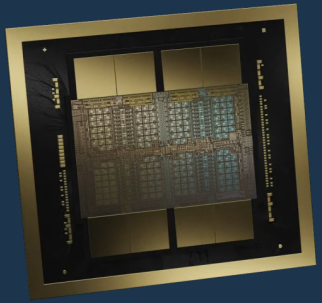
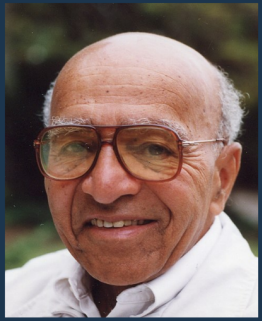




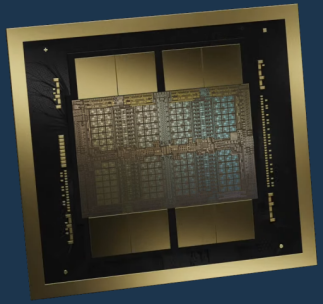
David Harold Blackwell (1919 - 2010)

Statistician and **mathematician** :
- **Game theory**
- **Probability theory**
- **Information theory**
- **Statistics**

2024 - Blackwell GPU

4 nm

B100 (Blackwell)

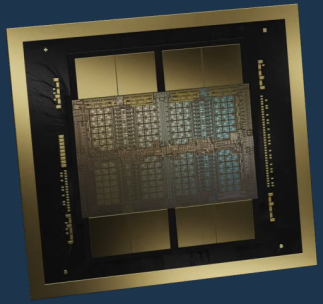


2024 - Blackwell GPU

4 nm

Compute Capabilites **10.0**

B100 (Blackwell)



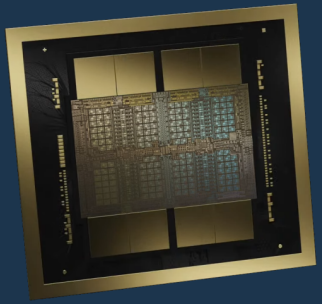
2024 - Blackwell GPU

4 nm

Compute Capabilites **10.0**

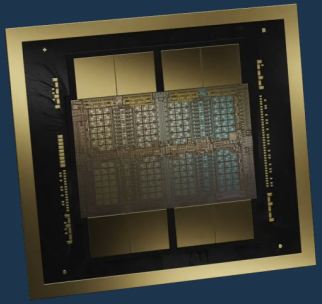
160 SMs (tensor core Gen4) 10240 Cores

B100 (Blackwell)



2024 - Blackwell GPU

B100 (Blackwell)



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160 SMs (tensor core Gen4) 10240 Cores

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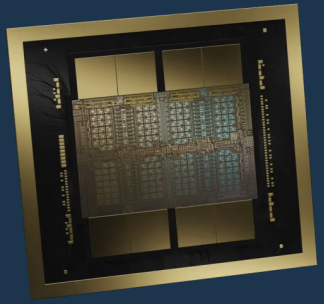
2024 - Blackwell GPU

B100 (Blackwell)



4 nm

Compute Capabilites **10.0**

160 SMs (tensor core Gen4) 10240 Cores

192 GB HBM3e

8 TB/s Bandwidth

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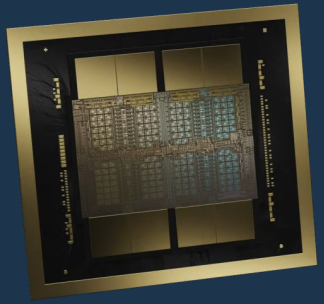

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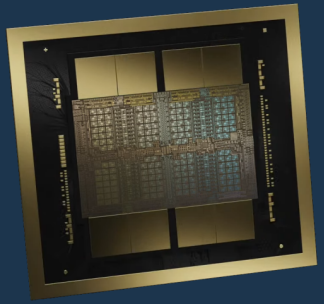

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More computing precisions

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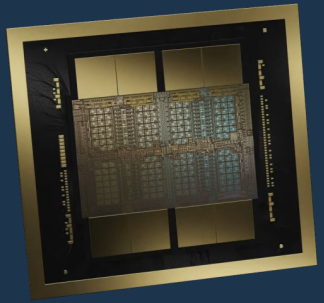

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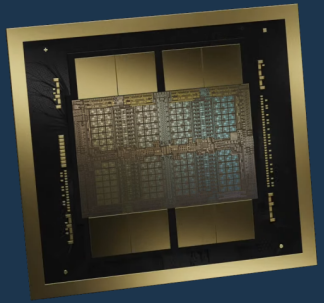

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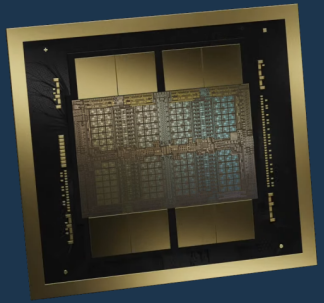

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Secure AI : full performance encryption

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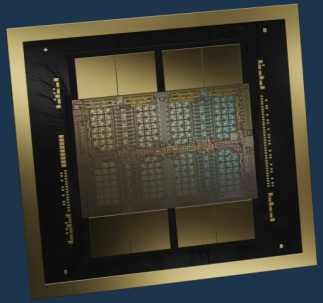

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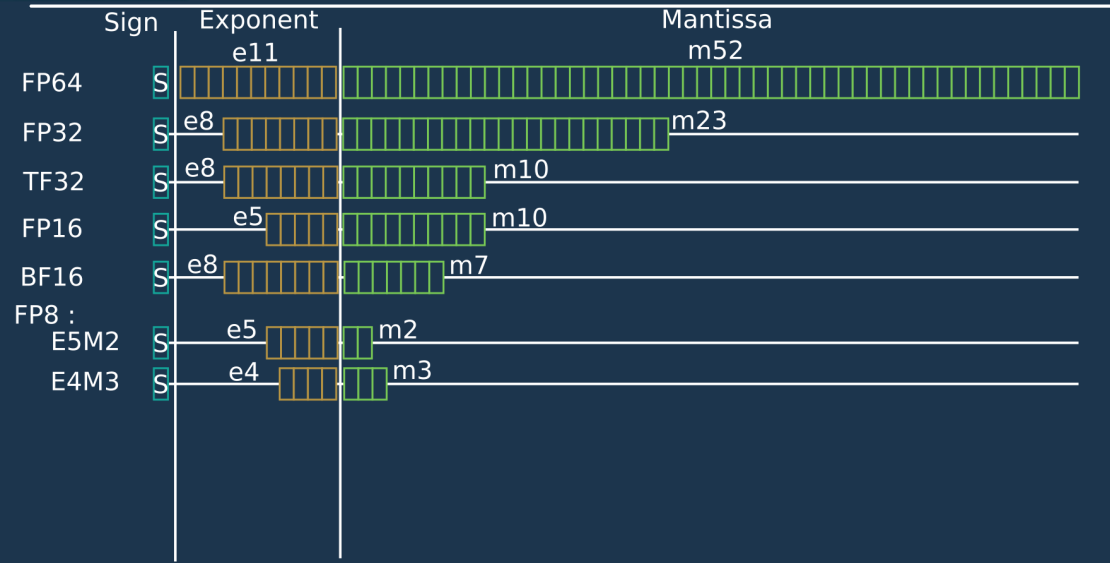
RAS Engine

More Computing Precision



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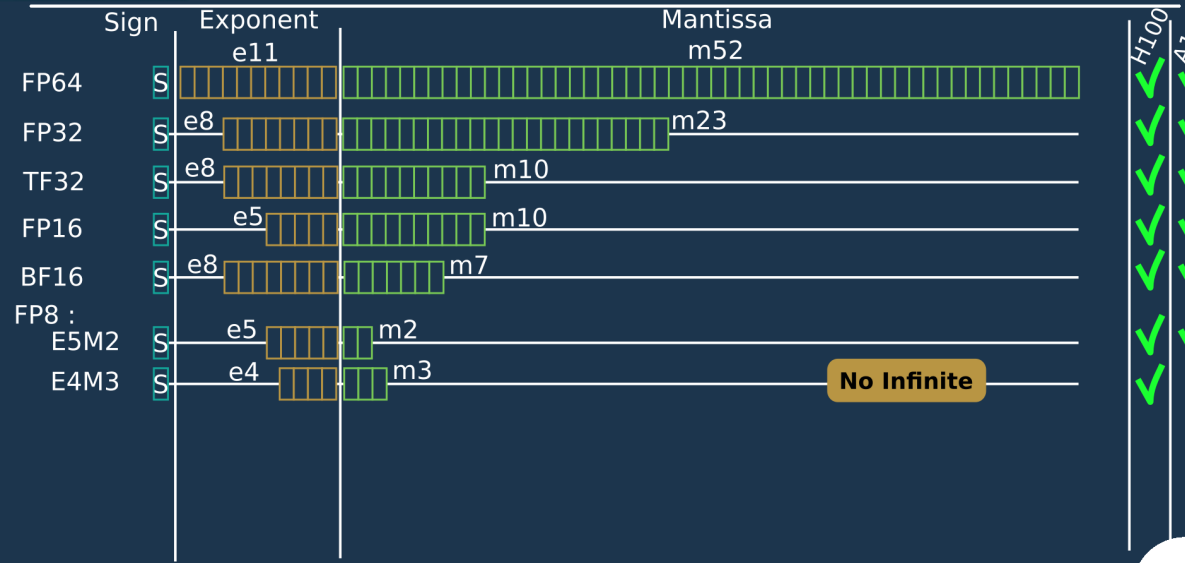

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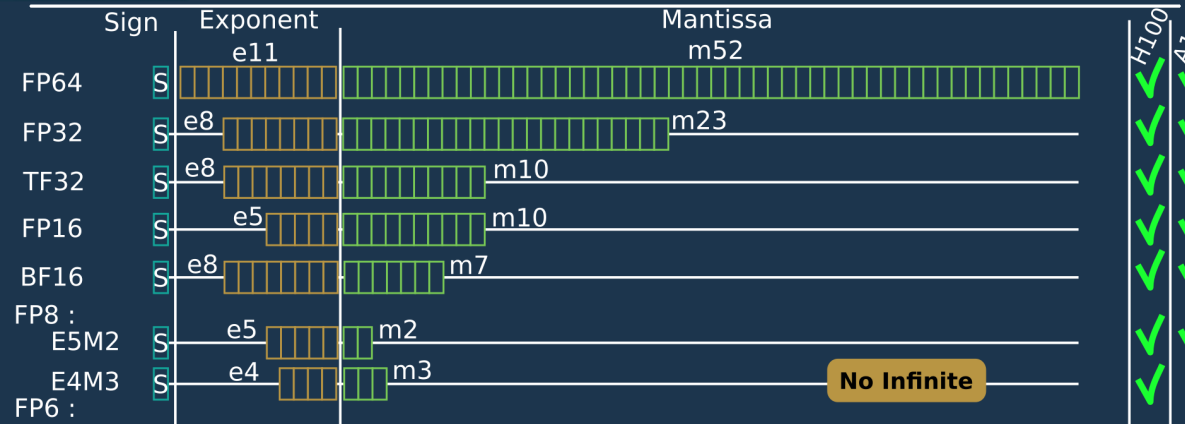

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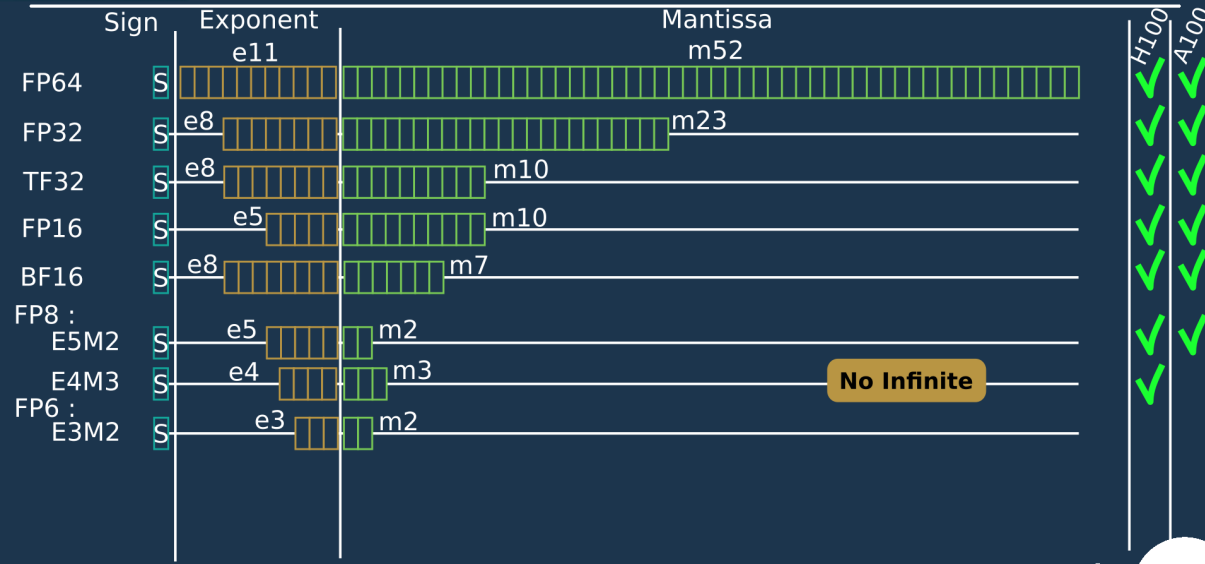

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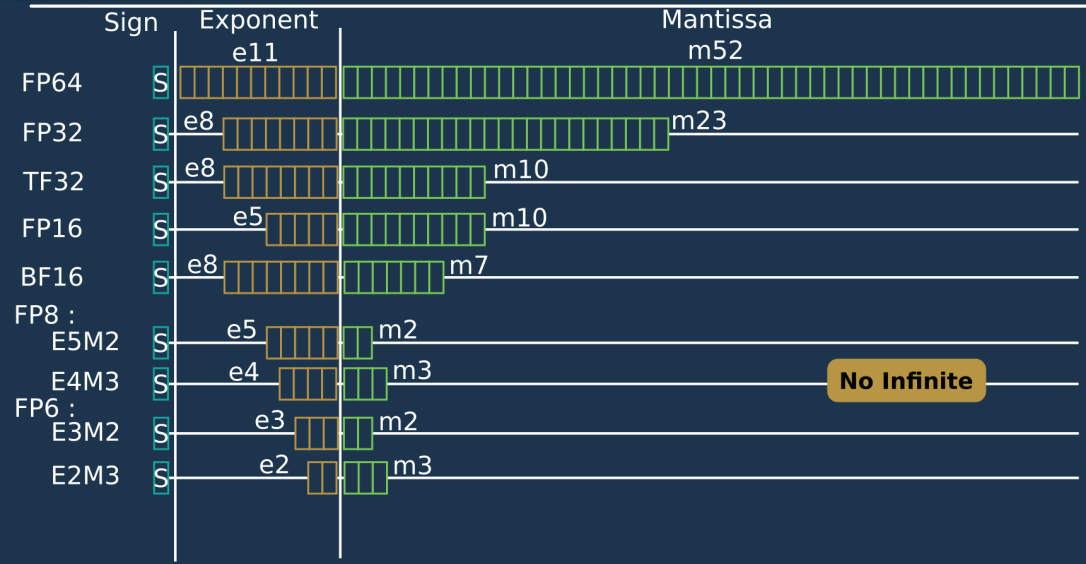

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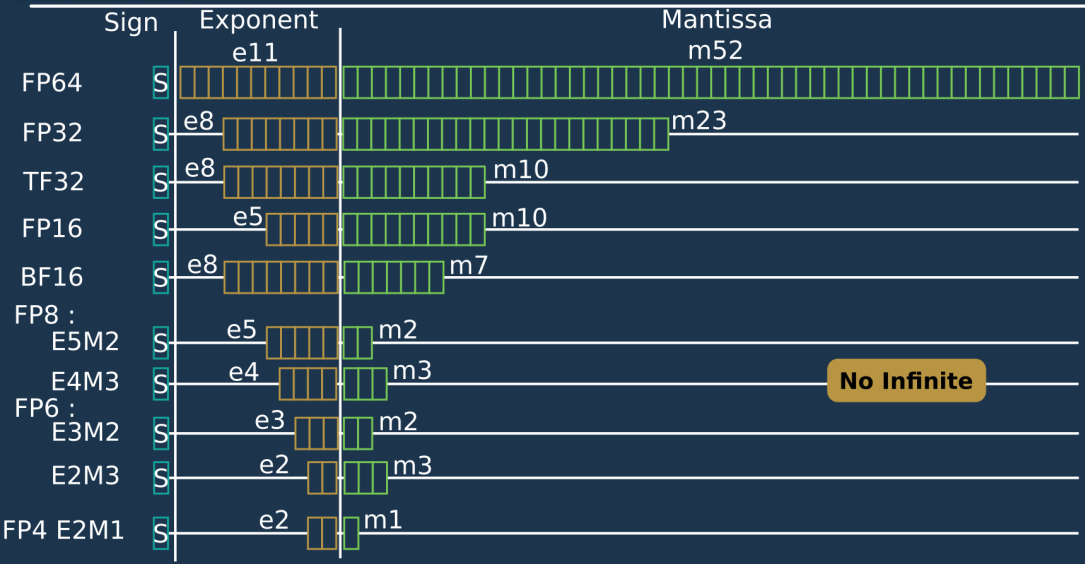

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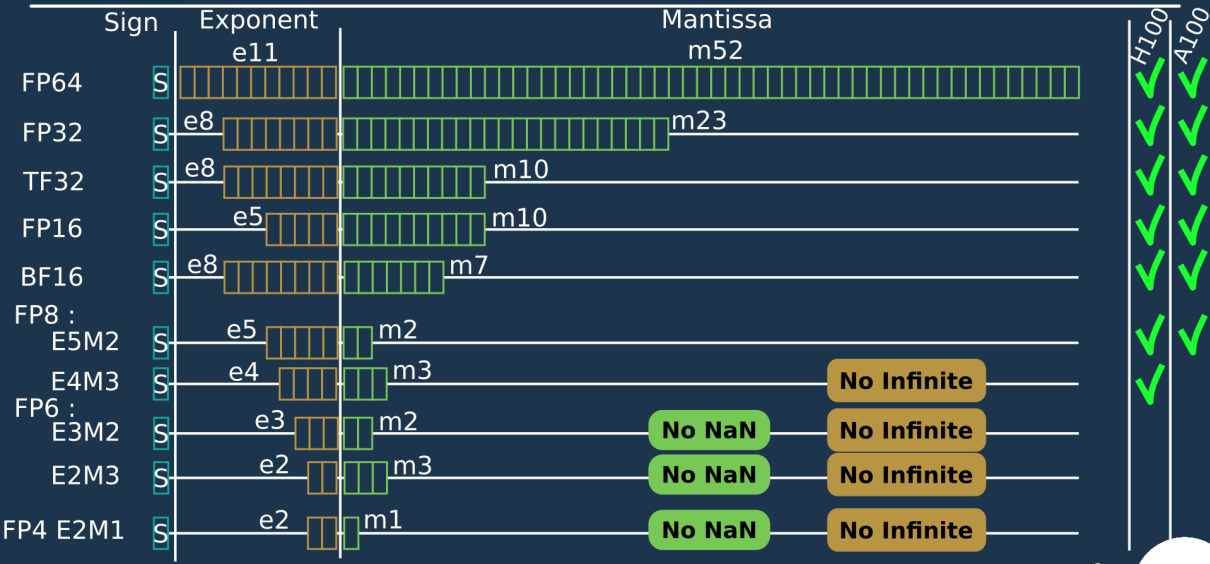

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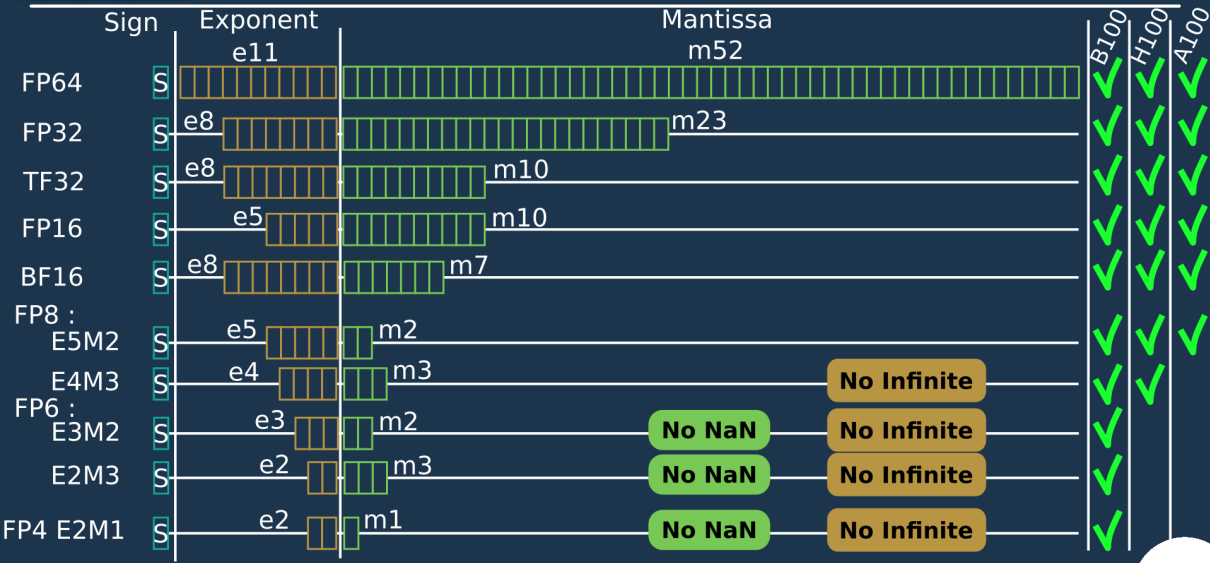
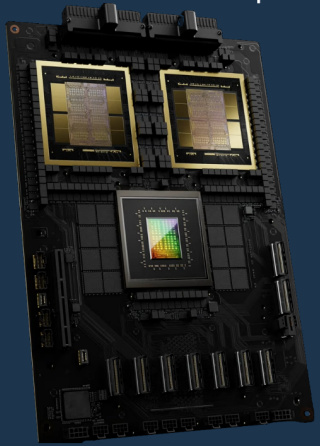


Grace Blackwell Superchip

1 Grace CPU + **2 Blackwell** GPU

GB200
(Grace Blackwell Superchip)



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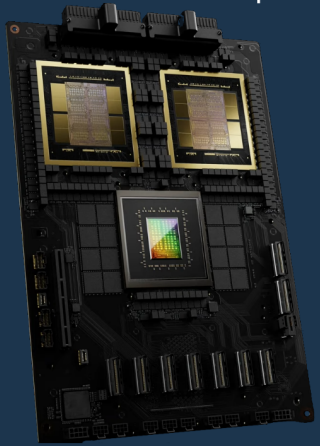

1 Grace CPU + **2 Blackwell** GPU

GPU

- **90** TFlops : **FP64** Tensor Core
- **5** PFlops : **TF32** Tensor Core
- **10** PFlops : **FP16** / **BF16** Tensor Core
- **20** PFlops : **FP8** / **FP6** Tensor Core
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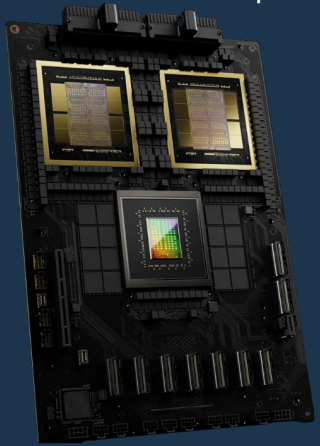

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CPU (Grace **7** TFlops)
- **480** GB LPDDR5X
- **512** GB/s Bandwidth
- NVLink (3.6 TB/s)

Grace Blackwell Superchip

Grace Blackwell Superchip

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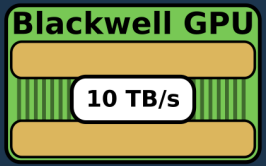

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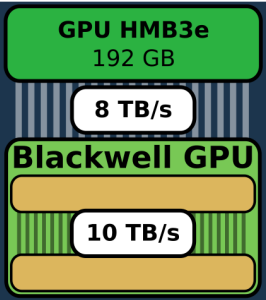

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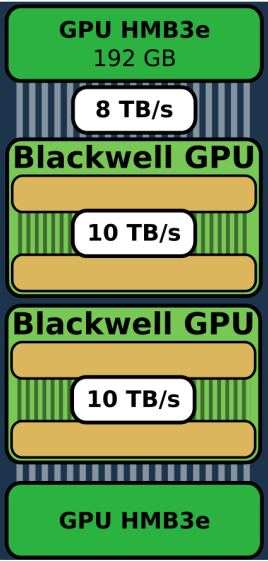

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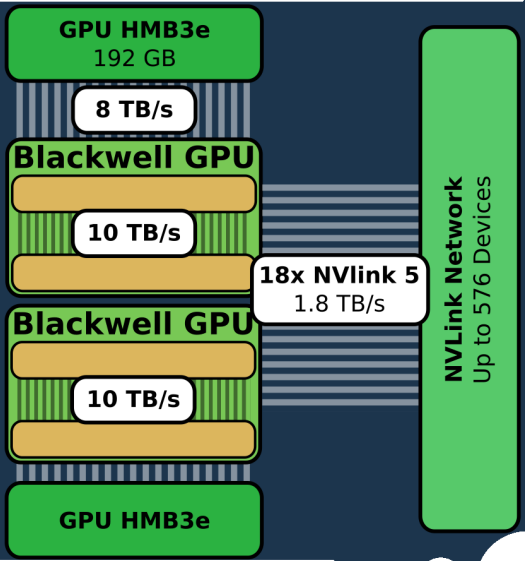

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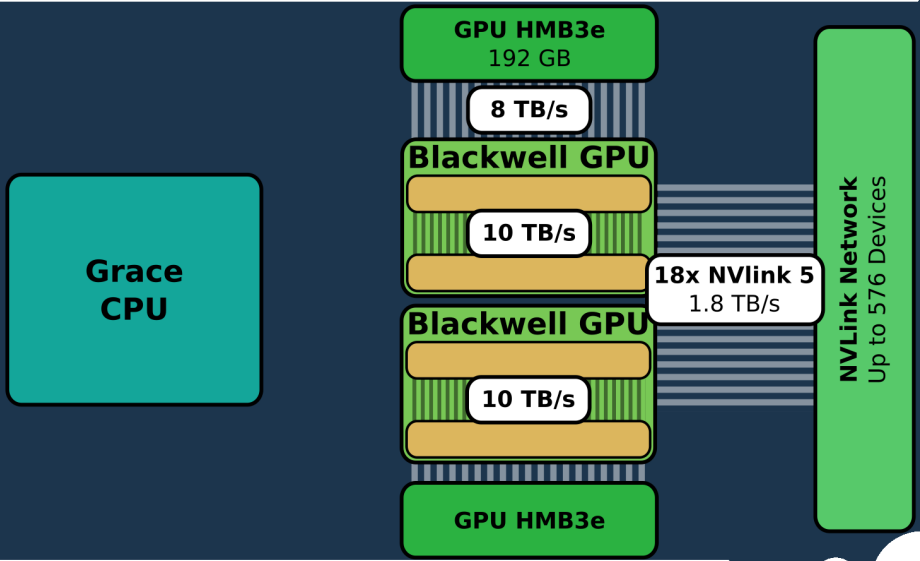

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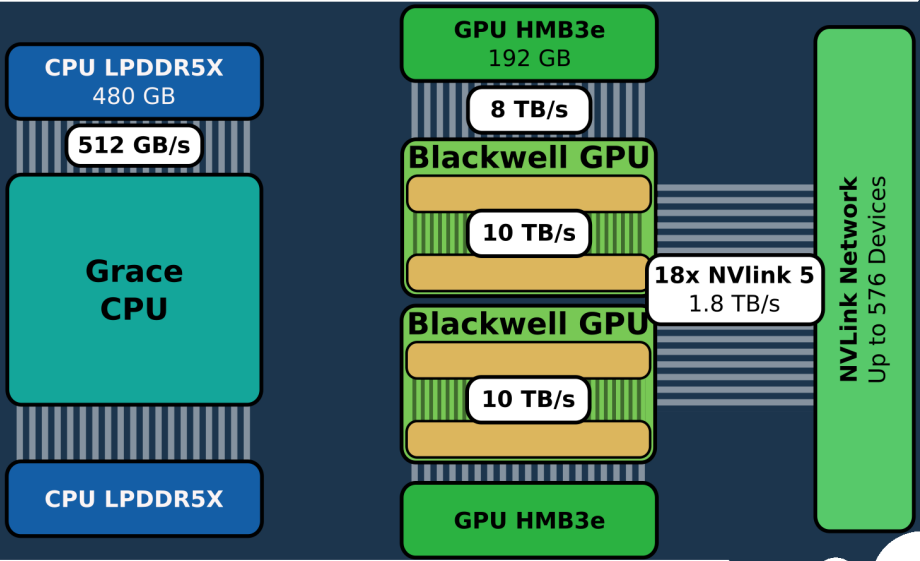

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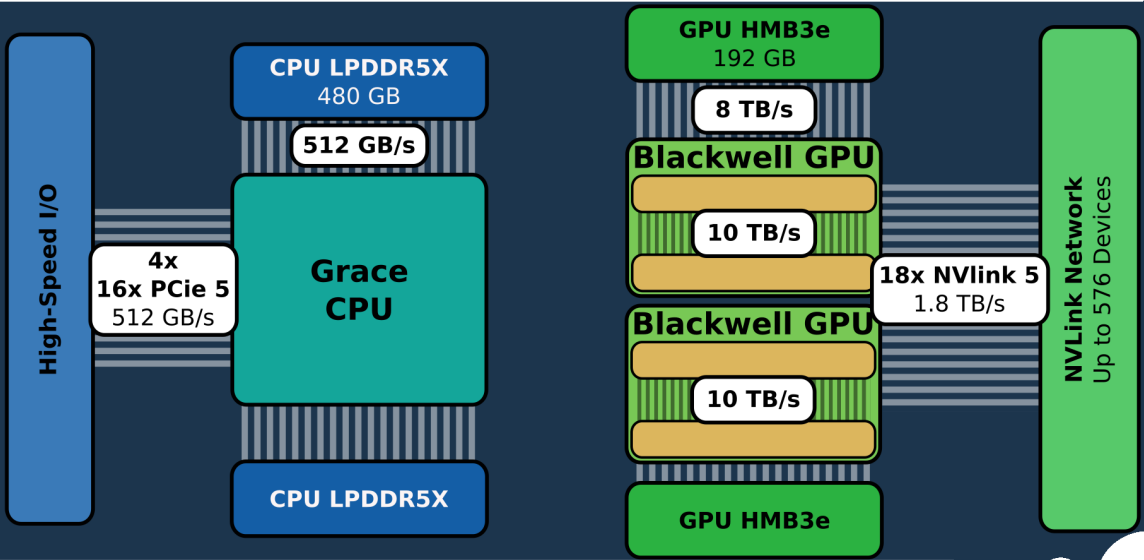

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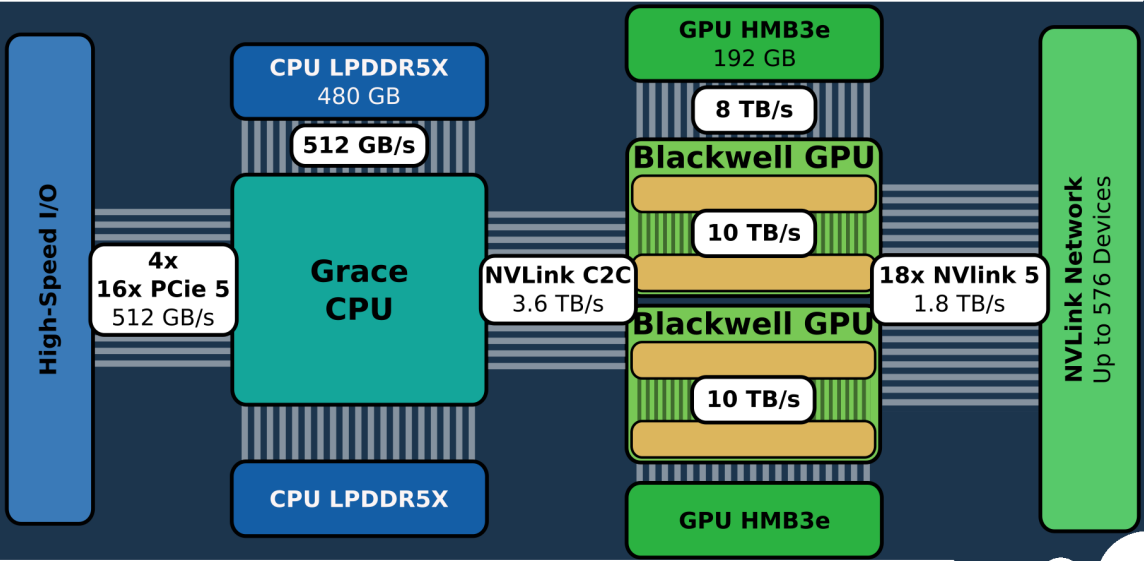

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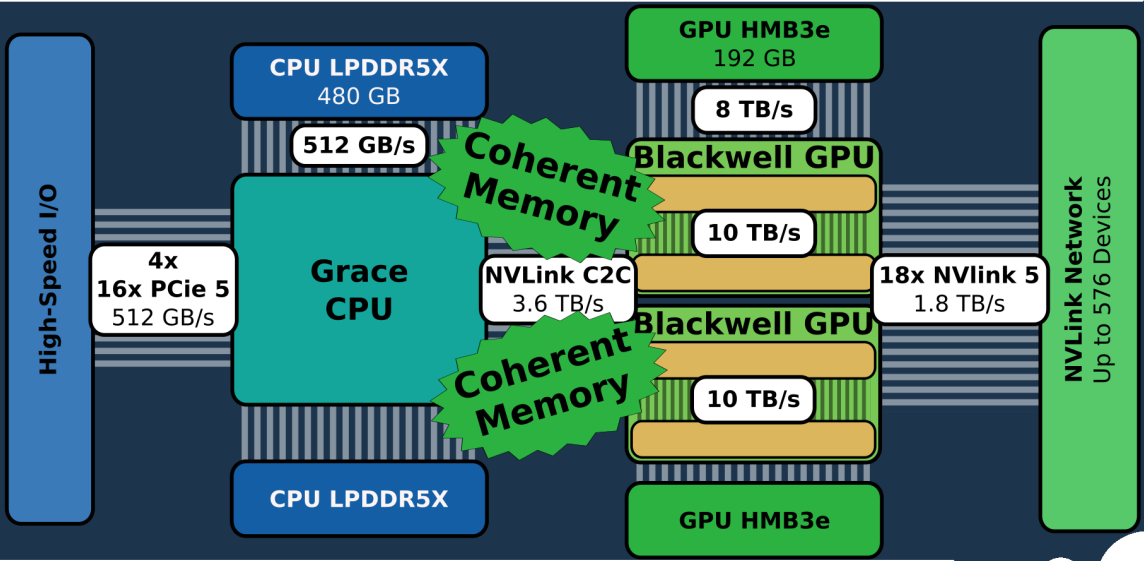
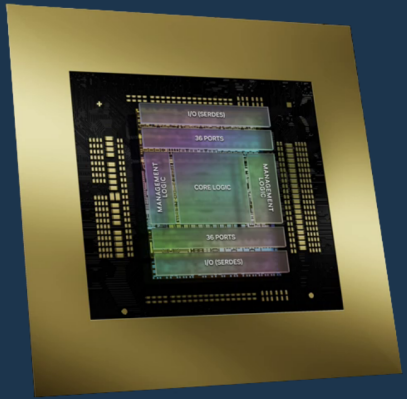


NVLink Switch Chip



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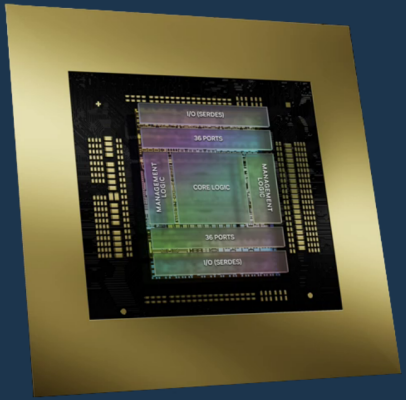
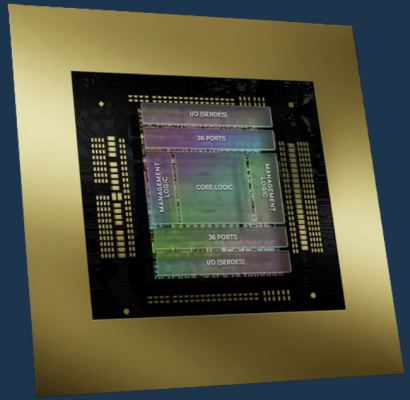


50B Transistors

NVLink Switch Chip



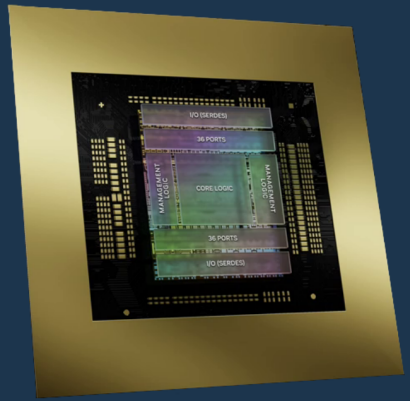
50B Transistors

72-Ports dual **200** Gb/s SerDes

4 NVlink at **1.8** TB/s

7.2 TB/s full duplex bandwidth

NVLink Switch Chip



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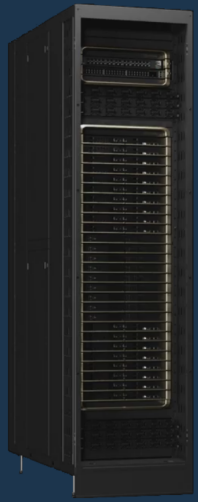
Sharp-In Network compute **3.6** TFlops **FP8**

Blackwell Rack

Blackwell Rack



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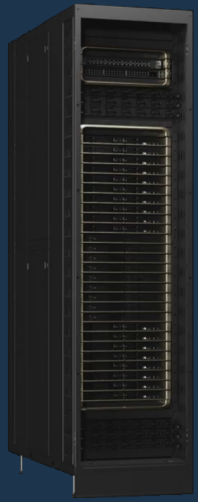

36 Grace CPU + **72 Blackwell** GPU

Blackwell Rack

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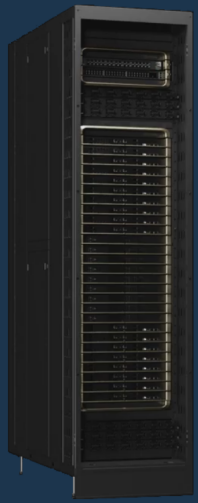

36 Grace CPU + **72 Blackwell** GPU

Mixed Precision Performance :

720 PFlops : Training

1440 PFlops : Inference (with **FP4**/**FP6** and sparsity)

Blackwell Rack

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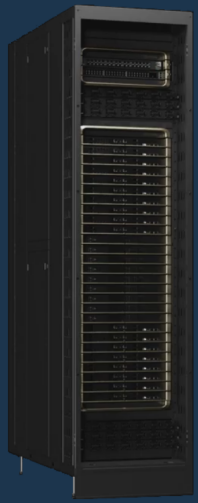

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Water Cooling : in **25**°C, out **45**°C at **2** l/s

Weight : **1.5** t (**600 000** parts)

5000 NVLink cables

Blackwell Rack

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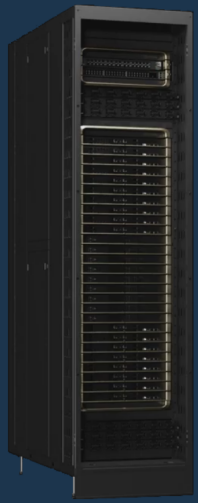

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First EFlop Rack

Blackwell Plateform

Blackwell Plateform

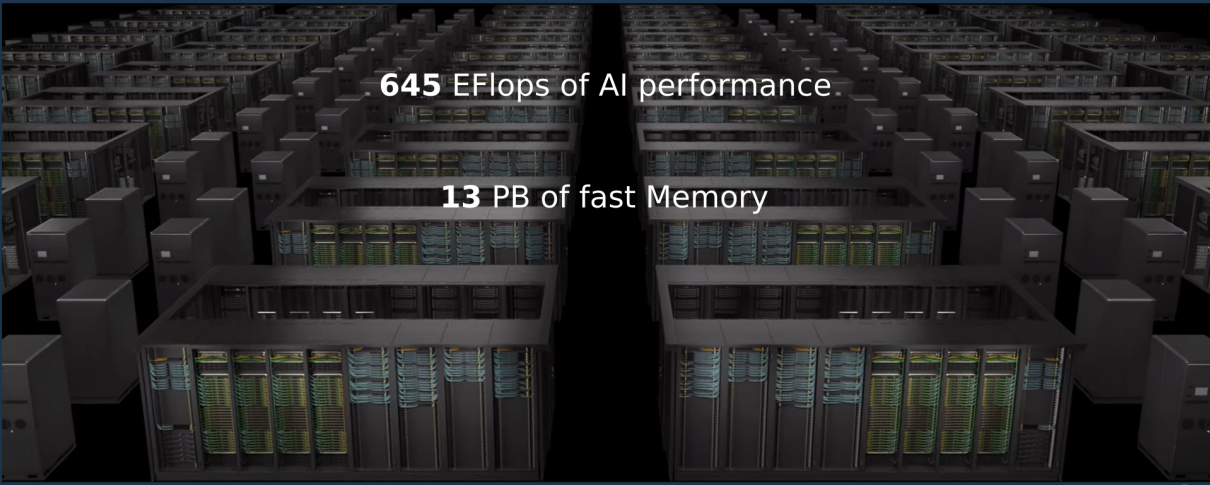
32000 Blackwell GPU

Blackwell Plateform

32000 Blackwell GPU

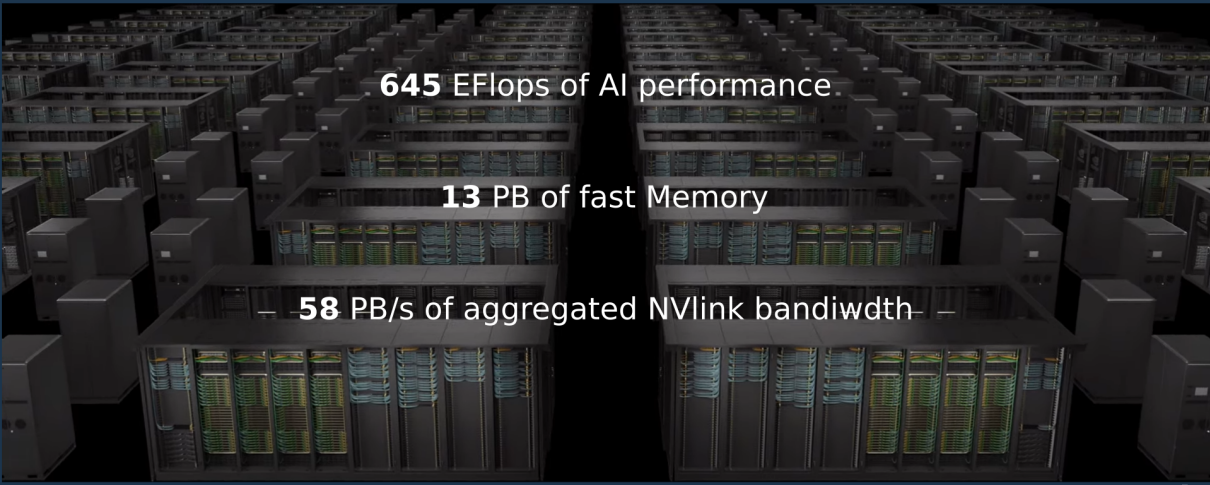
Blackwell Plateform

32000 Blackwell GPU



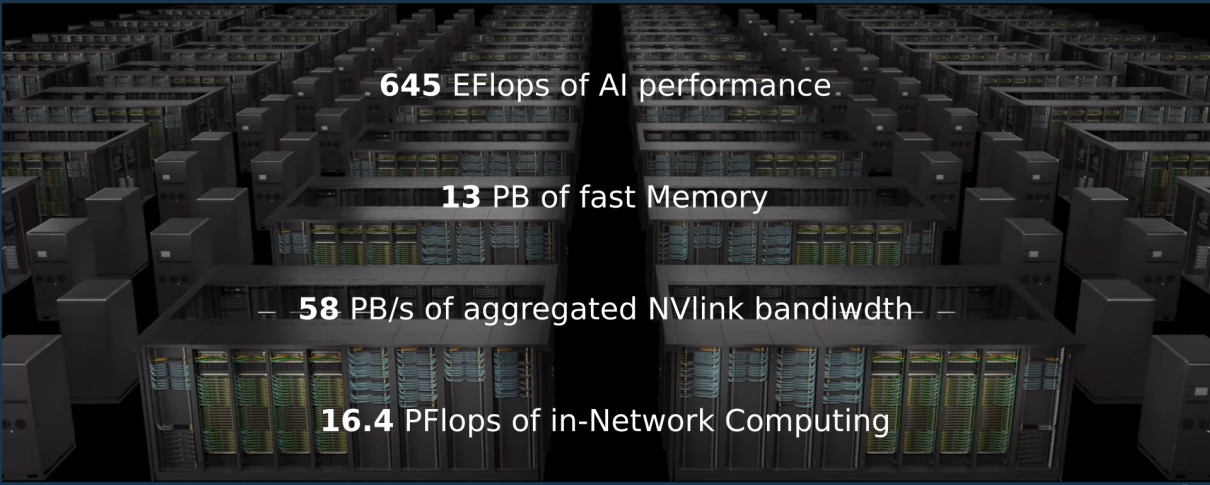
Blackwell Plateform

32000 Blackwell GPU



Blackwell Plateform

32000 Blackwell GPU



645 EFlops of AI performance

13 PB of fast Memory

58 PB/s of aggregated NVlink bandiwdth

16.4 PFlops of in-Network Computing

Photo-lithography

Photo-lithography

Reverse Lithography

Photo-lithography

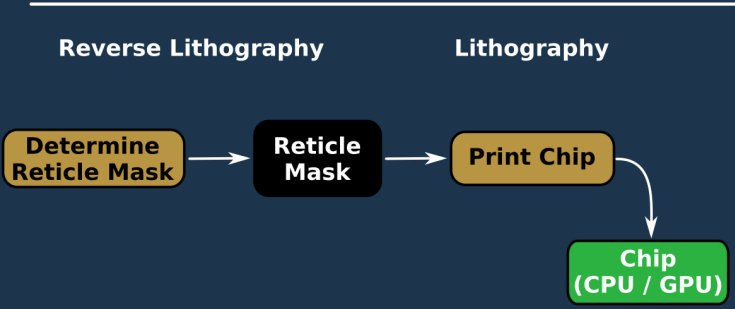


Photo-lithography

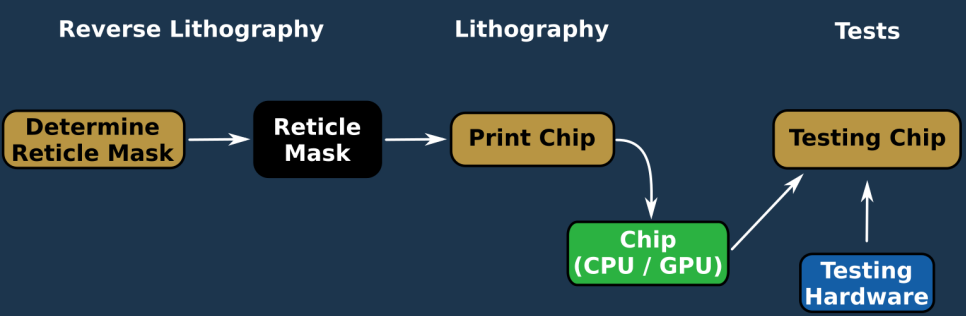


Photo-lithography

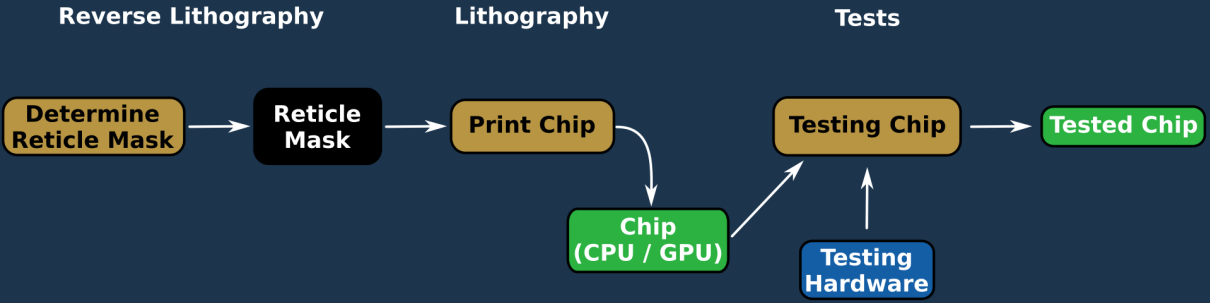


Photo-lithography

Reverse Lithography | **Lithography** | **Tests**

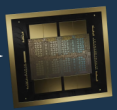
Determine Reticle Mask → **Reticle Mask** → **Print Chip** → **Chip (CPU / GPU)** → **Testing Chip** ← **Testing Hardware** → **Tested Chip**

Computing Centers become chips

Titan (2012)
7MW

20 PFlops

Blackwell (2024)
1 kW



20 PFlops

Photo-lithography

Reverse Lithography

Determine Reticle Mask → **Reticle Mask**

Lithography

Print Chip → **Chip (CPU / GPU)**

Tests

Testing Chip → **Tested Chip**

Testing Hardware

Chip +
Test Components

RAS Engine

Computing Centers become chips

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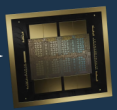

20 PFlops

Photo-lithography

Reverse Lithography

Lithography

Tests

Determine Reticle Mask → Reticle Mask → Print Chip → Testing Chip → Tested Chip

Chip (CPU / GPU)

Testing Hardware

Enable test Monitoring

Chip + Test Components

RAS Engine

Computing Centers become chips

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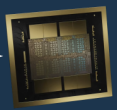
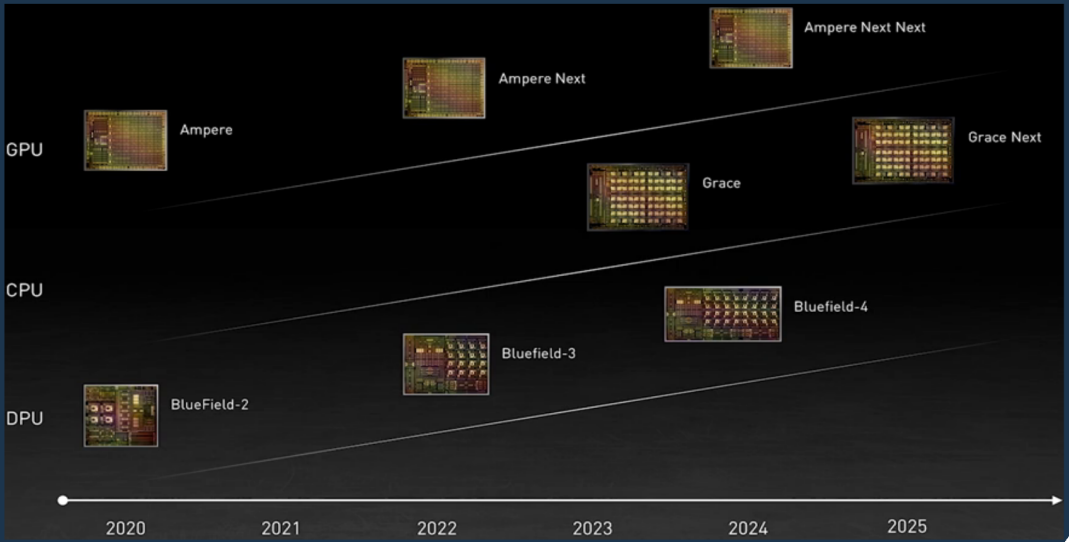


20 PFlops

NVidia roadmap



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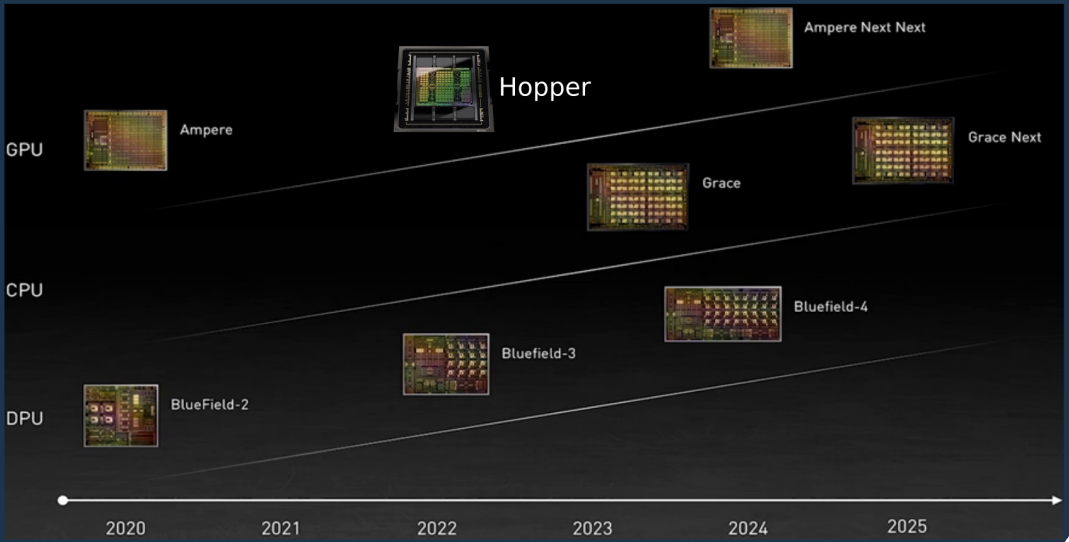

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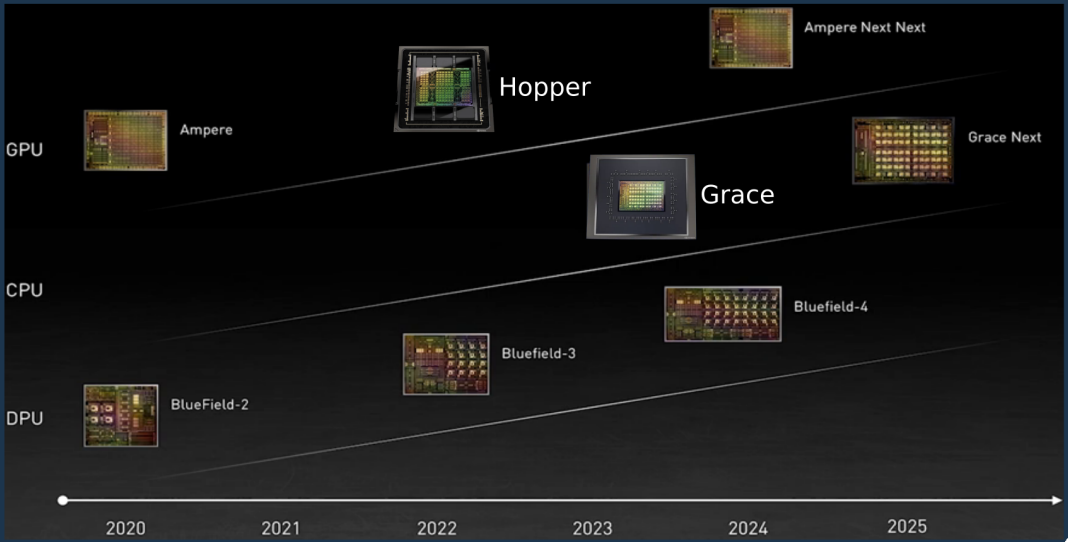

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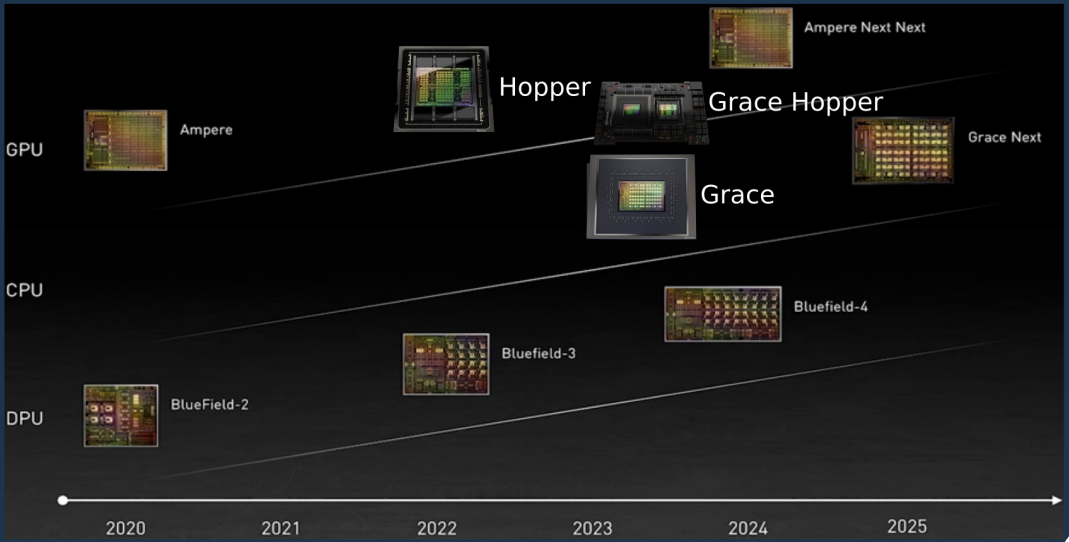

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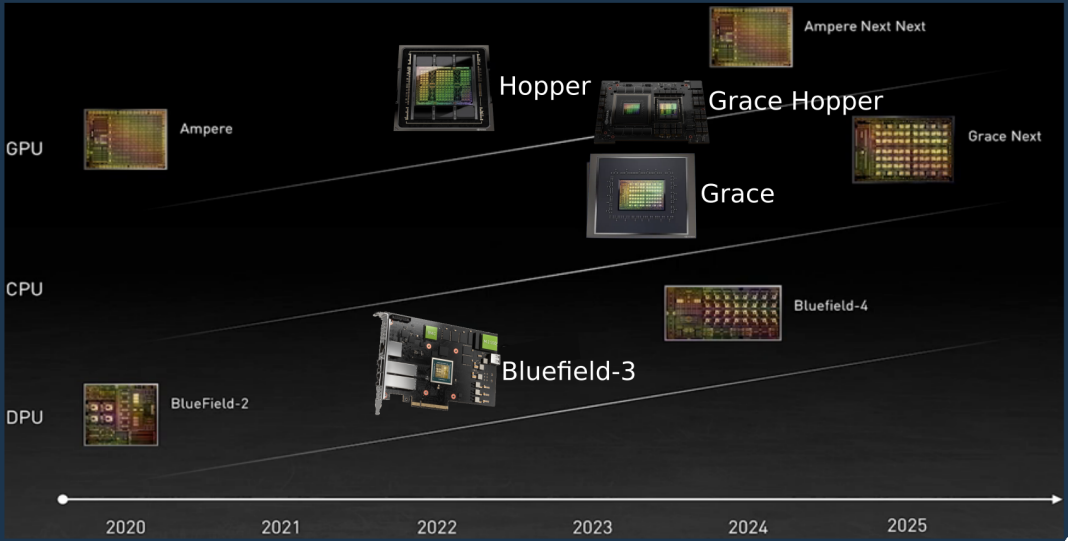

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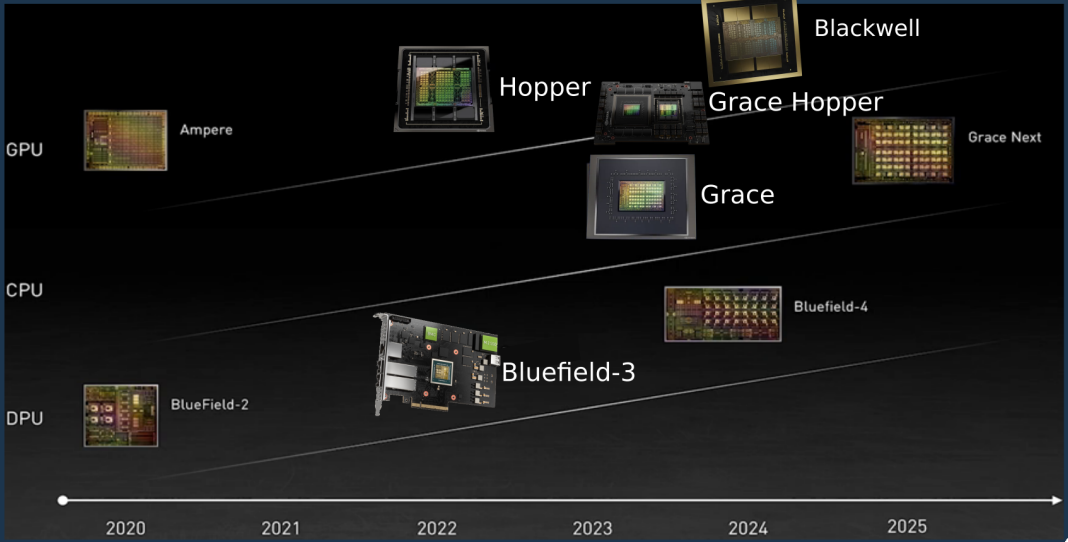
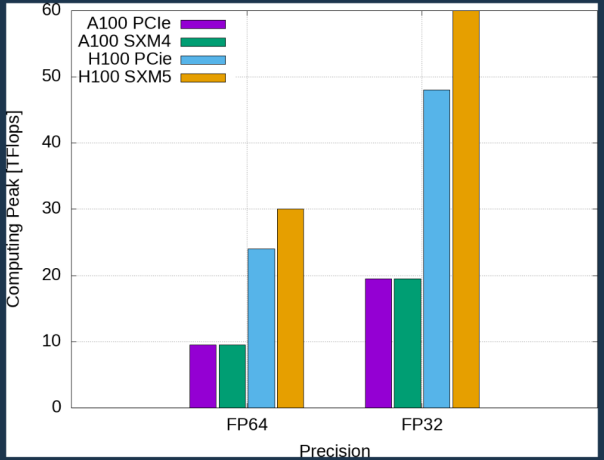


Why using Tensor Cores ?

CUDA Cores



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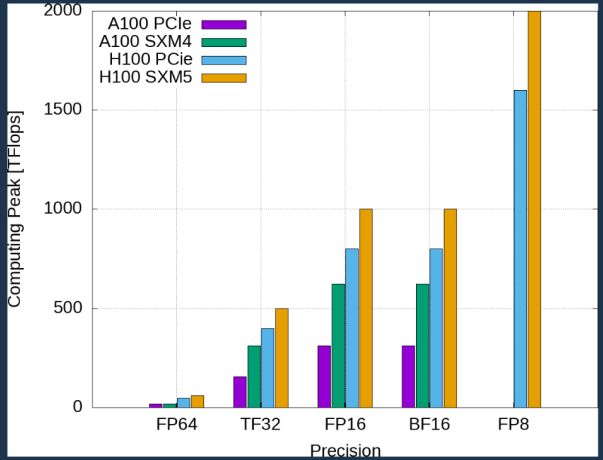

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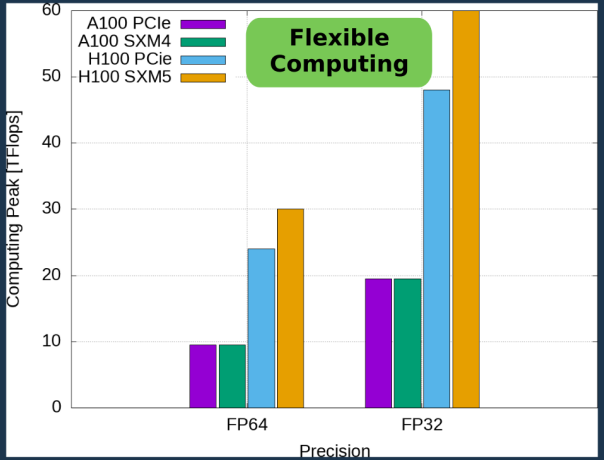

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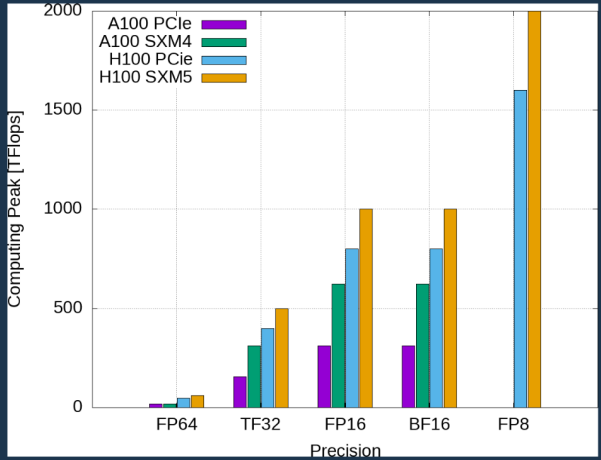

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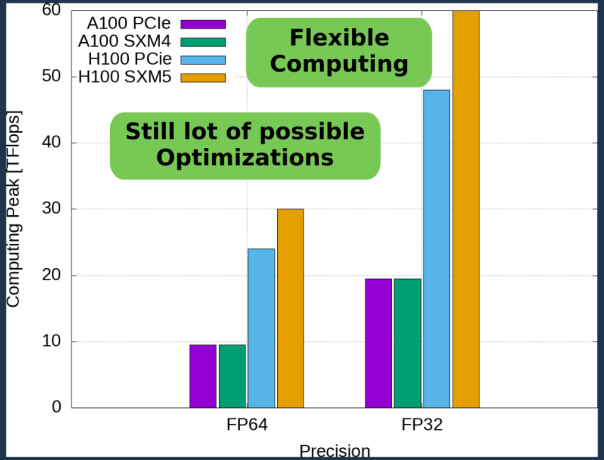

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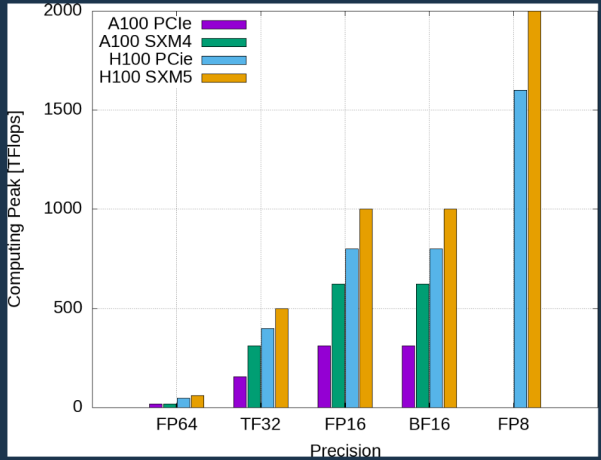

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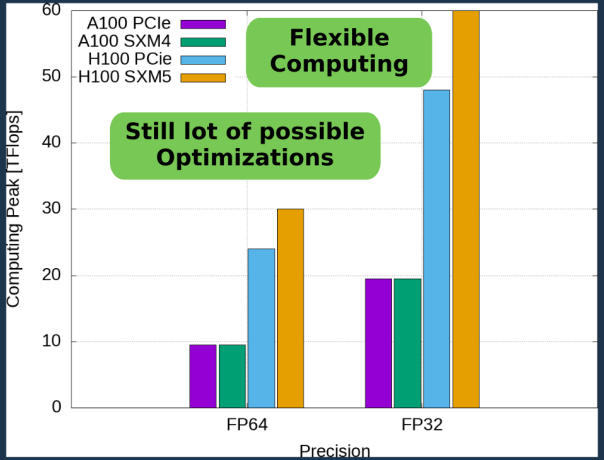

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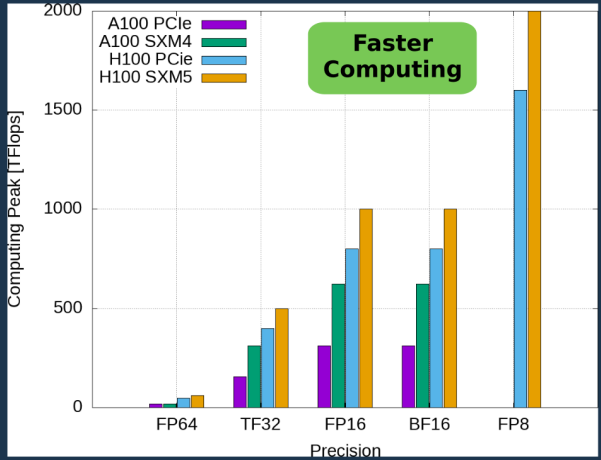

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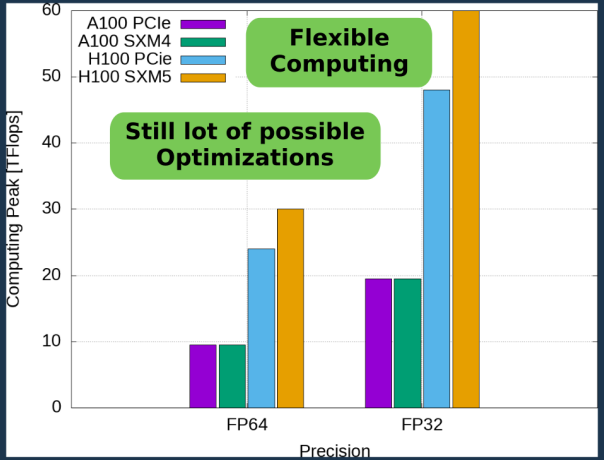

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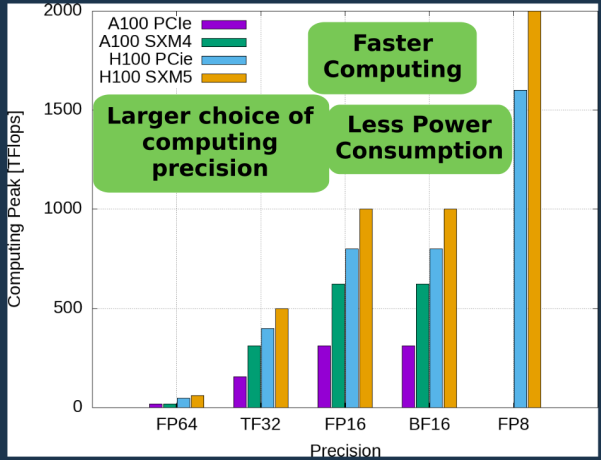

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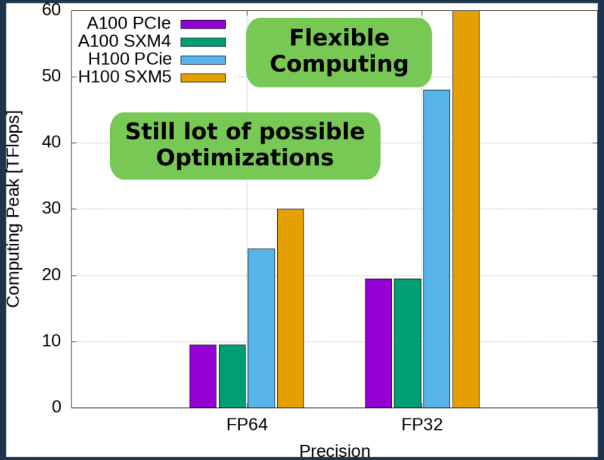

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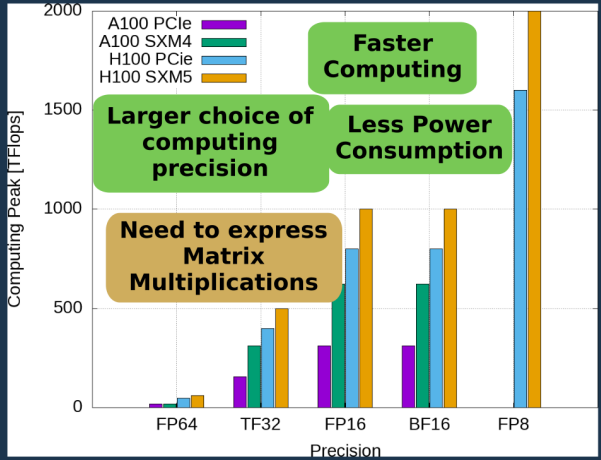

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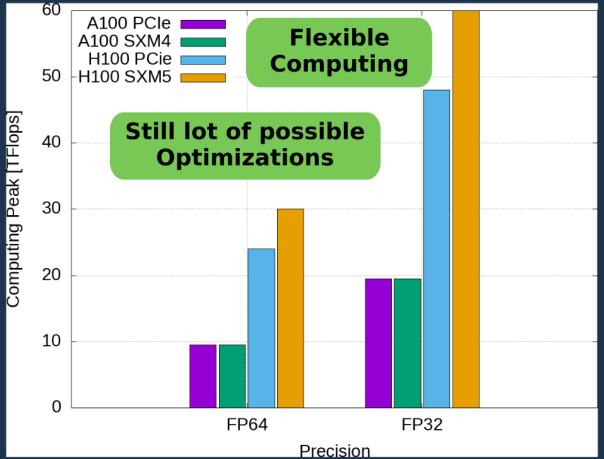

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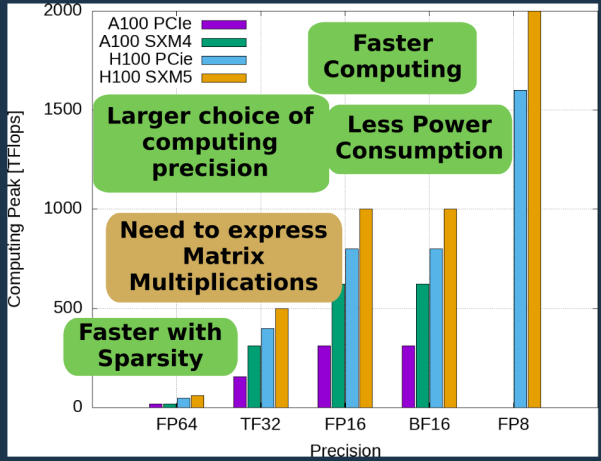

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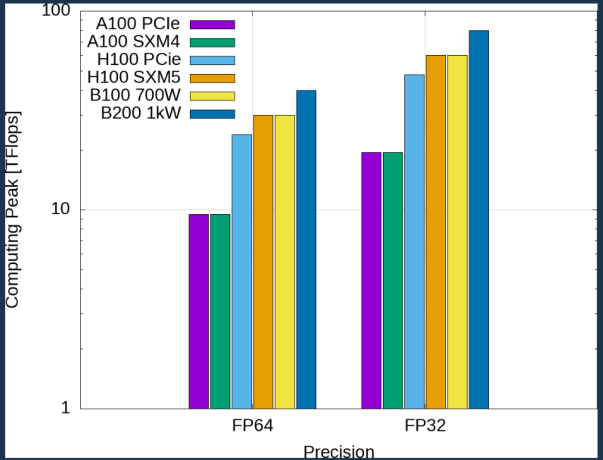

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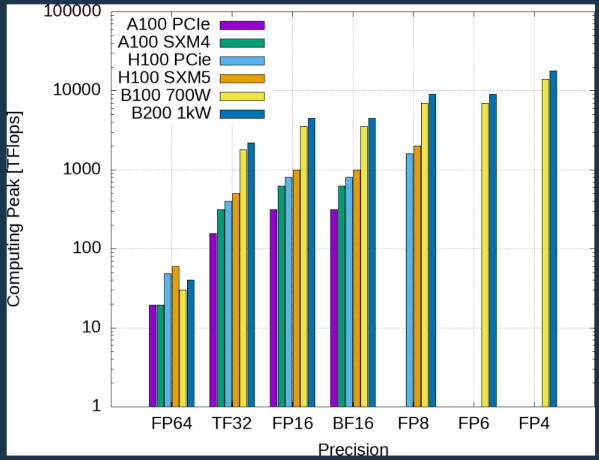

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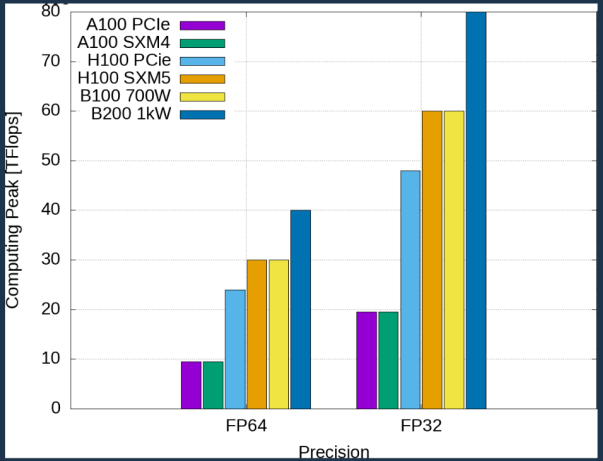

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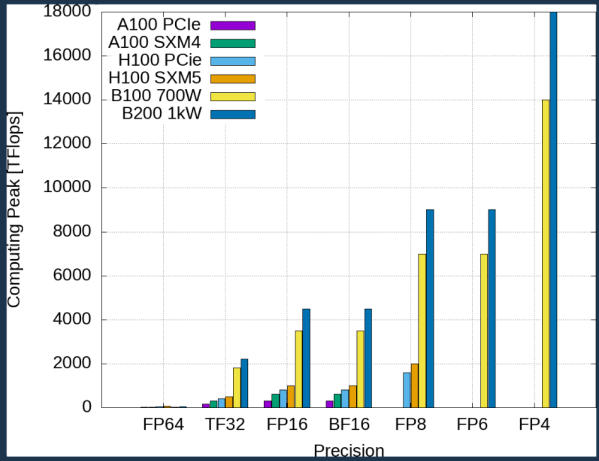

How to use Tensor Cores ?

How to use Tensor Cores ?

Use Existing LIbraries

CUTLASS

BLAS **LAPACK** **PBLAS** **SCALAPACK**

TENSOR **SPARSE** **RAND** **FFT**

cunumeric **legate**

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And libraries based on these ones

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LU decomposition
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Ongoing studies on **weather forecasting** (**ALPS**)

Hardware can **mix automatically** :
- **V100** : **FP32** + **FP16**
- **H100** : **All** available
- **B100** : **All** available
and keep desired precision

CUTLASS

Open Source: https://github.com/NVIDIA/cutlass

CUTLASS

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GEMM

CUTLASS

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GEMM **Convolution**

CUTLASS

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CUTLASS

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Precision : From **FP64** to **FP8**

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GEMM **Convolution** **Reduction**

Precision : From **FP64** to **FP8**

Mixed Input GEMM

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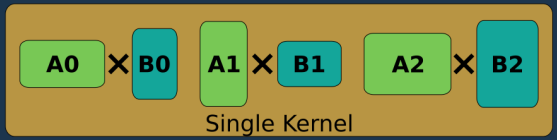
GEMM **Convolution** **Reduction**

Grouped GEMM



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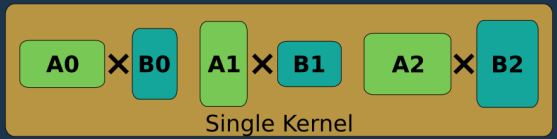

Efficient for **Mixture of Experts**

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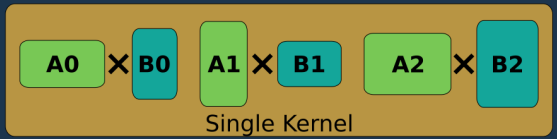

Efficient for **Mixture of Experts**

Composable Load Balancing

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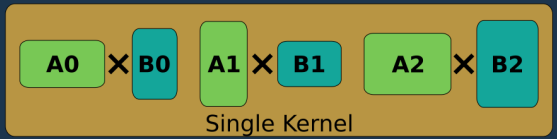

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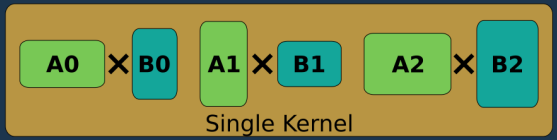

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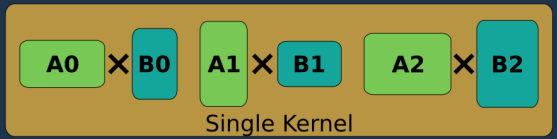

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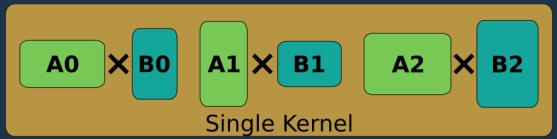

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Computing Backend PyTorch

NSight Profiler Update

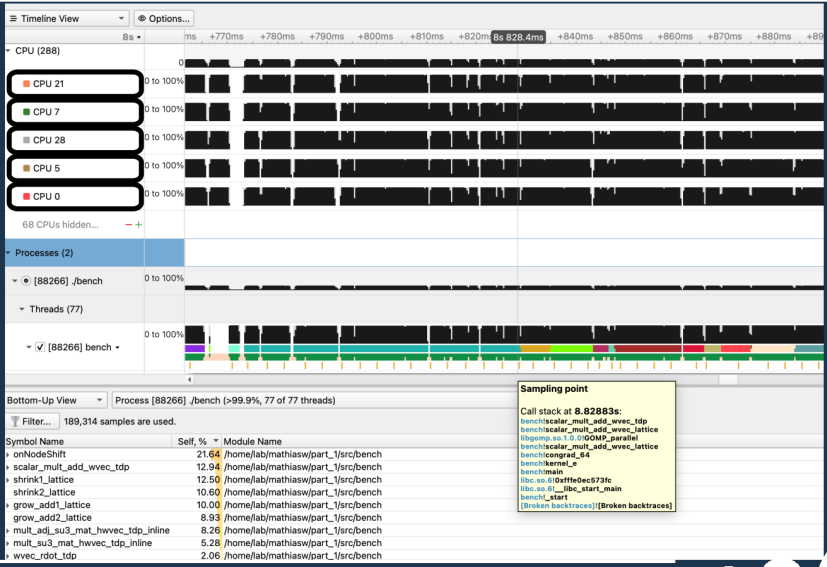
NSight Profiler Update

Laboratoire d'Annecy de Physique des Particules

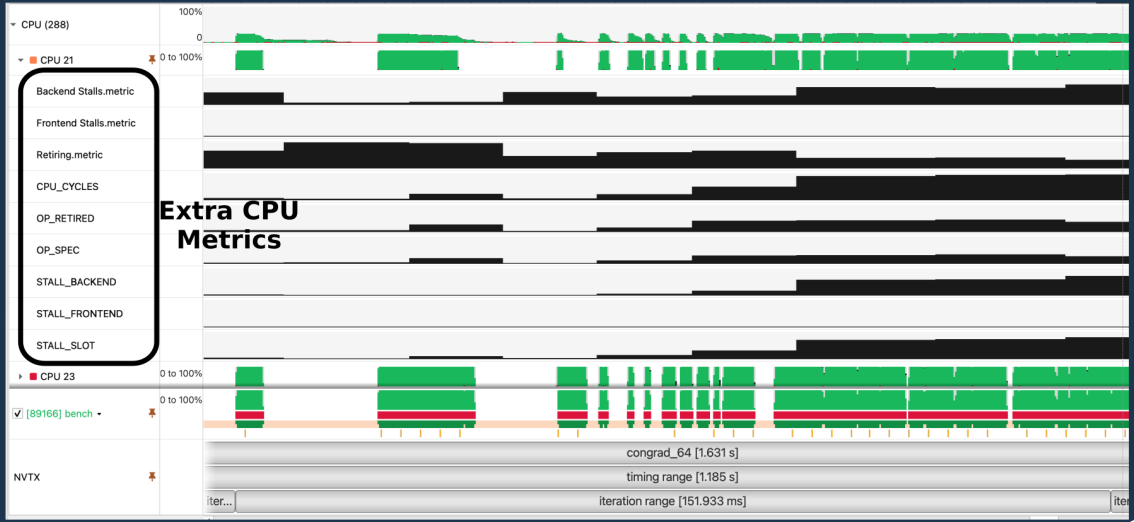
Multi GPU

NSight Profiler Update

Multi CPU



NSight Profiler Update



NSight Profiler Update

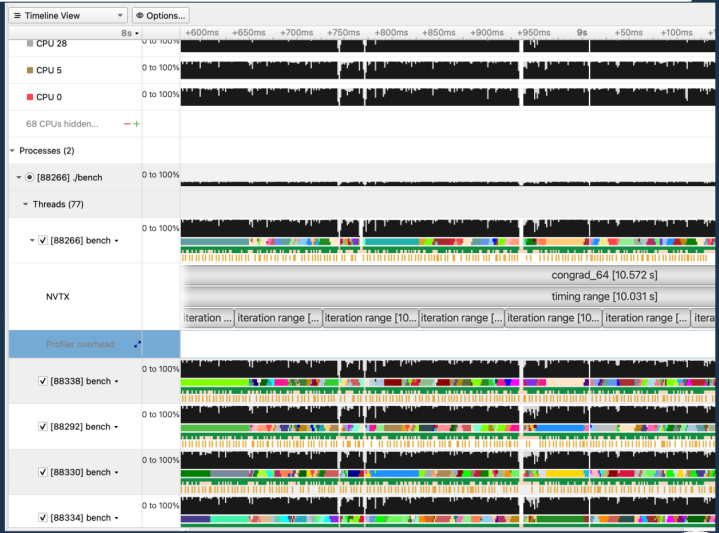
NVTX

Code :
- **Annotation**
- **Provenance**

NSight Profiler Update

NVTX

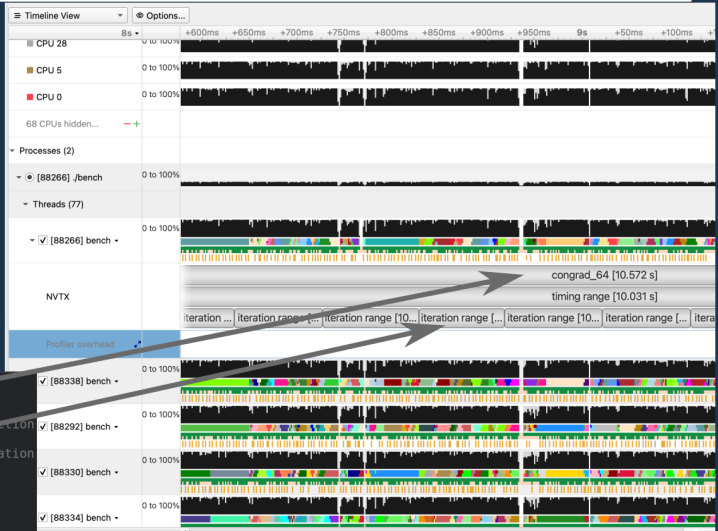
Code :
- **Annotation**
- **Provenance**



NSight Profiler Update

NVTX

Code :
- **Annotation**
- **Provenance**




```cpp
#include <nvtx3/nvToolsExt.h>

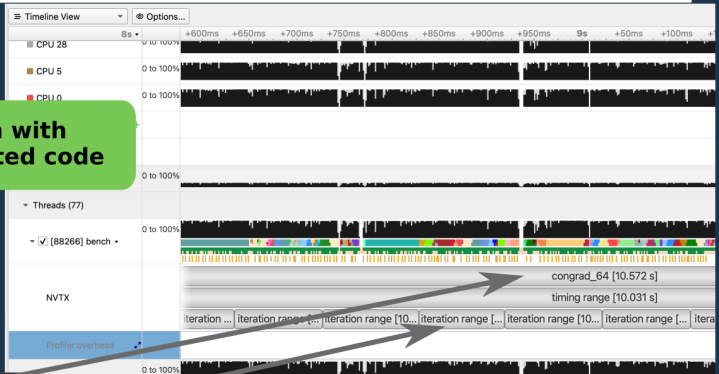
void congrad_64(){
    nvtxRangePush(__func__); // Range around the whole function
    for(int i = 0; i < 6; ++i) {
        nvtxRangePush("loop range"); // Range for iteration
        // Do ab iteration
        nvtxRangePop(); // End the inner range
    }
    nvtxRangePop(); // End the outer range
}
```

NSight Profiler Update

NVTX

Code :
- **Annotation**
- **Provenance**

Even with generated code




```
1  #include <nvtx3/nvToolsExt.h>
2
3  void congrad_64(){
4  »       nvtxRangePush(__func__); // Range around the whole function
5  »       for(int i = 0; i < 6; ++i) {
6  »       »       nvtxRangePush("loop range"); // Range for iteration
7  »       »       // Do ab iteration
8  »       »       nvtxRangePop(); // End the inner range
9  »       }
10 »       nvtxRangePop(); // End the outer range
11 }
```

CUDA Graph

CUDA Graph

Classic
CUDA Kernel Launch

A

B

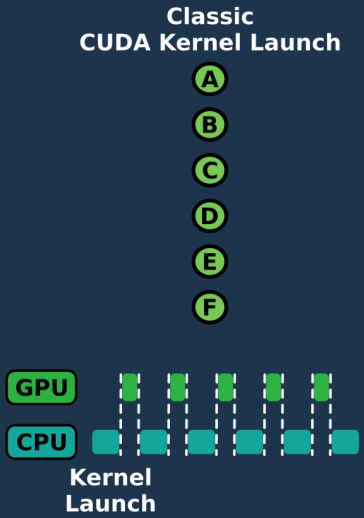
C

D

E

F

CUDA Graph



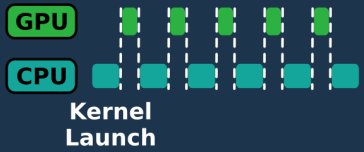
CUDA Graph

Classic
CUDA Kernel Launch

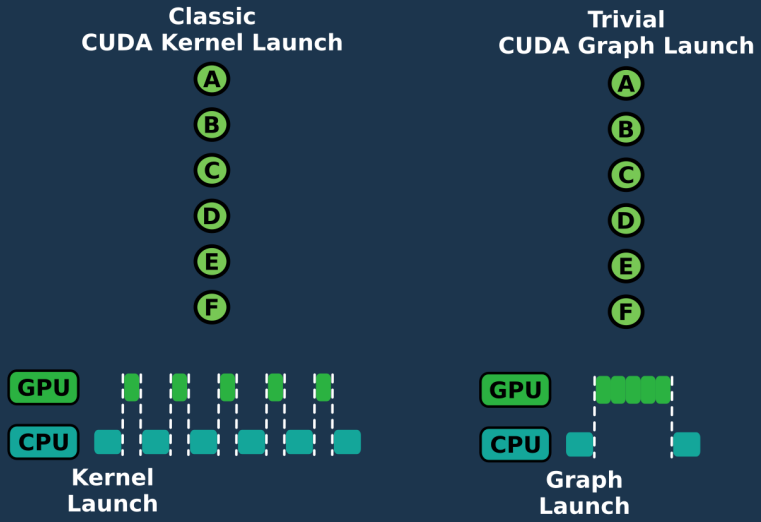
A
B
C
D
E
F

Trivial
CUDA Graph Launch

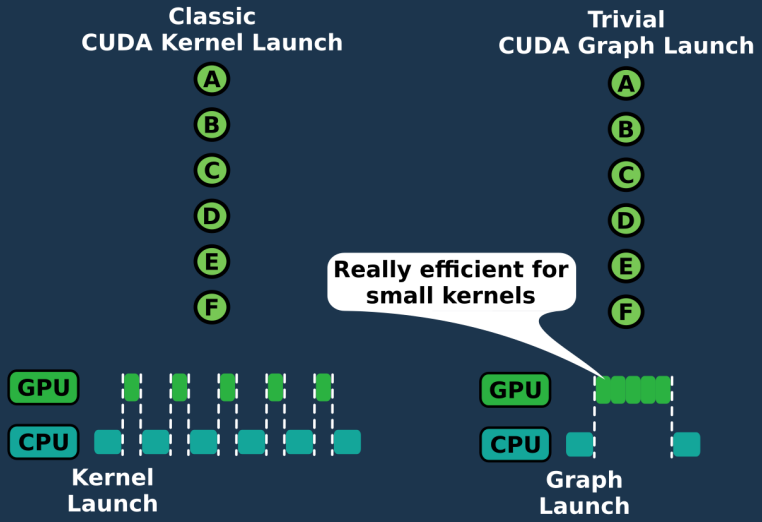
A
B
C
D
E
F



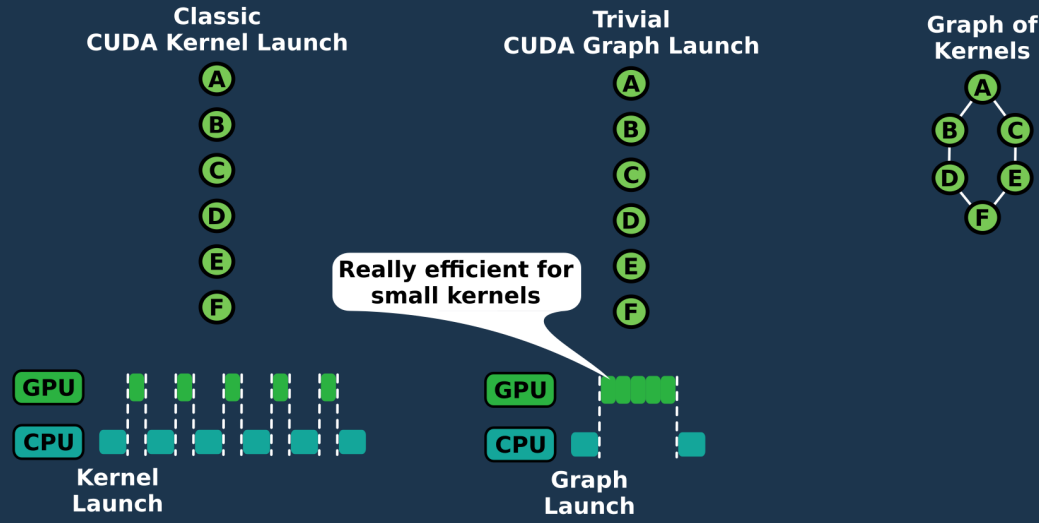
CUDA Graph


Classic
CUDA Kernel Launch
A
B
C
D
E
F
GPU
CPU
Kernel
Launch
Trivial
CUDA Graph Launch
A
B
C
D
E
F
GPU
CPU
Graph
Launch

CUDA Graph


Classic
CUDA Kernel Launch
A
B
C
D
E
F
GPU
CPU
Kernel
Launch
Trivial
CUDA Graph Launch
A
B
C
D
E
F
Really efficient for
small kernels
GPU
CPU
Graph
Launch

CUDA Graph


Classic
CUDA Kernel Launch
A
B
C
D
E
F
Trivial
CUDA Graph Launch
A
B
C
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E
F
Graph of
Kernels
A
B
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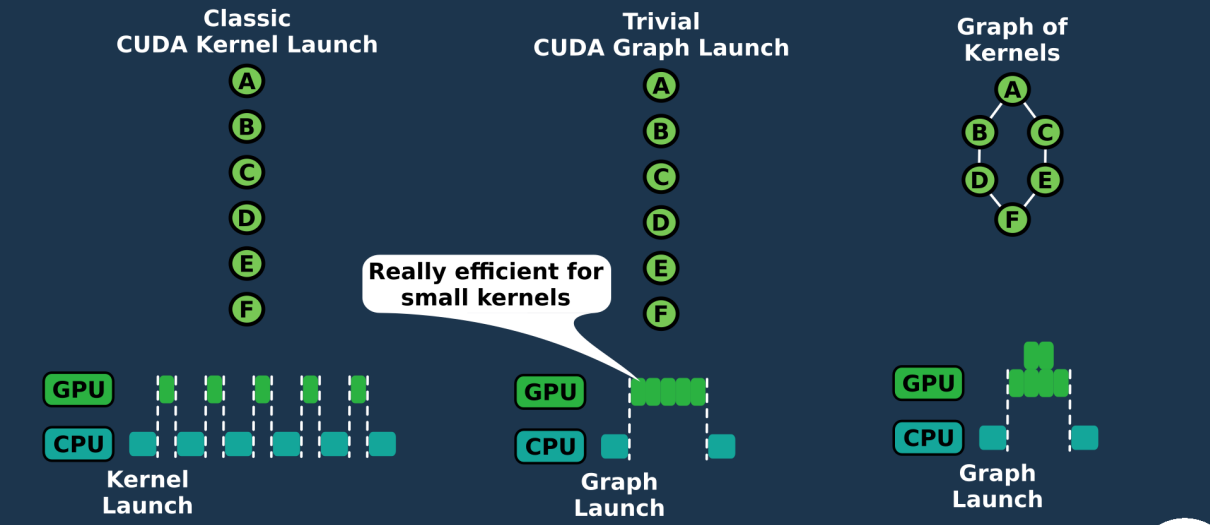
E
F
Really efficient for
small kernels
GPU
CPU
Kernel
Launch
GPU
CPU
Graph
Launch

CUDA Graph


Classic
CUDA Kernel Launch
A
B
C
D
E
F
Trivial
CUDA Graph Launch
A
B
C
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E
F
Graph of
Kernels
A
B
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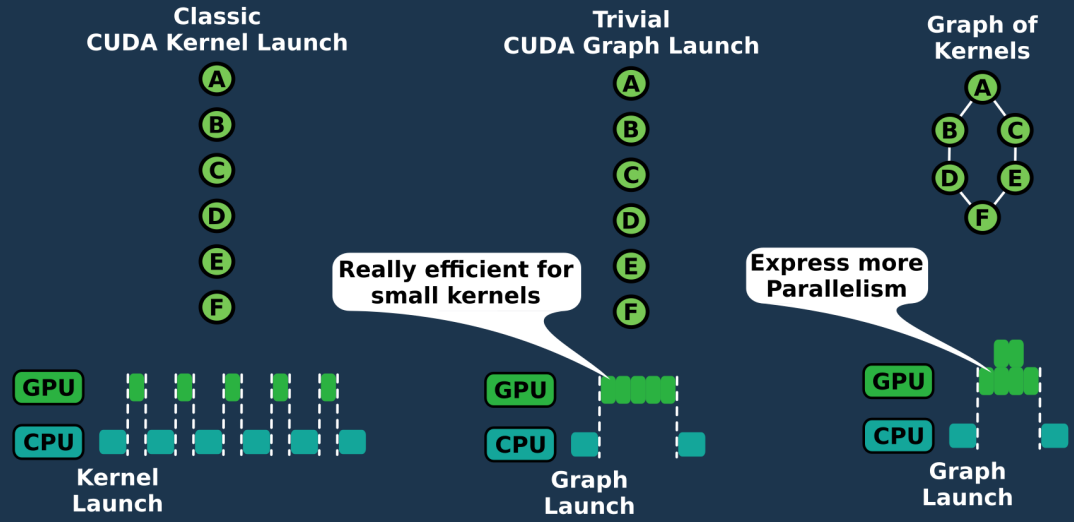
F
Really efficient for
small kernels
GPU
CPU
Kernel
Launch
GPU
CPU
Graph
Launch
GPU
CPU
Graph
Launch

CUDA Graph

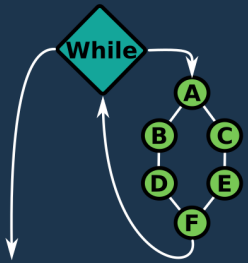

Classic
CUDA Kernel Launch
A
B
C
D
E
F
GPU
CPU
Kernel
Launch
Trivial
CUDA Graph Launch
A
B
C
D
E
F
Really efficient for
small kernels
GPU
CPU
Graph
Launch
Graph of
Kernels
A
B
C
D
E
F
Express more
Parallelism
GPU
CPU
Graph
Launch

CUDA Graph Update

Problem appears again on iterative algorithms

CUDA Graph Update

With Iterative Execution

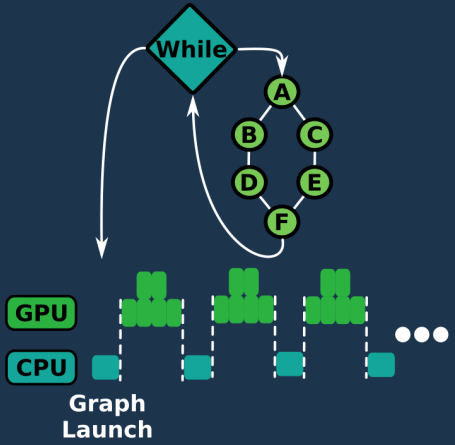


Problem appears again on iterative algorithms

CUDA Graph Update

With Iterative Execution

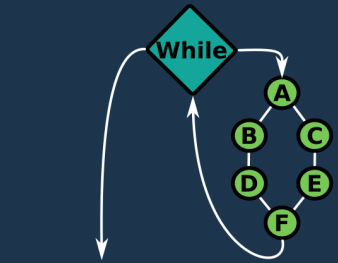
Problem appears again on iterative algorithms

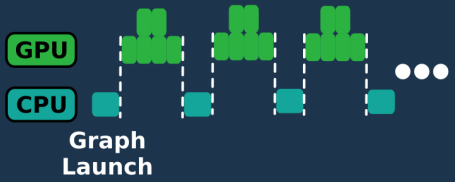


CUDA Graph Update

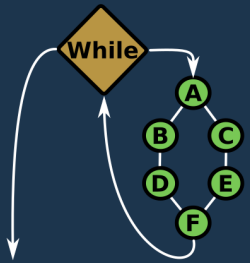
Problem appears again on iterative algorithms

With Iterative Execution

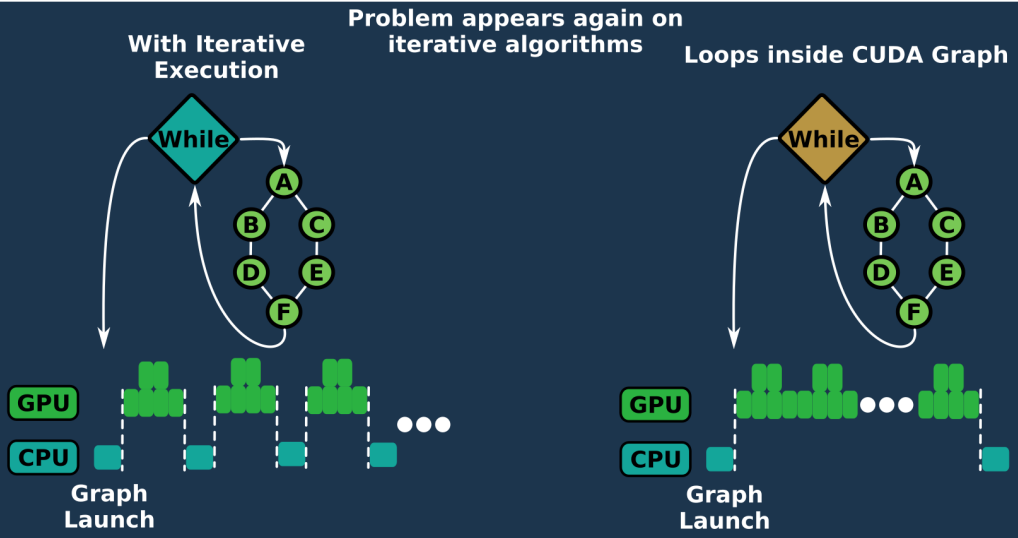




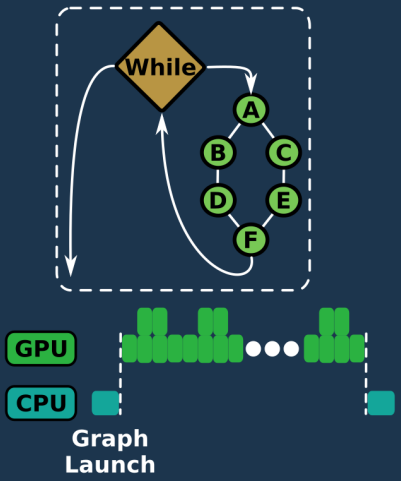
Loops inside CUDA Graph



CUDA Graph Update

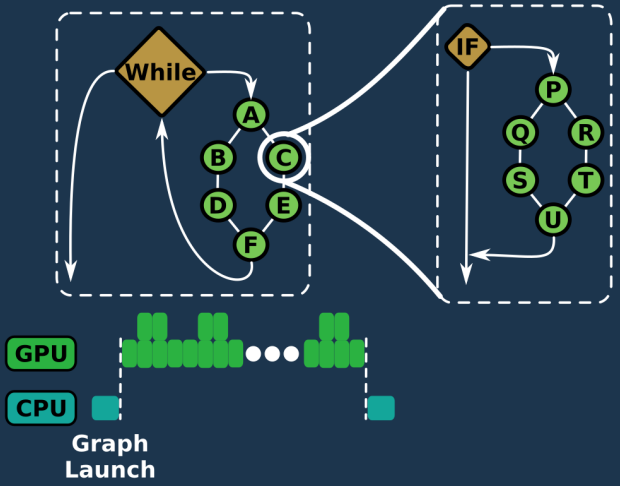


CUDA Graph Update



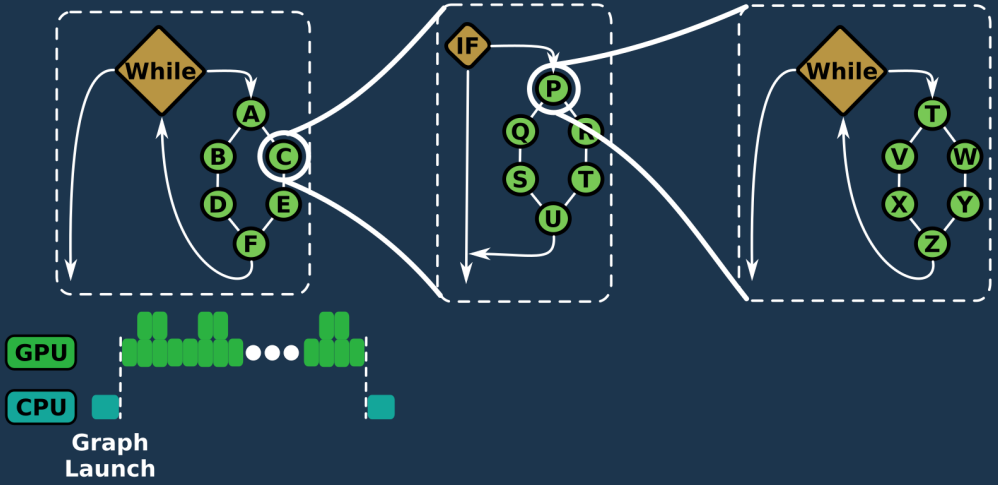
CUDA Graph Update

Sub Graphs, Loops and Conditions



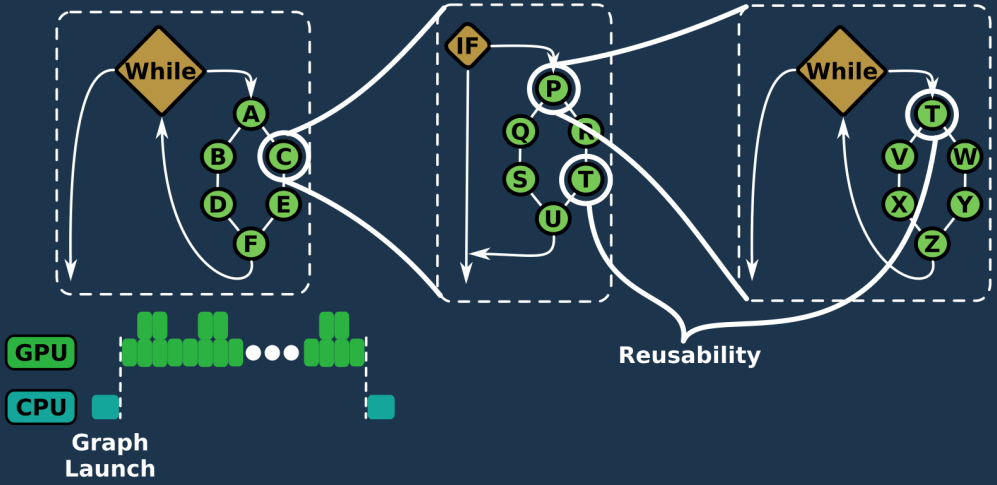
CUDA Graph Update

Sub Graphs, Loops and Conditions



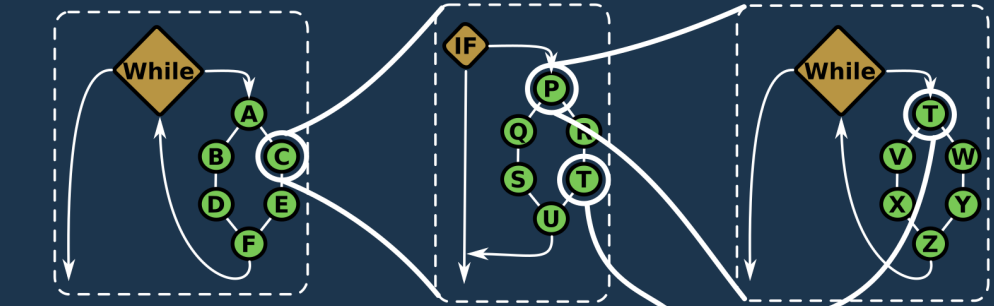
CUDA Graph Update

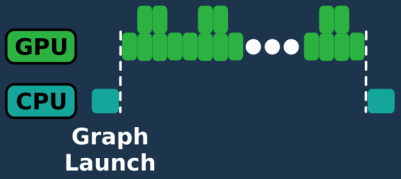
Sub Graphs, Loops and Conditions



CUDA Graph Update

Sub Graphs, Loops and Conditions



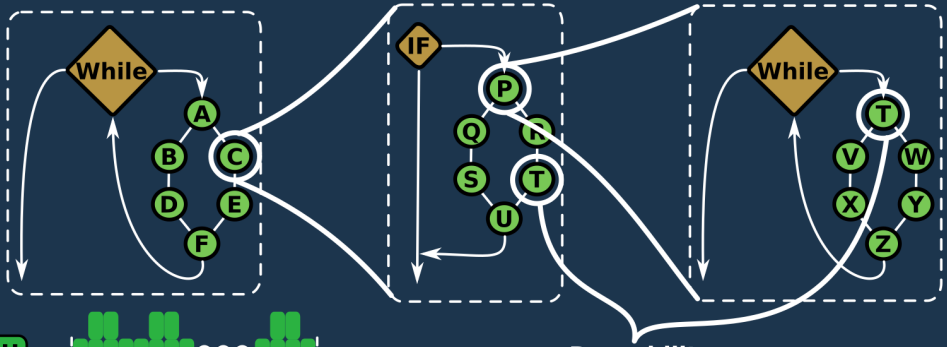


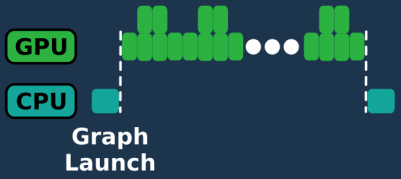
Reusability

cuFFT, NCCL, NVShmem, ...
can be used with CUDA Graphs

CUDA Graph Update

Sub Graphs, Loops and Conditions





Reusability

cuFFT, NCCL, NVShmem, ...
can be used with CUDA Graphs

Available in **CUDA 12.4**

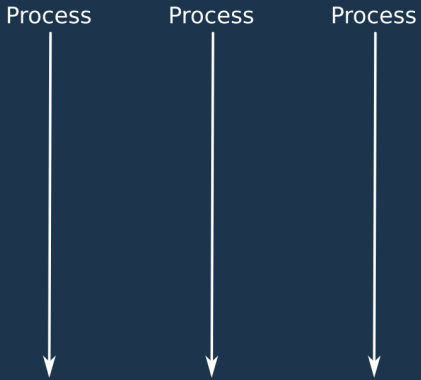
DPU and MVAPICH 2

DPU and MVAPICH 2

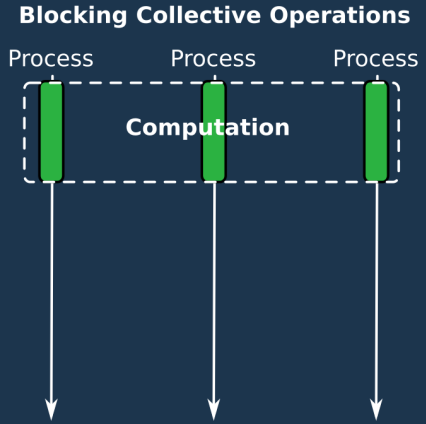
Blocking Collective Operations

DPU and MVAPICH 2

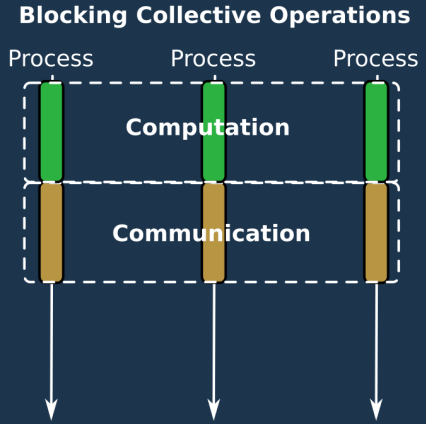
Blocking Collective Operations



DPU and MVAPICH 2

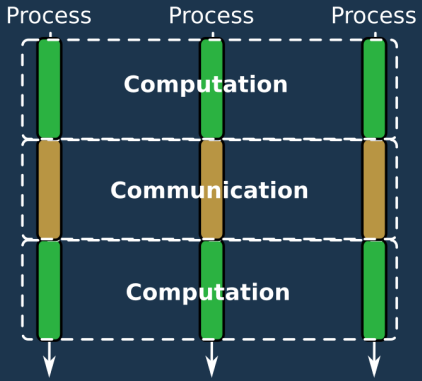


DPU and MVAPICH 2

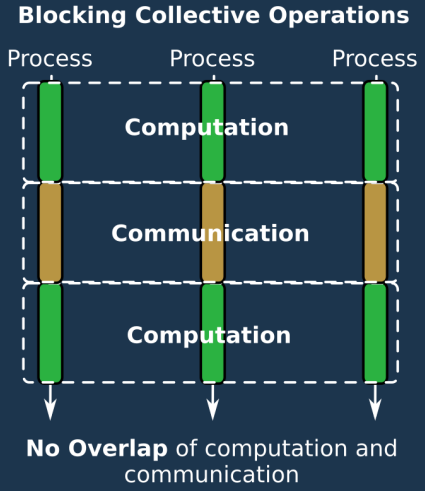


DPU and MVAPICH 2

Blocking Collective Operations

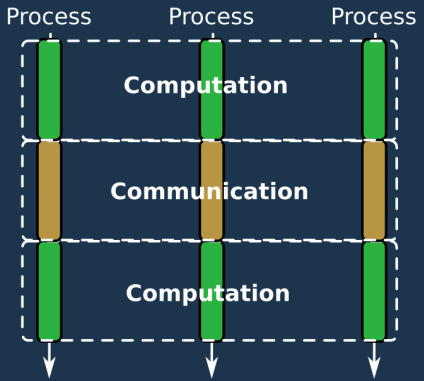


DPU and MVAPICH 2



DPU and MVAPICH 2

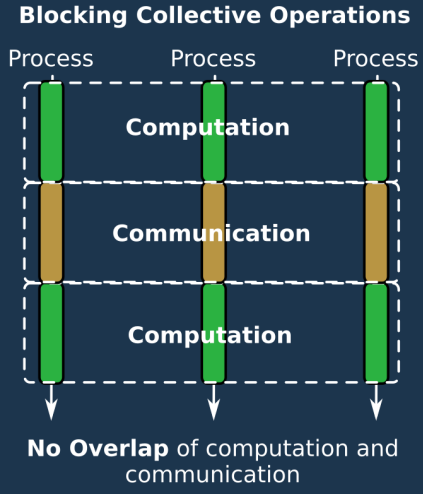
Blocking Collective Operations

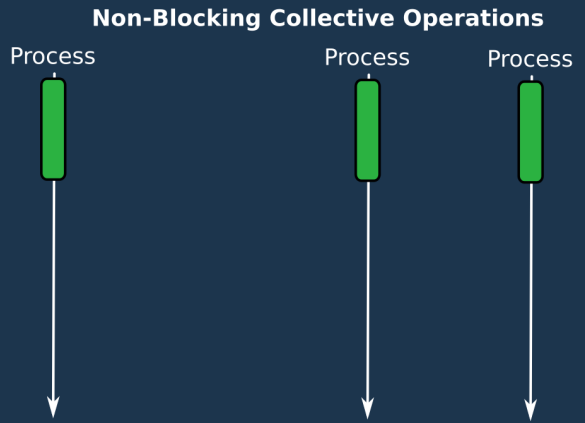


No Overlap of computation and communication

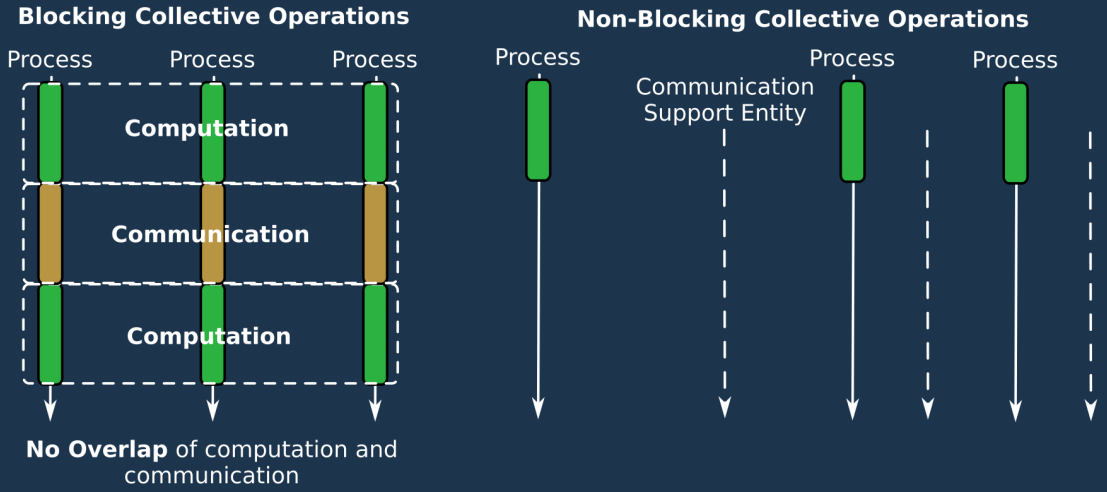
Non-Blocking Collective Operations

DPU and MVAPICH 2

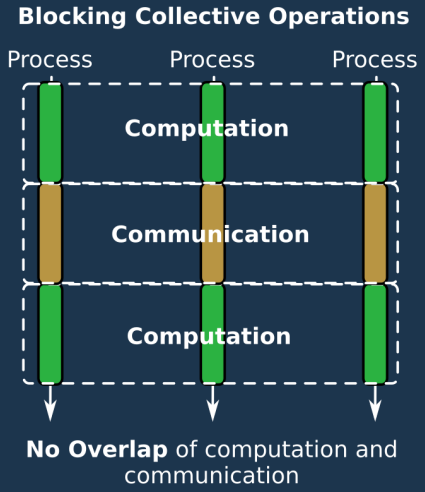


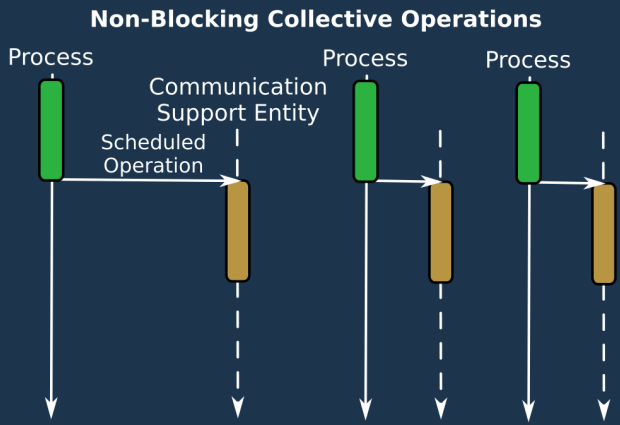


DPU and MVAPICH 2

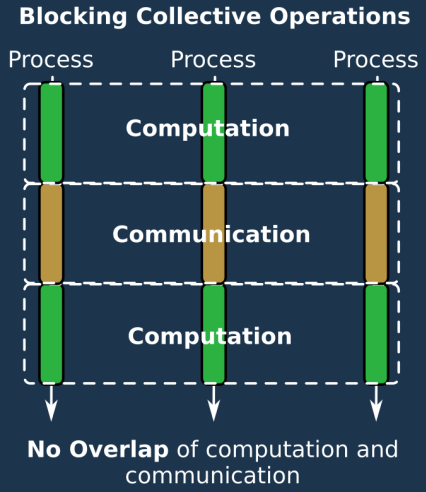


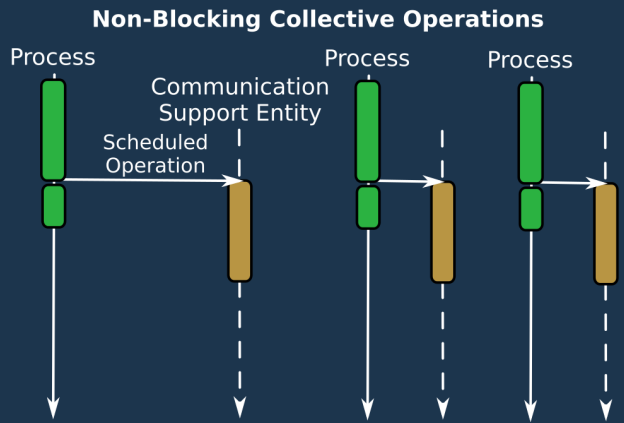
DPU and MVAPICH 2



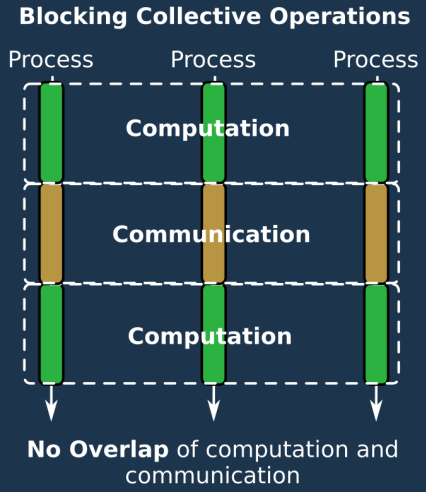


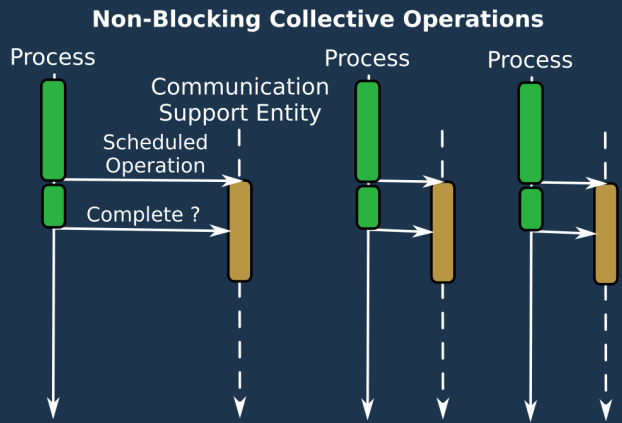
DPU and MVAPICH 2



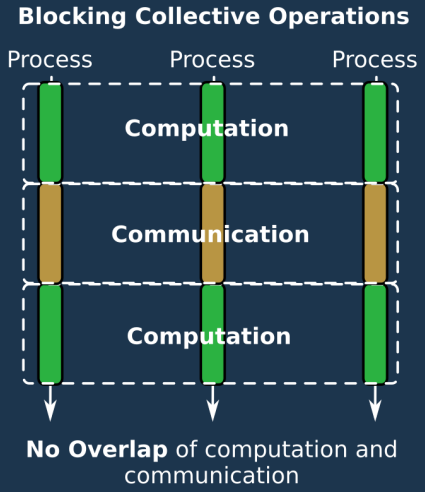


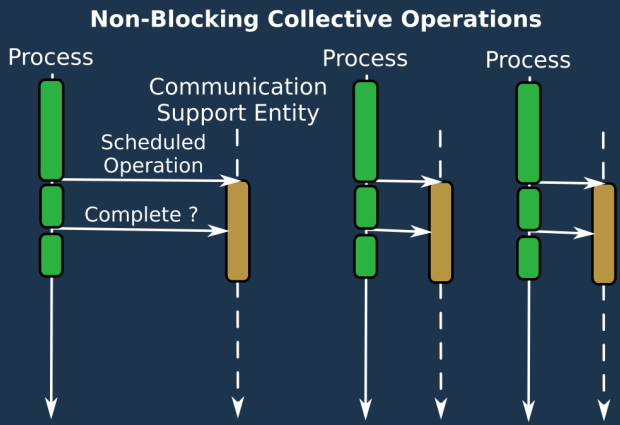
DPU and MVAPICH 2





DPU and MVAPICH 2





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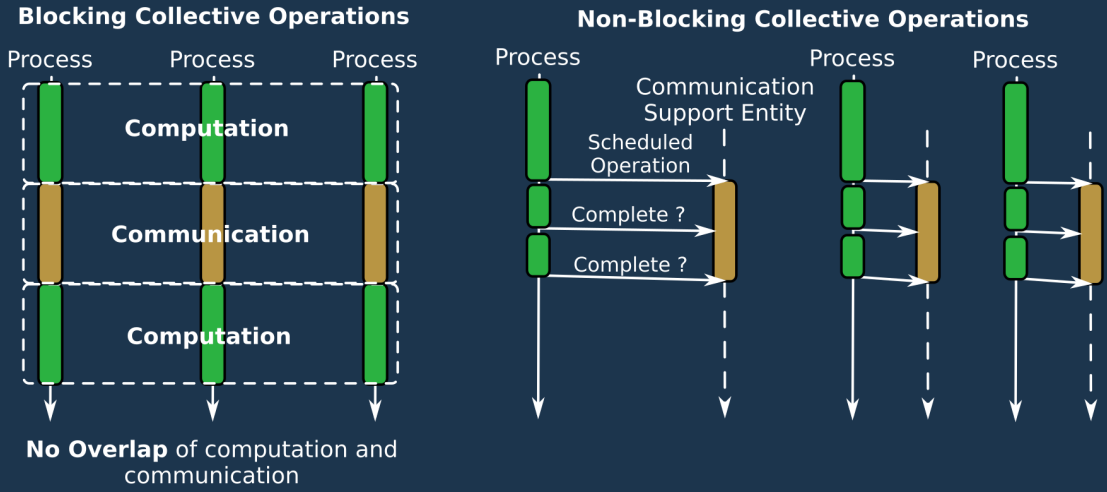

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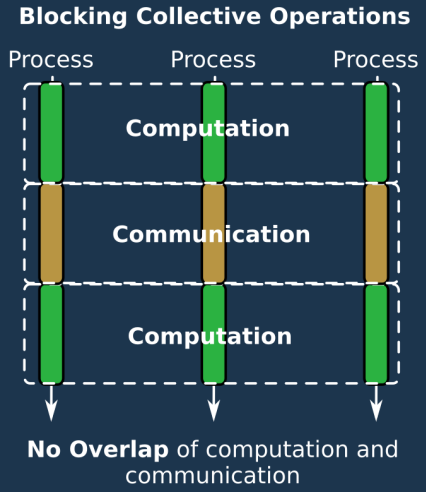

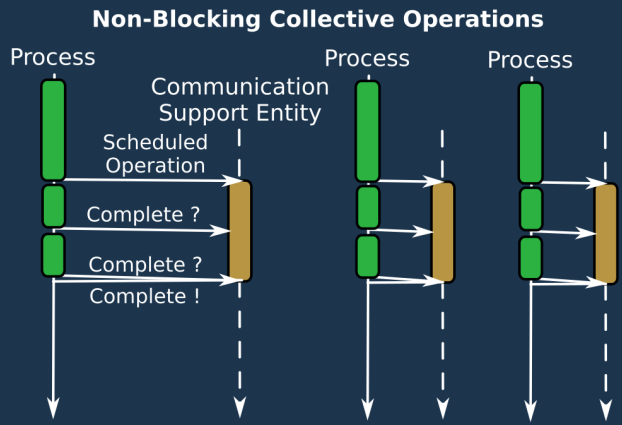

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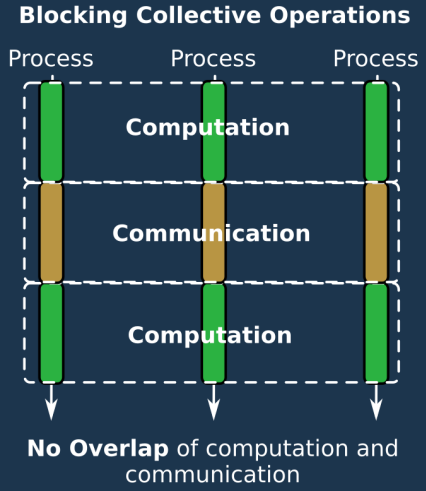

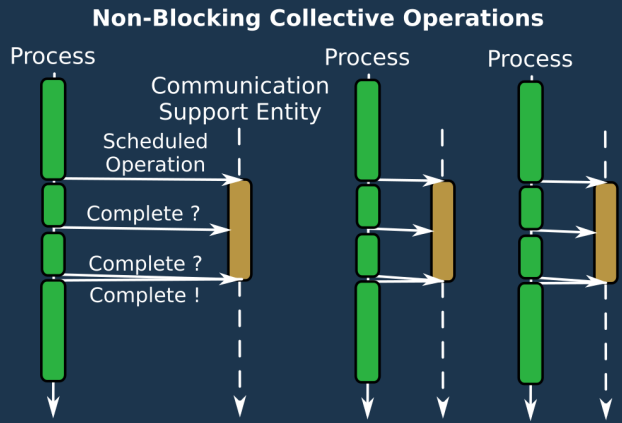

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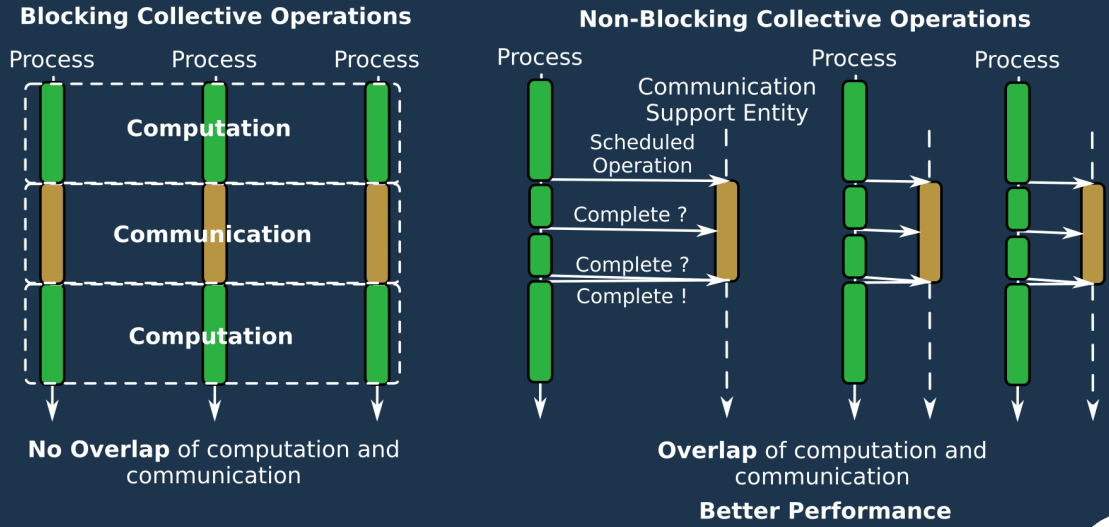

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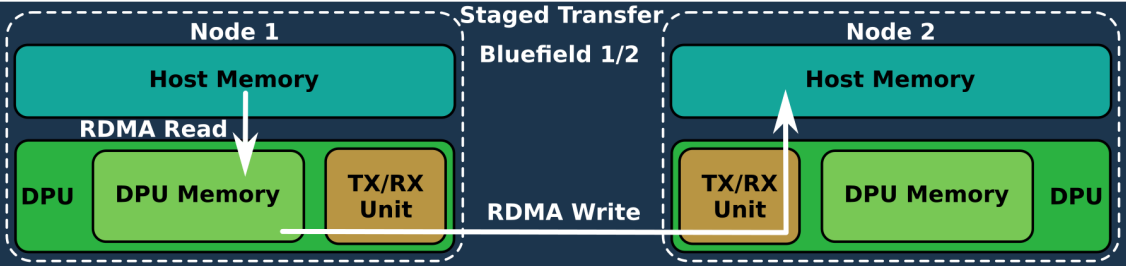

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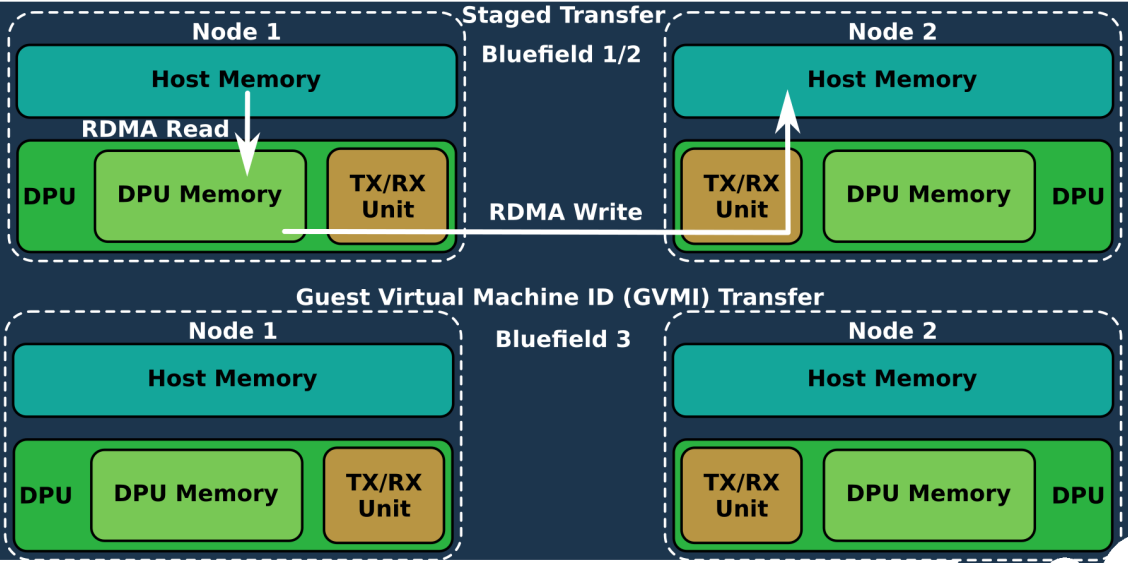

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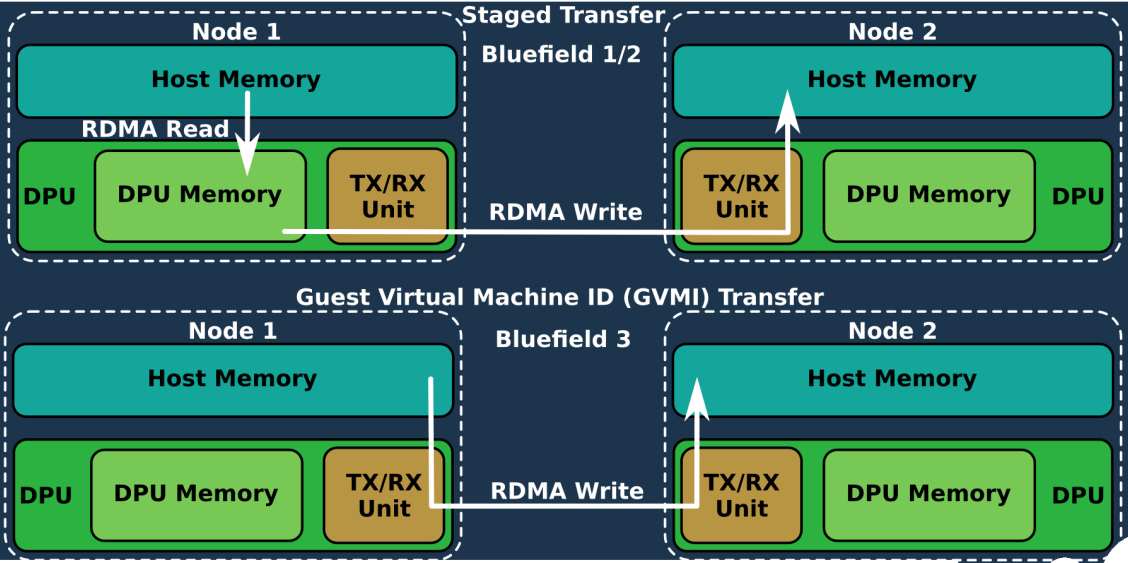

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Exploiting **DPUs** for **Deep Neural Network Training** (**Data Augmentation**, **Testing Processes**)

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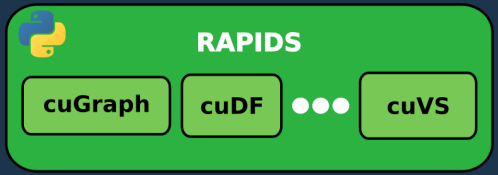

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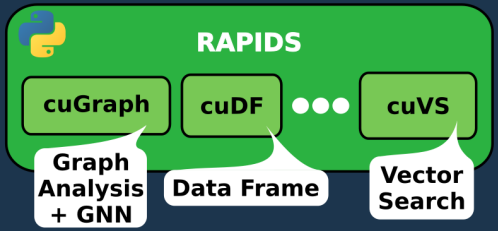

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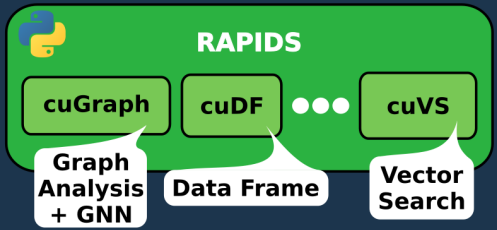

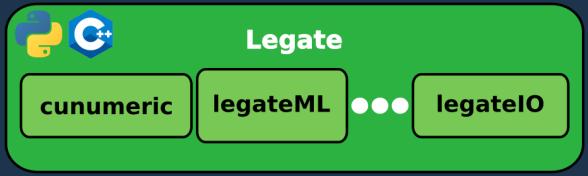

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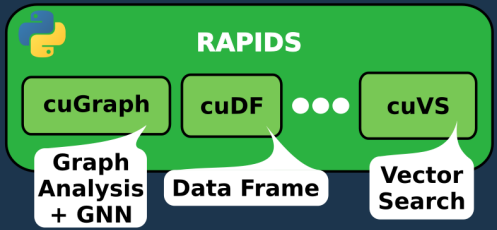

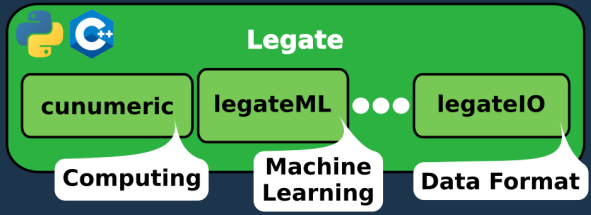

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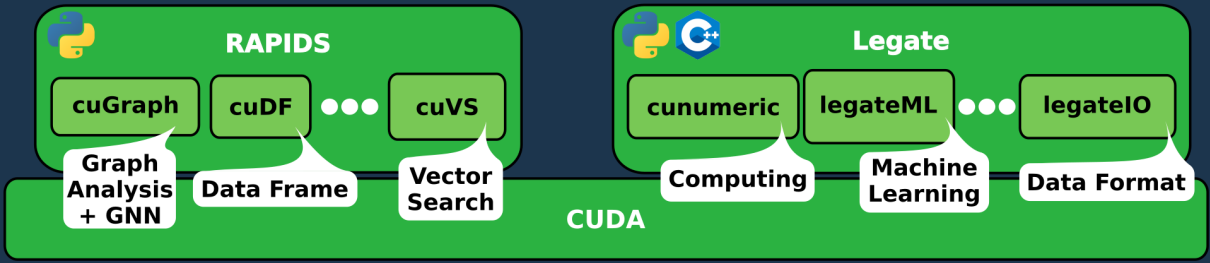

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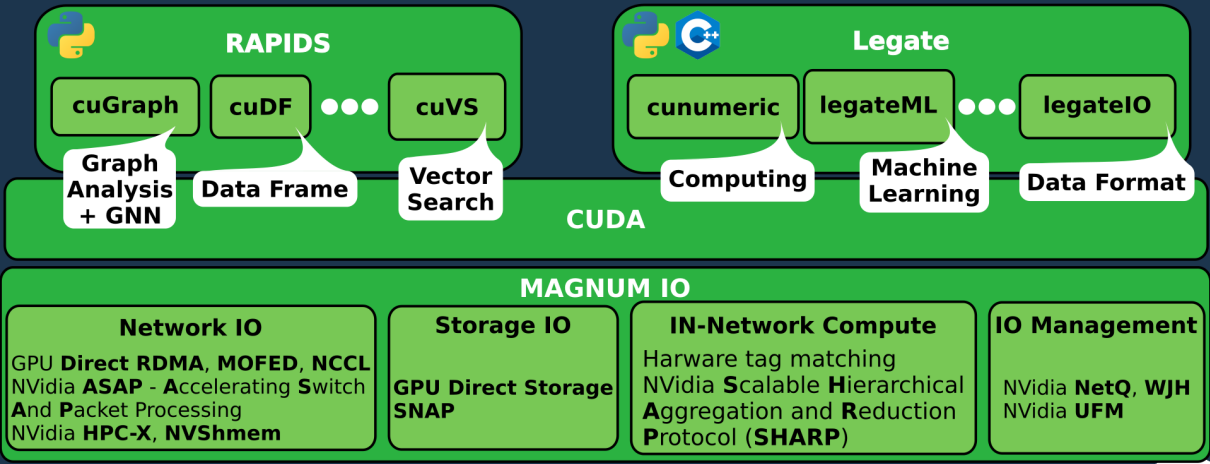

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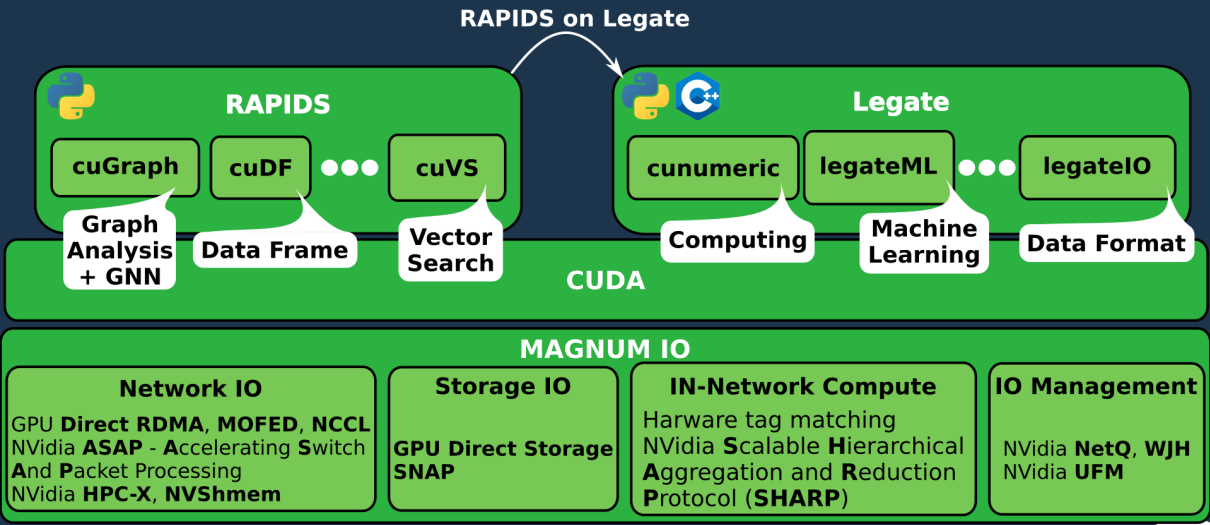

cuDF : Cuda Data Frame

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pandas

Core functionnalities but on GPU

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cuDF passes **94%** of **Pandas unit tests** (some edge cases have to be solved)

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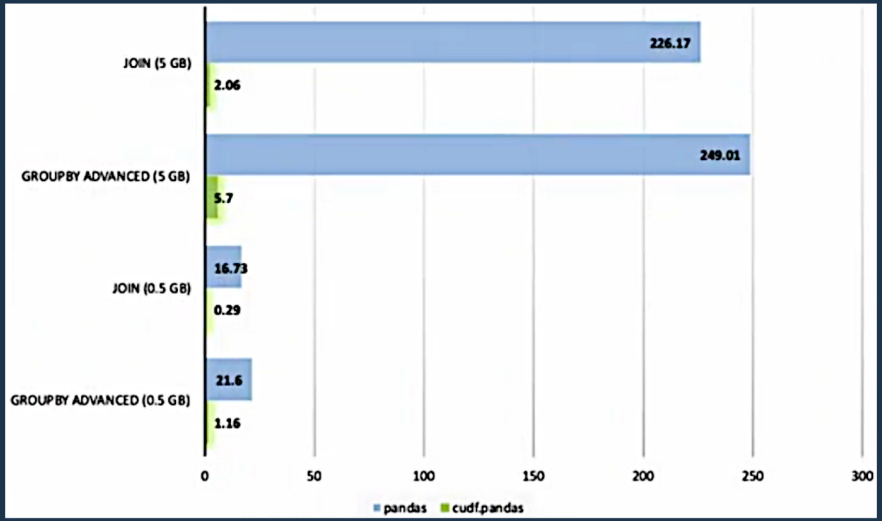

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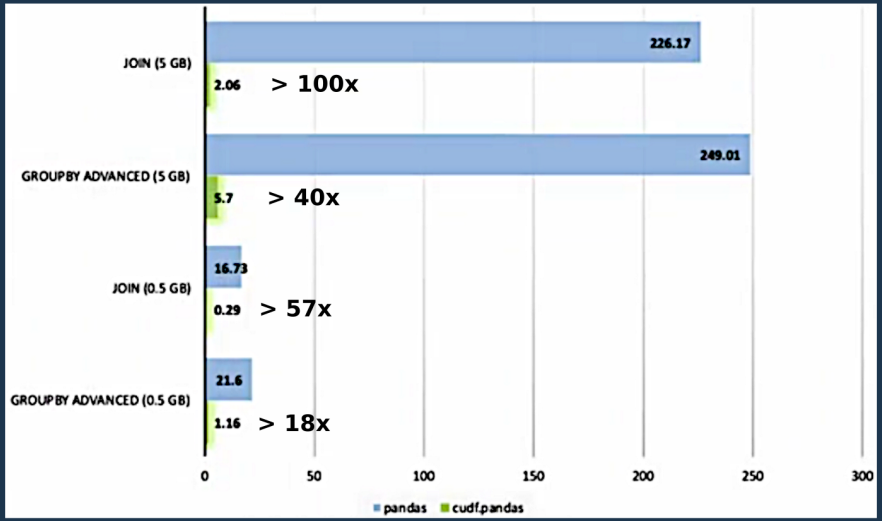

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For multiple GPU : dask.cudf

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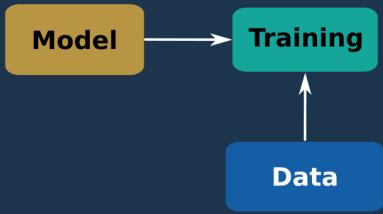

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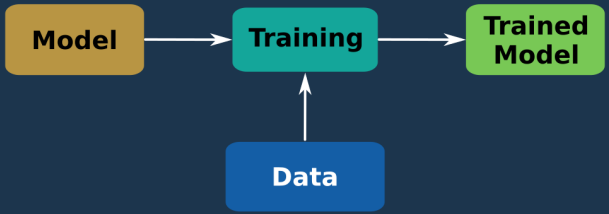

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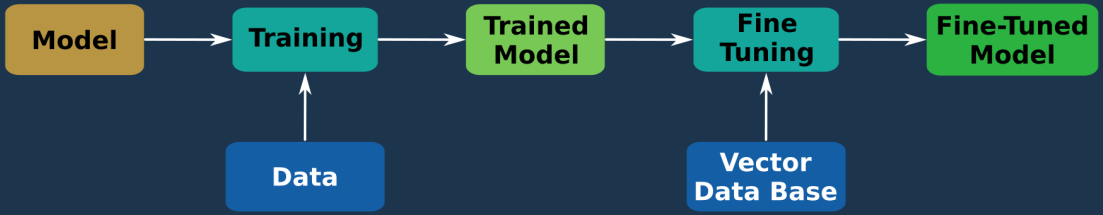

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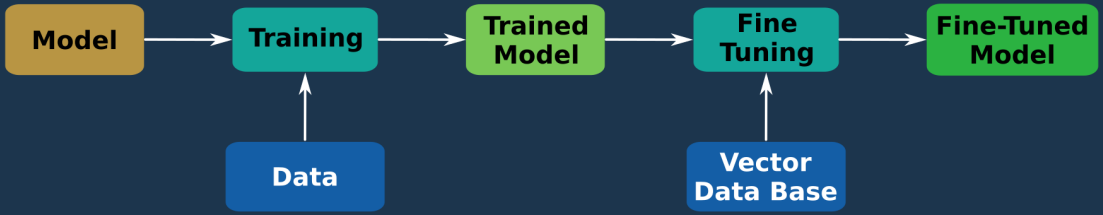
Retrieval-Augmented Generation (RAG)
- **Avoid hallucination**
- **Improve accuracy**



GPU Accelerated

cuGraph : Graph at network scale

Graphs are everywhere : **Images**, **Text**, **Molecules**,
Networks (**Computer**, **Social**, **Citation**), **Product Catalogs**, etc

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Graphs exploit meaning of sparsity

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Need **Larger Graphs** (**Network Scale**) :
- **100 TB** Graph
- **1 Trillion** Edges
- Feature Size **~1 k** vector lengths

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Graphs exploit meaning of sparsity → **Sparse Matrix** → **Tensor Cores**

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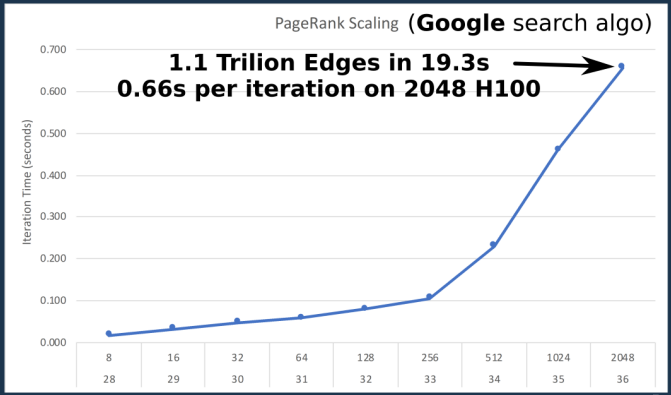

cuGraph : Libraries

Fast GPU Graph Accelerated Algorithms

Class	Algorithms	MNMG
Centrality	Katz	Yes
	Betweenness Centrality	Yes
	Edge Betweenness Centrality	Yes
	Eigenvector Centrality	Yes
	Degree Centrality (Python only)	Yes
Community	Leiden	Yes
	Louvain	Yes
	Ensemble Clustering for Graphs	Python in 24.04
	Spectral-Clustering - Balanced Cut	
	Spectral-Clustering - Modularity	
	Subgraph Extraction	Yes
	Triangle Counting	Yes
	K-Truss	
Components	Weakly Connected Components	Yes
	Strongly Connected Components	
Core	K-Core	Yes
	Core Number	Yes
Layout	Force Atlas 2	not planned
Link Analysis	PageRank	Yes
	Personal PageRank	Yes
	HITS	Yes
Link Prediction / Similarity	Jaccard Similarity	Yes
	Weighted Jaccard Similarity	Yes
	Overlap Similarity	Yes
	Sorensen	Yes
Traversal	Breadth First Search (BFS)	Yes
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- **PyG (cugraph-pyg)**

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C
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Service
- **cuGraph as Service** (coming soon)

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NetworkX

Graphs are everywhere (again)

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Open Source project about Graphs :
- **Connectivity**
- **Shortest path**
- **Route planning**
- ...

NetworkX

Graphs are everywhere (again)

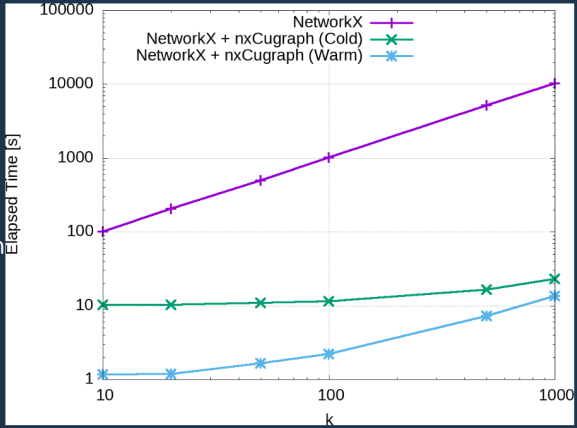
Open Source project about Graphs :
- **Connectivity**
- **Shortest path**
- **Route planning**
- ...

No need to **change** script

NETWORK_BACKEND_PRIORITY=**cugraph python** bc_demo.py

NetworkX

- **Dataset** : U.S. patent dataset, National Bureau of Economic Research (https://snap.stanford.edu/data.cit-Patents.html)
- **Directed Graph** : **3.7 M Nodes**, **16.5 M Edges**
- **CPU** : Intel Xeon Gold 6128 CPU @ 3.40 GHz, 45 GB
- **GPU** : NVidia Quadro RTX 8000, 48 GB



NETWORKX_BACKEND_PRIORITY="cugraph" python

```
>>> import networkx as nx
>>> G = nx.DiGraph()
...
>>> nx.betweenness_centrality(G, k=k)
```

https://github.com/rapidsai/cugraph/blob/branch-24.04/benchmarks/nx-cugraph/pytest-based/bench_algos.py

RMM : Rapids Memory Management

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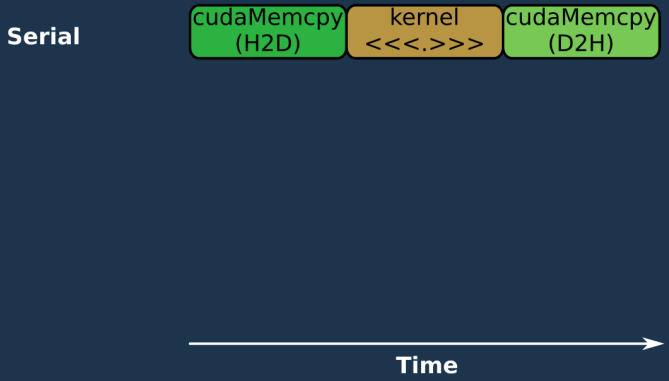

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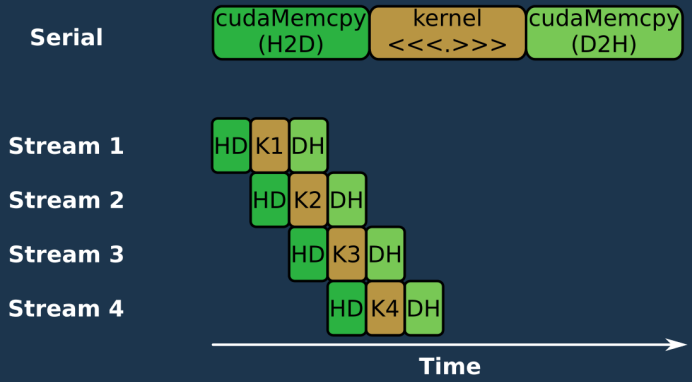

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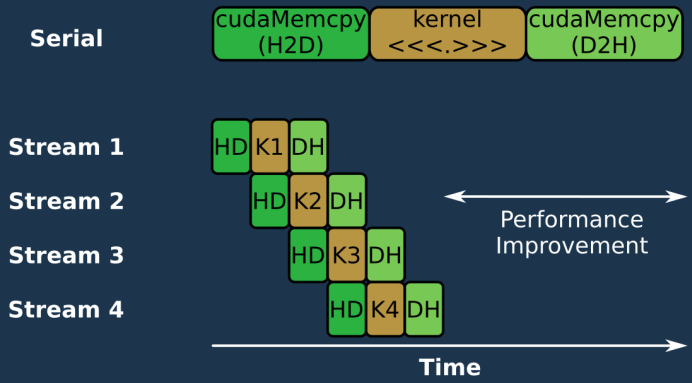

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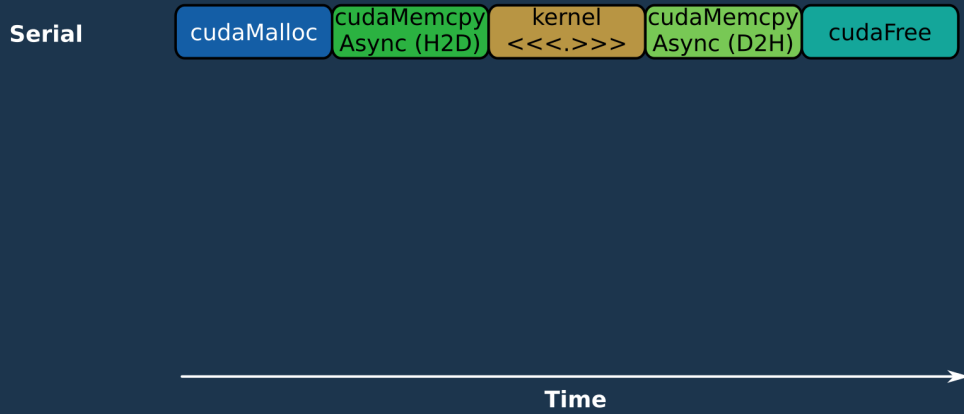

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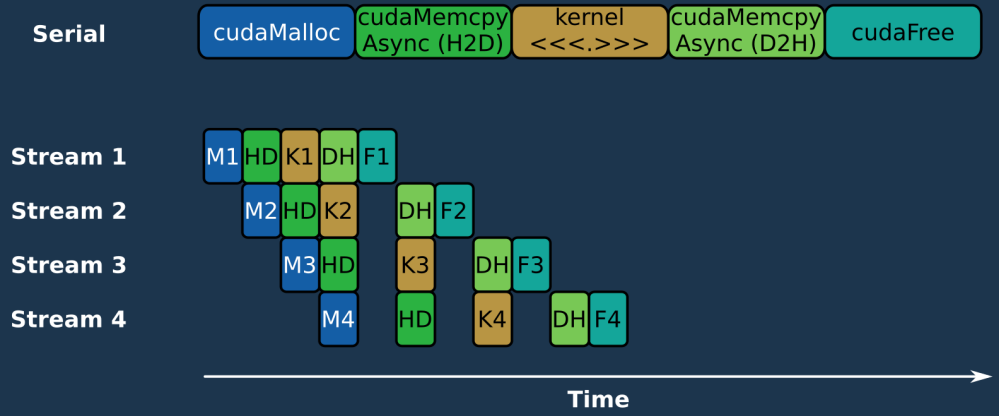

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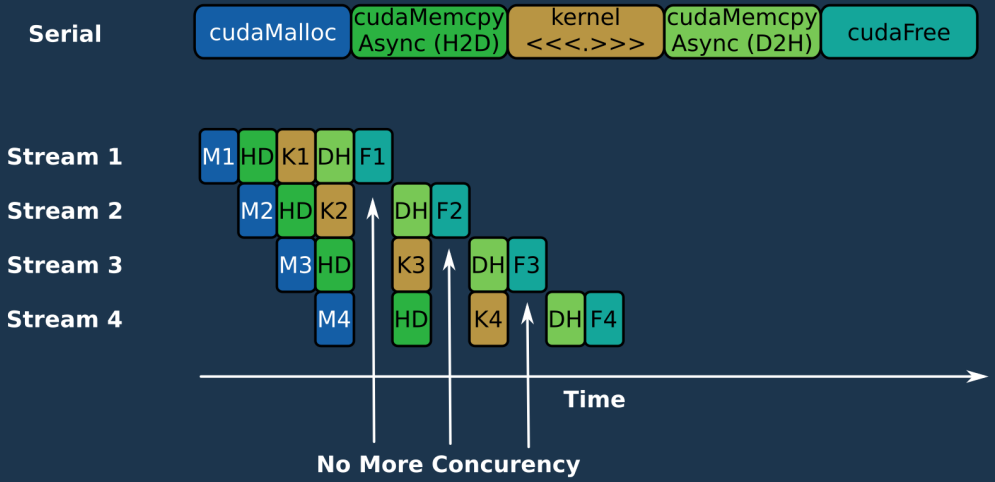

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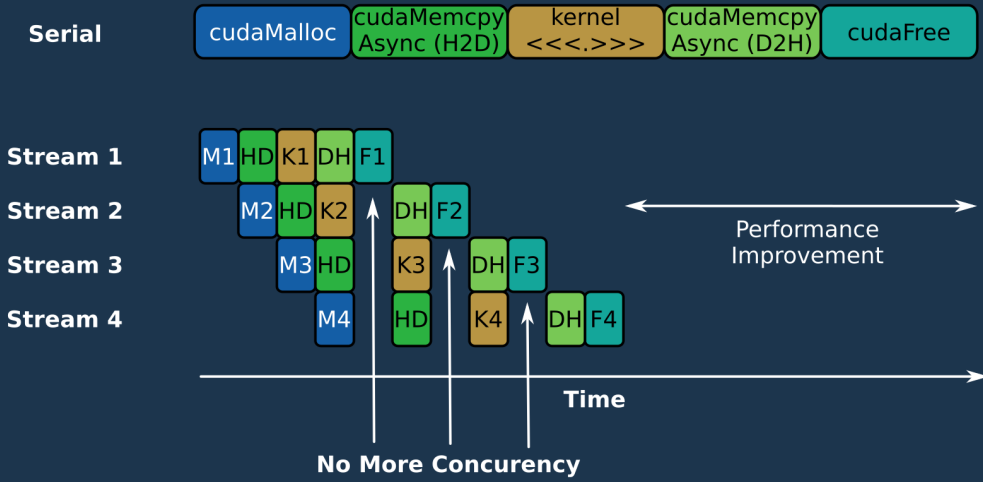

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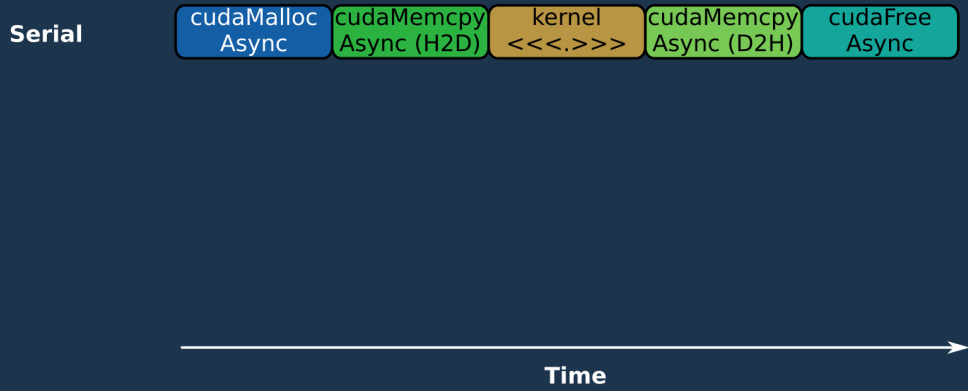

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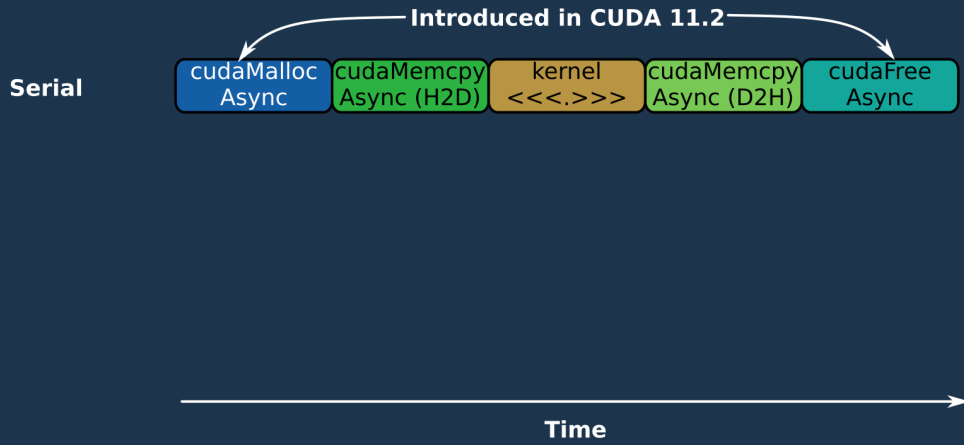

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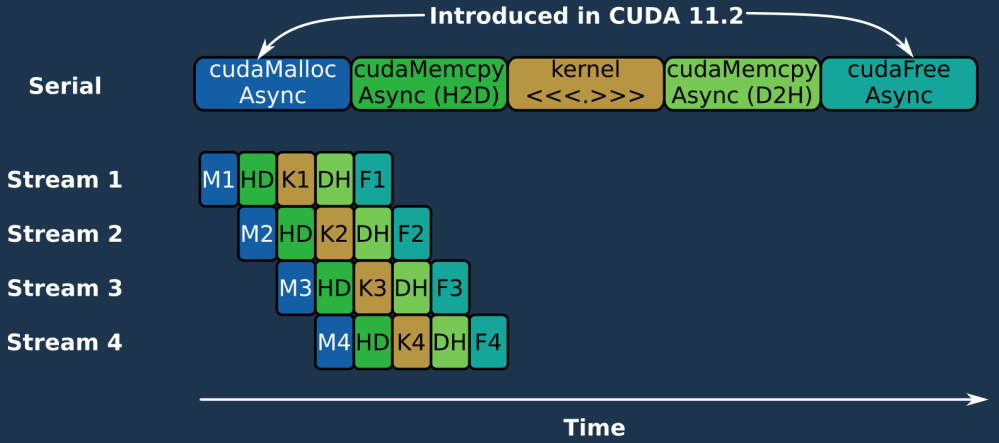

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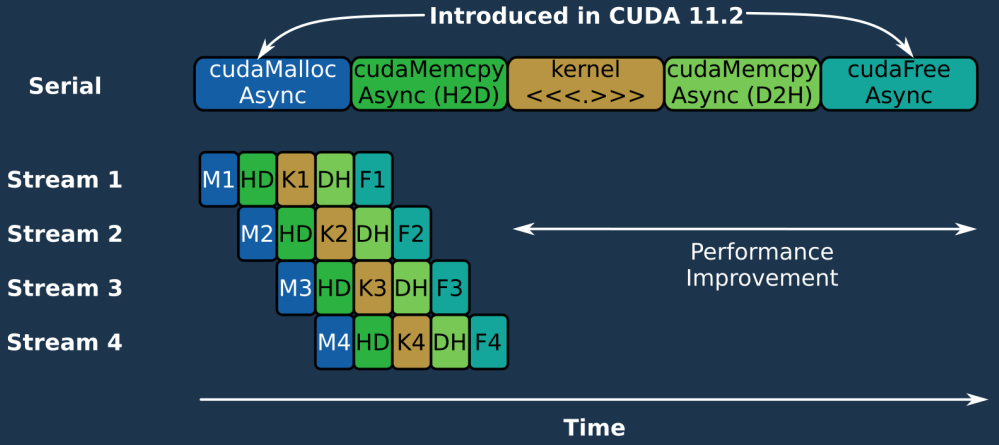

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Running
App A

GPU

Memory

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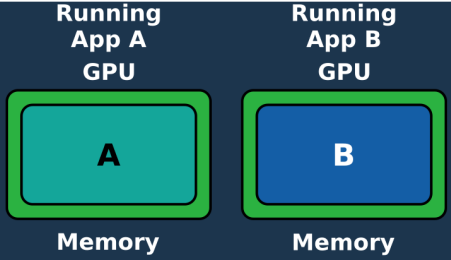

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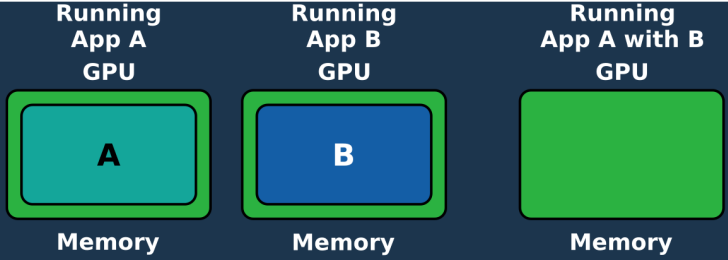

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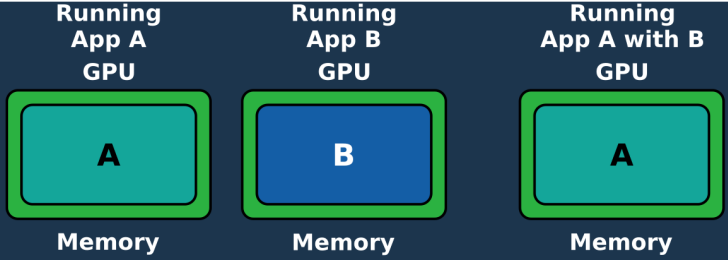

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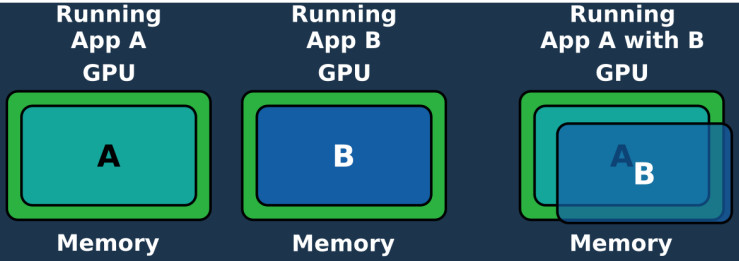

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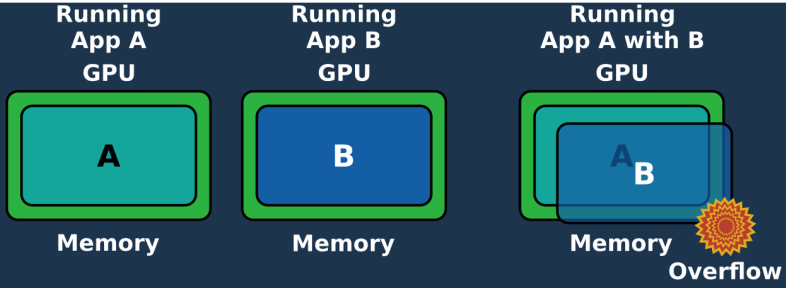

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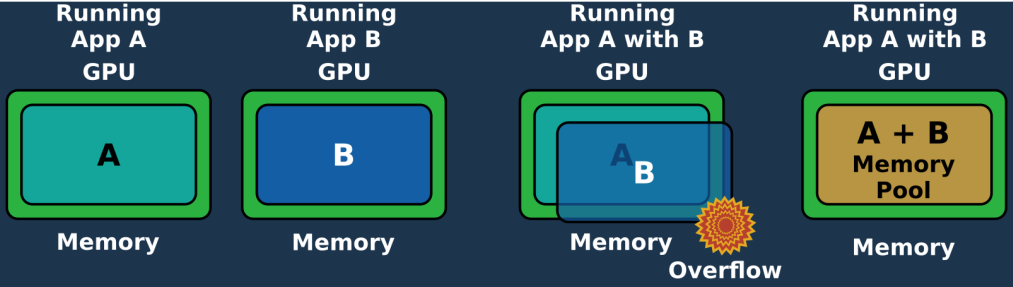

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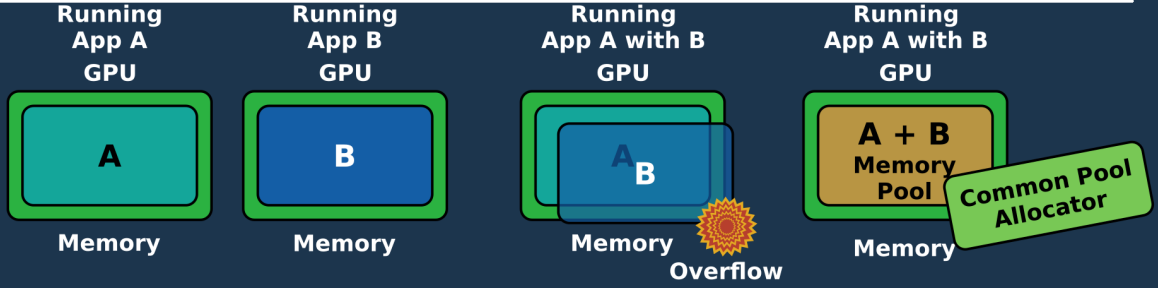

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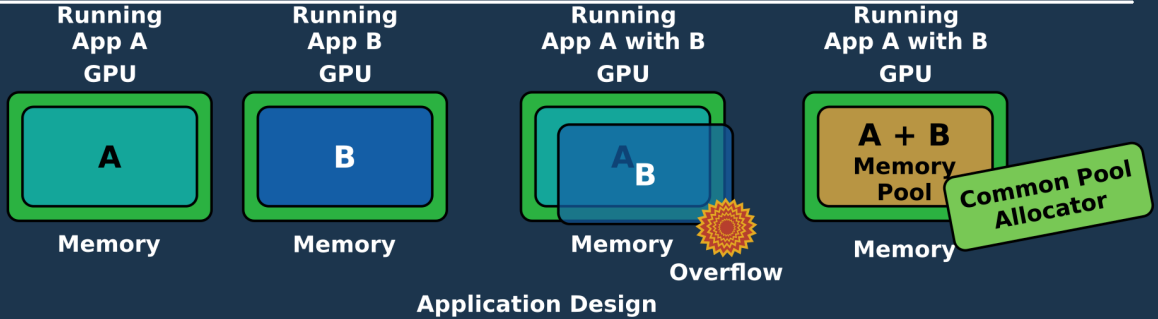

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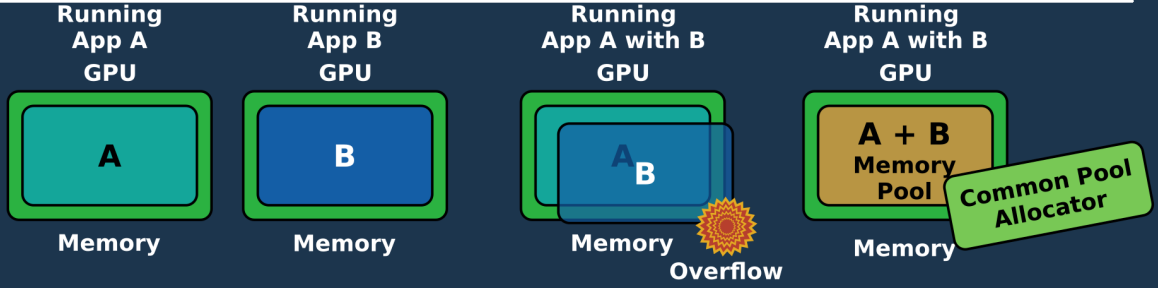

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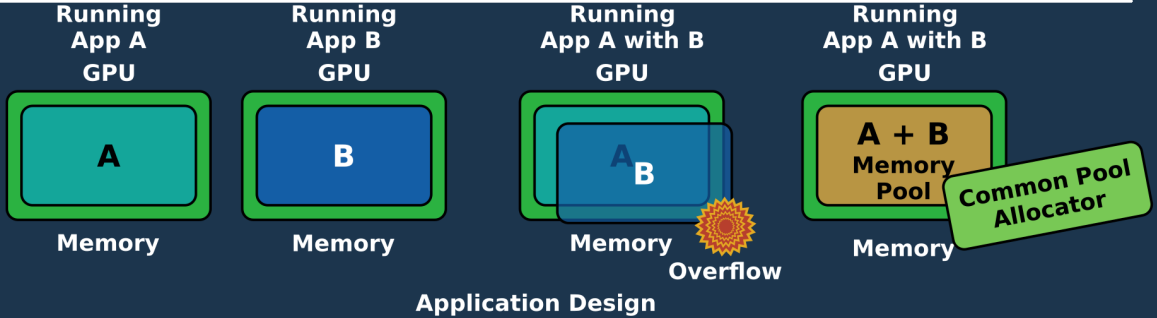

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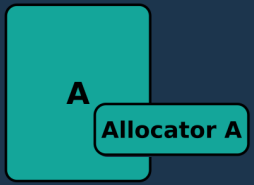

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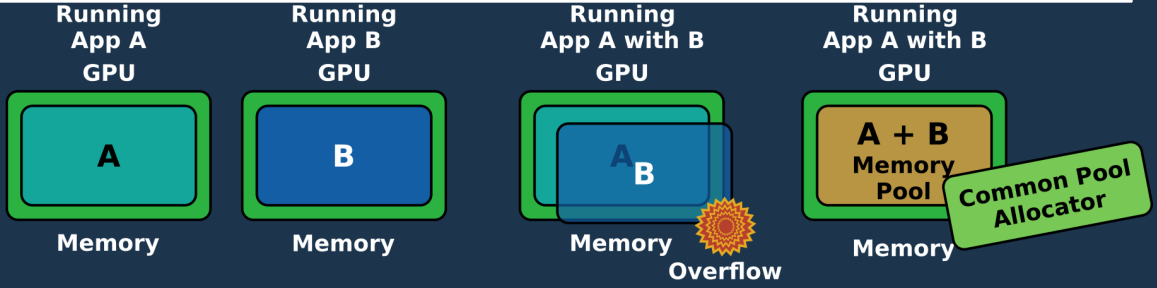

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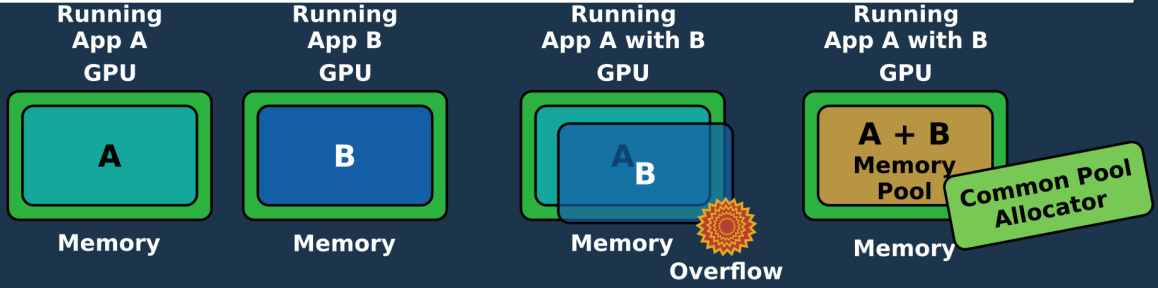

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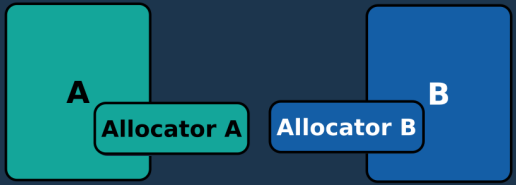

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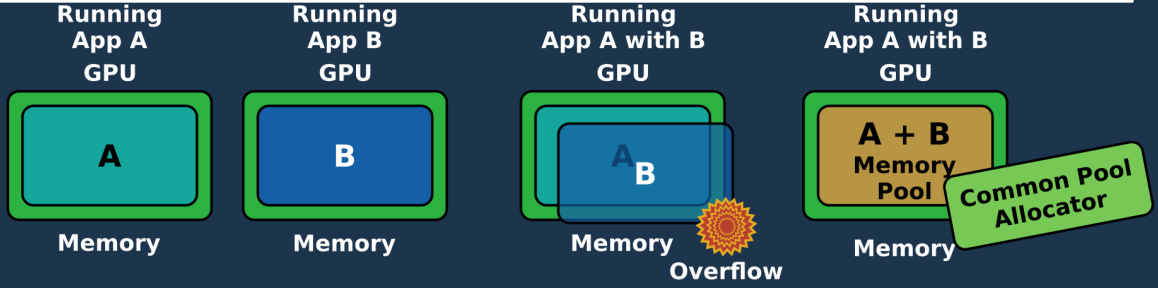

Application Design

RMM : Rapids Memory Management

Fast and Flexible Memory Management

Customize Allocation :
- **Pool**, **Cached**, **Fixed Size**
- **Logging**, **Reporting**, **Statistics**, **Debugging**
- **Tracking**, **Leak Detection**
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https://github.com/rapidsai/rmm/

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Common Interface for
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RMM : Rapids Memory Management

Laboratoire d'Annecy de Physique des Particules

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Essential for libraries cooperation

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Used in :
- **cuDF**
- **cuML**
- **RAFT**

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Legate

Legate

Accelerate Computing of well used **Python packages**


Legate

Accelerate Computing of well used **Python packages**

NumPy SciPy pandas scikit learn dmlc XGBoost HDF

Scalability on Heterogeneous Hardware

CPU **GPU** **CPU + GPU** **Multiple CPU and GPU** **Supercomputer & Cloud**

Legate

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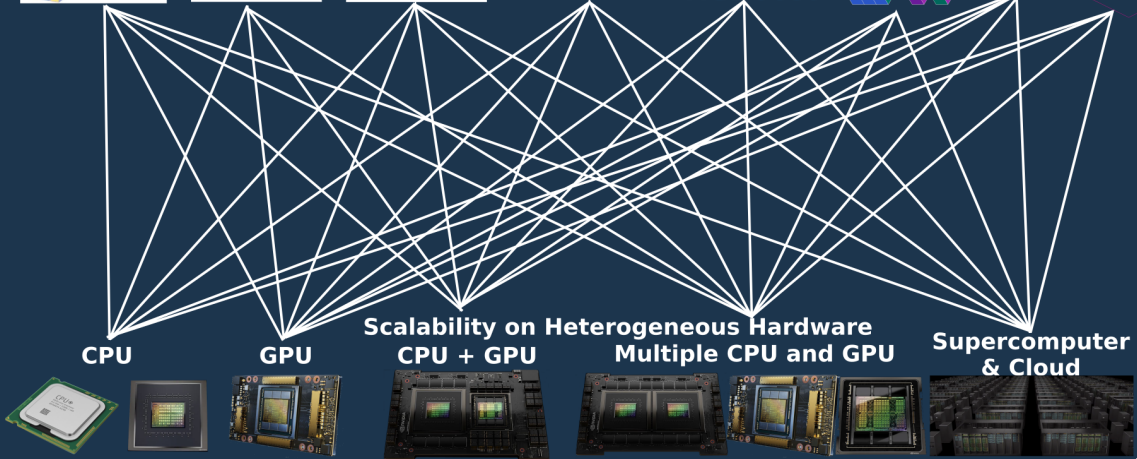

Legate

Accelerate Computing of well used **Python packages**

Too much work
Impossible to maintain

Scalability on Heterogeneous Hardware

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Legate - Productivity and Composable layer

Legion - Implicit Parallelism Layer

Realm - Runtime for Scalable and Portable Execution

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Coherent Backends

Coherent Transfers & Allocations

Scalability on Heterogeneous Hardware

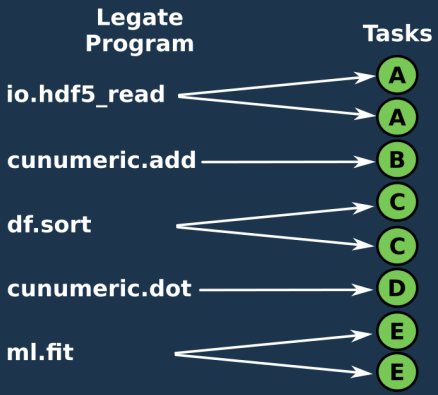
CPU | GPU | CPU + GPU | Multiple CPU and GPU | Supercomputer & Cloud

Legate Scaling

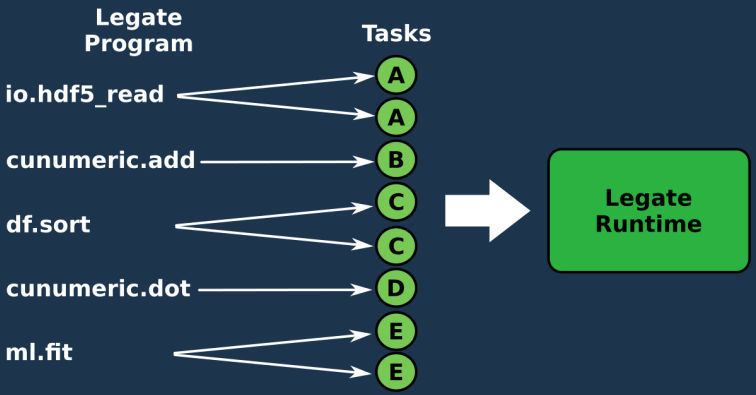
Legate Scaling

Legate Program
io.hdf5_read
cunumeric.add
df.sort
cunumeric.dot
ml.fit

Legate Scaling



Legate Scaling



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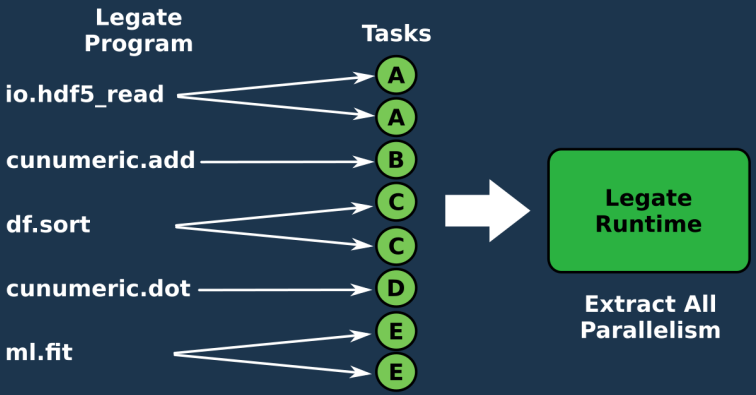

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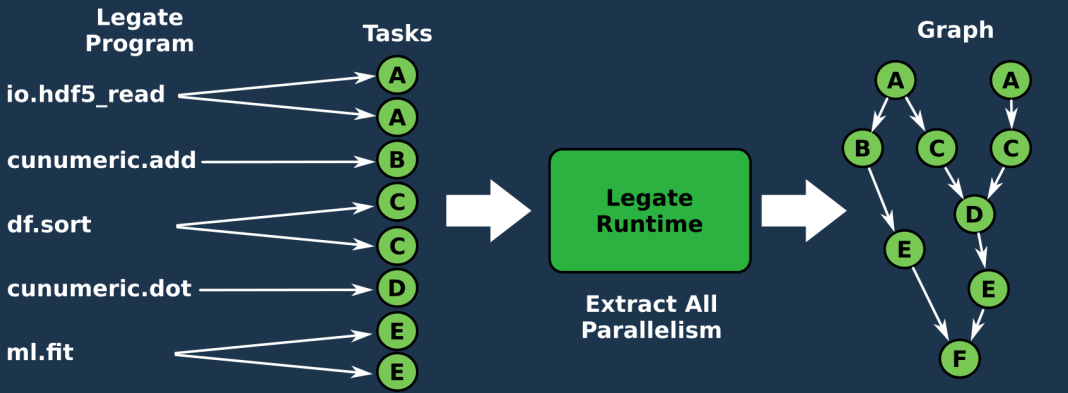

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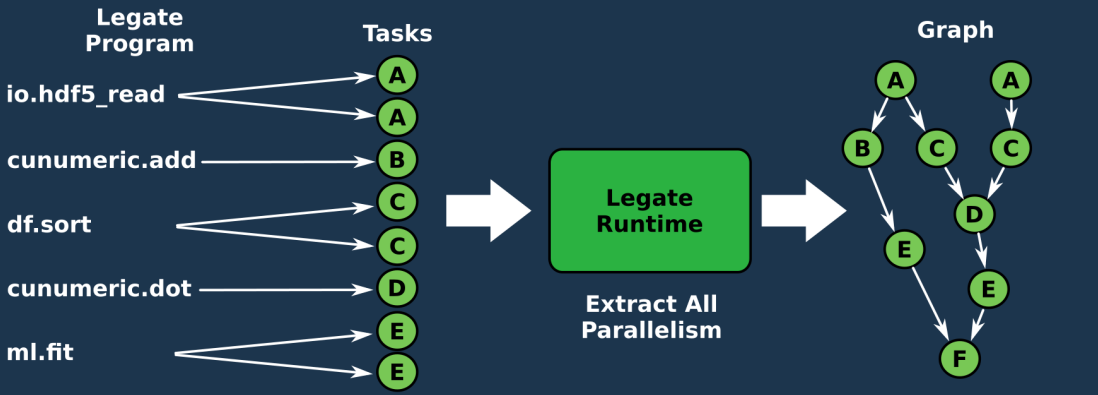

Legate JAX

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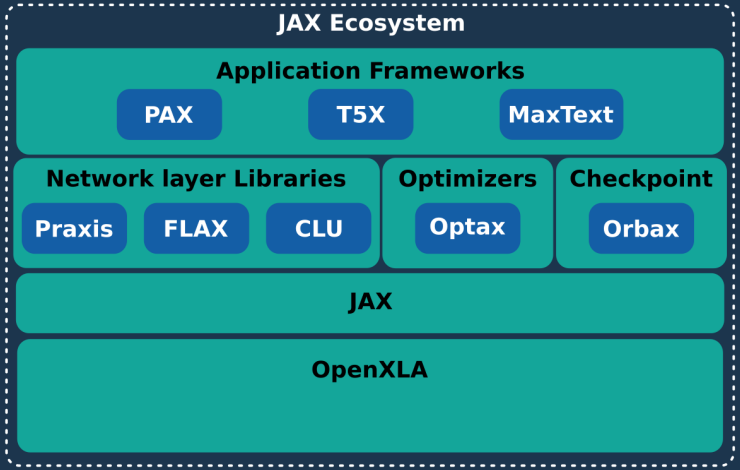
JAX Ecosystem
Application Frameworks
PAX
T5X
MaxText
Network layer Libraries
Praxis
FLAX
CLU
Optimizers
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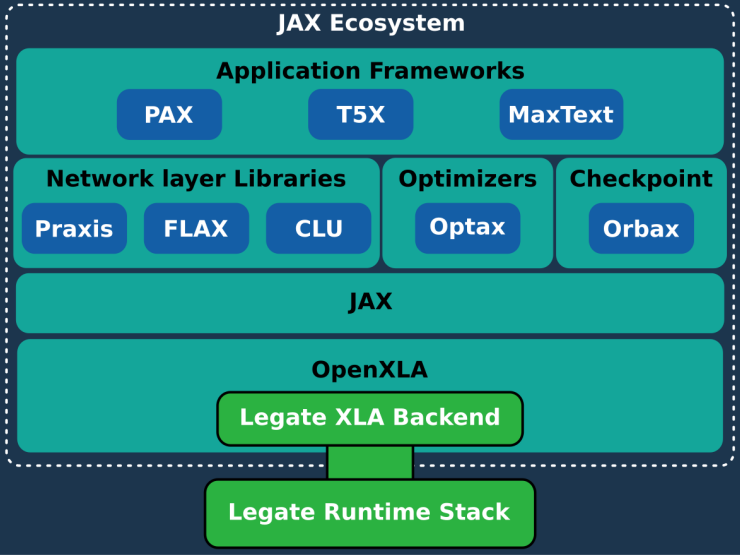
Checkpoint
Orbax
JAX
OpenXLA

Legate JAX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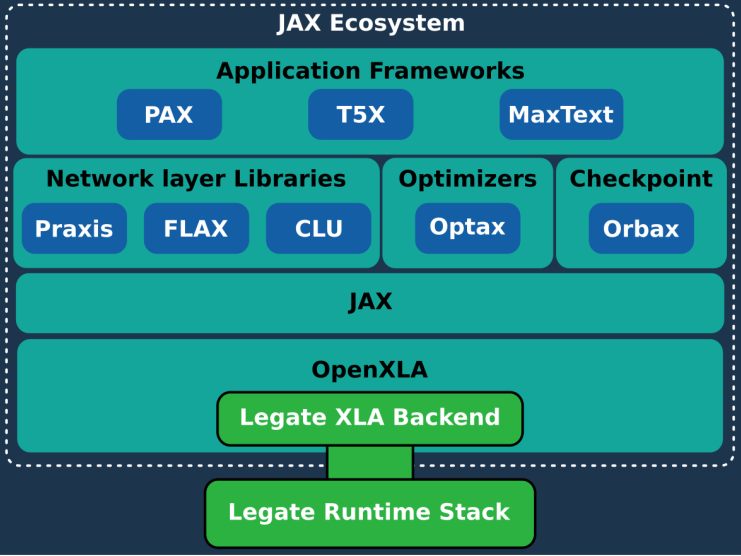
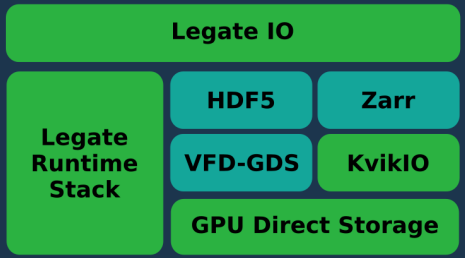
Legate XLA Backend
Legate Runtime Stack

Legate JAX

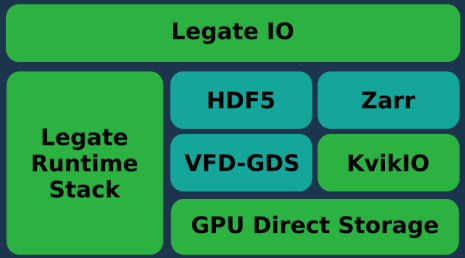


Scalability comparable to State of the art **PAXML (PP)** and **ALPA** on OPT 175B with BFloat16 From **128** to **512 GPU A100**

Legate I/O

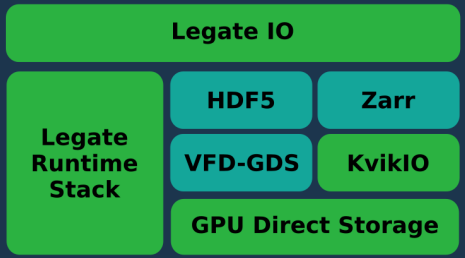

Legate IO
Legate Runtime Stack
HDF5
Zarr
VFD-GDS
KvikIO
GPU Direct Storage

Legate I/O



Real Open-Source Standards

Legate I/O

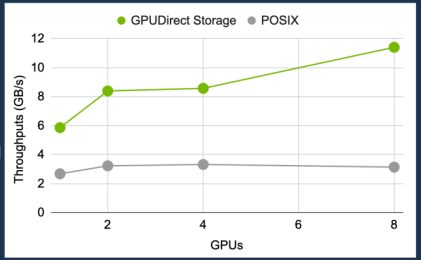


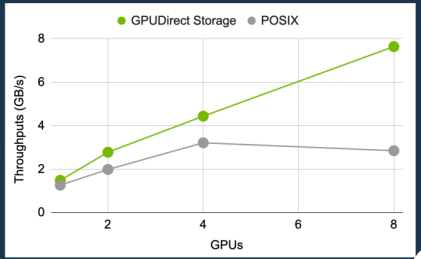
Zarr read with Legate tasking 4GB data per GPU

Real Open-Source Standards

HDF5 read with Legate Tasking 3GB data per GPU

Preliminary weak Scaling Results





Legate CPU/GPU Switch

Example : **multi-physics solver**

```
u, v, p, c, u_coarse, v_coarse, mask = \
    init(nx, ny, nx_coarse, ny_coarse)
for _ in range(nsteps):
    # Run solve with a fine mesh on GPUs

    u, v, p = solve_fluid(u, v, p)
    u_coarse = u[mask].reshape(ny_coarse, nx_coarse)
    v_coarse = v[mask].reshape(ny_coarse, nx_coarse)
    # Run solve with a coarse mesh on CPUs

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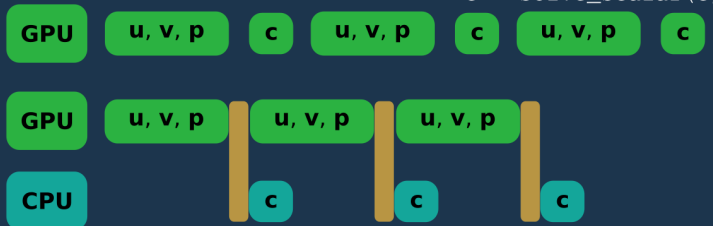

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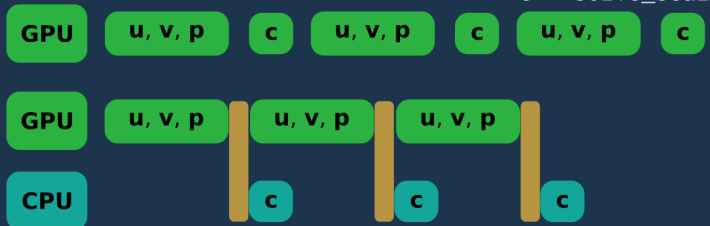

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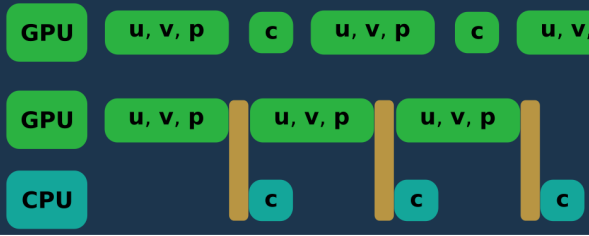

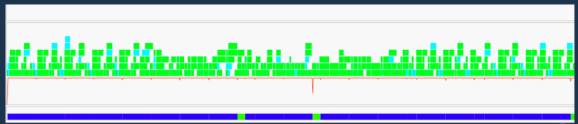

Legate Kernel Fusion

Legate Kernel Fusion

SpMV(**M**, **v** + **w** + **t**)

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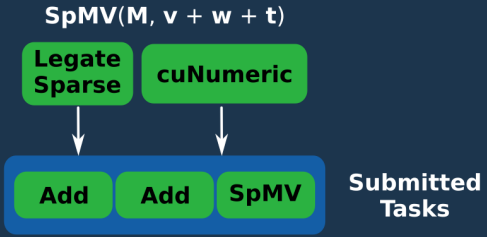
SpMV(**M**, **v** + **w** + **t**)

Legate Sparse **cuNumeric**

Legate Kernel Fusion



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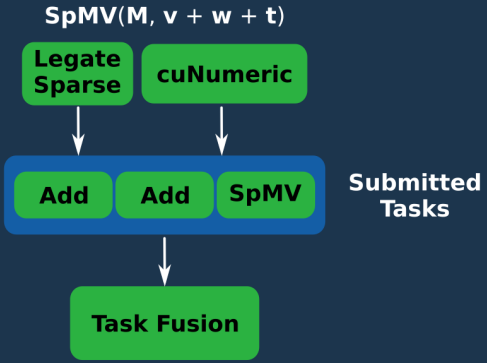

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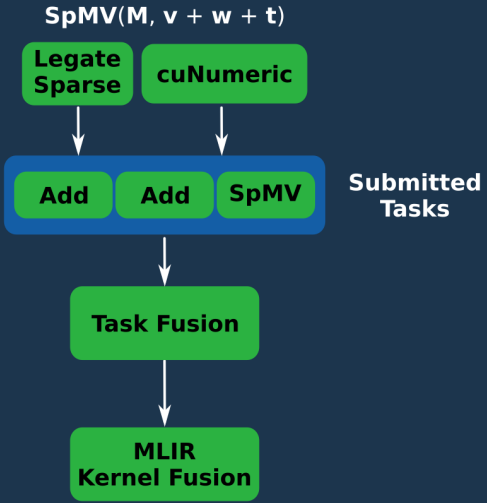

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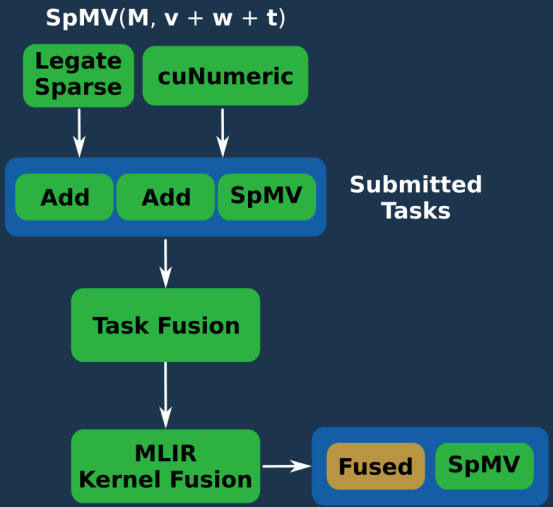

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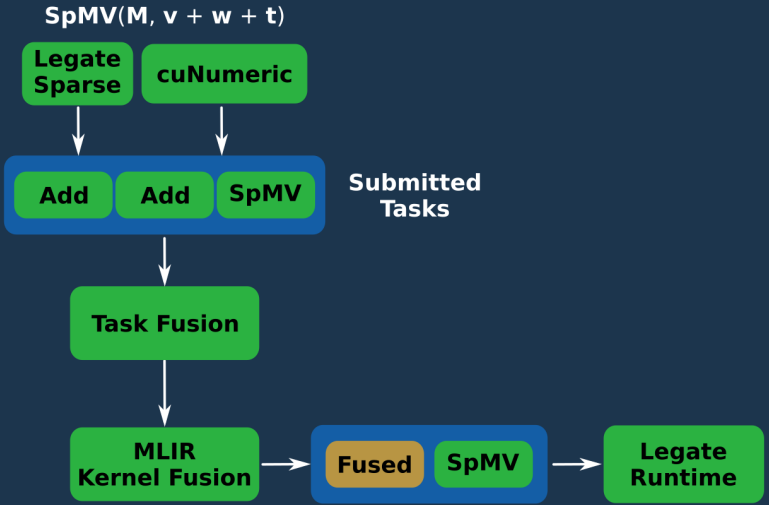

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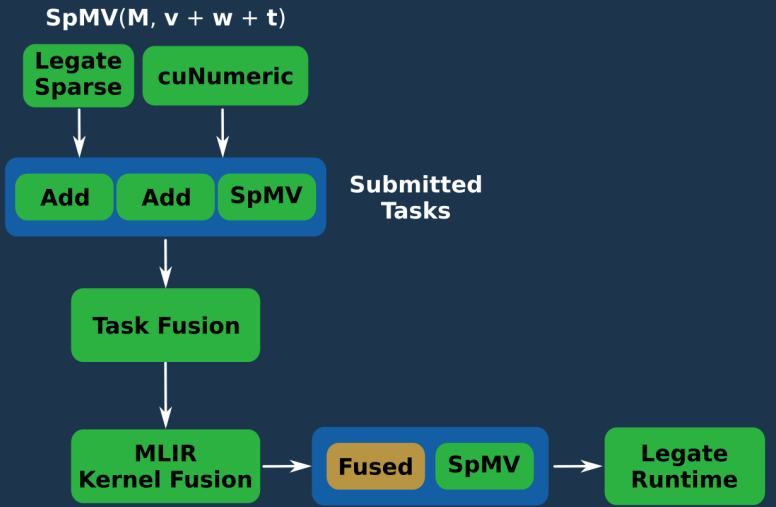
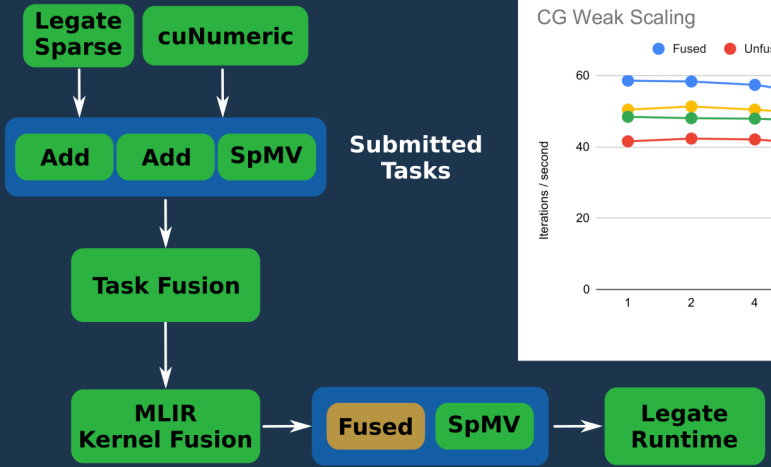


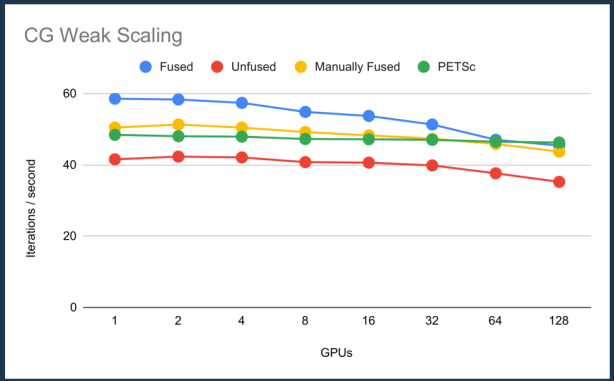
- **No tmp allocation**
- **2** kernel **launch** instead of **3**
- **No Synchro** between kernels
- **No Data Movement**

Legate Kernel Fusion

SpMV(M, v + w + t)



Conjugate Gradient Throughput on DGX-A100 cluster



- **No tmp allocation**
- **2** kernel **launch** instead of **3**
- **No Synchro** between kernels
- **No Data Movement**

Legate Core

Legate Core

Complete **rewrite** of the **core** framework in **C++**

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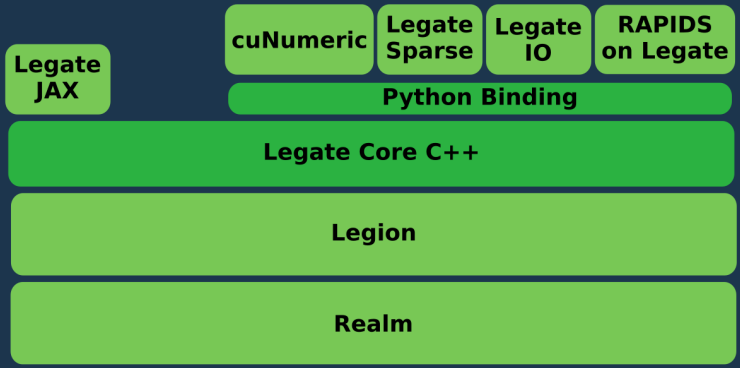

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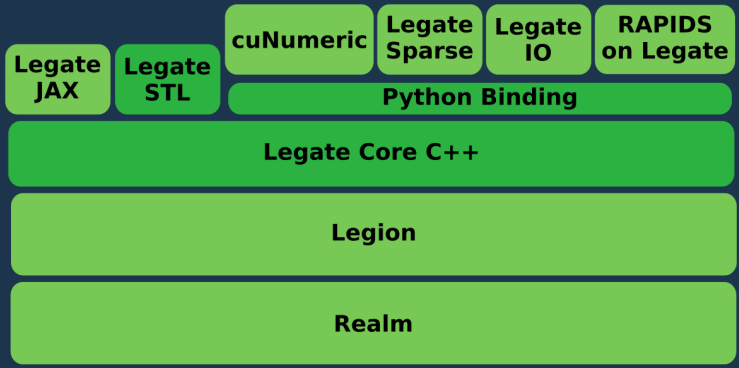

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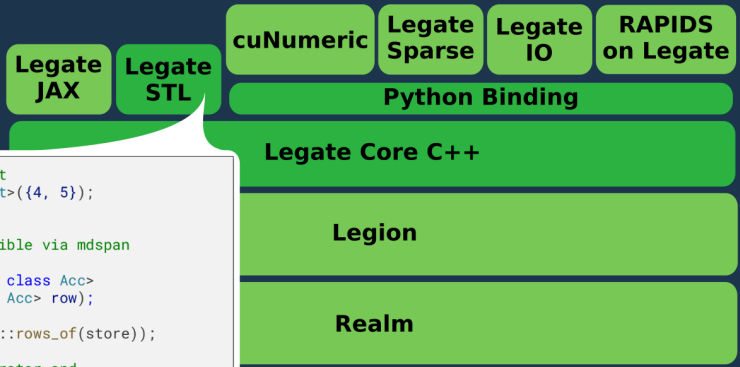


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// Create a 2-D Legate store and initialize it
auto store = legate::stl::create_store<int64_t>({4, 5});
legate::stl::fill(store1, 1.);

// Operate on a row of data at a time, accessible via mdspan
struct MungeRow {
  template <class Elem, class Ext, class Map, class Acc>
  void operator()(std::mdspan<Elem, Ext, Map, Acc> row);
};
legate::stl::for_each(MungeRow{}, legate::stl::rows_of(store));

// Transform the store with a pre-defined operator and
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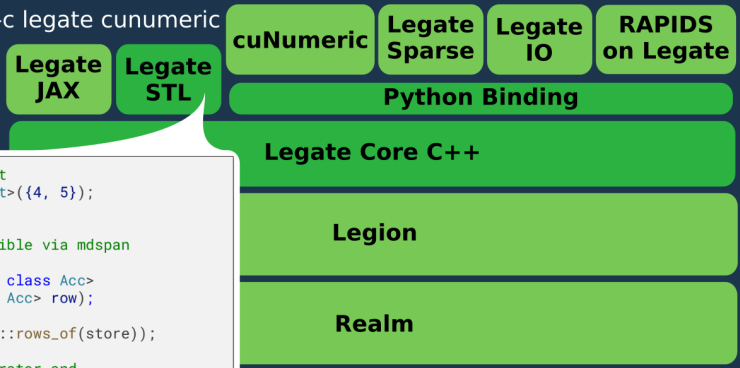
Complete **rewrite** of the **core** framework in **C++**

conda install -c nvidia -c conda-forge -c legate cunumeric

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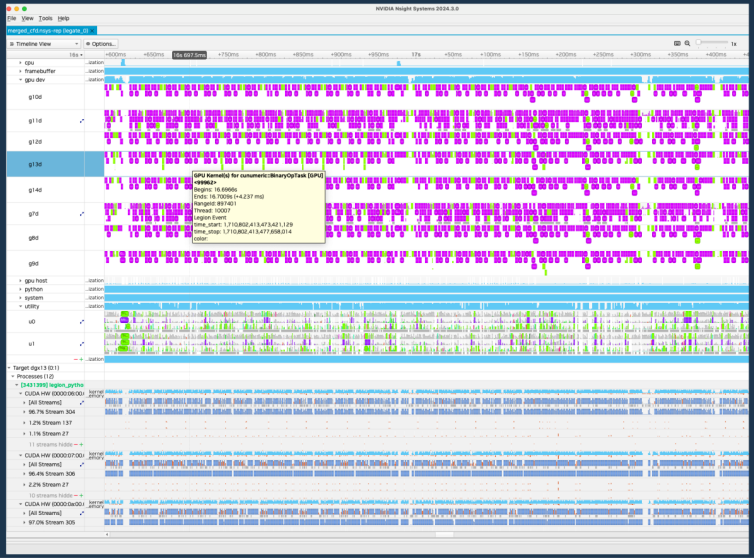
Legate and NSight



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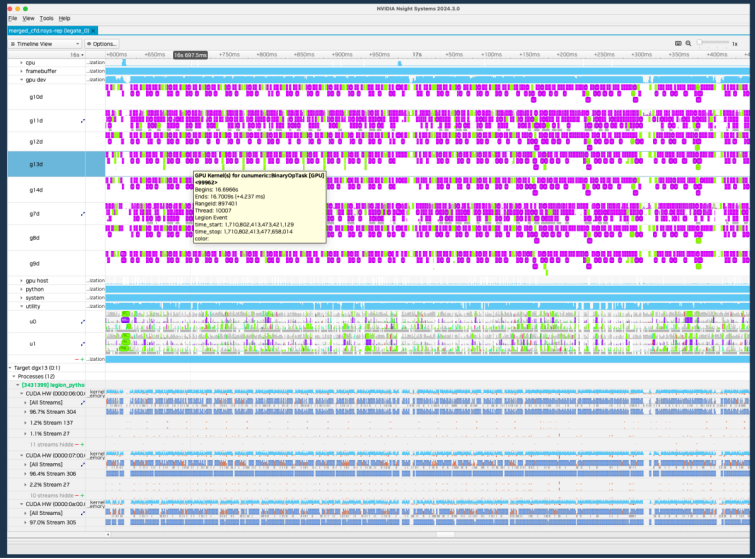
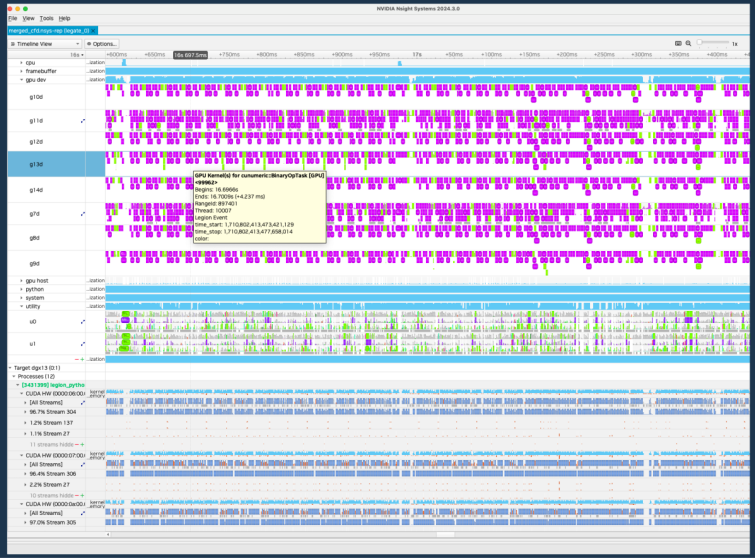


Logical view
Legate tasks,
Legate stores,
runtime activities

Legate and NSight



Logical view
Legate tasks,
Legate stores,
runtime activities

Physical view
GPU (kernels), CPU,
OS, network

Warp : Differentiable Kernels

Differentiable Spatial Computing for Python

Warp : Differentiable Kernels

Differentiable Spatial Computing for Python

Simulation :
- **Rigid Bodies**
- **Particles**
- **Constraints**
- **Geometry**
- **Forces**
- **etc**

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```python
import warp as wp

@wp.kernel
def integrate(p: wp.array(dtype=wp.vec3),
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    # thread id
    tid = wp.tid()

    # Semi-implicit Euler step
    v[tid] = v[tid] + (f[tid] * m[tid] + wp.vec3(0.0, -9.8, 0.0)) * dt
    x[tid] = x[tid] + v[tid] * dt

# kernel launch
wp.launch(integrate, dim=1024, inputs=[x, v, f, …], device="cuda:0")
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Interoperability

PyTorch · JAX · NumPy · NanoVDB

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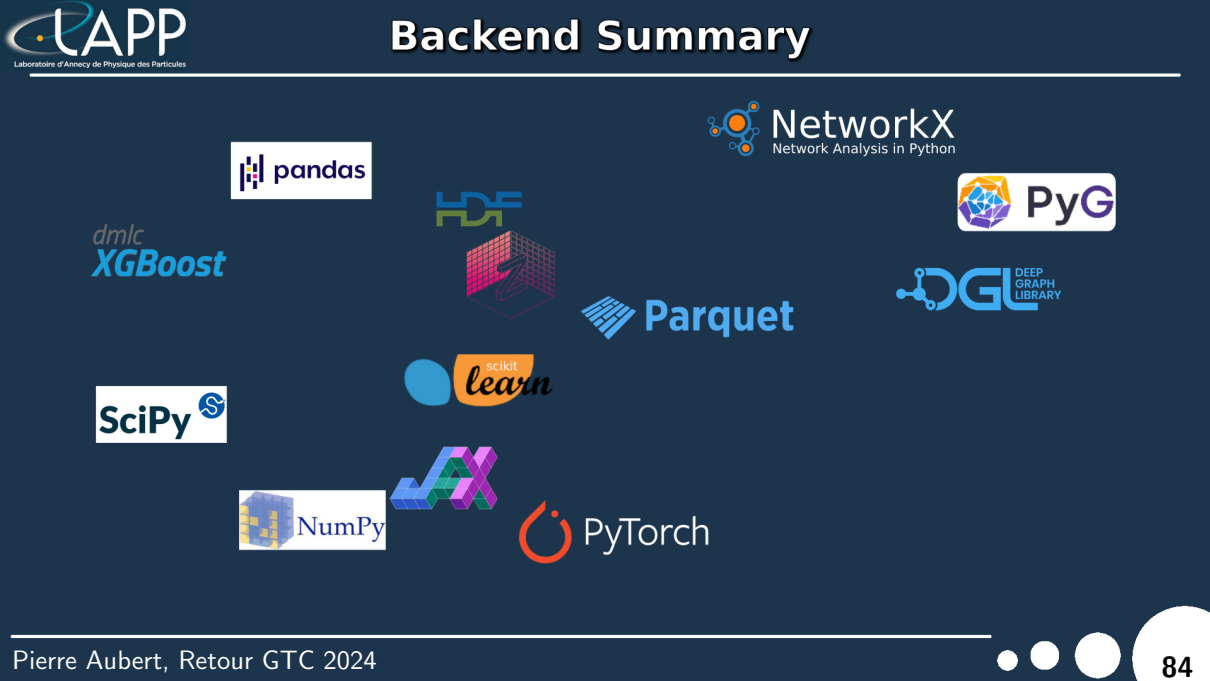
pip install warp-lang

Backend Summary



Backend Summary

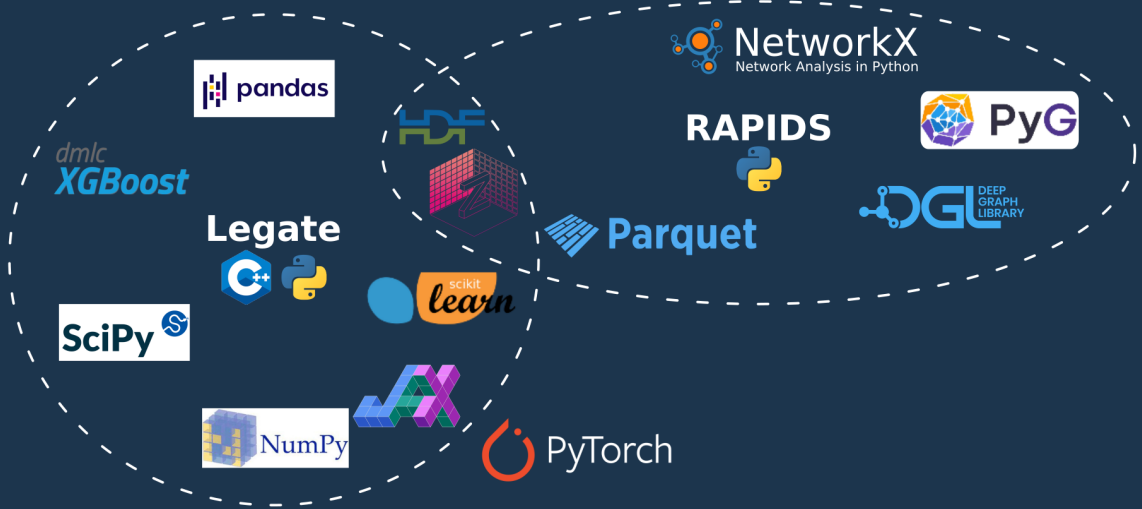
NetworkX
Network Analysis in Python

PyG

DGL DEEP GRAPH LIBRARY

Parquet

Backend Summary



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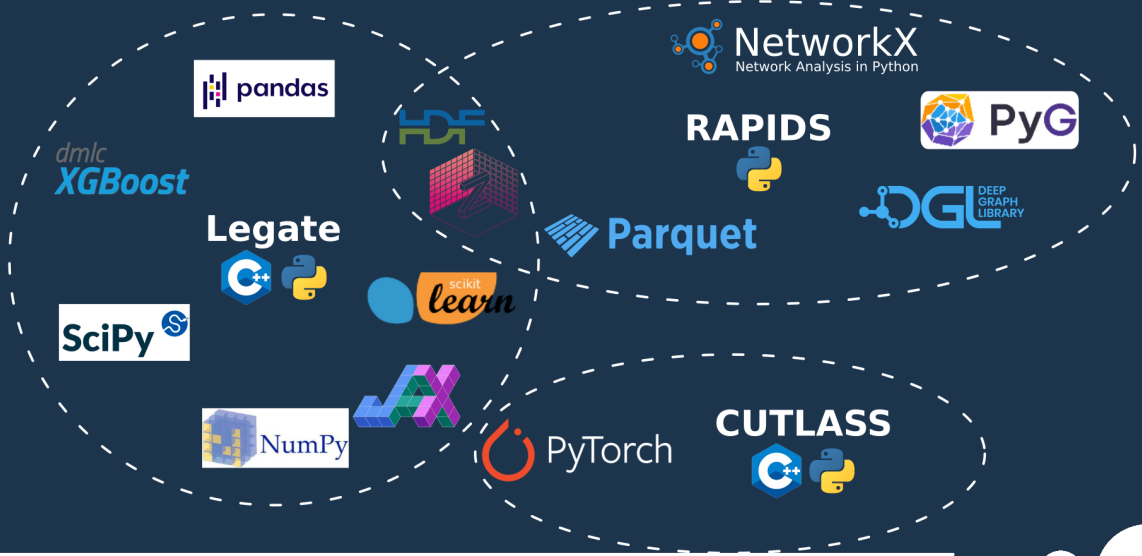

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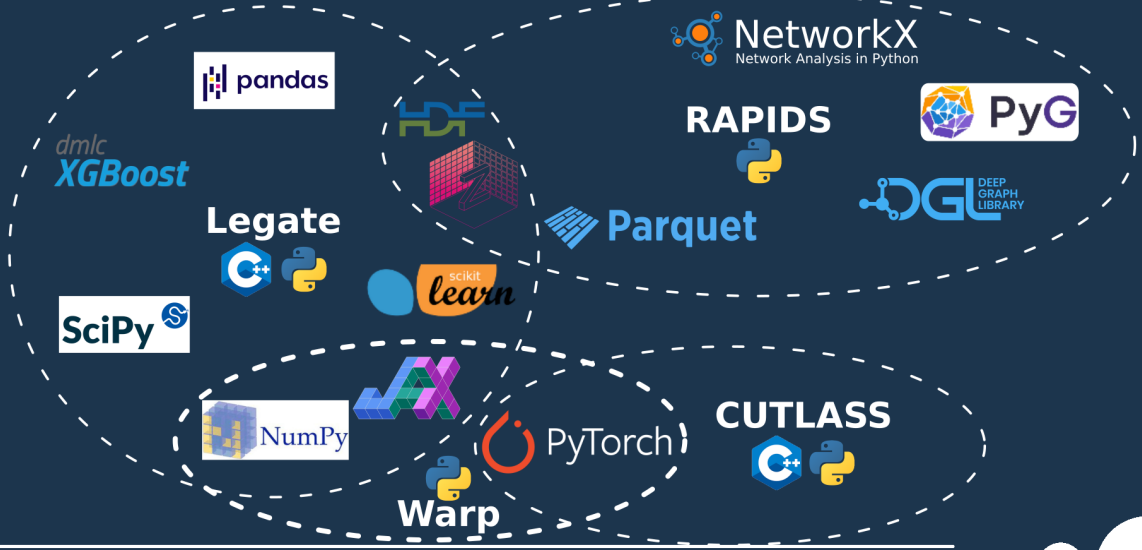

Chip Design and Simulation

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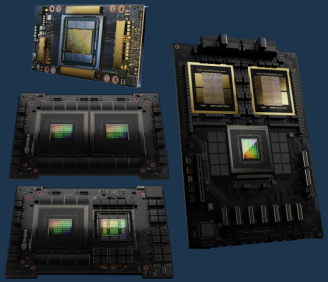
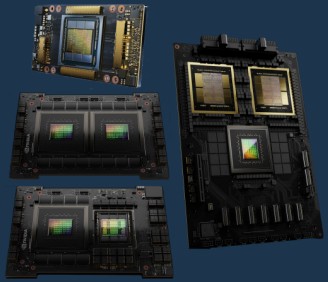


Complex Chips

16 months to produce a chip

3 months to print it for real tests

Chip Design and Simulation



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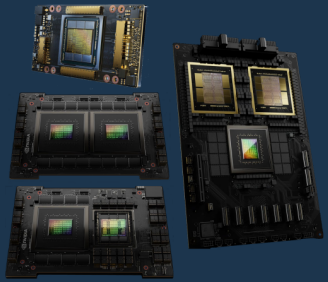

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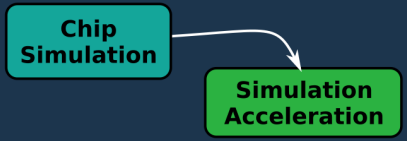

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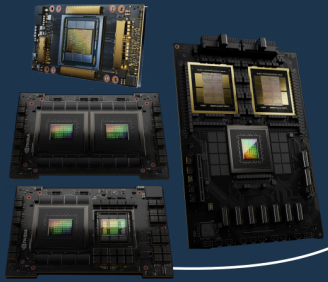

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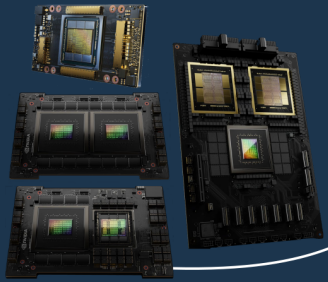

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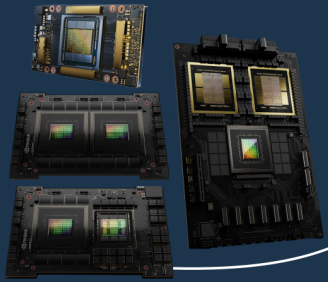

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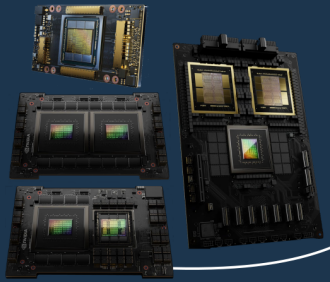

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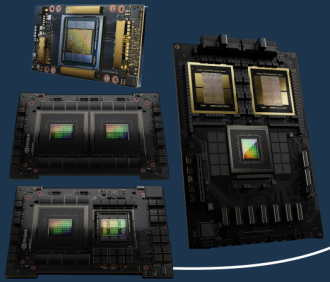

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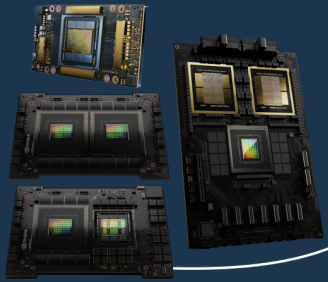

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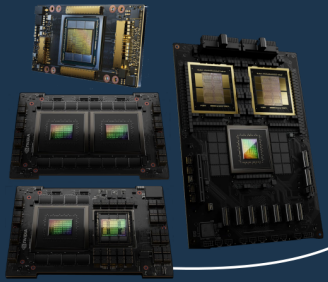

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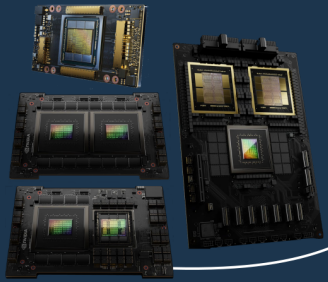

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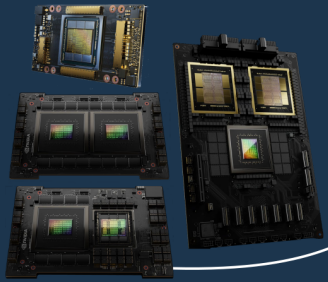

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But helps engineers to find where the problem is

From 2 days to 10 min to find most of problems location

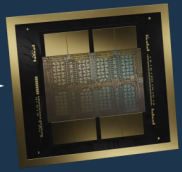
Does not find the solution

Conclusion

Conclusion

Titan 20 PFlops (2012)
7 MW

Blackwell 20 PFlops (2024)
1 kW



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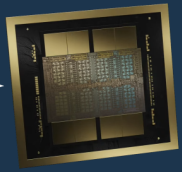

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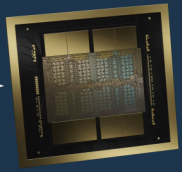

Need to be used efficently

The **Work** has been **done** for **standards**

NumPy SciPy pandas scikit learn dmlc XGBoost JAX HDF Parquet

CPU + GPU scaling up to a full computing center

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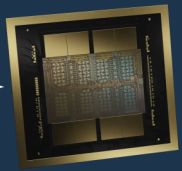
Blackwell 20 PFlops (2024)
1 kW



Need to be used efficently

The **Work** has been **done** for **standards**

CPU + GPU scaling up to a full computing center

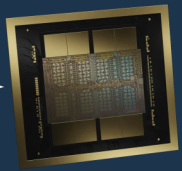
Hardware selling => efficient backends

Open Source Community

Conclusion

Titan 20 PFlops (2012)
7 MW

Blackwell 20 PFlops (2024)
1 kW



Need to be used efficently

We have to use standards

The **Work** has been **done** for **standards**

NumPy SciPy pandas scikit-learn dmlc XGBoost JAX HDF Parquet

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NVIDIA intel

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Link to a big summary

GTC 2024 notes from Reprises website