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The H2M project: Porting the functionality of a hybrid readout chip into a monolithic 65 nm CMOS imaging process

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Monolithic active pixel sensors (MAPS) are attractive candidates for the next generation of vertex and tracking detectors for future lepton colliders. Especially an only recently accessible 65 nm CMOS imaging technology, that allows for higher logic density at lower power consumption compared to previously used imaging processes, is of high interest. To investigate this technology, explore the design challenges of porting a hybrid pixel detector architecture into a monolithic chip, and to exercise the digital-on-top design methodology, the H2M (Hybrid-to-Monolithic) test chip has been developed and manufactured. It features a 64x16 pixel matrix with a pitch of $35 \times 35 \mu\text{m}^2$, resulting in a total active area of approximately 1.25 mm^2 . The sensitive pixel matrix is designed in the so called n-gap layout to optimise charge collection and boost the detection efficiency. This contribution introduces the H2M chip and presents results from calibration and test-beam measurement campaigns.

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