

# The H2M project: Porting the functionality of a hybrid readout chip into a monolithic 65 nm CMOS imaging process

3rd ECFA workshop on e+e- Higgs, Electroweak and Top Factories, Paris

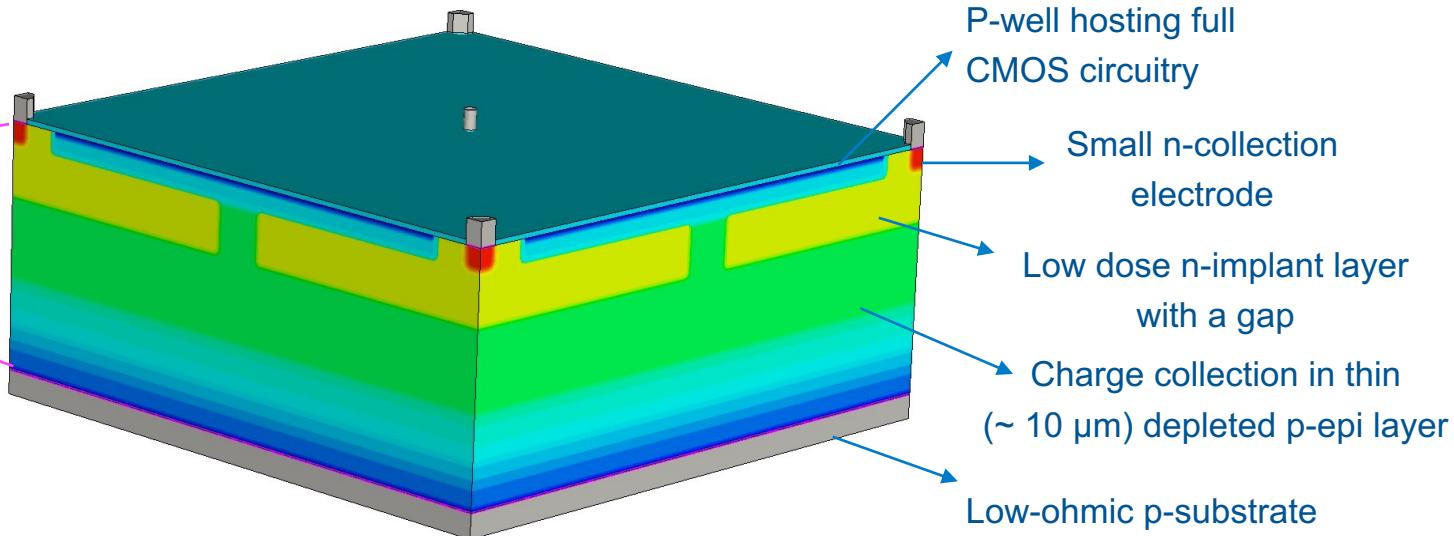
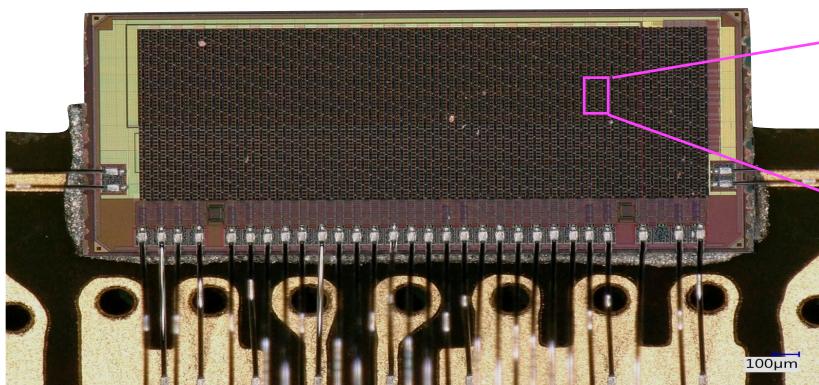
October 9<sup>th</sup>, 2024

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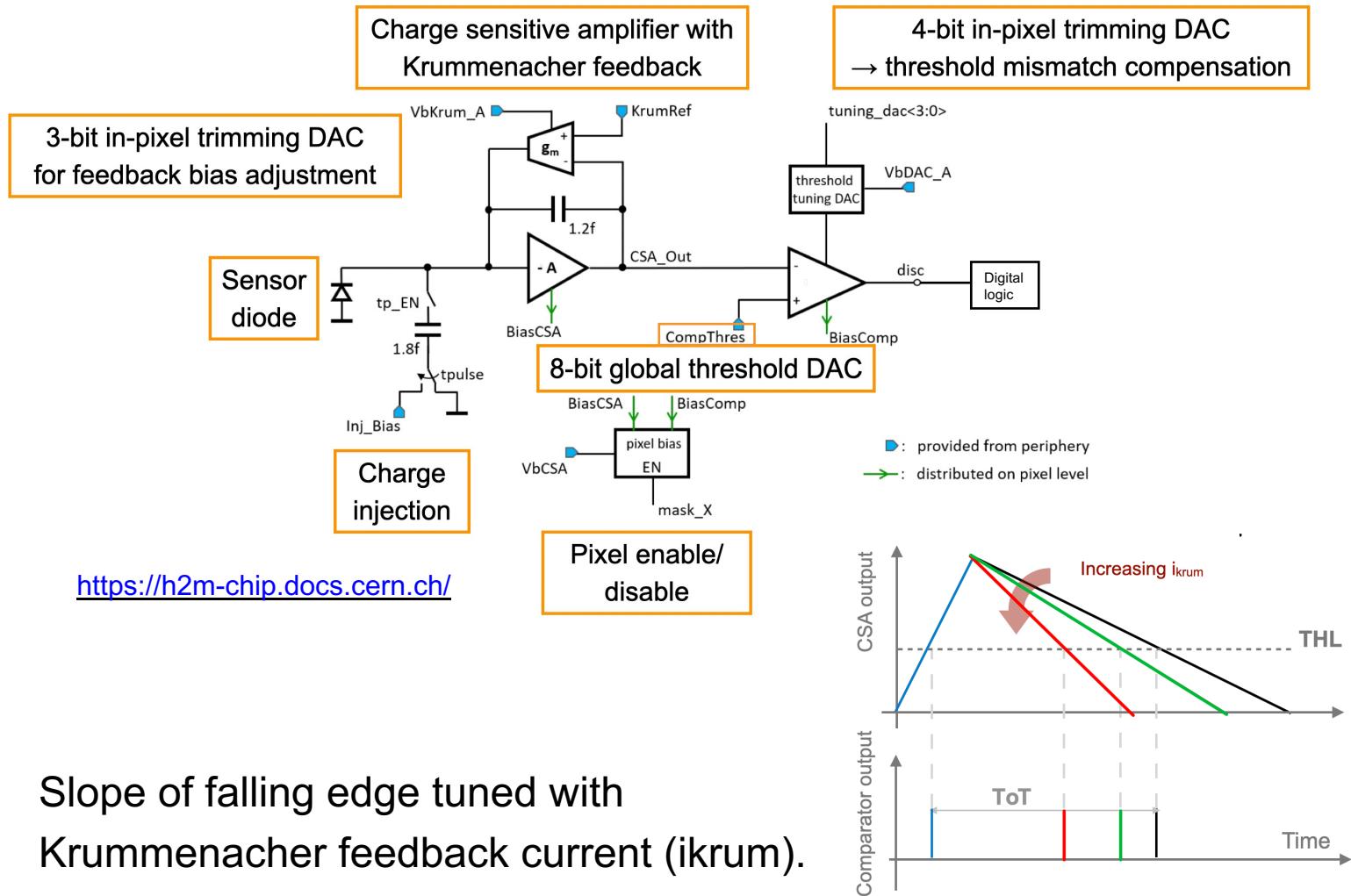


# H2M (Hybrid-to-Monolithic)

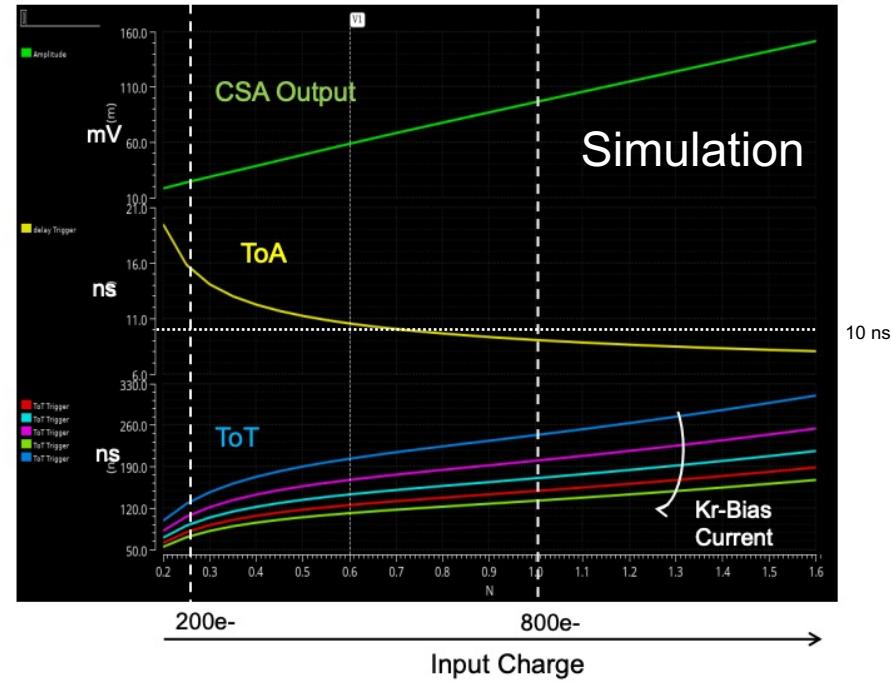
- Ports a **hybrid pixel detector architecture** into a **monolithic chip**.
- **Digital-on-top** design workflow.
- Manufactured in a TPSCo **65 nm CMOS imaging process**.
- **35 µm pixel pitch in 64x16 pixel matrix** (total sensitive area:  $2.24 \times 0.56 \text{ mm}^2$ ). Total thickness  $\sim 50 \mu\text{m}$ .  
(p-epitaxial layer  $\sim 10 \mu\text{m}$ )
- Analog and digital front-end per pixel.



# Analog front-end design



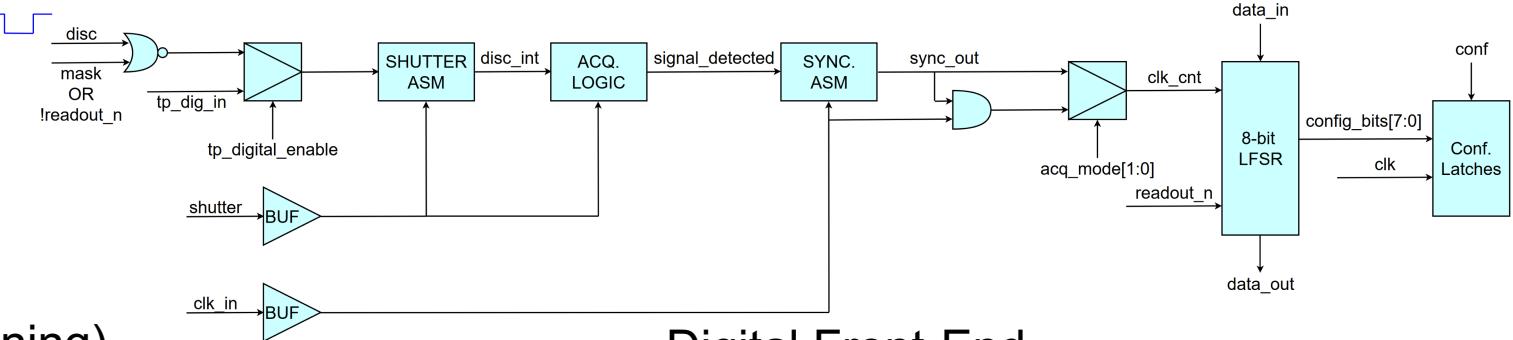
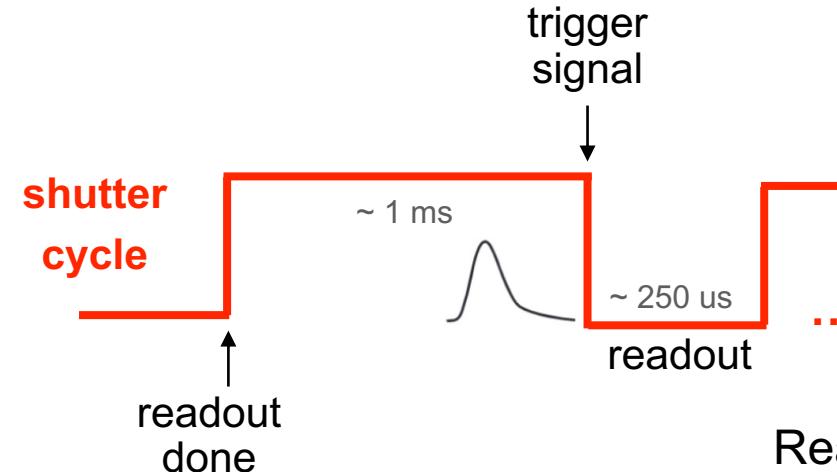
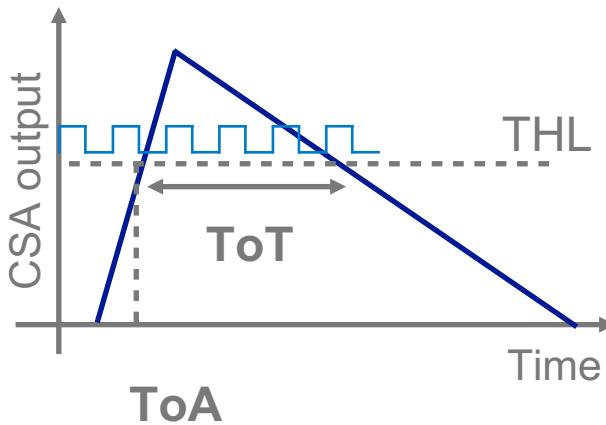
ToA/ToT as function of input charge



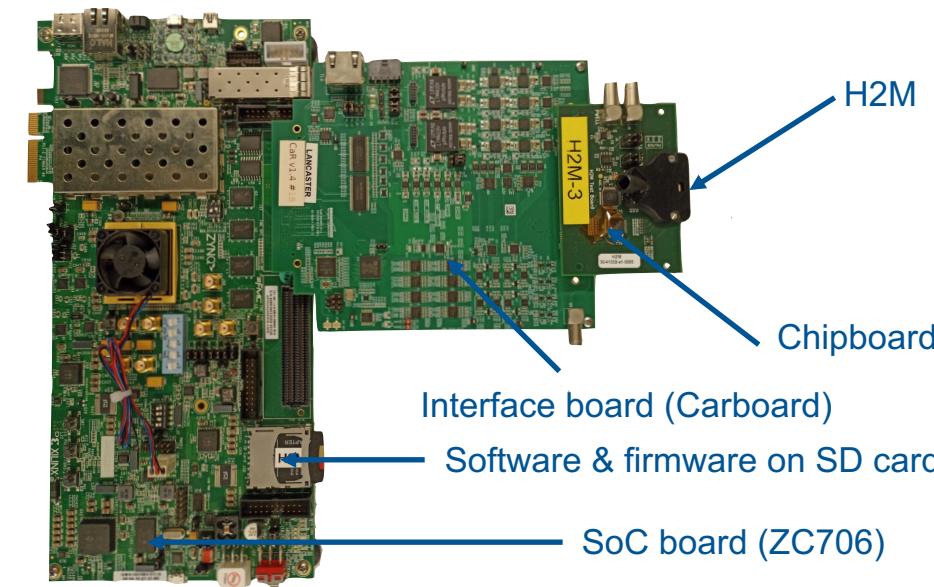
Simulated time walk below 10 ns for input charges larger than 400 electrons.

# Data Acquisition

- **4 acquisition modes** per pixel:
  - 8 bit ToT,
  - 8 bit ToA (100 MHz clock - 10 ns binning),
  - counting (#number of hits above threshold),
  - triggered.
- **Readout:** 40 MHz clock, frame-based without zero-suppression.



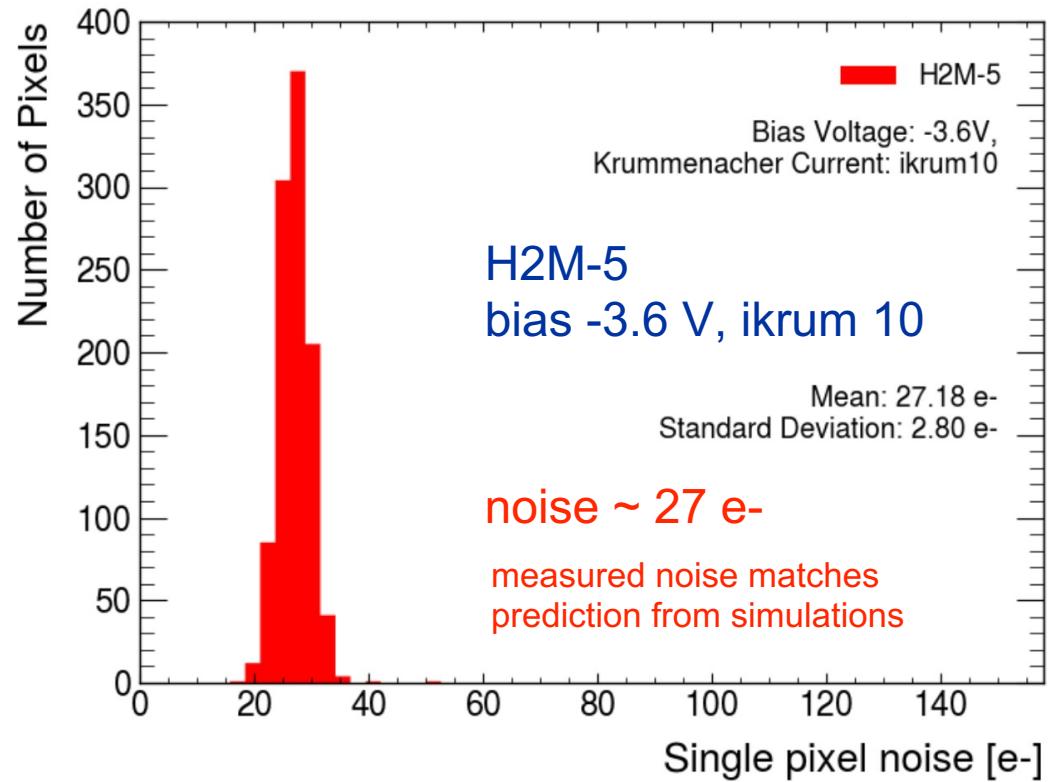
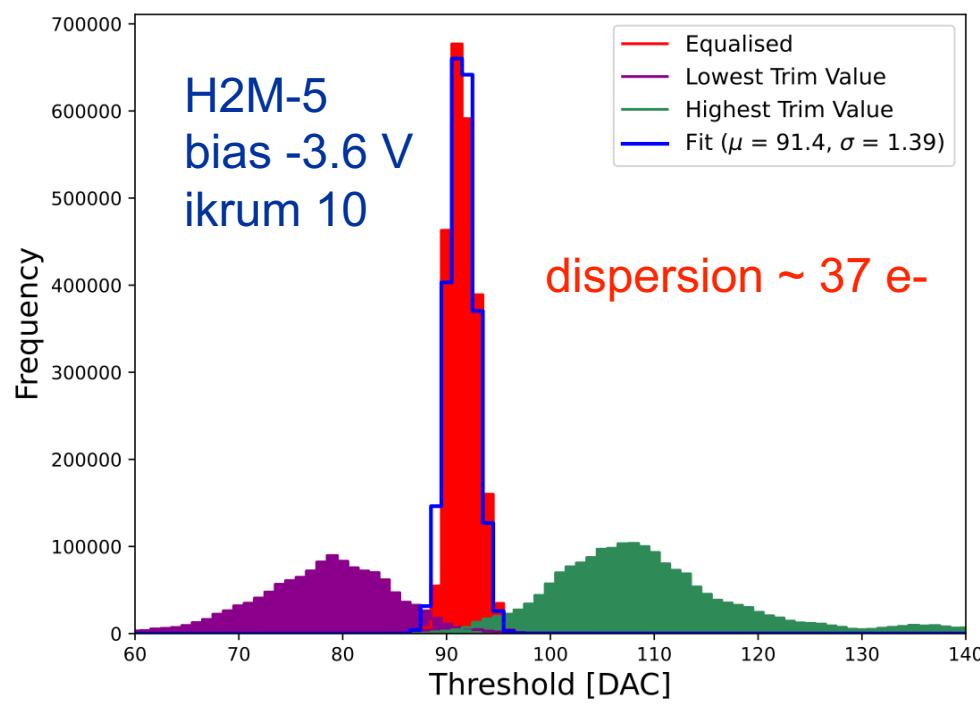
Digital Front-End



T. Vanat, TWEPP2019:100, 2020.

Readout system based on the **Caribou DAQ**.

# Threshold equalisation and single-pixel noise



Equalisation of the hit detection threshold:

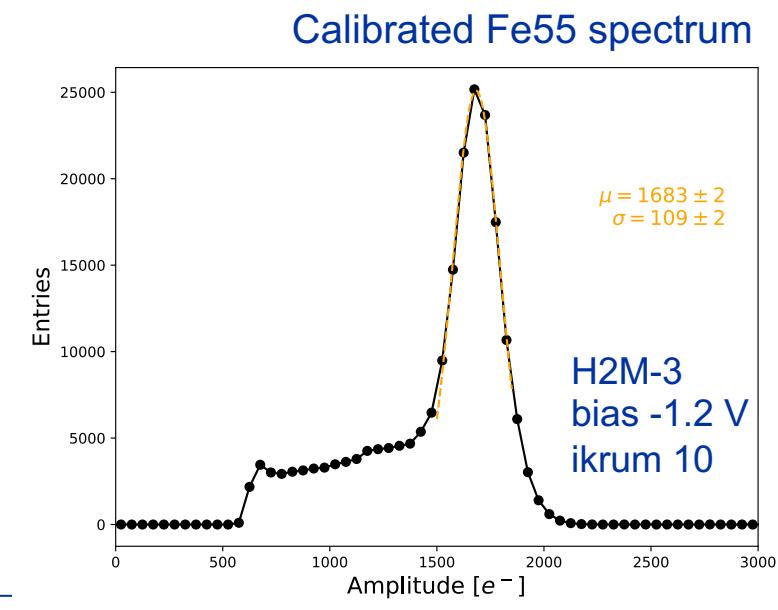
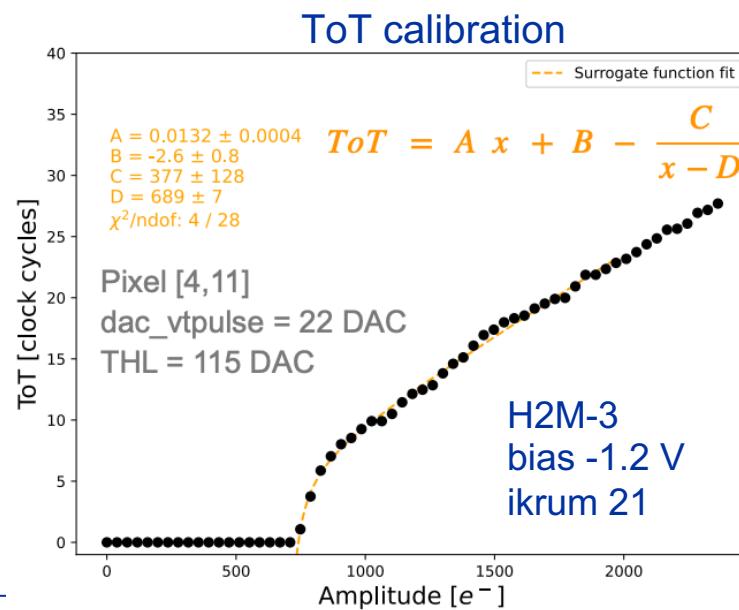
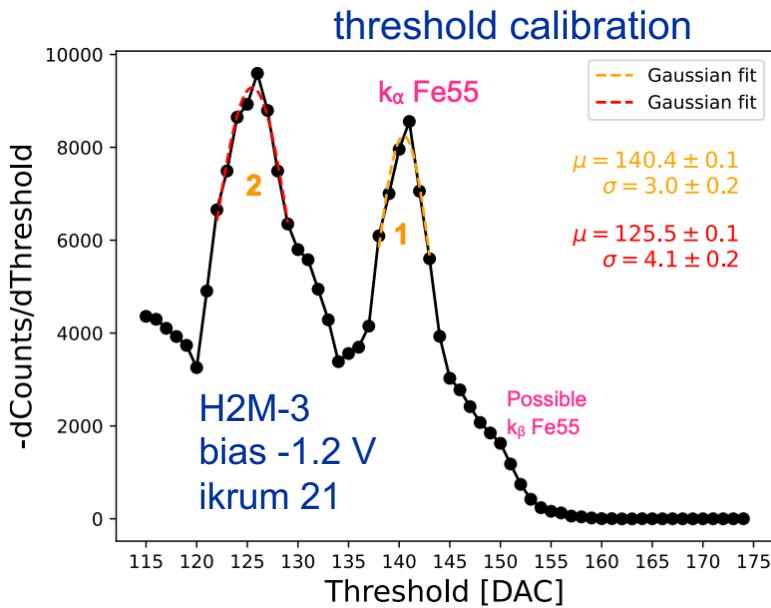
- 1) Threshold scan in counting mode for the 16 trimming values.
- 2) Determine the baseline for each pixel for each trimming value.
- 3) For each pixel, the trimming DAC is adjusted to the one with baseline closest to a fixed trimming target.
- 4) Single-pixel noise obtained from width of threshold turn-on curves.

# Threshold and ToT calibration

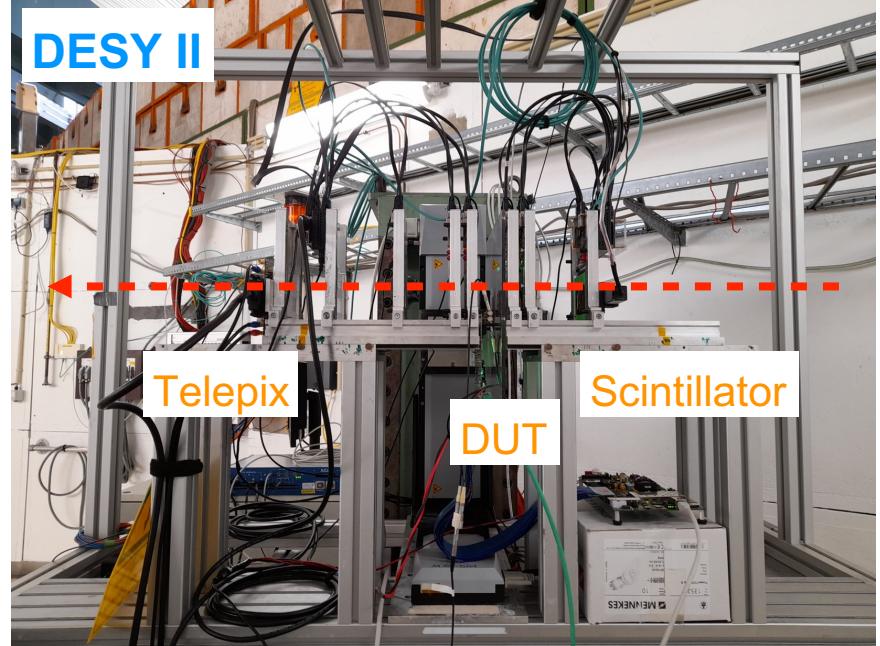
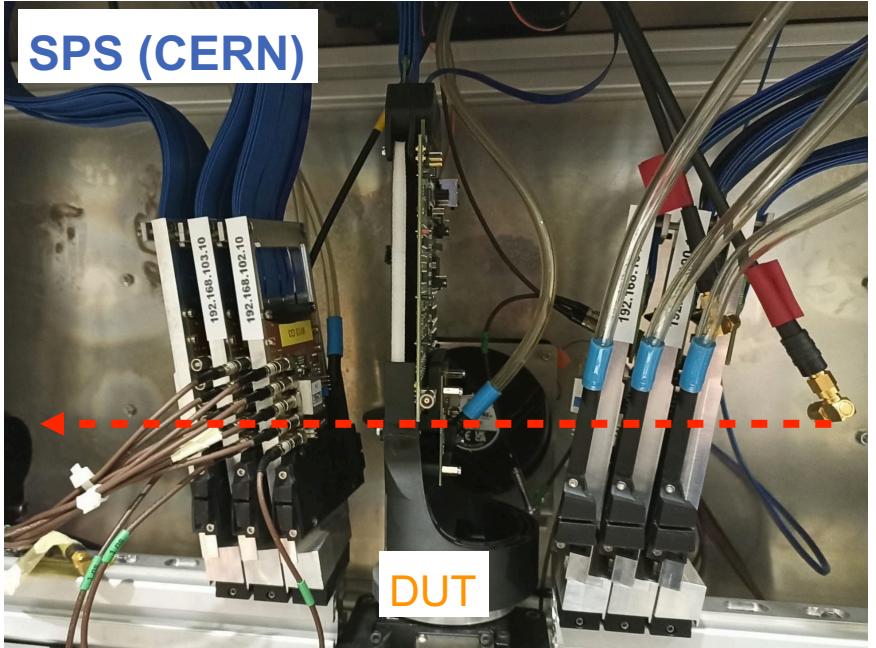
H2M-2, pixel [2,14]  
Vbias -1.2V,  
ikrum 21,  
thr 120 DAC



- Source measurement (Fe-55 and Ti) for global energy calibration of threshold and for calibration of test-pulse injection energy scale  
→ two peaks originating from fast/slow charge-collection regions inside pixel (ballistic deficit + CSA response, depends on Krummenacher feedback current)
- Calibration of per-pixel ToT scale with test-pulse injection
- Calibrated ToT accuracy ~5%



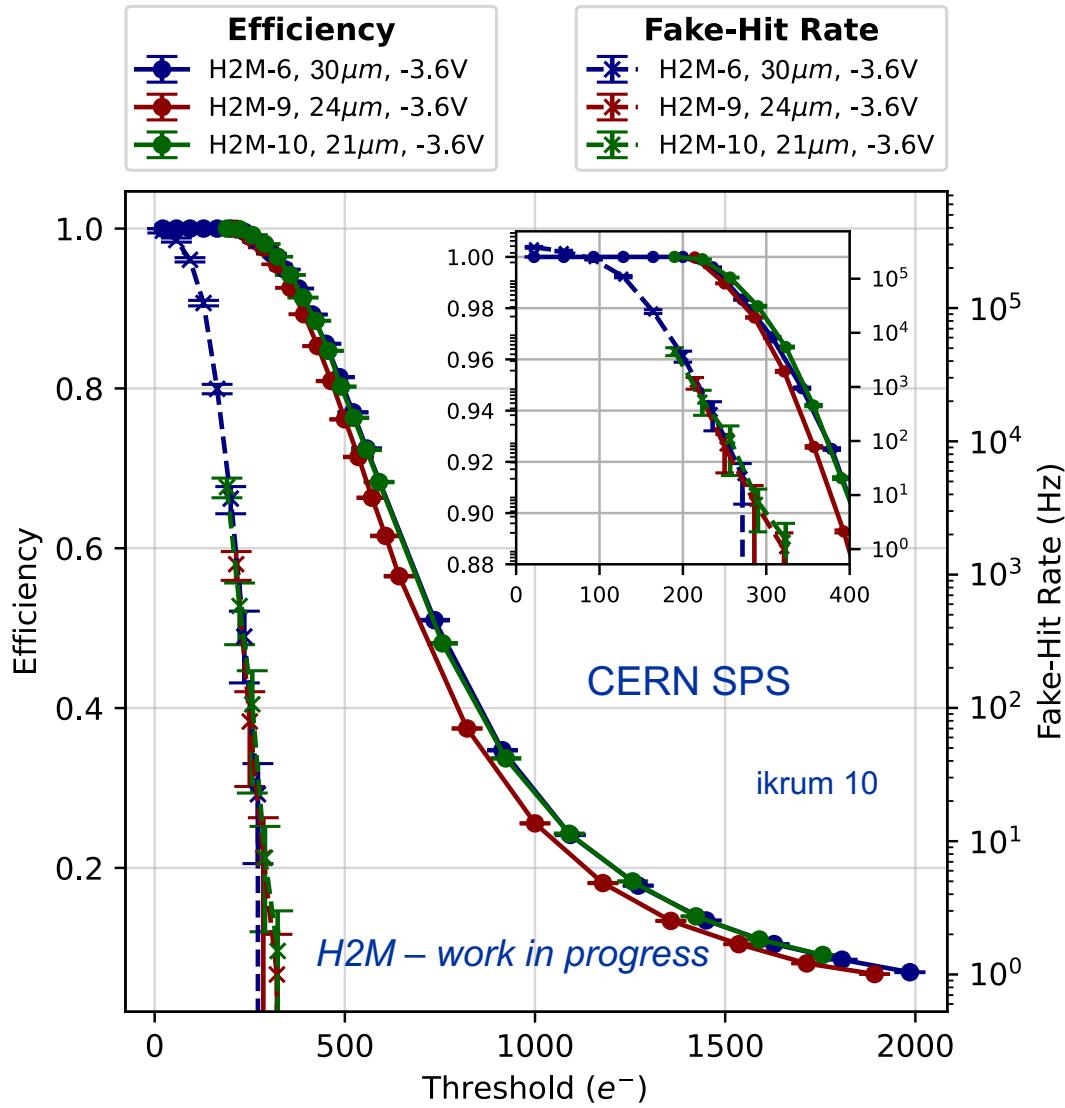
# Test beam campaigns



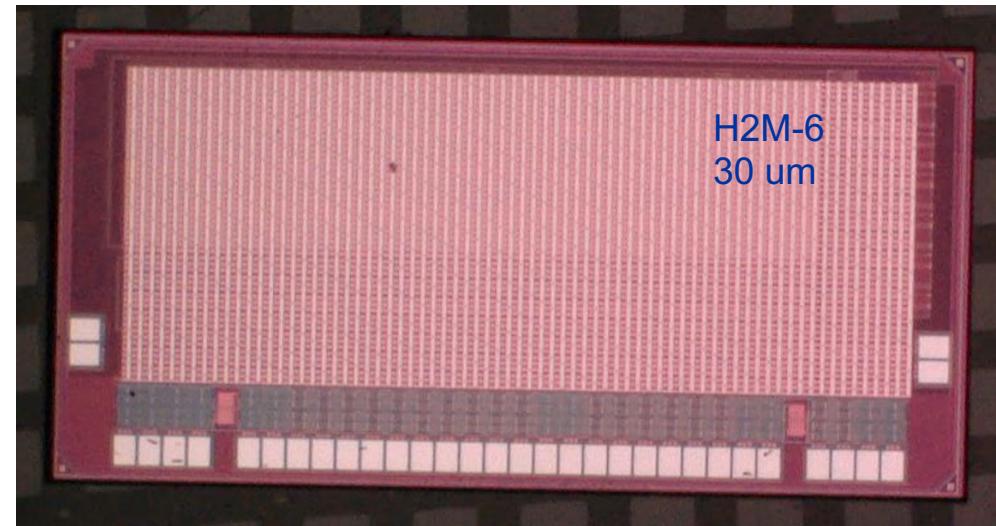
- H6 beam line, 120 GeV charged pions.
- **Timepix3 reference telescope.**
  - Pointing resolution  $\sim 1.5 \mu\text{m}$ ,
  - Track time resolution  $\sim 1 \text{ ns}$ ,
  - Continuous readout with 150  $\mu\text{s}$  (2.56  $\mu\text{s}$ ) shutter duration for ToT (ToA) mode.

- Beamlne 22, electron beam  $\sim 4.8 \text{ GeV}$ .
- **ALPIDE reference telescope.**
  - Pointing resolution  $\sim 3 \mu\text{m}$
  - Scintillator & Telepix used as region-of-interest triggers ( $\sim 5\text{ns}$  resolution).

# Efficiency and fake hit rate of thinned samples

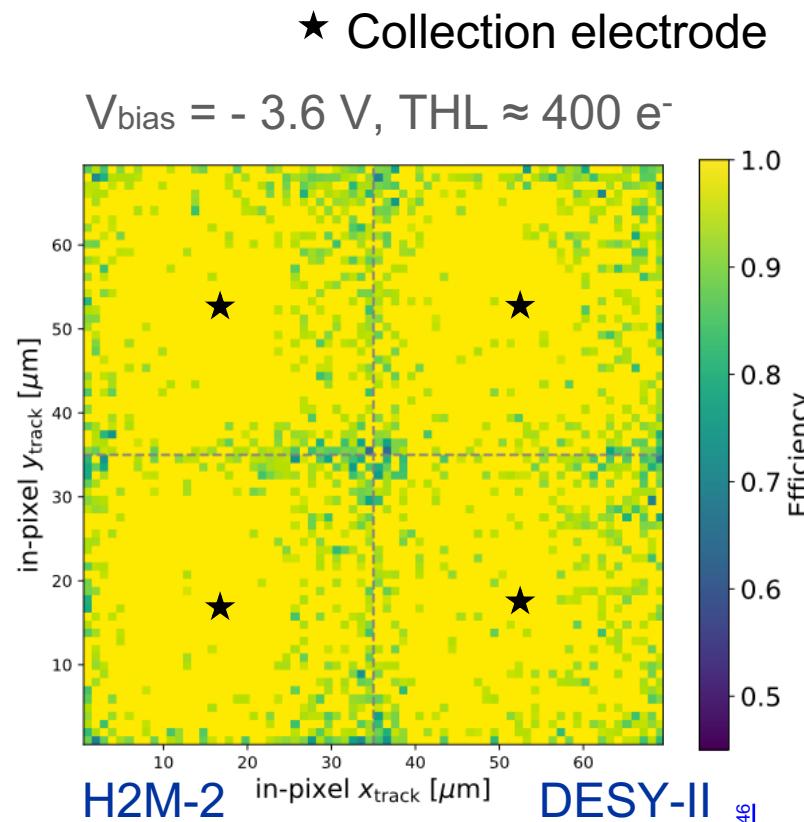
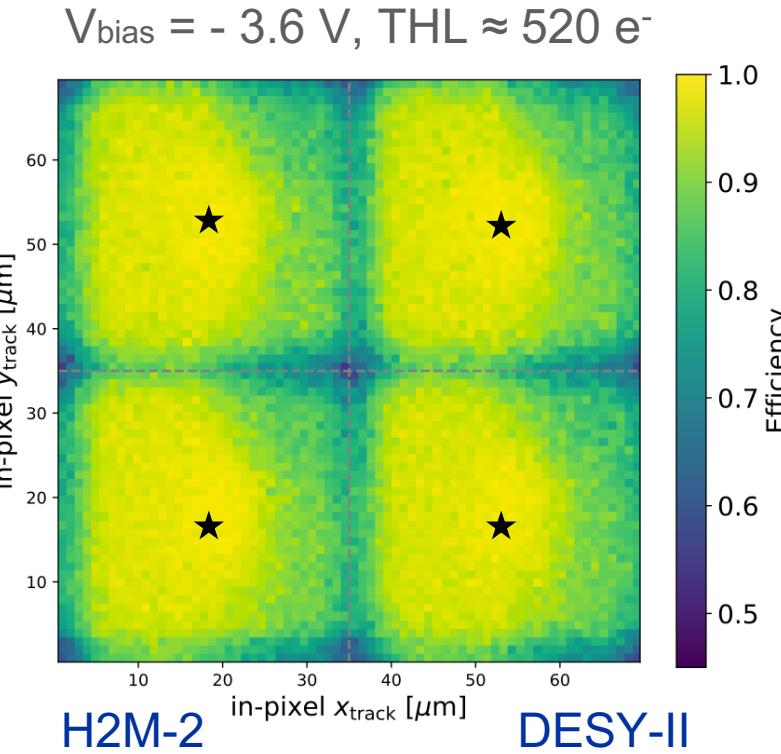
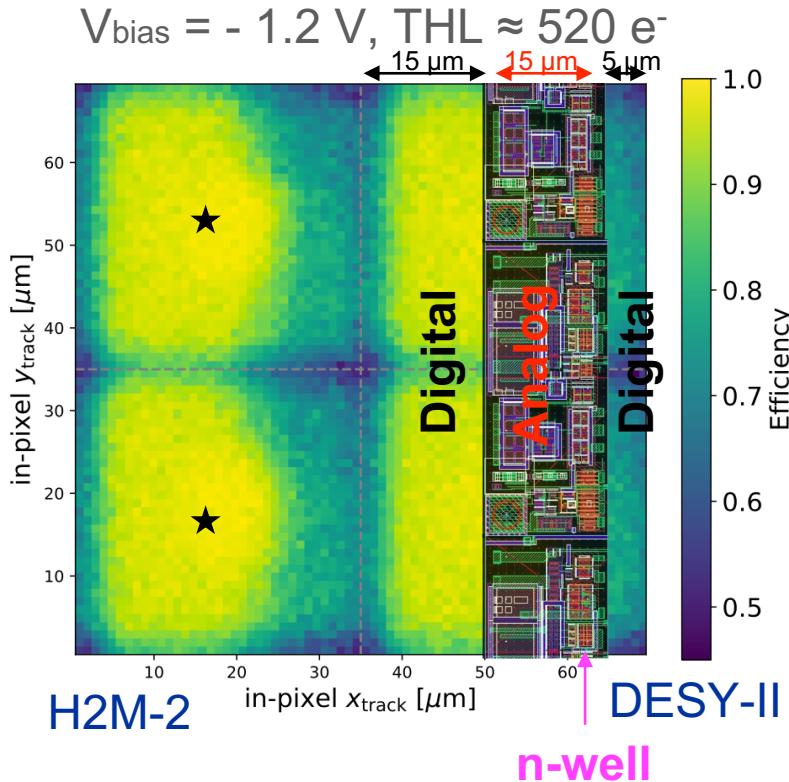


- Single-die backside thinning of H2M samples, performed by [OPTIM WS](#)  
→ 30-21  $\mu$ m physical thickness
- Includes ~5  $\mu$ m circuitry + ~10  $\mu$ m epitaxial layer



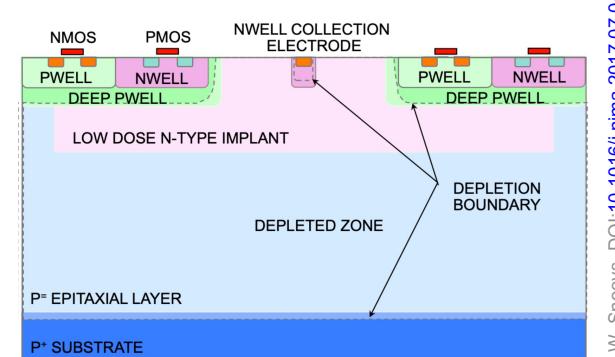
- Efficiency >99% for ~250  $e^-$  threshold @ ~100 Hz fake-hit rate (with up to 11 pixels masked)
- No performance degradation from thinning

# In-pixel efficiency map



## Non-uniform in-pixel efficiency:

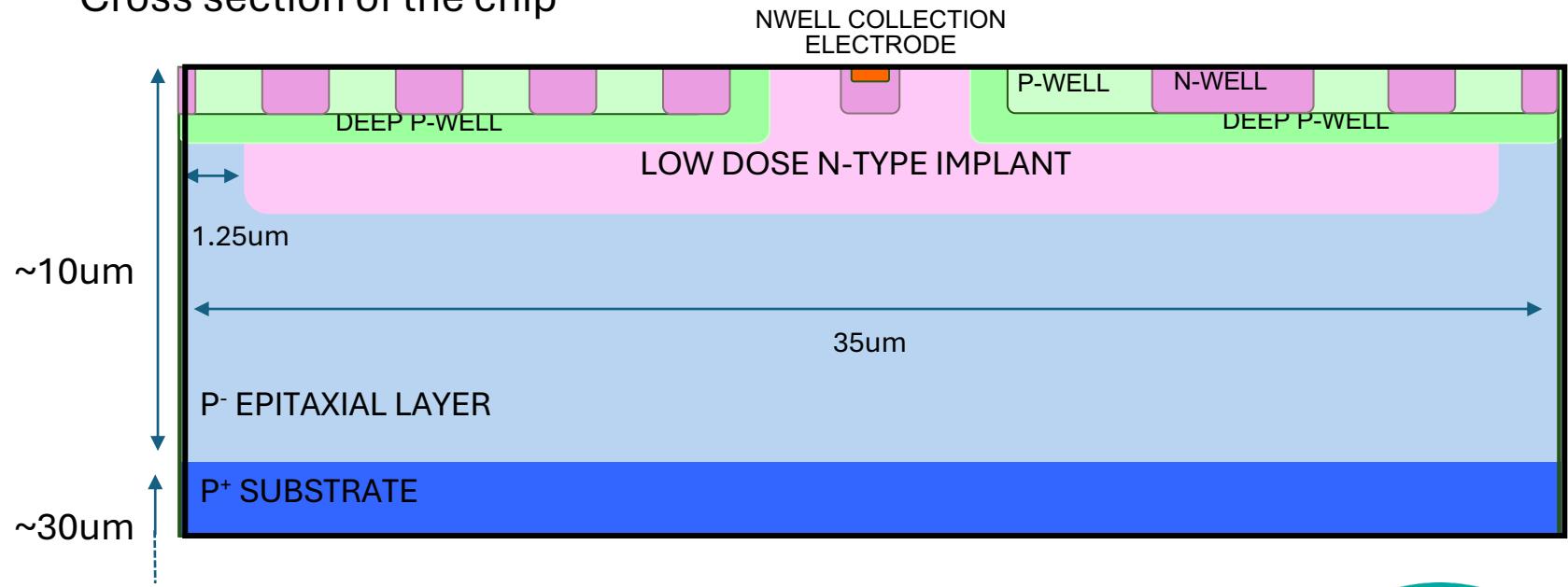
- Related to the size and location of the n-wells of the analog circuitry.
- Mitigated at larger  $V_{bias}$  and lower thresholds.
- Additionally, effects of fast front-end and large pixel size.



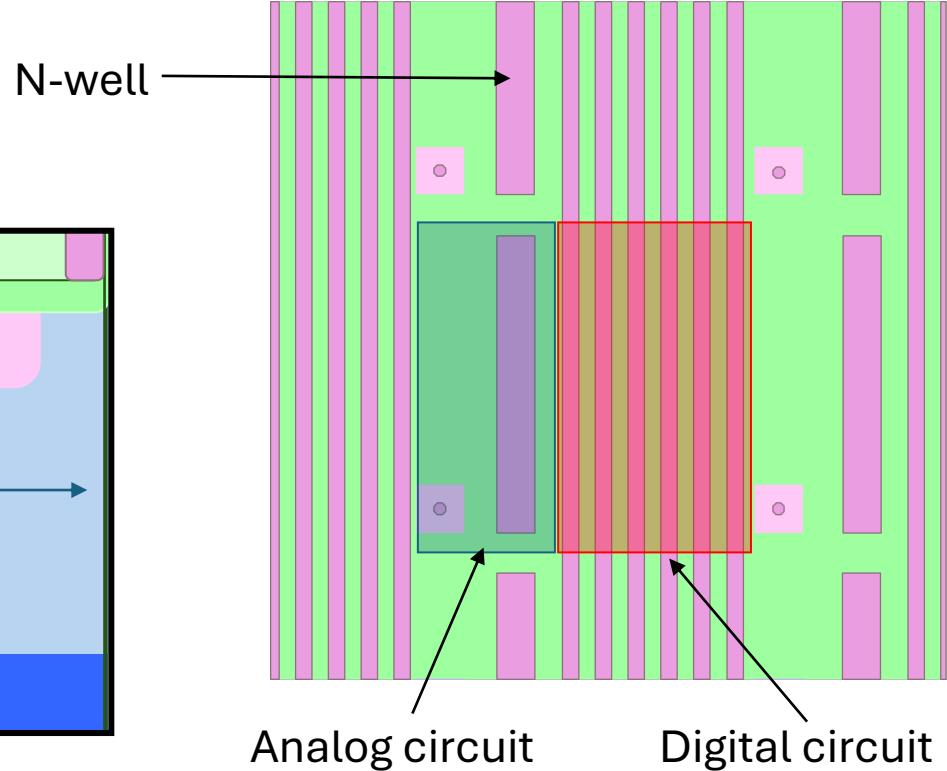
W. Snoeys, DOI:10.1016/j.nima.2017.07.046

# TCAD+MC simulation workflow

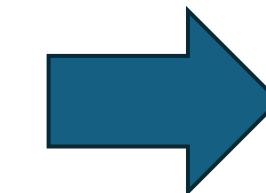
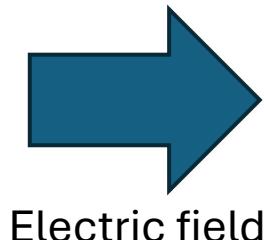
Cross section of the chip



Layout of the H2M (top view)



**Sentaurus  
TCAD**  
**SYNOPSYS**

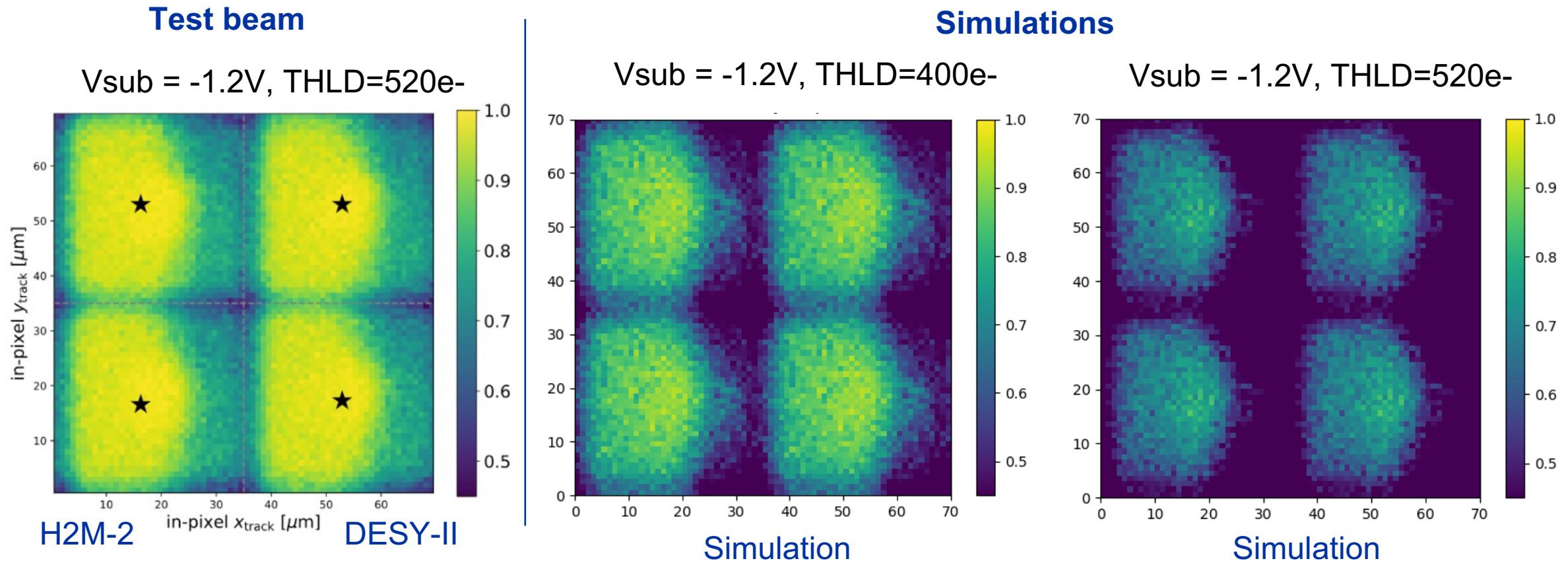


Pixel hits

Analysis

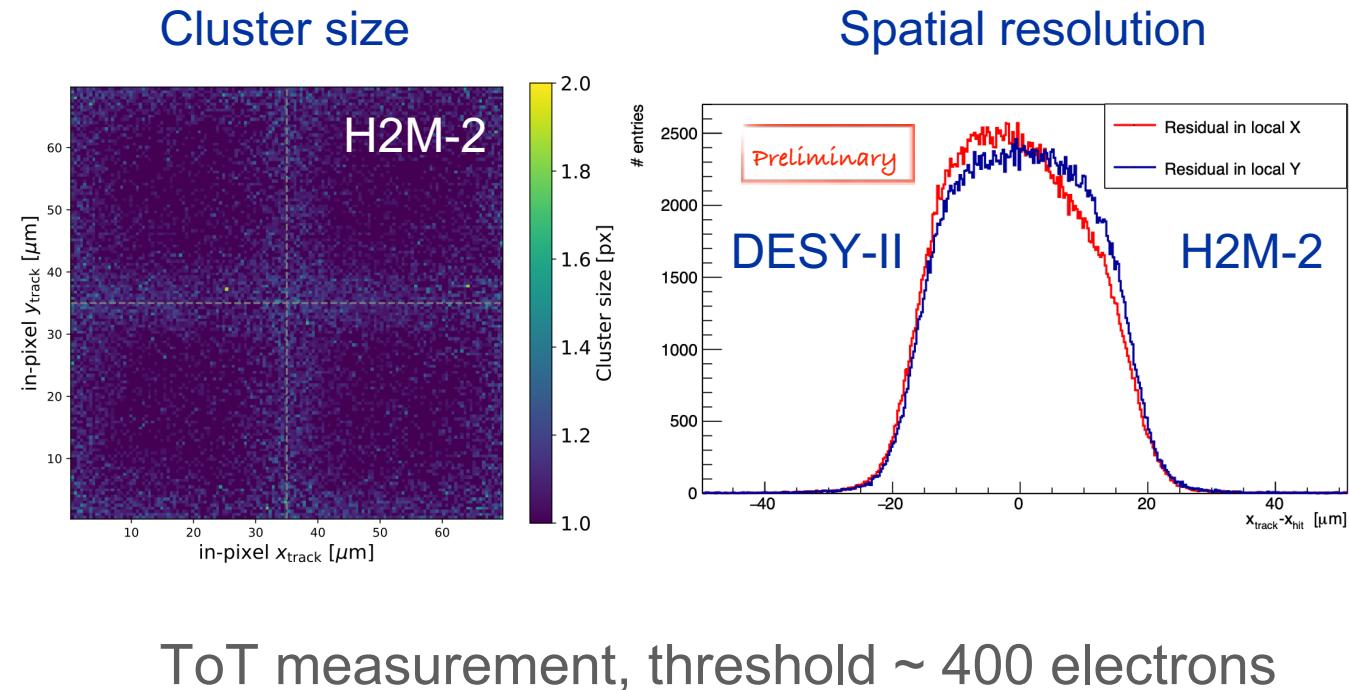
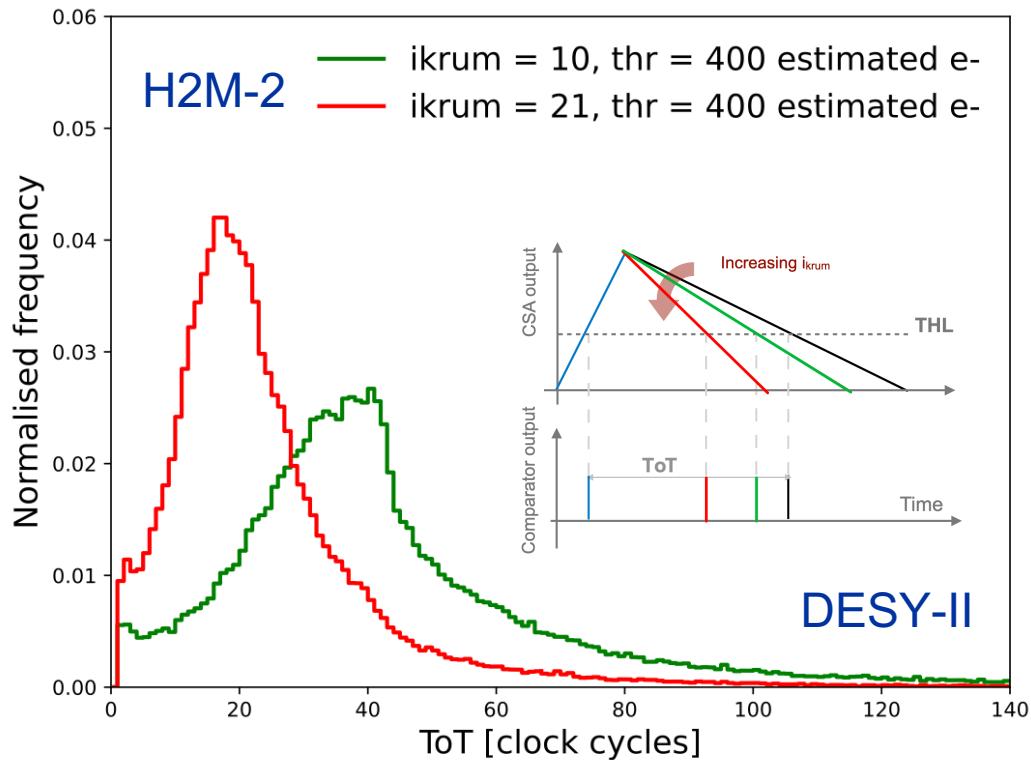
(added custom CSA model in Allpix-Squared)

# In-pixel efficiency in measurements and simulations



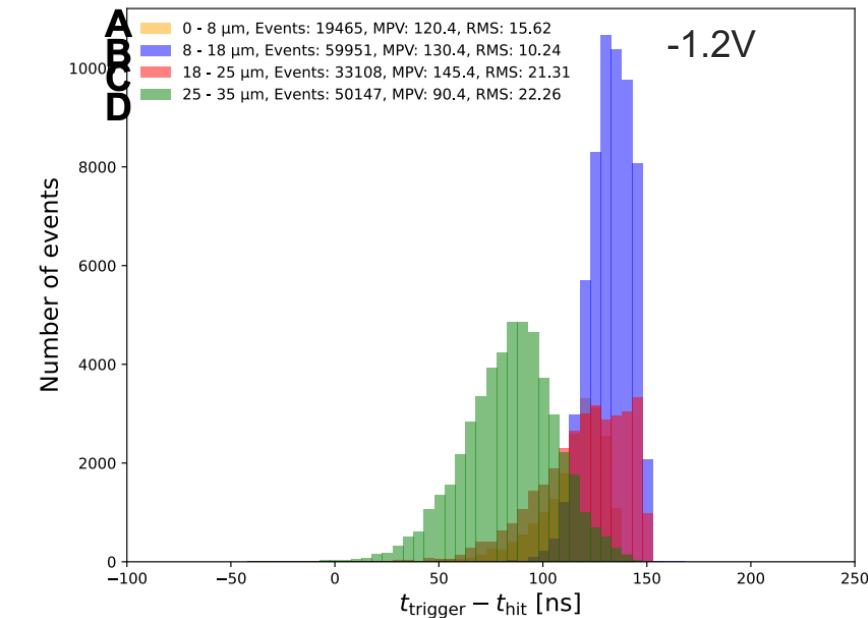
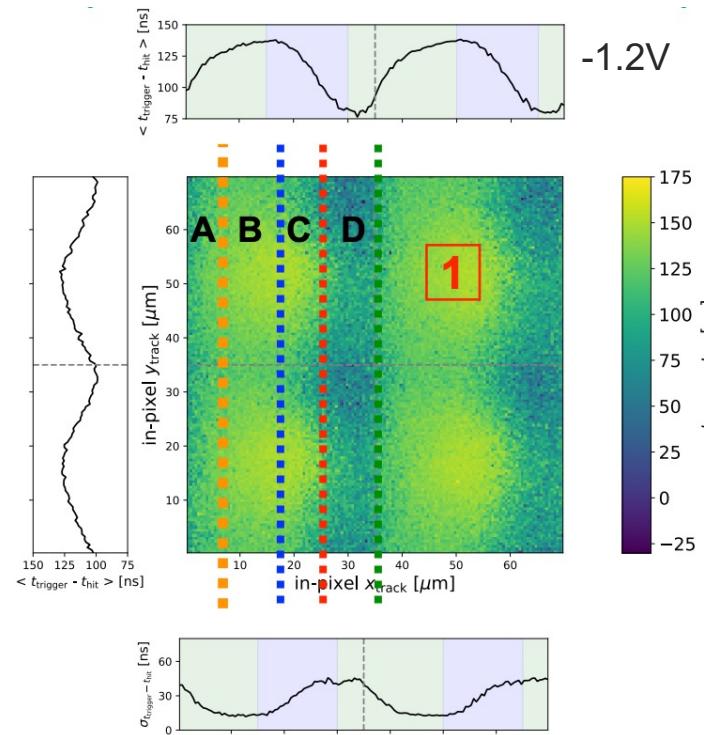
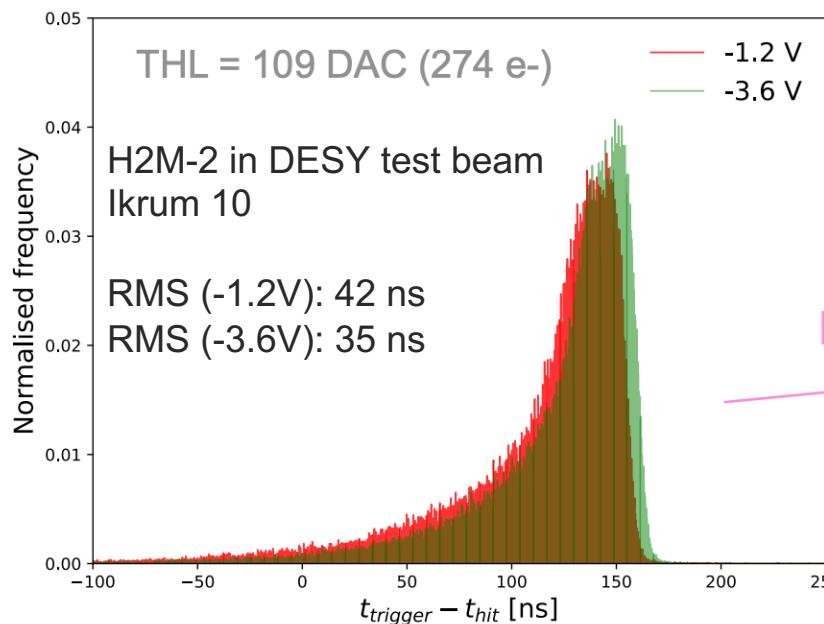
Good qualitative matching of the pattern. Current simulation predicts too low efficiency:  
quantitative matching is ongoing work.

# ToT, cluster size and spatial resolution

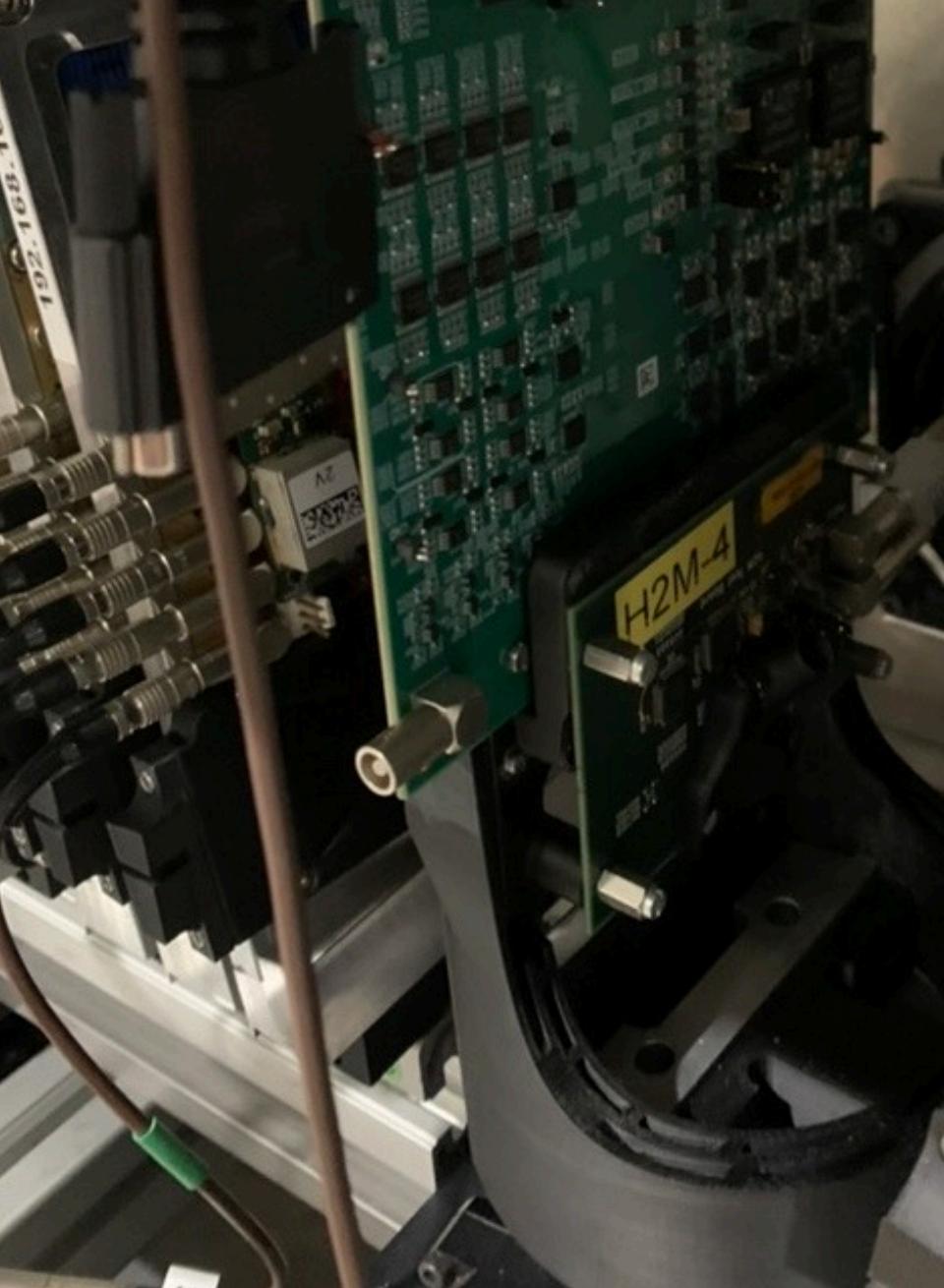


- Spatial resolution and cluster size dominated by the  $\sim 35 \mu\text{m}$  pitch and the high threshold.
- Asymmetric residuals in X due to the low-efficiency part.

# Time resolution (ToA)



- **Better timing resolution for -3.6 V than -1.2 V.**  
Due to more uniform charge-collection time across the pixel cell.
- **Strong dependency of arrival time on track impact position**  
→ timing limited by non-uniformity of charge collection



## Conclusions

### Fully functional digital-on-top monolithic sensor in 65 nm CMOS

Calibration and characterization of performance with laboratory and test beam measurements.

- Excellent performance in test beam
  - <30 e- noise, ~200 e- minimum threshold, >99.1% efficiency
  - Thinning down to ~20 microns w/o performance loss
- Impact of n-wells on charge-collection observed and qualitatively confirmed by simulations
- Timing limited by non-uniform charge collection to ~30 ns

## Outlook

- Analysis of rotation data (grazing-angle study)  
→ extract active thickness
- Further improvements/tuning of simulation
- Long-term: Follow-up project in DRD3 for 65 nm CMOS sensor targeting Higgs-Factory vertex detector  
→ smaller pixels, optimized sensor and frontend  
(<https://indi.to/vMzqK>)