Fermilab | U.S. DEPARTMENT OF ENERGY | Office of Science

Development of precision tracking detectors at Fermilab

Artur Apresyan

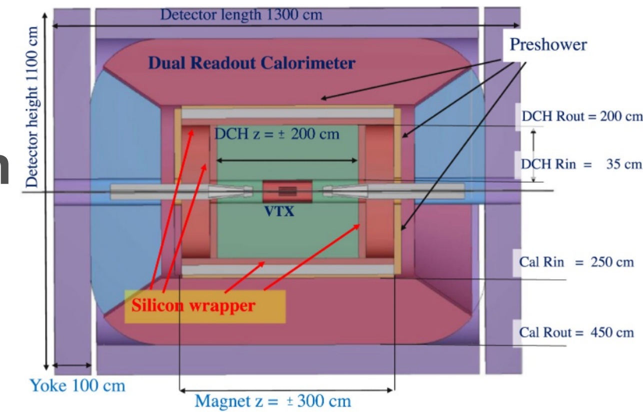
The third ECFA workshop on e^+e^- Higgs, EWK and Top Factories

9-11 October 2024

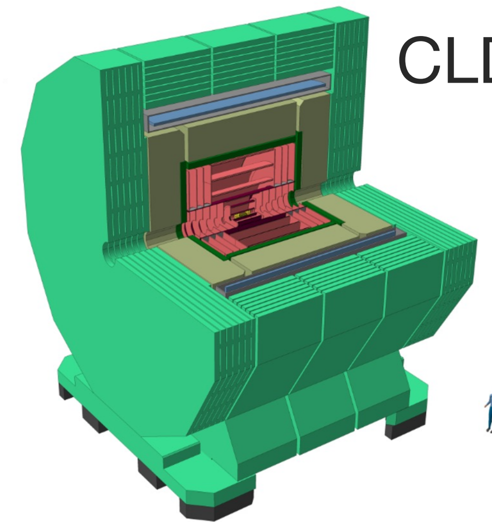
Requirements

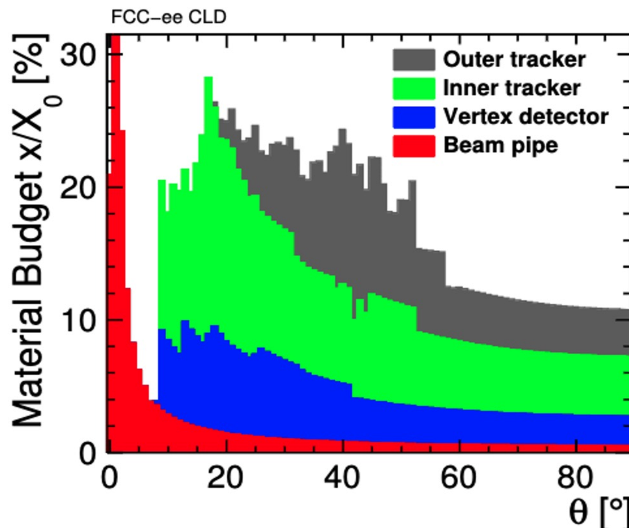
- Physics goals
  - Identify b/c quarks and tau leptons from **Higgs**
  - Perform a precise measurements of the **Z boson**
- Require a **5 μm** spatial resolution, angular resolution of **0.1 mrad**
- Very low mass budget
  - First detector layer material budget of 0.2% X_0
  - Total tracking material budget < 30% X_0
- Particle ID with time-of-flight

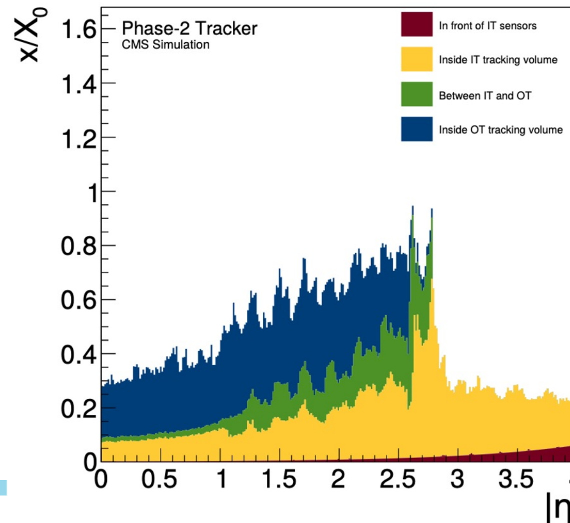
IDEA



CLD







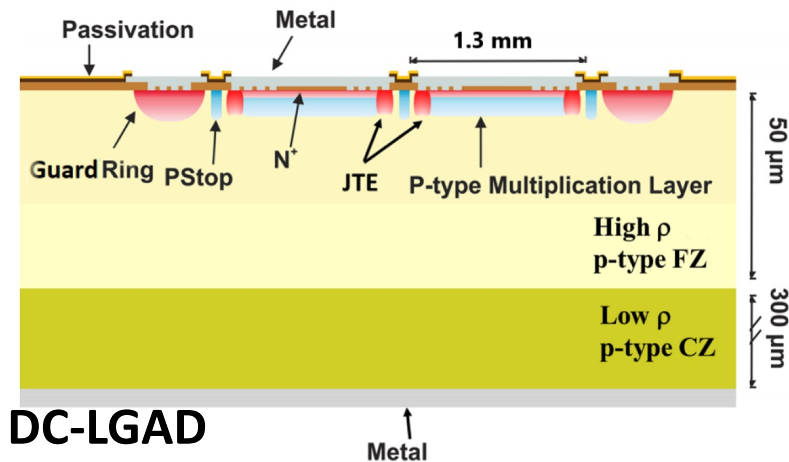
Activities in Fermilab

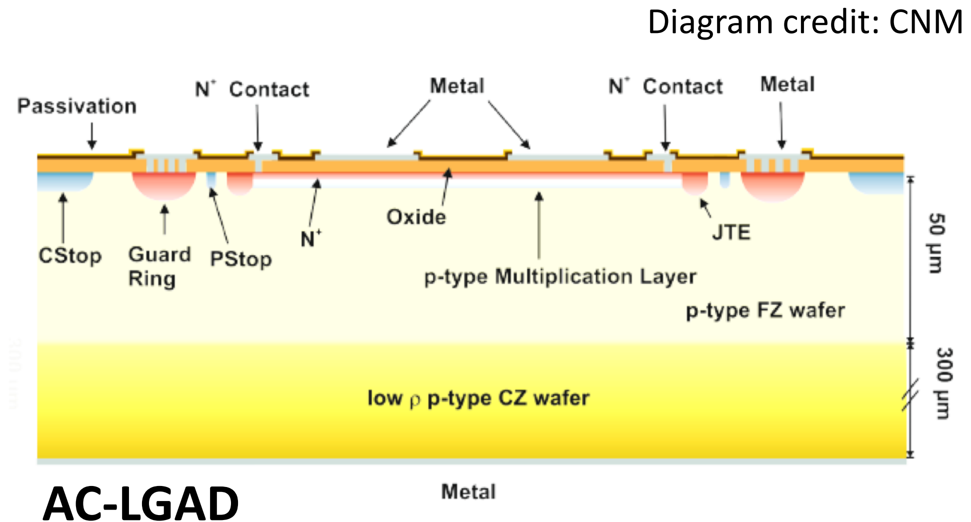
- Many active directions of R&D ongoing, some highlights:
  - Development of Low-Gain Avalanche Diode sensors and electronics
  - Monolithic Active Pixel Sensors
  - 3D-integrated sensors
  - AI-enabled pixelated sensors

AC-coupled LGADs

- **Improve 4D-trackers to achieve 100% fill factor, and high position resolution**
- Active R&D, many applications in colliders and beyond
  - 100% fill factor, and fast timing information at a per-pixel level
  - Signal is still generated by drift of multiplied holes into the substrate and AC-coupled through dielectric

Diagram credit: CNM





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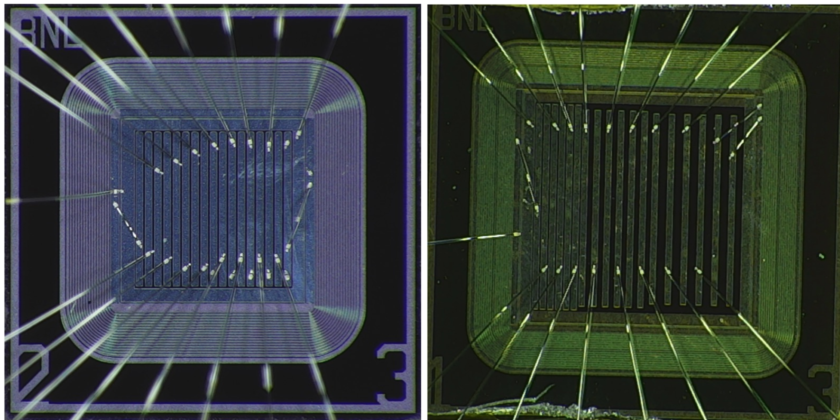
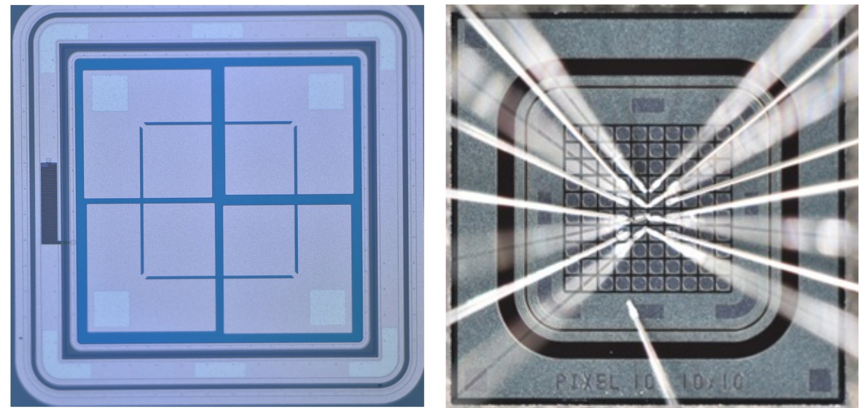
AC-LGAD sensors prototypes

- Several rounds manufactured over the last few years
  - R&D from developments for HL-LHC, synergies between HEP and NP
  - Optimize position resolution, timing resolution, fill-factor, …
- Extensive characterization and design studies
  - Optimize the geometry of readout, and sensor design for performance



BNL strip AC-LGAD

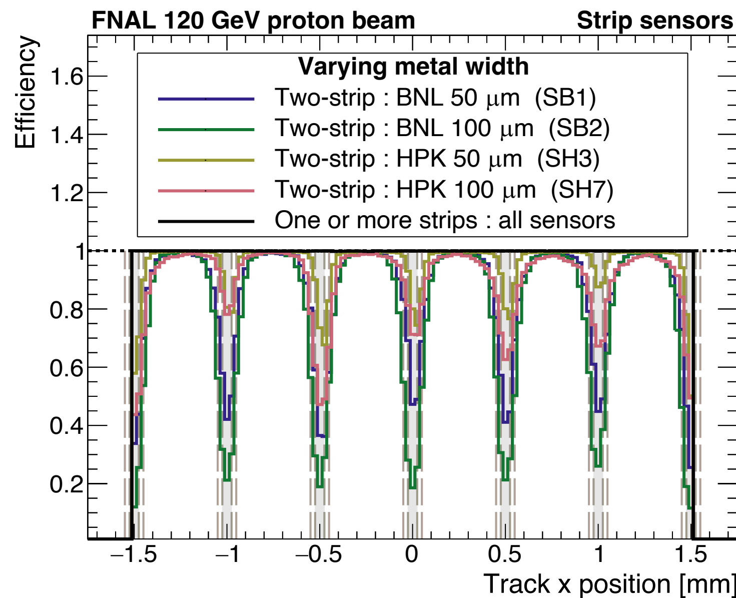


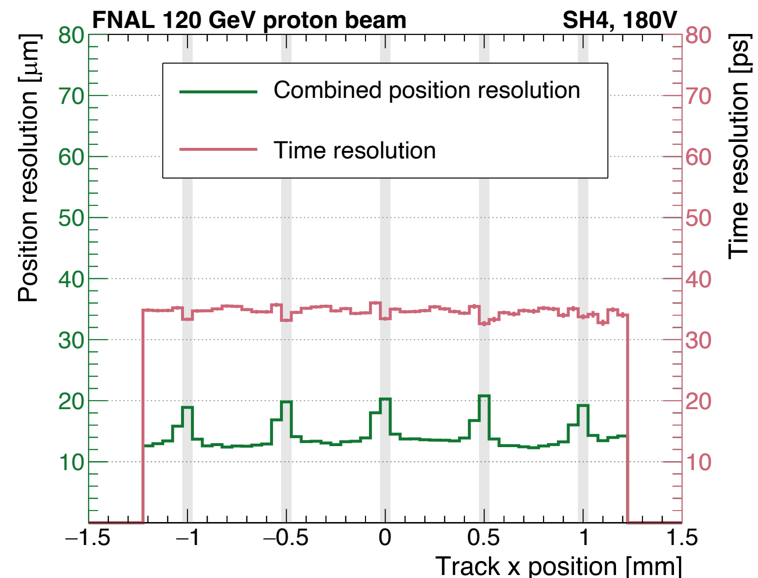
HPK pads AC-LGAD

arXiv:2407.09928

Long AC-LGAD strip sensors performance

- Position reconstruction
  - Achieve 15-20 µm resolution in 10mm strips, 500 µm pitch
- Excellent time resolution
  - Achieve 30-35 ps for 10 mm strips





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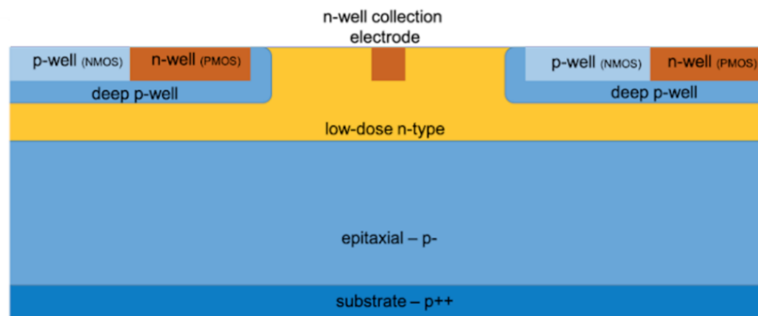
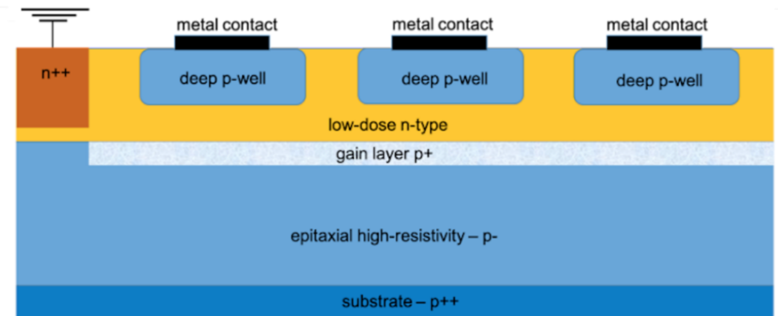
Development of monolithic AC-LGADs

- Develop MAPS sensors in a commercial process that will provide fast timing (10 ps) and precise spatial resolution (5 μm)
  - Target application 4D tracking detectors for future e^+e^- Higgs factories
- Electronics for signal processing are placed in dedicated p– and n-wells contained within a deep p-type well
  - Intrinsic gain will allow MAPS detectors to perform precise time measurements in addition to spatial measurements



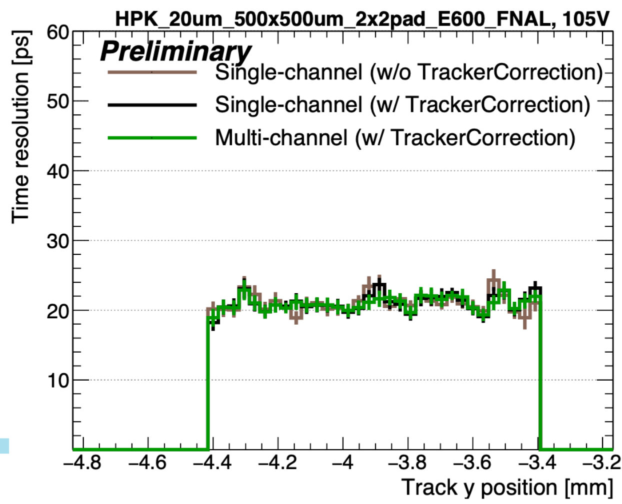
CMOS sensor

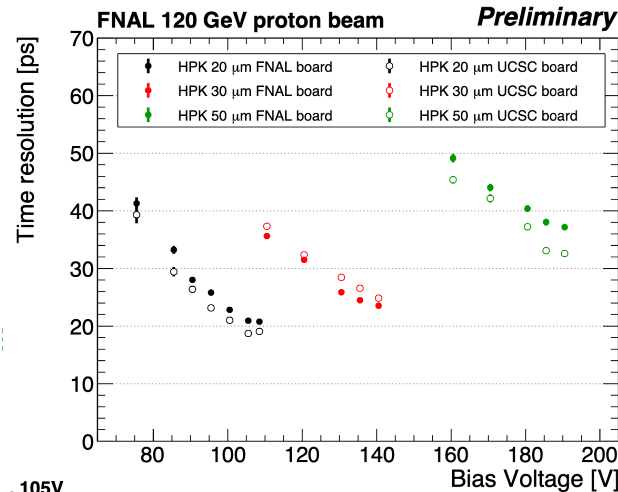


Monolithic AC-LGAD

US-Japan funded R&D

- Within this research program, the main activities of our proposal:
  - Optimize the design and geometry of AC-LGADs that will serve as the basis of the MAPS design.
  - Produce small-scale MAPS prototypes, from which the most promising architectures will be determined. Optimize the isolation of the signal collection in the sensing parts of the chip from the readout electronics.
  - Produce and characterize the full-scale prototypes

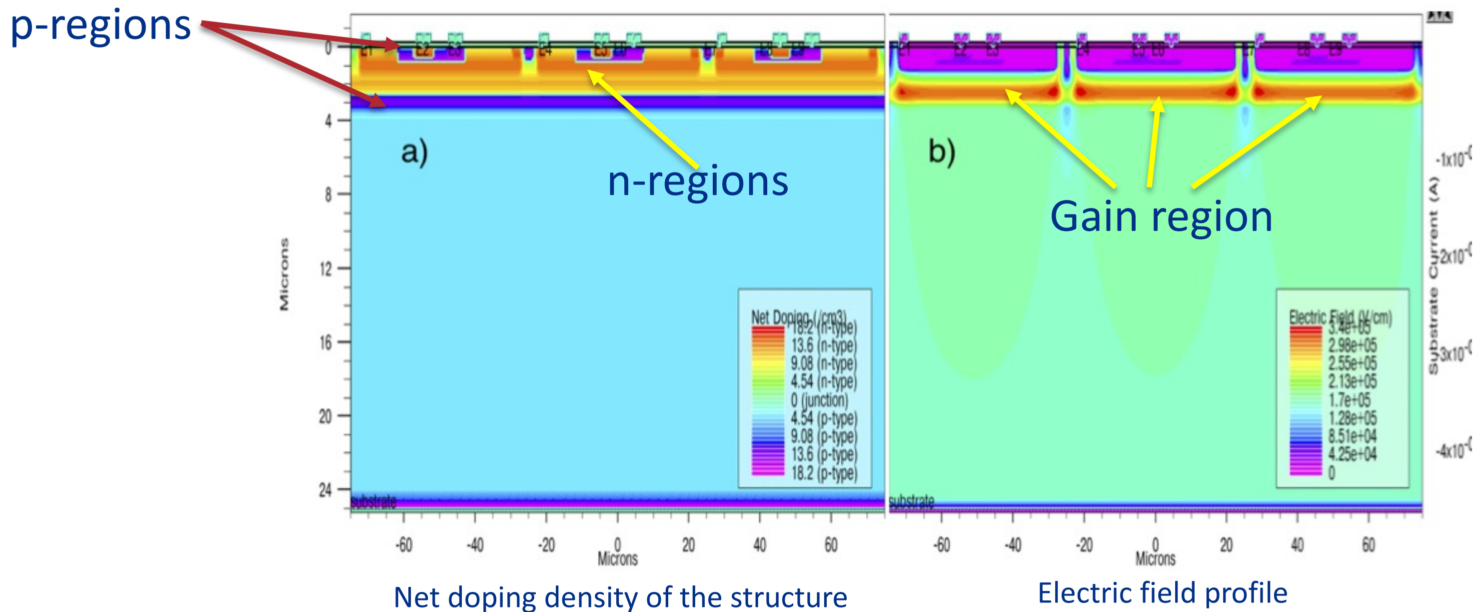




arXiv:2407.09928

Simulations

- TCAD simulations were used to establish the feasibility of the proposed work, and we started discussions with a US vendor.
  – The initial TCAD studies are based on our previous work to establish designs for 8” sensor wafer production



Net doping density of the structure

Electric field profile

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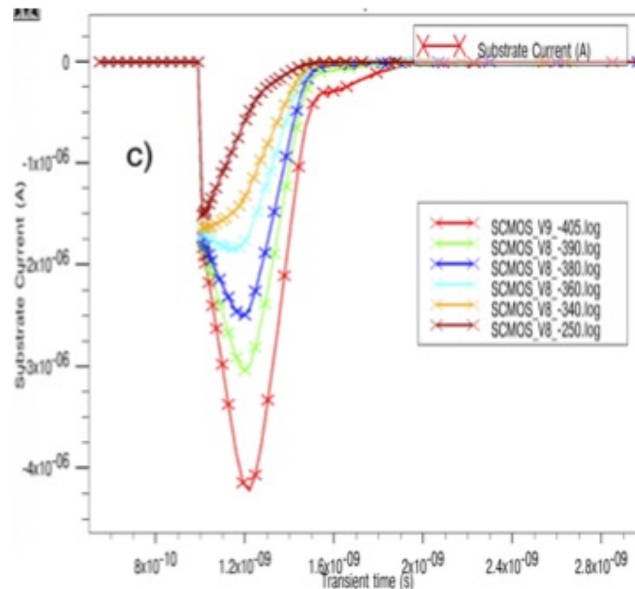


- Substrate current pulses for bias voltages from 250 (brown) to 405 (red) volts showing the onset of gain.
- Rise time of the top electrodes will be determined by the details of the CMOS well capacitance

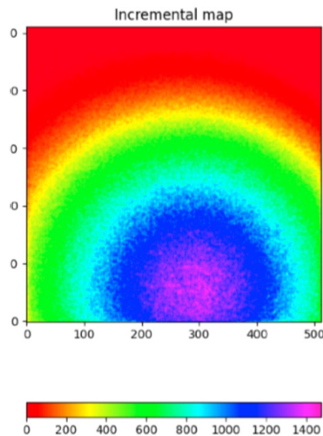
R&D program for 2024-2025

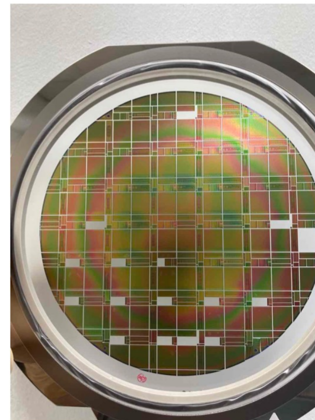
- In the coming calendar year, the goals are:
  - BNL will design and produce AC-LGAD sensors with 55x55 μm^2 and 100x100 μm^2 pixel sizes, and flip-chip to available readout
  - Fermilab will focus on ASIC design and electronics for testing
  - KEK will design and manufacture AC-LGAD sensors, and flip chipping with readout ASIC

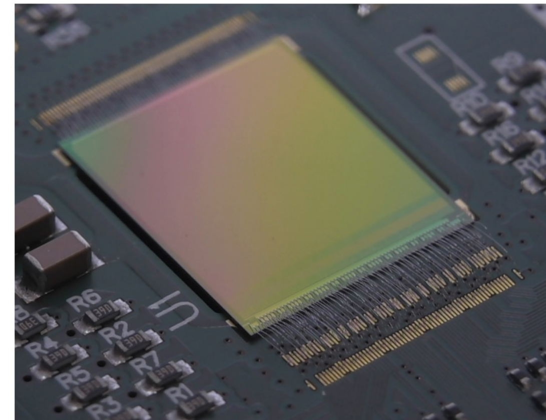
- Work with SkyWater to modify their standard epi layer
  - Adapt and optimize SkyWater process to develop particle detectors
  - Use thicker, higher-resistivity epitaxy with deep-well implants on a standard CMOS substrate

ARCADIA DMAPs sensors

- Sensor design and fabrication platform on LF11is technology
  - Full-chip FDMAPS for Future Lepton Colliders and Space Instruments
  - Scalable architecture with very low-power: 10 mW/cm^2
- Technology demonstrators
  - Main demonstrator (512 x 512 pixels) 25x25 μm^2 pixels
  - Several other demonstrators produced: pixel and strip test structures down to 10 μm pitch, small-scale demonstrator for fast timing, etc

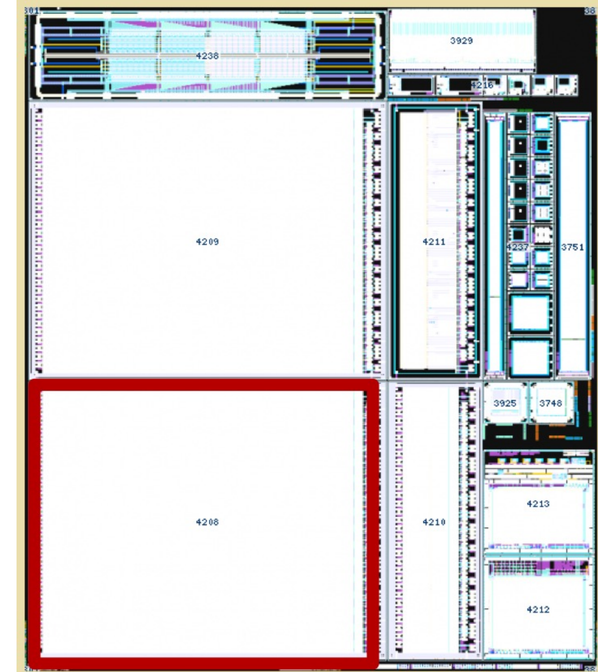


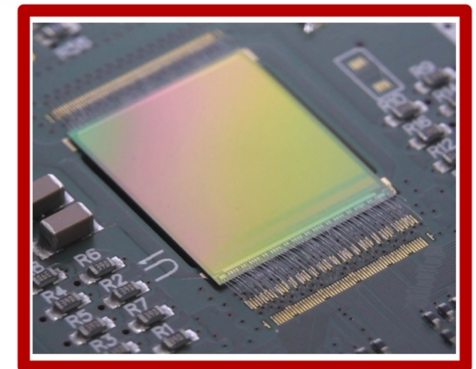




ARCADIA-MD3 Main Demonstrator

- Pixel size 25 μm x 25 μm
  - 1.28 x 1.28 cm2 silicon active area, “side-buttable”
  - Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
  - Event rate up to 100 MHz/cm^2
  - High-rate operation (16 Tx): 17-30 mW/cm^2 depending on transceiver driving strength
  - Low-power operation (1 Tx): 10 mW/cm^2 (all data conveyed in 1 transceiver, others turned-off)

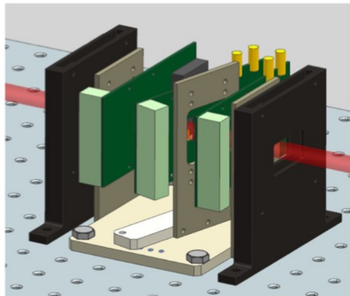


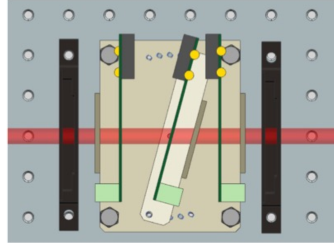


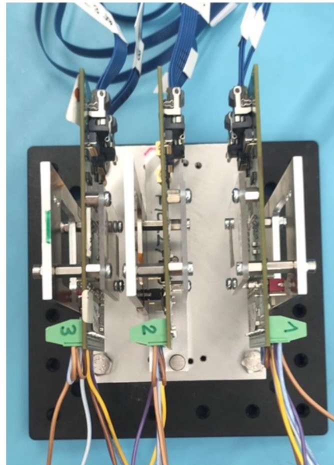
Manuel Rolo [INFN]

Test beam with ARCADIA-MD3

- Test beam at FNAL (120 GeV protons) in Summer 2024
  - Mini-telescope with 3 ARCADIA-MD3 sensors
  - Threshold, sensor HV and incidence angle parametrization: study of cluster size, collection efficiency, spatial resolution

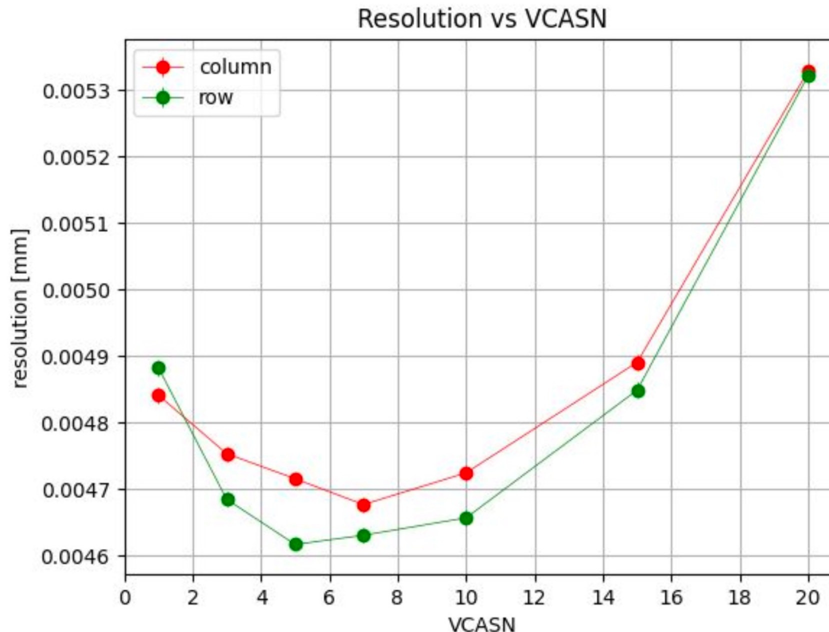


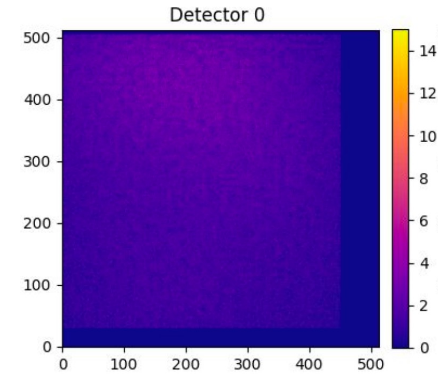


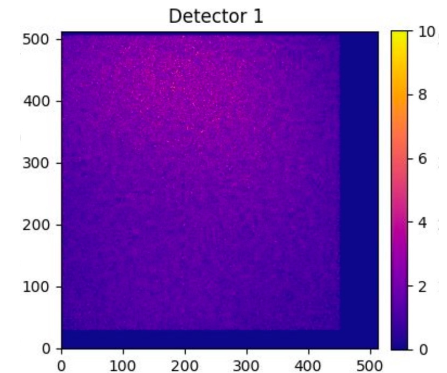


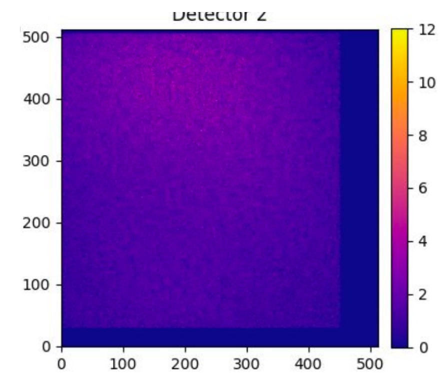
Characterization of ARCADIA-MD3

- Excellent performance demonstrated in test-beam
  - Position resolution around 5 µm
- Efficiency near 100%
- Detailed measurements are now continuing with laser









Three layers of the ARCADIA telescope in the beam

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ARCADIA
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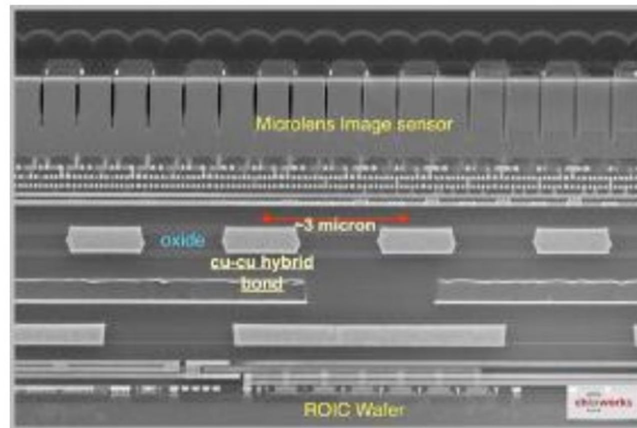
3D-integrated sensors project

- Development of low-power, highly granular detectors in ($\vec{x}$, t)
  - Required to achieve breakthroughs across HEP, NP, BES, and FES
  - Adoption of 3D-integration has been cost-prohibitive in academia
- Supported by DOE “Accelerated Innovation in Emerging Technologies”
  - Joint development effort of SLAC, FNAL and LLNL teams
  - Partner with industry leaders to implement new technologies
  - Design goal is to achieve position resolution ~5 µm, timing ~ 5-10 ps



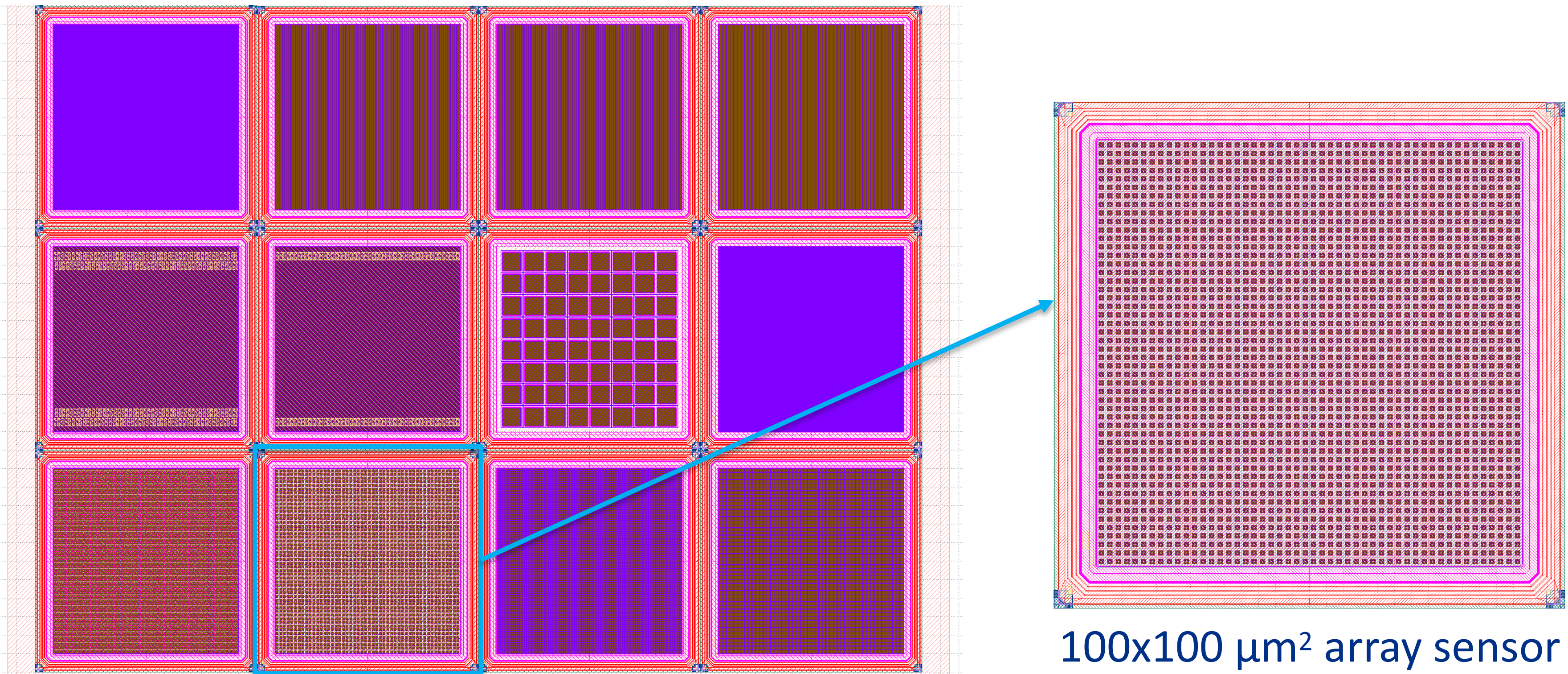
Section of the Sony Exmor camera chip showing the hybrid bond interface

Technical approach

- The research program consists of three main thrusts towards developing the proposed detector:
  - **Thrust 1:** *Design and manufacture Low-Gain Avalanche Diodes (LGADs) devices compatible with 12'' foundry processes*
  - **Thrust 2:** *Design application specific integrated circuit (ASIC) techniques to meet various application needs for granularity, precision timing, and power*.
  - **Thrust 3:** *Enable a new generation of particle detectors that utilize 3D-integration, combining state-of-the-art 12" wafers from different foundries*.

Development of sensors

- In partnership with Tower Semiconductor
  - Full wafer run on 12” process, using their 65 nm process
  - Layout Variations: pixels vs. strips



Sensor designs on the reticule

100x100 μm^2 array sensor

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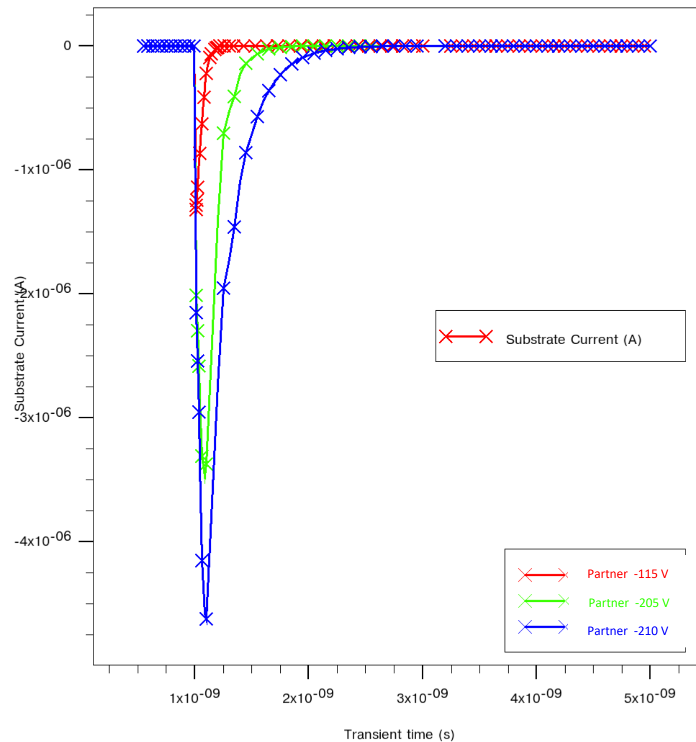
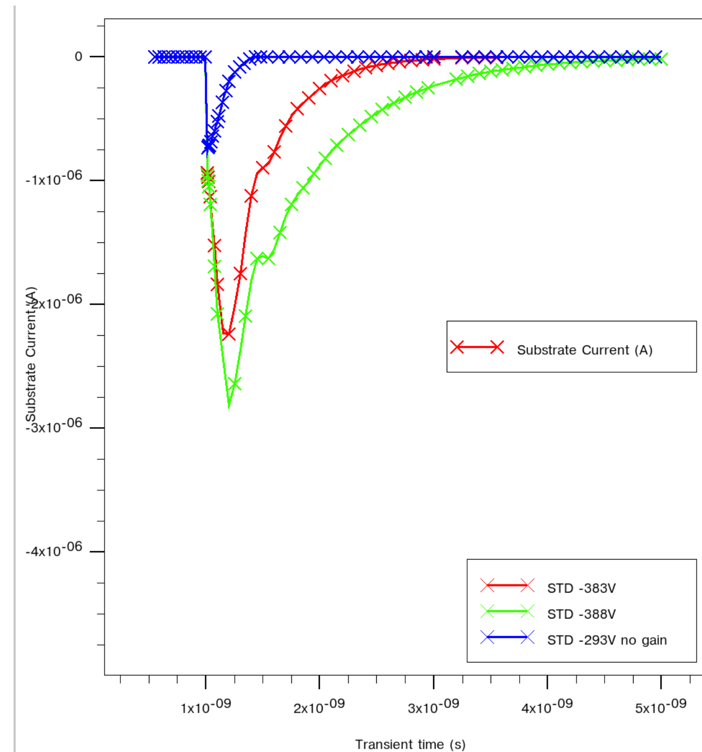
Pulse simulations





- Simulations of a “standard” LGAD and Tower’s process.
  - ”Standard” process - 20 µm thick high resistivity
  - “Tower” process - 10 µm thick, moderate resistivity
- Signals from Tower process are narrower and faster rise time

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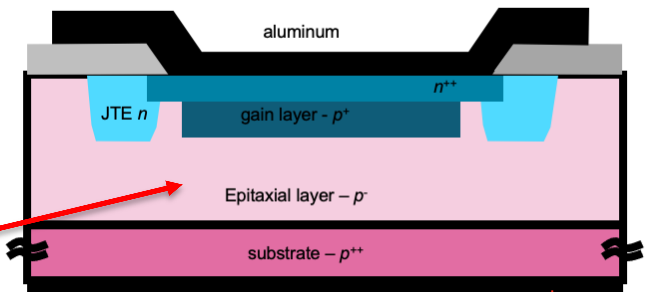
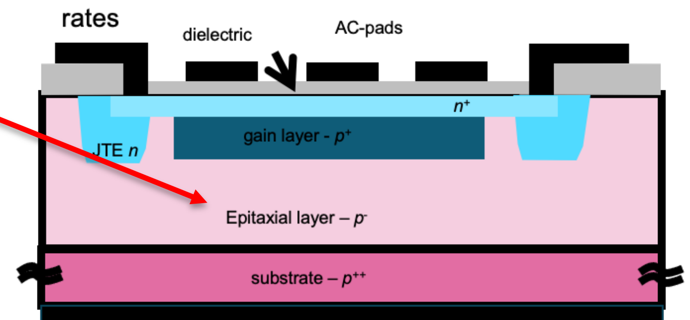
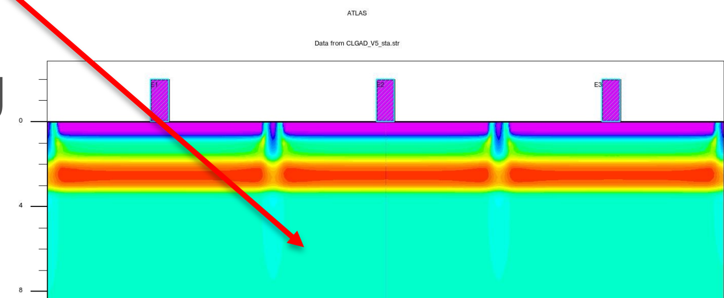
Additional processing

- The basic functionality of the device looks good with 10 µm epitaxy.
- Structures to be produced:
  - DC LGAD: ”standard” devices
  - AC LGAD: 100% fill factor, good position resolution
  - Deep junction LGAD: for higher radiation hardness
- Design status:
  - Device simulations and layout ongoing
  - Fabrication run at Tower Semiconductor expected to start before the end of the year



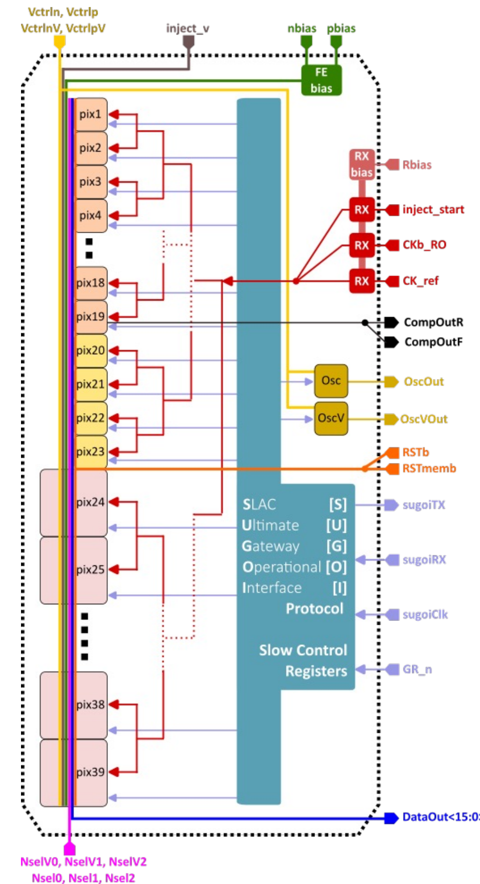


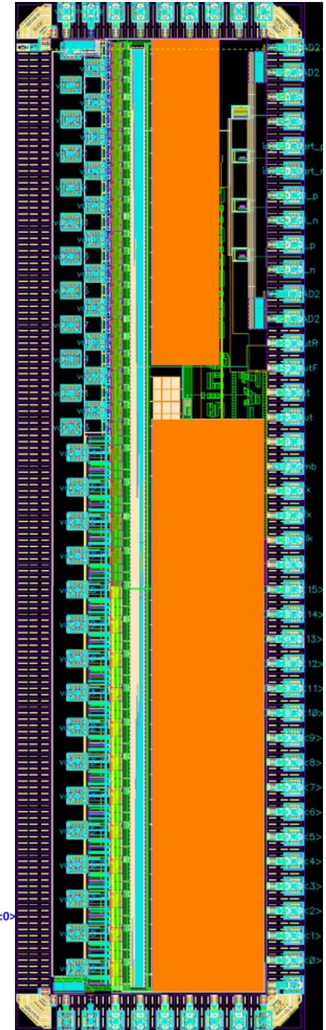


Readout ASIC Design

- The first 28nm readout ASIC prototype ($1x3\ mm^2$) submitted to TCMS in August
  - Linear pixel array: two variants of 50μm and one variant of 100μm size pixels
  - Main goals are to test the main ingredients to implement in the full chip
- During the next year, we will tape-out another MPW run ($5x6\ mm^2$)
  - Main priority is a 50x50 μm^2 pixels, but can be bump-bonded also to larger pitch
- For the next project phase, we would proceed to wafer-to-wafer bonding of 12” LGAD and 12” 28nm ASIC wafers.

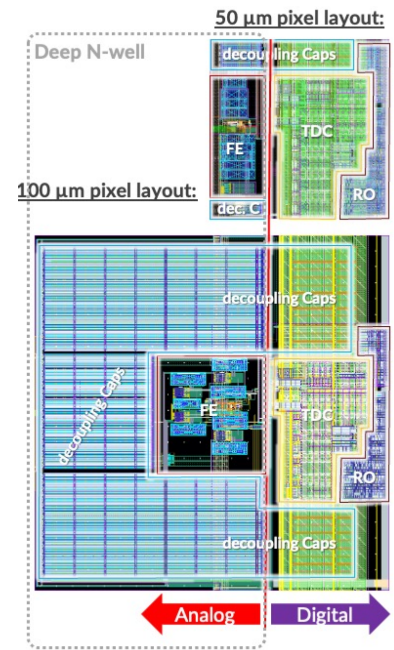
First readout ASIC prototype: block schematic and layout

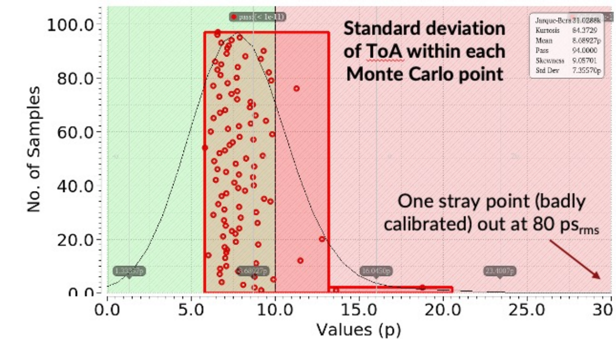


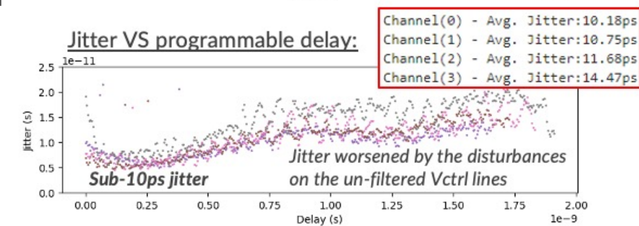


Readout ASIC Design

- Analog frontend in deep n-well shared between column pixels
  - Analog section is about 40% of the 50 μm pixel area
  - Minimum input charge: 1.3 fC
  - Time of Arrival (ToA) Jitter: 10 ps RMS
- Digital section includes:
  - TDC performing both TOA and TOT measurements
    - 2D Vernier Architecture: time resolution 6.25 ps
    - Implementation based on silicon demonstrated design
    - Overall good performance: few issues observed that are well understood and will be fixed in the next round
  - Readout logic:
    - Sparsified readout; SLAC's SUGOI protocol for ASIC slow-control configuration;

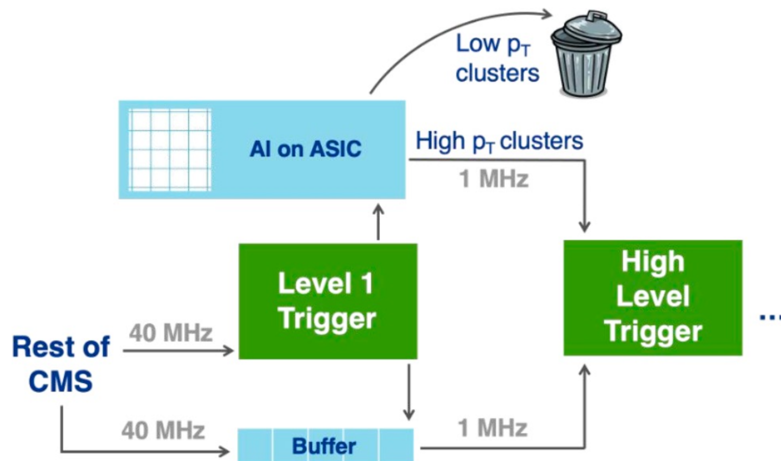






Smart Pixels project

- AI embedded on a chip to:
  - Filter data at the source for data reduction
- Data reduction through
  - Filtering through removing low p_T clusters
  - Featurization through converting raw data to physics information
- Customizable (reprogrammable weights) neural networks implemented directly in the front-end



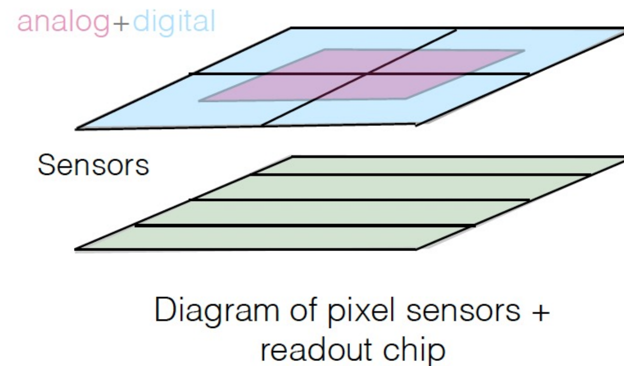
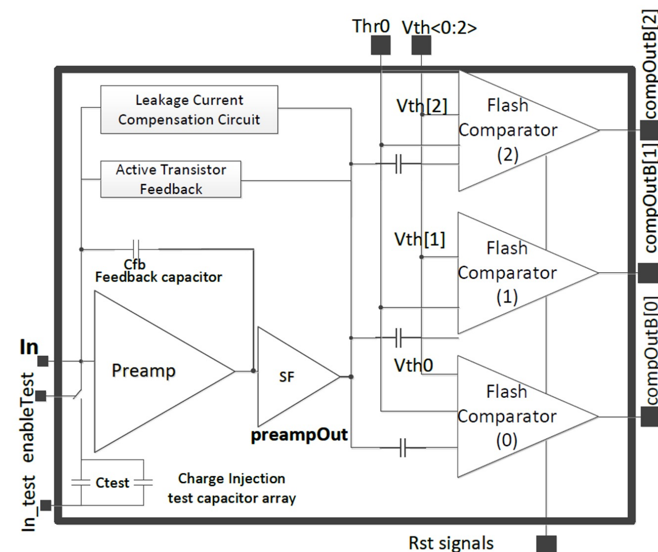
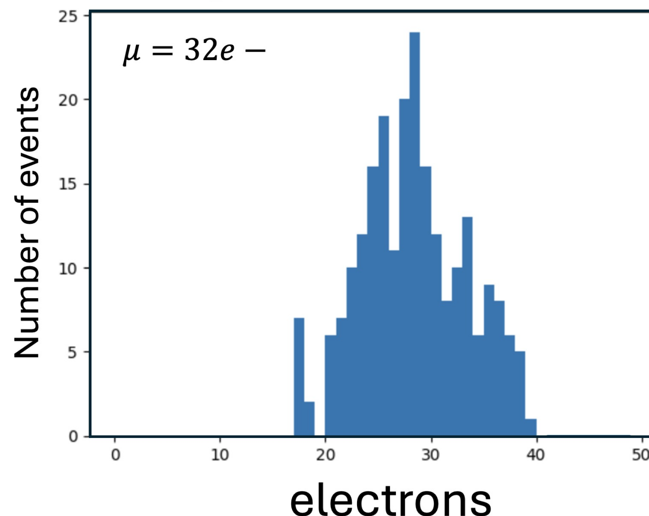
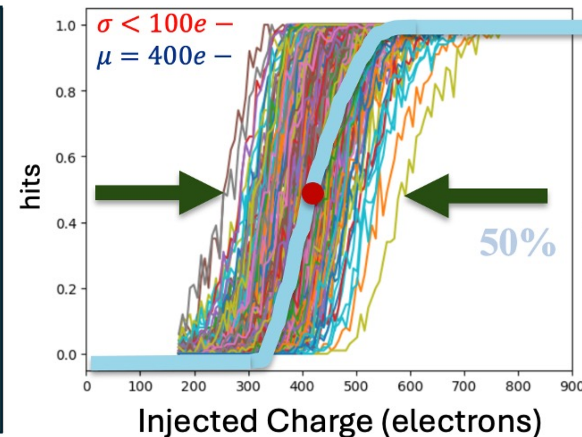


Diagram of pixel sensors + readout chip

Analog frontend prototype

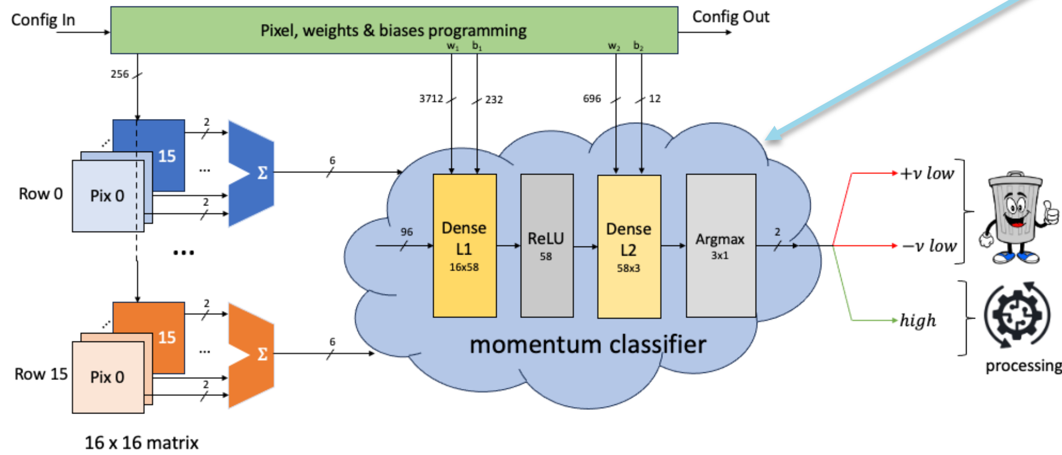


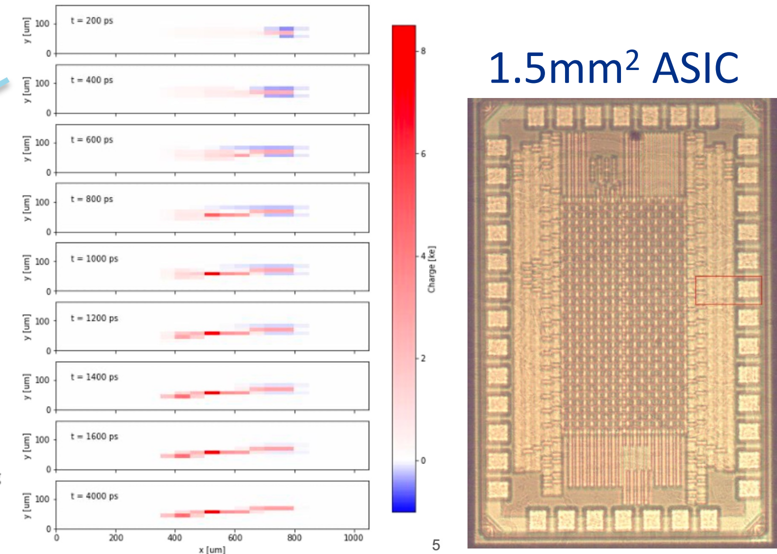




- The AFE prototype designed in HPC+ 28nm
  - ROIC pixel size is 25 μm^2
  - Low power performance : ~5µW/pixel
- Preamplifier dynamic range 64 aC – 2.1 fC
  - Equivalent noise charge (ENC) 31e⁻ with 400e⁻ threshold (no sensor cap)
  - Total charge dispersion < 100e⁻ across entire matrix with 400e⁻ threshold (no sensor cap)

AI/ML Implementation





- Use AI/ML due to complicated pulse shapes, and drift & induced currents
  - y-profile is sensitive particle's p_T, x-profile uncorrelated with p_T
- Co-Design development with analog frontend pixels connected to a fully combinatorial digital classifier
  - Combinatorial design reduces dynamic power
  - Digital power estimated to be 300 µW for 256 pixels: ~1 µW/pixel
- Total power density (AFE + digital) < 1 W/cm^2

Summary

- Many exciting R&D areas that promise to enable and enrich the physics potential of the FCC-ee experiments
  - New, disruptive technologies are emerging

- Collaborative efforts are a key for the progress in many challenging directions
  - Integration with the ongoing international efforts within DRD and RDC efforts are crucial!