CMOS R&D targeting a vertex detector for Higgs factories

On behalf of IPHC-Strasbourg teams and collaborators

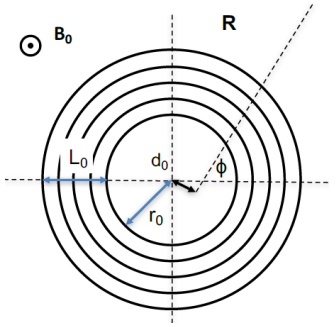
- Large size sensor: MIMOSIS program
- CMOS sensor R&D in TPSCo 65 nm technology
- Strategy toward a vertex detector for FCCee

- Not covered here but contributions from IPHC: OBELIX for Belle-2 upgrade, MOSAIX for ALICE-ITS-3

FCCee VTX requirements

FCCee
$\sigma_{d_0} = a \oplus \frac{b}{p \sin^{3/2}\theta}$
$a \simeq 5\,\mu m; \quad b \simeq 15\,\mu m\,GeV$

$b \sim r_0\sqrt{material}$
$a \sim \sqrt{r_0}$



$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0 \sin\theta}}\sqrt{1+\frac{1}{2}\left(\frac{r_0}{L_0}\right)+\frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$

d = layer thickness, N = # layers

Drasal, Riegler, https://doi.org/10.1016/j.nima.2018.08.078

Spatial resolution per layer	$\simeq 3$	μm
Pixel pitch	14-20	μm [1]
read-out time	$\simeq 500$	ns [2]
Power dissipation	$\simeq 20-50$	mW/cm^2
Sensor thickness	$40-50$	μm [3]
Safety factor on particle rate	3	[4]
Maximum Hit rate	75 / 25	MHz/cm^2 [5]
Maximum Hit rate	22.5×10^{-3} / 7.5×10^{-3}	$hits/mm^2/BX$ [5]
Assumed cluster multiplicity	5	
Fired pixel rate	375 / 125	MHz/cm^2 [5]
Fired pixel rate	0.33 / 0.11	$fired\ pixels/mm^2/BX$ [5]
Occupancy/pixel/read-out	3.45×10^{-3} / 1.15×10^{-3}	$/pixel/readout$ [5]
Ionising radiation (1^{st} layer)	30 / 10	$MRad/year$ [5 6]
Corresponding Fluence	$\simeq 1.8\times10^{14}$ / 6×10^{13}	$n_{eq(1\ MeV)}/year$ [5 7]

[1] Depending on charge sharing/encoding
[2] Compromise between power dissipation and pile-up at $\sqrt{s} = 91\ GeV$
[3] To allow bending
[4] due to beam background uncertainties estimates
[5] With / without safety factor
[6] assuming beam running 180 days/year, and average incident angle of $\simeq 70^o$.
[7] assuming NIEL factor of 5×10^{-2}

	thickness (mm)	Mat. Budget (X/X_0 %)
Beam pipe[1]		
Au	0.005	0.16%
AlBeMet162[2]	0.35	0.14%
Paraffin	1.0	0.18%
AlBeMet162[2]	0.35	0.14%
Total beam pipe	1.705	0.61%
Single layer		
Silicon sensor	0.050	0.05%
Cables, flex and support		$\simeq 0.10\%$
Material per layer		$\simeq 0.15\%$

[1] described in [6]
[2] 62% Be and 38% Al alloy

[6] A. Novokhatski et al. Estimated heat load and proposed cooling system in the FCC-ee Interaction region beam pipe. In *Proc. IPAC'23*, number 14 in International Particle Accelerator Conference, pages 260–263. JACoW Publishing, Geneva, Switzerland, 2023.

- Data flux
  - ✓ Continuous beam ⇒ Data flux significantly higher than ILC,
  - ✓ Higher radiations doses as well, for both ionising radiation and fluence.
- Beam pipe
  - ✓ Cooling mandatory as well as shielding,
  - ✓ Compensated by small inner radius ~12 mm
- Challenge:
  - ✓ How to reach the targeted resolution with an adapted read-out architecture while fulfilling all the other requirements ?
  - ✓ How to propose a robust but ambitious VTX concept ?
  - ✓ Spoiler:
    - Not easy

MIMOSIS program

MIMOSIS Sensor

Supported by Bundesministerium für Bildung und Forschung (05P19RFFC1)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871072

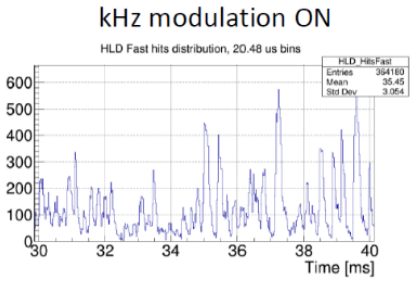
- MIMOSIS sensor for CBM-MVD @ FAIR
  - ✓ Based on ALPIDE architecture
    - Multiple data concentration steps
    - Elastic output buffer
    - 8 x 320 Mbps links (switchable)
    - Triple redundant electronics
  - ✓ A milestone for Higgs factories
    - « 5 µm / ≤5 µs » + enhanced bandwidth
    - Improve radiation hardness

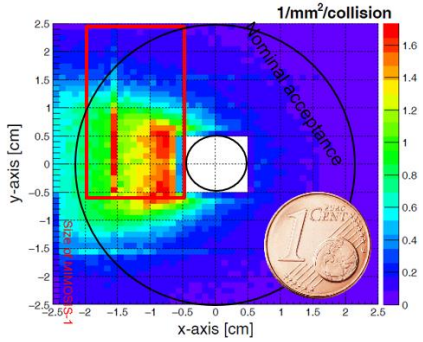
Physics parameter	Requirements
Spatial resolution	~ 5 um
Time resolution	~ 5 us
Material budget	0.05% X_0
Power consumption	< 100 – 200 mW/cm^2
Operation temperature	- 40 °C to 30 °C
Temp gradient on sensor	< 5K
Radiation tol* (non-ion)	~ 7 x 10^{13} n_{eq}/cm^2
Radiation tol* (ionizing)	~ 5 MRad
Data flow (peak hit rate)	@ 7 x 10^5 / (mm^{2}s) > 2 Gbit/s

J. Andary,[a] B. Arnoldi-Meadows,[a] O. Artz,[a] J. Baudot,[b] G. Bertolone,[b] A. Besson,[b] N. Bialas,[a] R. Bugiel,[b] G. Claus,[b] C. Colledani,[b] H. Darwish,[a,b] M. Deveaux,[c] A. Dorokhov,[b] G. Dozière,[b] Z. El Bitar,[b] I. Fröhlich,[a,c] M. Goffe,[b] F. Hebermehl,[a] A. Himmi,[b] C. Hu-Guo,[b] K. Jaaskelainen,[b] O. Keller,[f] M. Koziel,[a] F. Matejcek,[a] J. Michel,[a] F. Morel,[b] C. Müntz,[a] H. Pham,[b] C.J. Schmidt,[c] S. Schreiber,[a] M. Specht,[b] D. Spicker,[a] J. Stroth,[a,c,d] I. Valin,[b] R. Weirich,[a] Y. Zhao[b] and M. Winter[e]

[a] *Goethe-Universität Frankfurt, Germany*
[b] *Université de Strasbourg, CNRS, IPHC UMR 7178, Strasbourg, France*
[c] *GSI Helmholtzzentrum für Schwerionenforschung GmbH, Germany*
[d] *Helmholtz Forschungsakademie Hessen für FAIR, Germany*
[e] *IICLab, UMR9012 – CNRS / Université Paris-Saclay / France*
[f] *Facility for Antiproton and Ion Research in Europe GmbH, Germany*

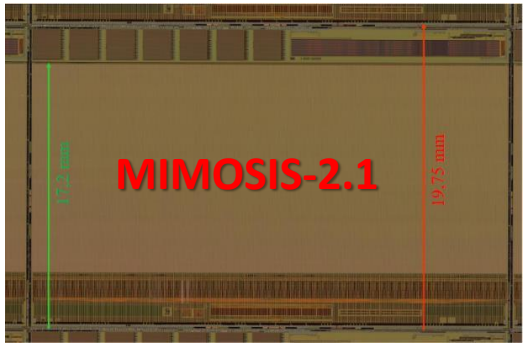
Ali Murteza ALTINGUN





Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	~ 25 µm
Epi layer resistivity	> 1kΩcm
Sensor thickness	60 µm
Pixel size	26.88 µm × 30.24 µm
Matrix size	1024 × 504 (516096 pix)
Matrix area	≈ 4.2 cm^2
Matrix readout time	5 µs (event driven)
Power consumption	40-70 mW/cm^2

Requirements already achieved with MIMOSIS-1



MIMOSIS-0 (2018)
- Demonstrate pixel concept.
- Demonstrate zero suppression.
- Demonstrate readout concept.

MIMOSIS-1 (2020)
- Full dimension sensor
- Add buffer structure.
- SEE hardening 1/2

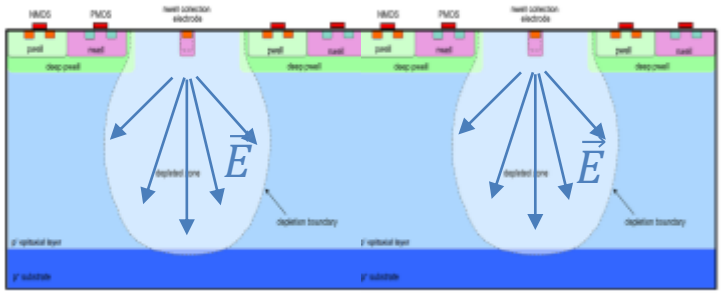
MIMOSIS-2 (Q2/2023) Major issues
- On-chip pixel grouping.
- Final pixels.
- SEE hardening 2/2
- MIMOSIS-2.1

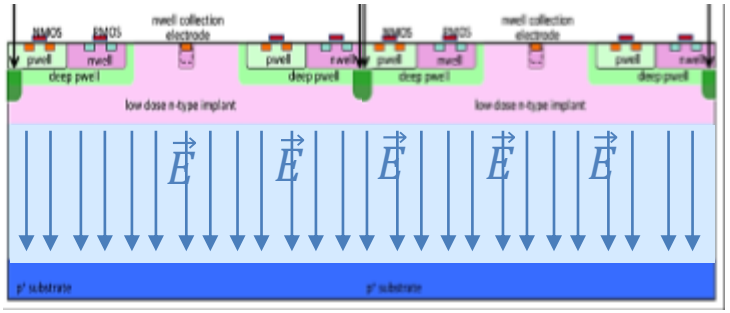
MIMOSIS-2.1 (Q4 2023)
- = M-2 corrected
- Delivered May 2024
- Tested in beam in July-September 2024

MIMOSIS-3
- Final sensor for mass production
- Submission in 2025

MIMOSIS (CBM-MVD) & options for sensing elements

Process modification: Standard? P-stop? N-Gap?





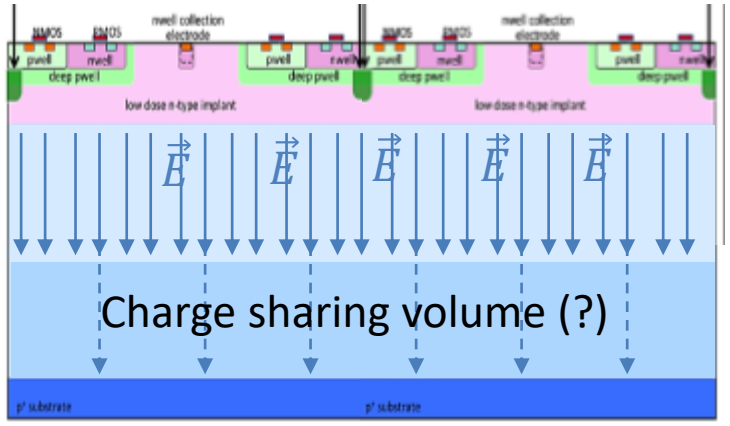
25 or 50 µm epi?

$\sigma = 4 - 5$ µm
> 3 x $10^{13} n_{eq}/cm^2$

Spatial resolution
Rad. hardness

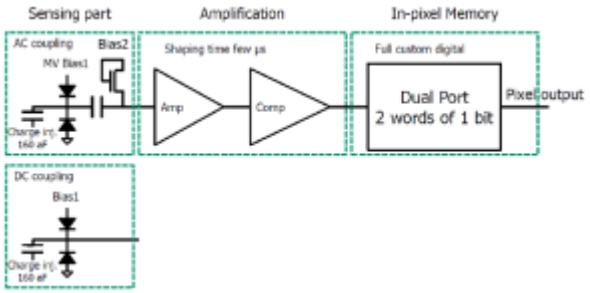
$\sigma = 5 - 7$ µm
> 30 x $10^{13} n_{eq}/cm^2$

Process options inherited from ALPIDE



- Better spatial res. at given rad. tolerance?
- Higher S/N => Robustness to external noise?
- Nuclear fragment ID by dE/dx?

AC? DC? pixel

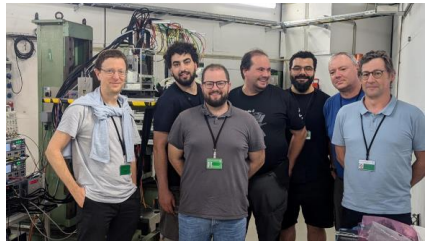


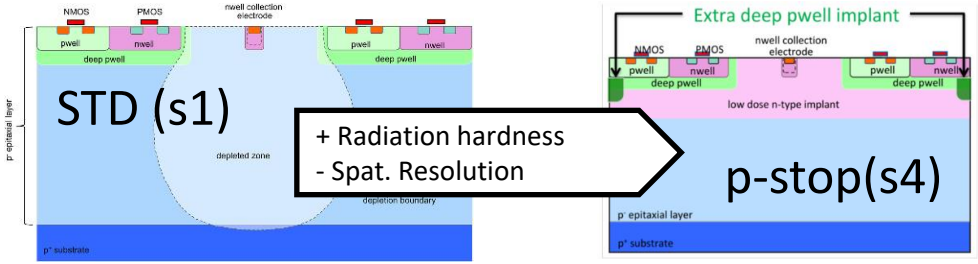
- DC pixel – limited rad. hardness.
- AC Pixel – more biasing lines.

W. Snoeys et al., NIM-A Vol.871 (2017) 90–96.
Munker, Vertex 2018, Status of silicon detector R&D at CLIC

DESY & CERN test beam

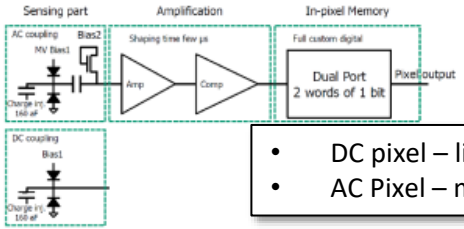
MIMOSIS-2.1: excellent performances





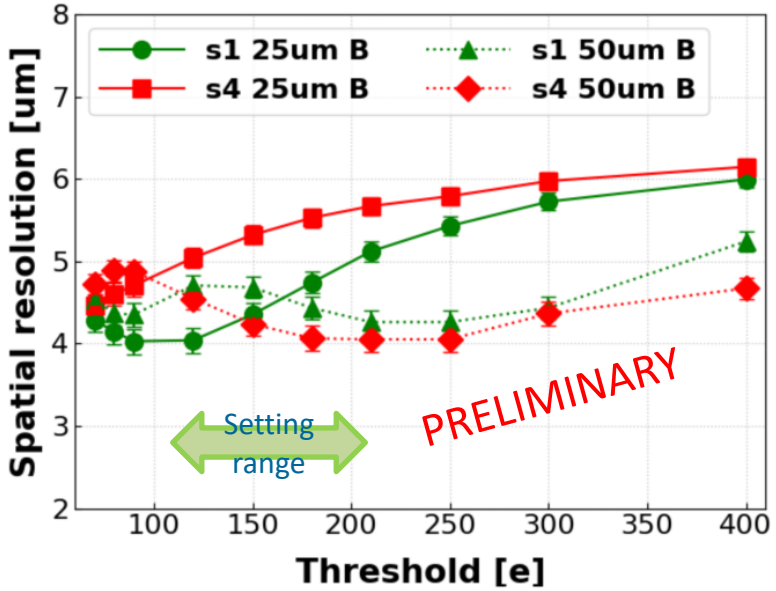
First proposed by W. Snoeys et al.
H. Pernegger et al., 2017 JINST 12 P06008

MIMOSIS-2.1: 25µm OR 50µm epitaxial layer

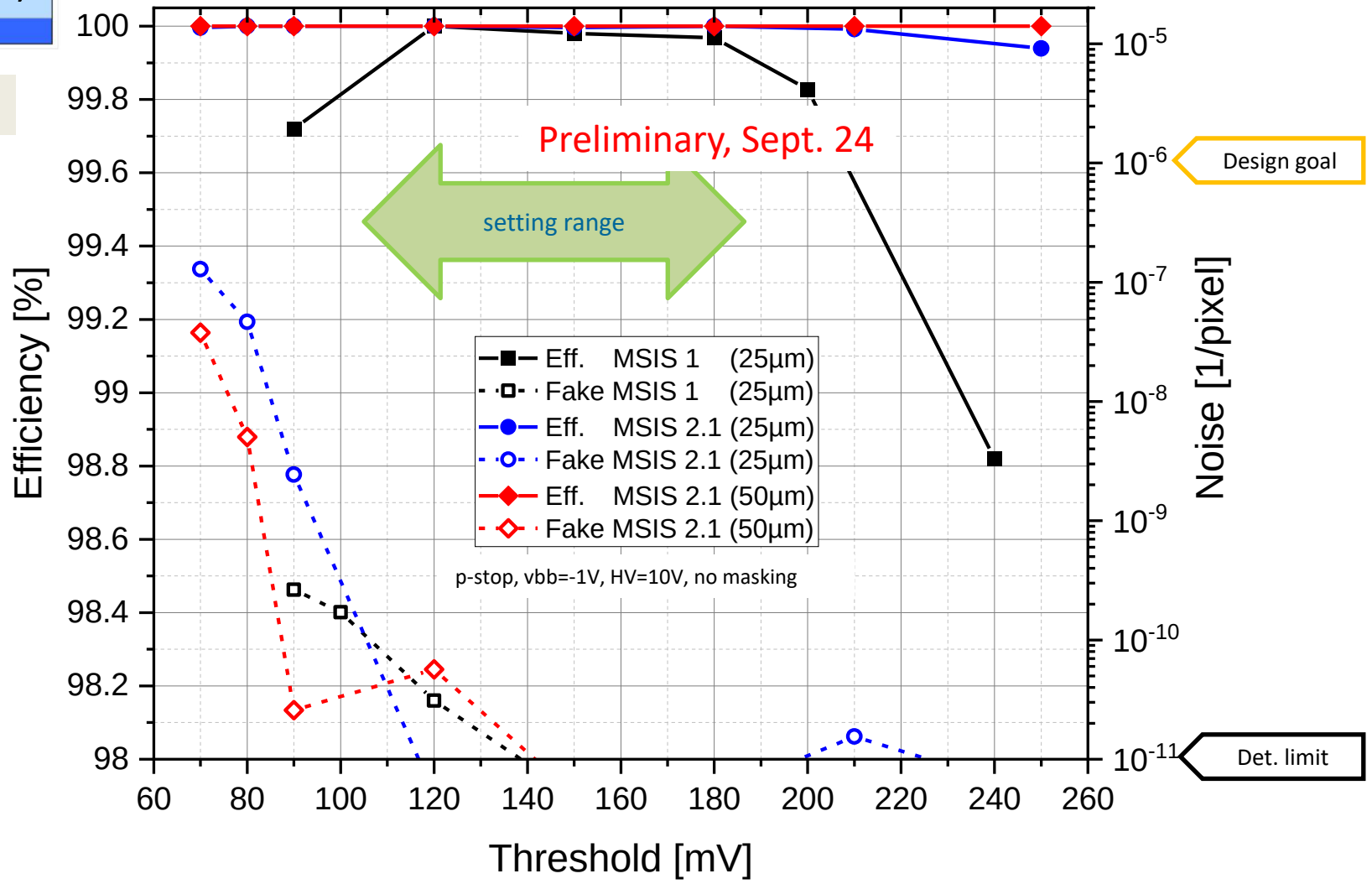


- DC pixel – limited rad. hardness.
- AC Pixel – more biasing lines.

AC

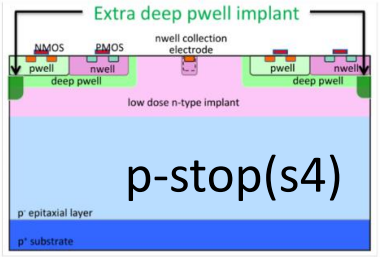


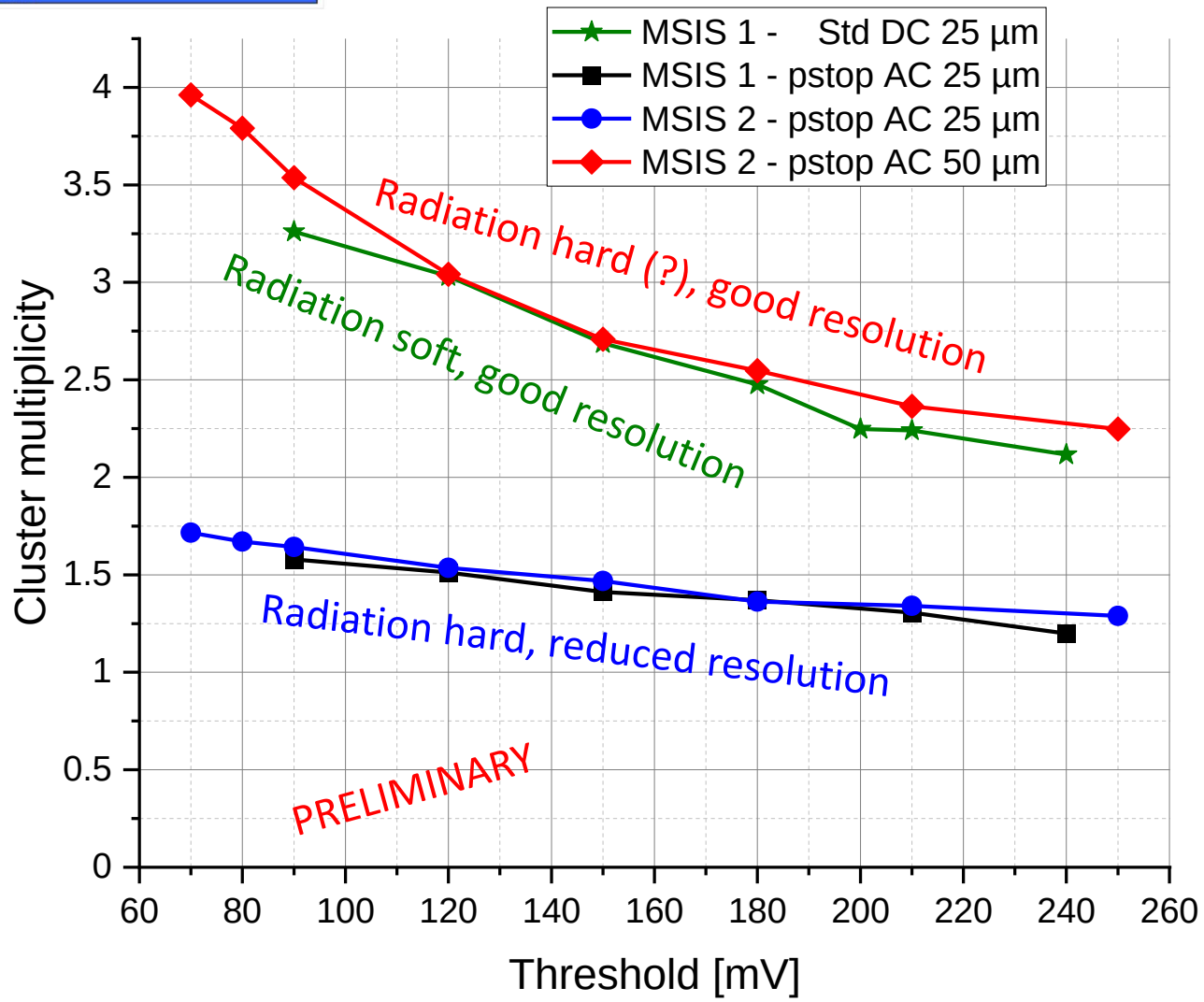
p-stop AC

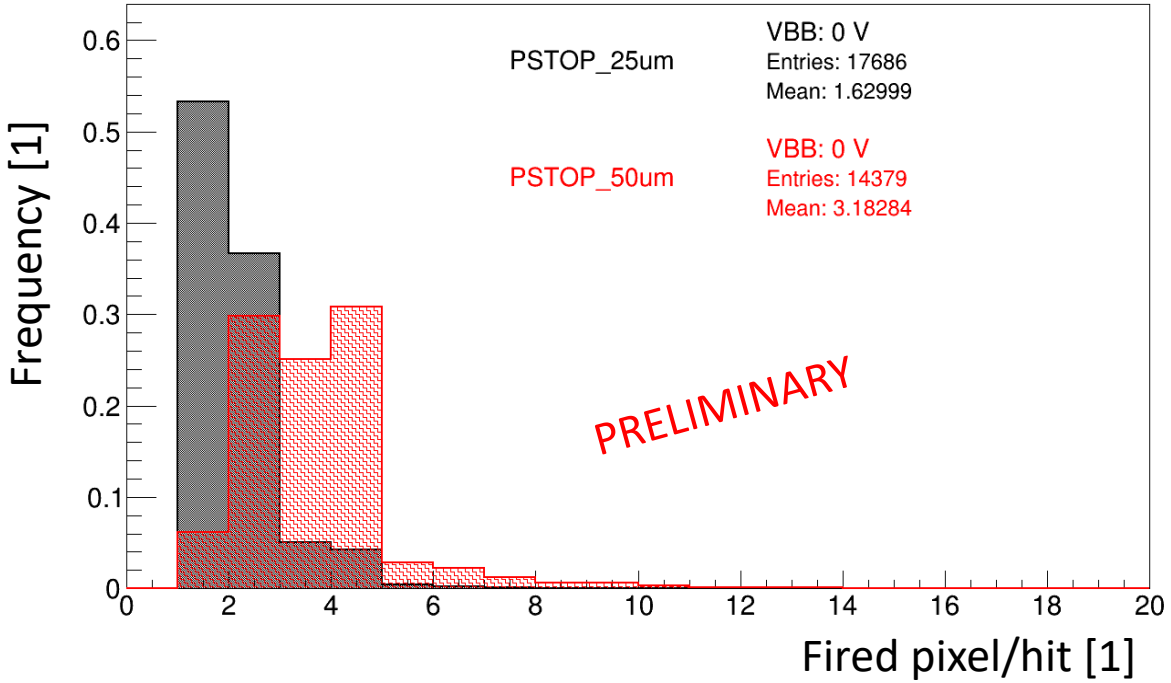


Optimizing resolution – radiation hardness

DESY & CERN test beam







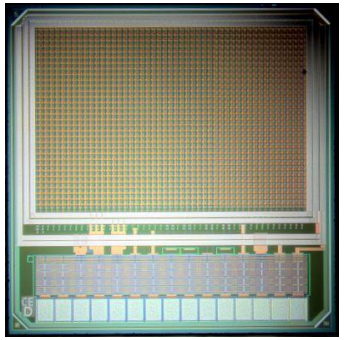
Observation:

⇒ MIMOSIS-2.1 p-stop 50µm combines high cluster multiplicity with rad. tolerant structure.

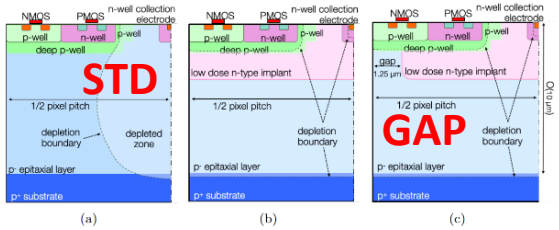
Might yield best combination of spatial resolution and radiation tolerance (rad tolerance t.b.c in 2025).

CMOS sensor R&D in TPSCo 65 nm technology

CE_65 family & SPARC chips

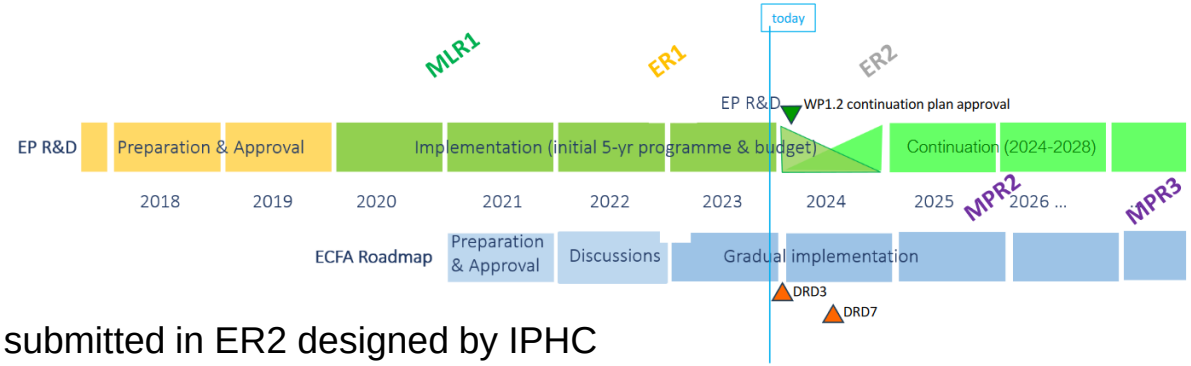


First proposed by W. Snoeys et al.
H. Pernegger et al., 2017 JINST 12 P06008



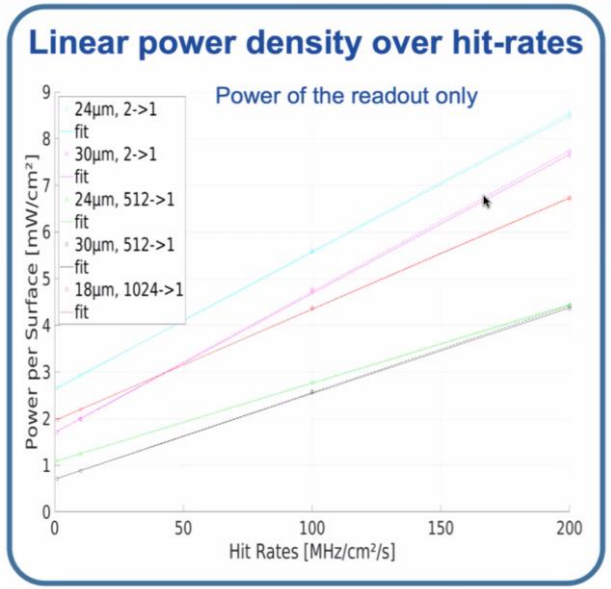
- ALICE ITS-3 and EP WP 1.2 R&D: TPSCo 65 nm (2020-2024)
  - ✓ Exploratory phase on the technology
  - ✓ APTS, DPTS, CE_65, etc.
  - ✓ Chips dedicated to ALICE ITS-3: MOSAIX in ER2
- 2021-2024: Prototypes CE_65 (MLR1 – ER1) designed by IPHC
  - ✓ Small size prototype family with analog output to explore charge
  - ✓ Different variants (epitaxial layer, etc.) and pitchs (15 to 25 µm), squared or hexagonal collecting diode position matrix
  - ✓ Working group (IPHC, APC, ETH Zurich, Prague, Japan)

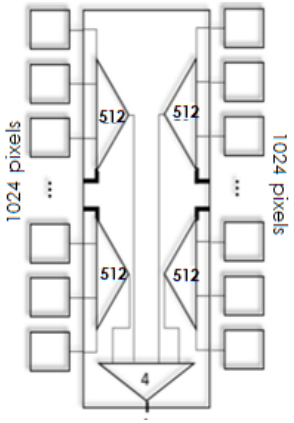
IPHC: A. Kumar, A. Dorokhov, S. Bugiel, J. Baudot, A. Besson, C. Colledani, Z. El Bitar, M. Goffe, C. Hu-Guo, K. Jaaskelainen, S. Senyukov, H. Shamas, I. Valin, Y. Wu(USTC)
Zürich: E. Ploerer, A. Ilg, A. Lorenzetti, A. Macchiolo
Prague: P. Stanek, L. Tomasez, A. Kostina
Hiroshima: Y. Yamaguchi, T. Katsuno
Tokyo: H. Baba, T. Gunji
Tsukuba: T. Chujo, J. Park, D.Shibata, S.Sakai



Jean Soudier, Frédéric Morel, Jérôme Baudot, Grégory Bertolone, Foudil Dadouche, Andrei Dorokhov, Xiaochao Fang, Abdelkader Himmi, Jean-Baptiste Kammerer, Anthony Krieger, Hung Pham, Wilfried Uhring, and Isabelle Valin. A versatile and fast pixel matrix read-out architecture for maps. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 1067:169663, 2024.

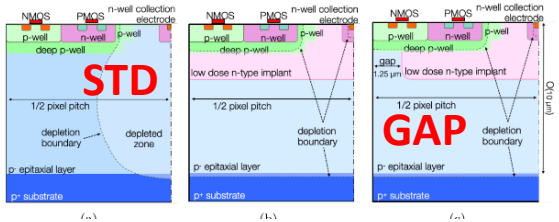
- SPARC to be submitted in ER2 designed by IPHC
  - ✓ Prototype to explore asynchronous read-out based on different stages of arbiters
    - 32 x 28 pixels
    - 16 x 24 µm pitch
  - ✓ Expected added value
    - Power optimization (linear with hit density) (Periphery + analog Power to be added)
    - Versatile architecture both for vertexing and tracking





First proposed by W. Snoeys et al.
H. Pernegger et al., 2017 JINST 12 P06008

TPSCo 65 nm & spatial resolution



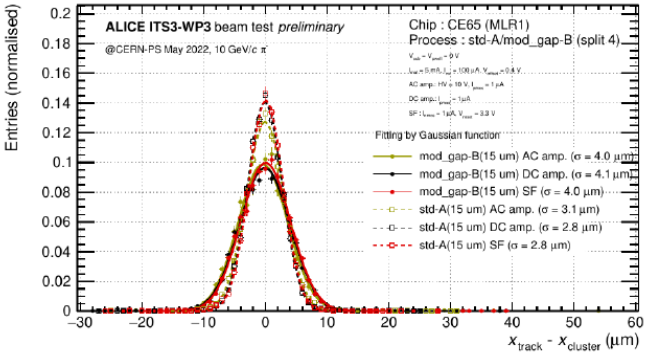
- 3 µm resolution with Analog output
  - ✓ STD ⇨ pitch ~ 25 µm
  - ✓ GAP ⇨ pitch ~ 14 µm
- 3 µm resolution with Binary ouput
  - ✓ STD ⇨ pitch ~ 17 µm
  - ✓ GAP ⇨ pitch ~ 14 µm
- Few bits ADC valuable with presence of charge sharing
  - ✓ On going studies

CE_65 results

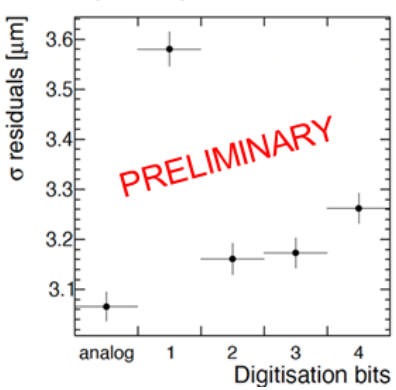
PCB	Geo	Process	Pitch(um)	HV(V)	Sp. Res.(um) (telescope resolution subtracted)
10	SQ	GAP	22.5	10	~5.1
02	SQ	GAP	18	10	~4.1
19	SQ	GAP	15	10	~3.2
18	SQ	STD	22.5	10	~2.4
23	SQ	STD	18	10	~1.8
06	SQ	STD	15	10	~1.3

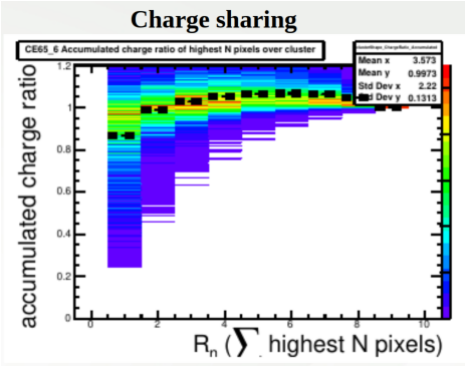
Telescope resolution: **~2.1um** (Calculated from https://mmager.web.cern.ch/telescope/tracking.html)

CE_65 results

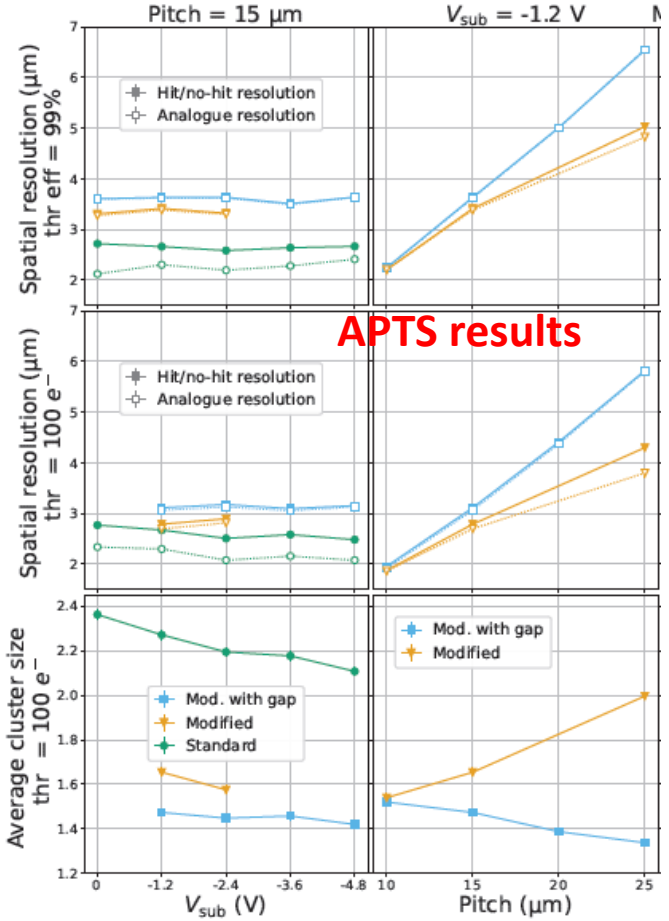


CE_65 + ADC emulated





APTS results



G. Aglieri et al. Characterization of analogue monolithic active pixel sensor test structures implemented in a 65 nm cmos imaging process. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 1069:169896, 2024.

- ✓ How to reach the resolution with an adapted read-out architecture and fulfilling all the other requirements ?
  - Implementing an adapted read-out architecture (power, time) ⇒ pitch ~ 20-25 µm
  - Binary read-out: ⇒ small pitch ~ 14 µm (GAP)

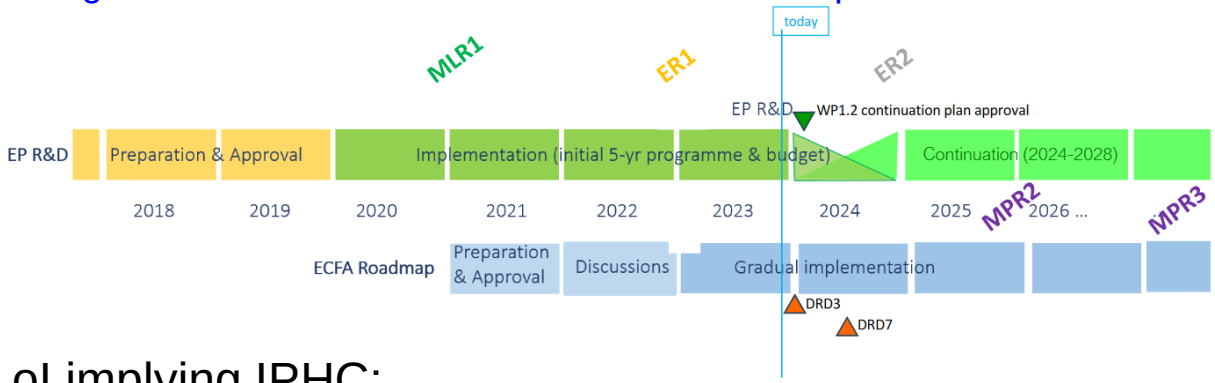
  ⇒ conflicting with the footprint of the read-out architecture
  - Idea: decouple the relationship pitch - resolution with charge sharing AND charge encoding (few bits ADC)

  ⇒ Keep seed S/N high enough but improve resolution

  ⇒ Optimum ? Allow ~30% of charge sharing

TPSCo65 nm R&D in DRD3/7

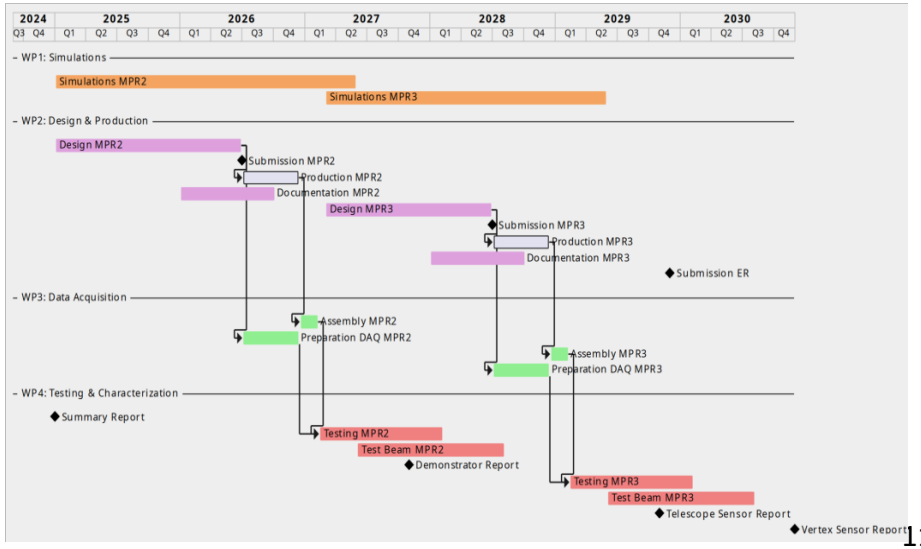
- Letter of intent submitted to DRD3 WP1:
  - ✓ OCTOPUS : Optimized CMOS Technology fOr Precision in Ultra-thin Silicon
    - Target 3 µm spatial resolution
    - Improve time resolution O(100ns)
    - Relax Power constraints
  - ✓ Step 1: explore architectures & spatial resolution ⇒ MPR2
    - Exploit previous MLR1/ER1/ER2 results
    - Determine the most suitable architecture (from SPARC in ER2)
  - ✓ Step 2: large size demonstrator usable for beam telescopes ⇒ MPR3



- Other LoI implying IPHC:
  - ✓ Generic R & D for trackers ⇒ Project submitted to DRD3 WP1
  - ✓ Potential targets: Belle-2, ALICE 3, LHCb, FCCee outer tracker, etc.
  - ✓ Opportunity for common read-out architecture development
- Other WPs, e.g.
  - ✓ Bent sensors, cooling in DRD8
  - ✓ Simulations in DRD7 WP2.c

Institute	Contact	Main areas of contribution
APC Paris	M. Bomben	Simulations, testing
Bonn University	J. Dingfelder	ASIC design, testing
CERN	D. Dannheim	Testing, DAQ, ASIC design support (through DRD7)
DESY	S. Spannagel	ASIC design, testing, DAQ, simulations
ETH Zurich	M. Backhaus	ASIC design, testing
FNSPE Prague	P. Svihra	ASIC design, DAQ, testing
GSI	M. Deveaux	Simulations, testing
HEPHY Vienna	T. Bergauer	DAQ, testing, ASIC design
IPHC Strasbourg	A. Besson	ASIC design, testing
Zurich University	A. Macchiolo	Testing, DAQ, simulations

Number	Deliverable/Milestone Title	WP project #	Lead	Type	Dissemination Level	Due Date
M1	Report on Demonstrators	4	DESY	Report	DRD3 report	Month 9 (Q1 2025)
D1 MPR2	Beam Telescope Demonstrator Matrix Submission 3 µm	1, 2	IPHC	Prototype Full column height	Manual / Presentation	Month 24 (Q2 2026)
M2	Report on Demonstrator Matrix Characterization	3, 4	DESY	Report	Publication	Month 36 (Q2 2027)
D2 MPR3	Full Beam Telescope Sensor Submission	2, 3	IPHC	Prototype ≥ 2cm² sensor	Manual / Presentation	Month 48 (Q2 2028)
M3	Report on Beam Telescope Sensor Performance	3, 4	DESY	Report	Publication	Month 60 (Q2 2029)
D3 ER	LC Vertex Sensor Demonstrator Submission	1, 2	IPHC	Prototype	Manual / Presentation	Month 66 (Q4 2029)
M4	Report on LC Vertex Sensor Demonstrator Performance	3, 4	DESY	Report	Publication	Month 78 (Q4 2030)

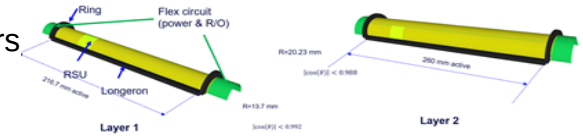


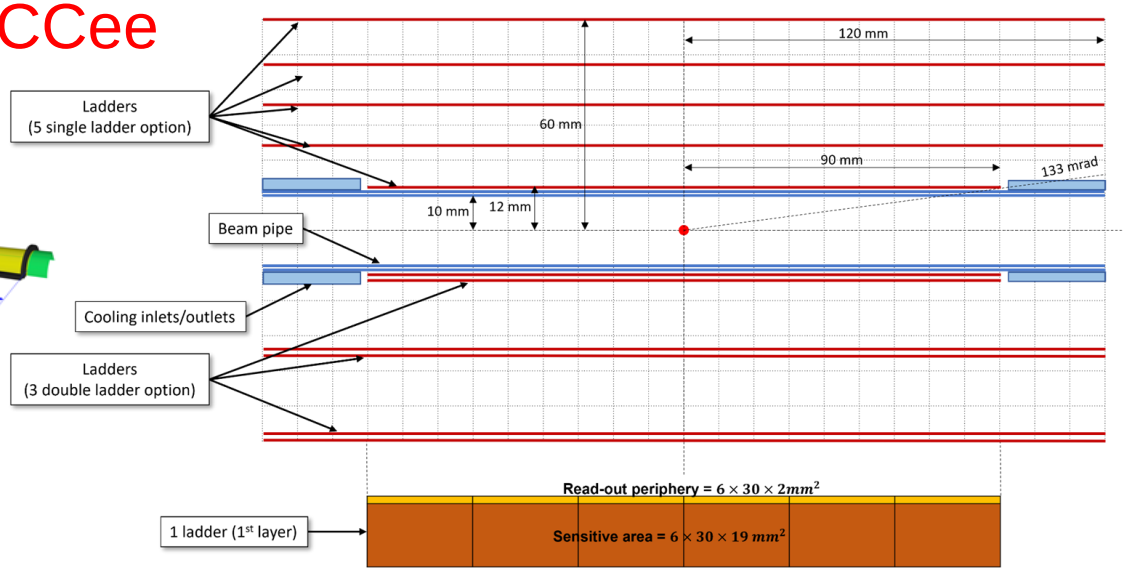
Institute	Contact	Domain of contribution
IPHC	J.Baudot	Simulation, design, test
IFIC-Valencia	C. Marinas	Design, test, integration
IGFAE-USC	A. Gallas	Test, integration
INFN Pavia/University of Bergamo	G. Traversi	Simulation, design, test
CPPM	M. Barbero	Design, test
IRFU	S. Panebianco	Design, test
GSI	M. Deveaux	Test, simulation
LPNHE	G. Calderini	Design, test

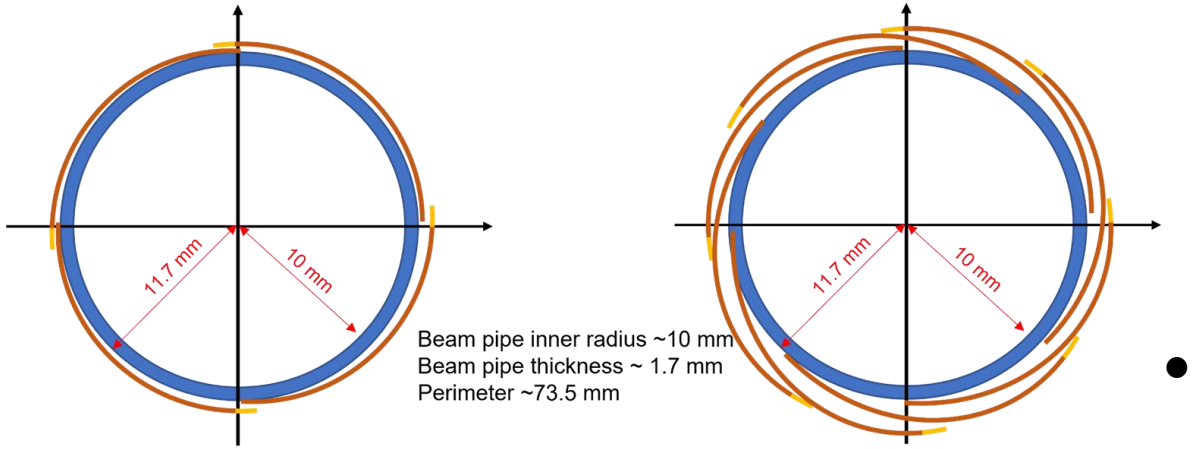
Strategy toward a vertex detector for FCCee

Schnecke: a vertex detector for FCCee

- À la CLD/ILD: 3 double ladders + discs
  - Robust but not optimized for material budget
- À la ALICE ITS-3 : 3/4 layers with stitched half cylinders
  - Fill factor not 100% per layer
  - Stitching mandatory
    - Pitch ? Power ? Yield ? Fill factor ? Bent radius ?
  - Very competitive for mat. budget but limitations (acceptance, resolution, radius ?)
- Alternative Proposal: Schnecke concept = bent ladders
  - Stitching or not stitching
  - Radius approaching constant value
  - Full acceptance in φ
  - Double sided can be considered.
  - Number of layers = free parameter
  - Competitive for mat. Budget. AND full azimuthal acceptance







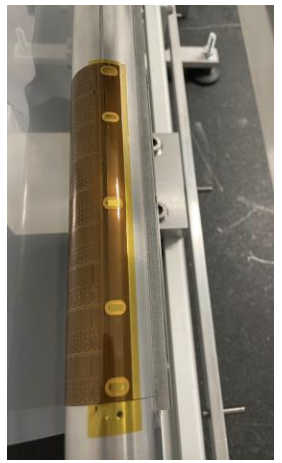
Beam pipe inner radius ~10 mm
Beam pipe thickness ~ 1.7 mm
Perimeter ~73.5 mm

Table 3: Barrel dimensions (single and double sided option)

Layer	1	2	3	4	5
Radius (mm)	12-13	24	36	48	60
Zmax (mm)	90	120	120	120	120
Perimeter (mm)	75	151	226	302	377
# Chips per ladder	6	8	8	8	8
# ladders	4	8	12	16	20

Layer	1-2	3-4	5-6
Radius (mm)	12-13	35-36	59-60
Zmax (mm)	90	120	120
Max perimeter (mm)	82	226	377
# Chips per ladder	6	8	8
# ladders	4	12	20
Single chip dimension			$30 \times 22.2\ mm^2$
Sensitive area chip dimension			$30 \times 19.2\ mm^2$

Bending setup @ IPHC

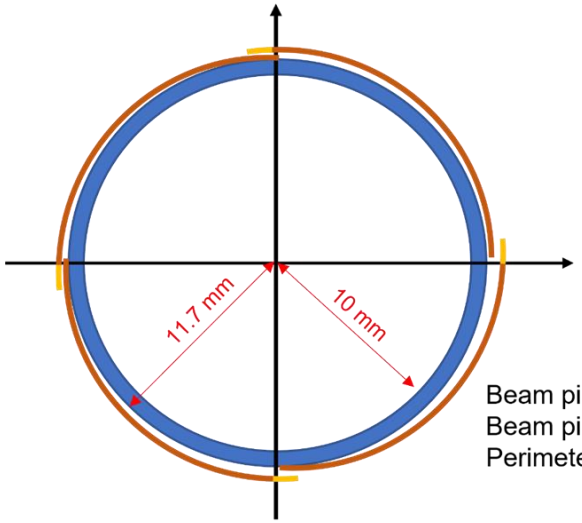


- Bent sensors pioneered by Alice ITS-3,
  - IPHC : working program dedicated to bent sensor with MIMOSIS
  - e.g. functional tests @ R = 12 mm

Summary

- TJ 180nm: MIMOSIS program on track
  - ✓ MIMOSIS-3 ⇒ to be submitted in 2025
  - ✓ MIMOSIS-2.1/3 ⇒ Suitable large scale prototypes for integration tests (e.g. bent sensors)
- TPSCo 65 nm
  - ✓ CE65 family (MLR1/ER1) ⇒ Exploration of resolution / charge sharing / charge encoding emulation
  - ✓ SPARC prototype ⇒ first asynchronous architecture to be submitted in ER2
  - ✓ OCTOPUS LoI in DRD3 ⇒ R&D program targeting fine resolution for Higgs factory VTX
  - ✓ Other EoIs (tracker, etc.) ⇒ synergies to be exploited
- Vertex detector for FCCee
  - ✓ Target: FCCee: EoI/LOI for sub-detector concept
    - Submit a realistic/robust vertex detector concept adaptable to all detector concepts
    - Backbone: chip design fulfilling the requirements based on an architecture developed through DRD3 projects
      - Optimize charge sharing / charge encoding for resolution
      - Global design: versatile enough to cope with stitched / unstitched approaches.
      - Simulation: quantify precisely figures of merit (resolution down to tagging capabilities)
      - Integration: bent sensors and ladders to demonstrate the feasibility of the Schnecke concept

Back up



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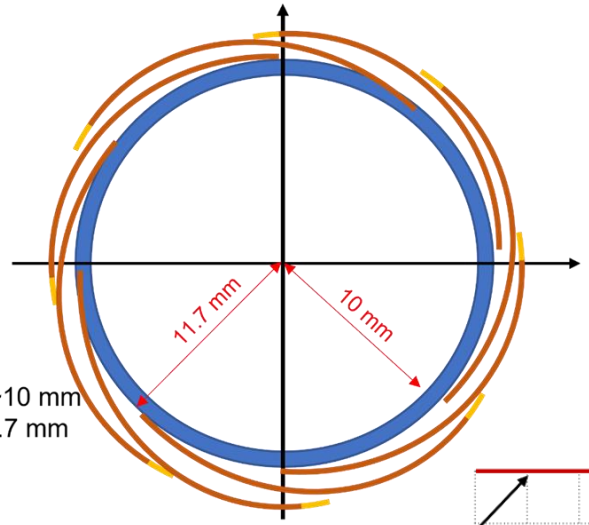
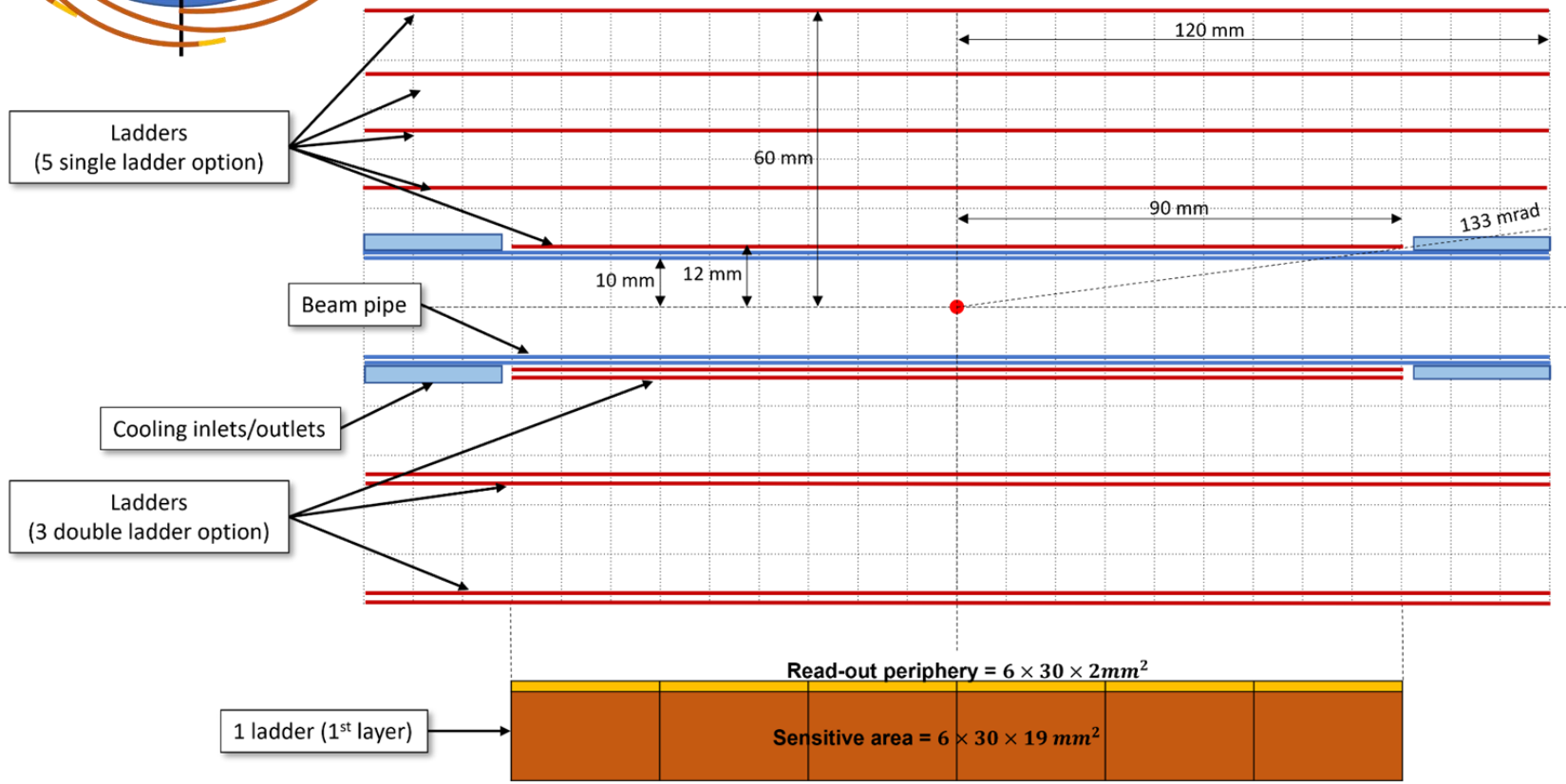
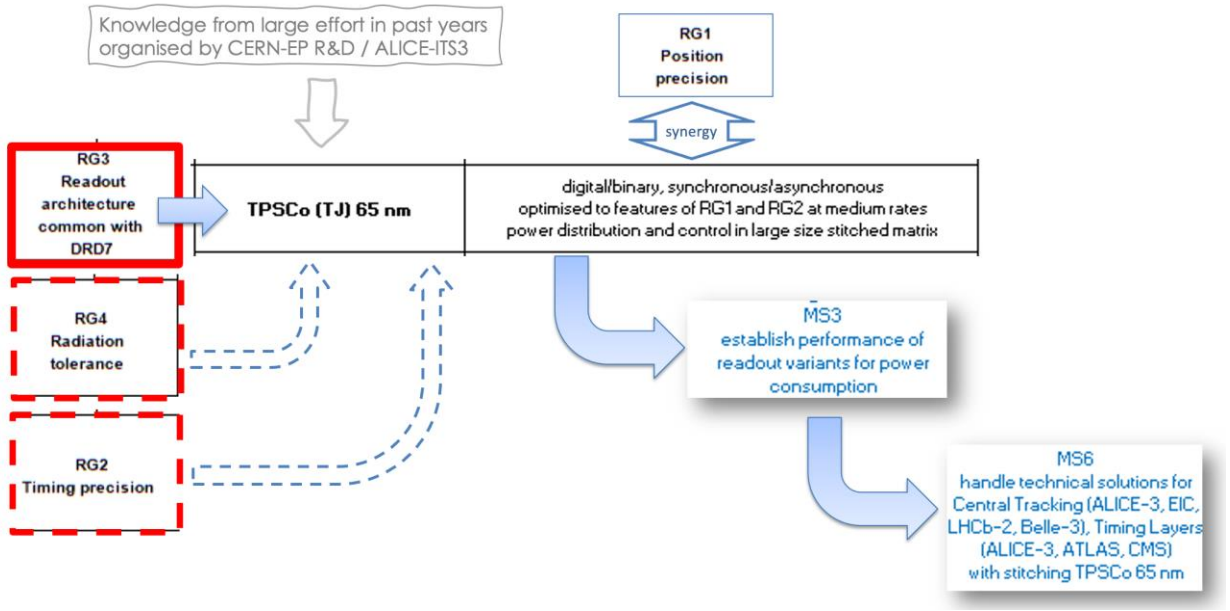




DRD3 Tracker Project Calendar

- Generic R & D for trackers
  - ✓ Project submitted to DRD3 WP1
- Milestones
  - ✓ M1 Q1-2025: matrix design concept established
  - ✓ M2 Q3-2025: test system concept established
  - ✓ M3 Q2-2026: tape-out of sensor prototype(s) within MPR2
  - ✓ M4 Q4-2026: test system operational
  - ✓ M5 Q1-2027: early test results
  - ✓ M6 Q4-2027: main figures of merit evaluated
- Ongoing discussions inside Belle-2, ALICE 3 and LHCb communities
  - ✓ Integrate DRD3 ?



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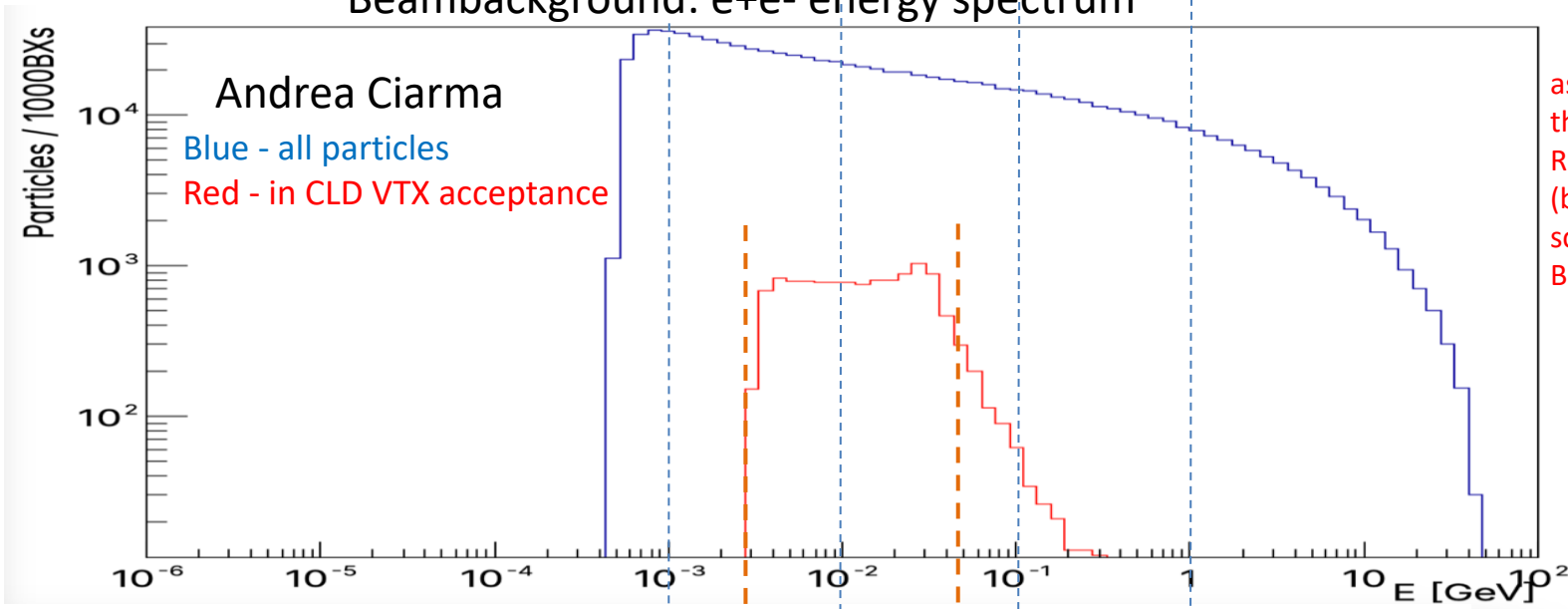
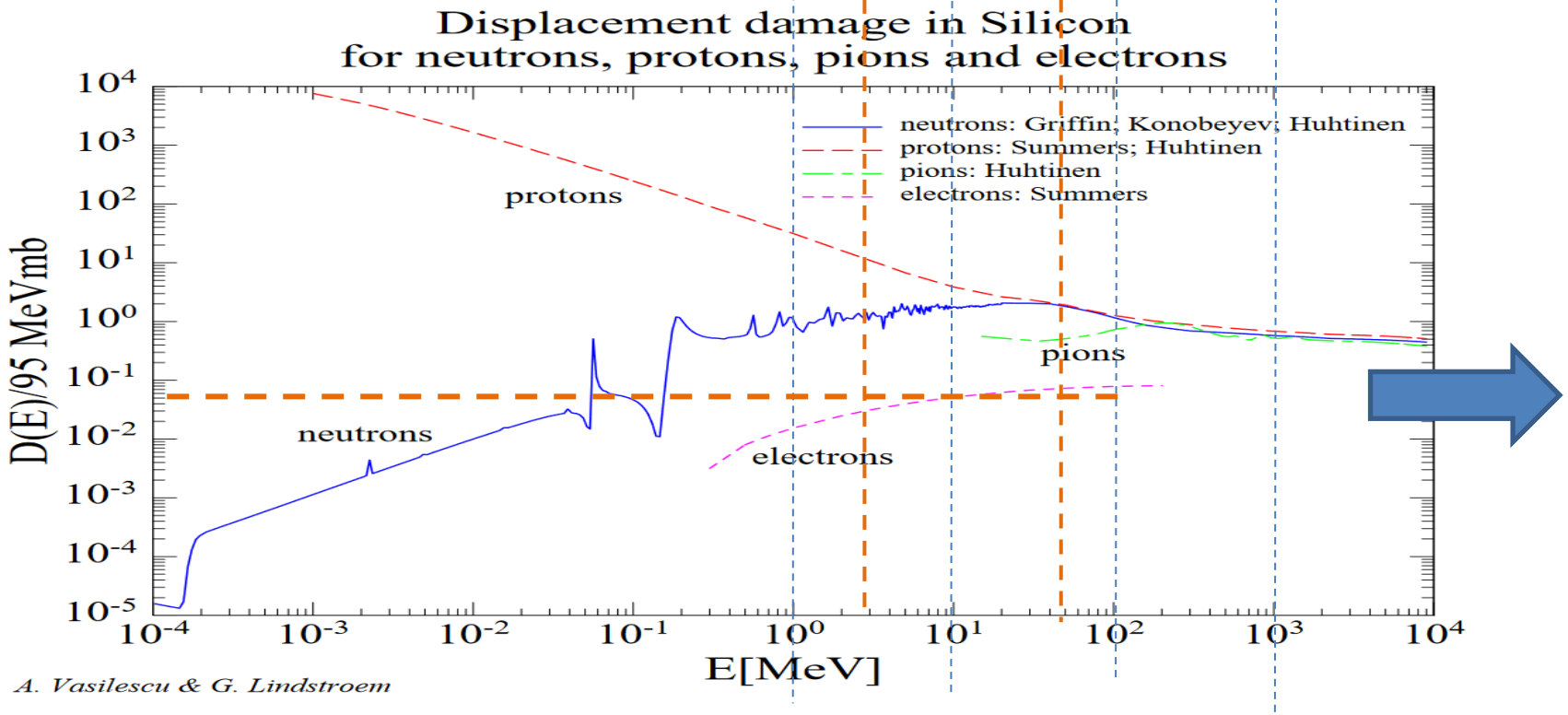
Beambackground: e+e- energy spectrum



assumptions:
theta > 100mrad ;
R > 10mm ;
(beampipe radius to account for scattering/secondaries) ;
B = 2T —> pT > 3MeV

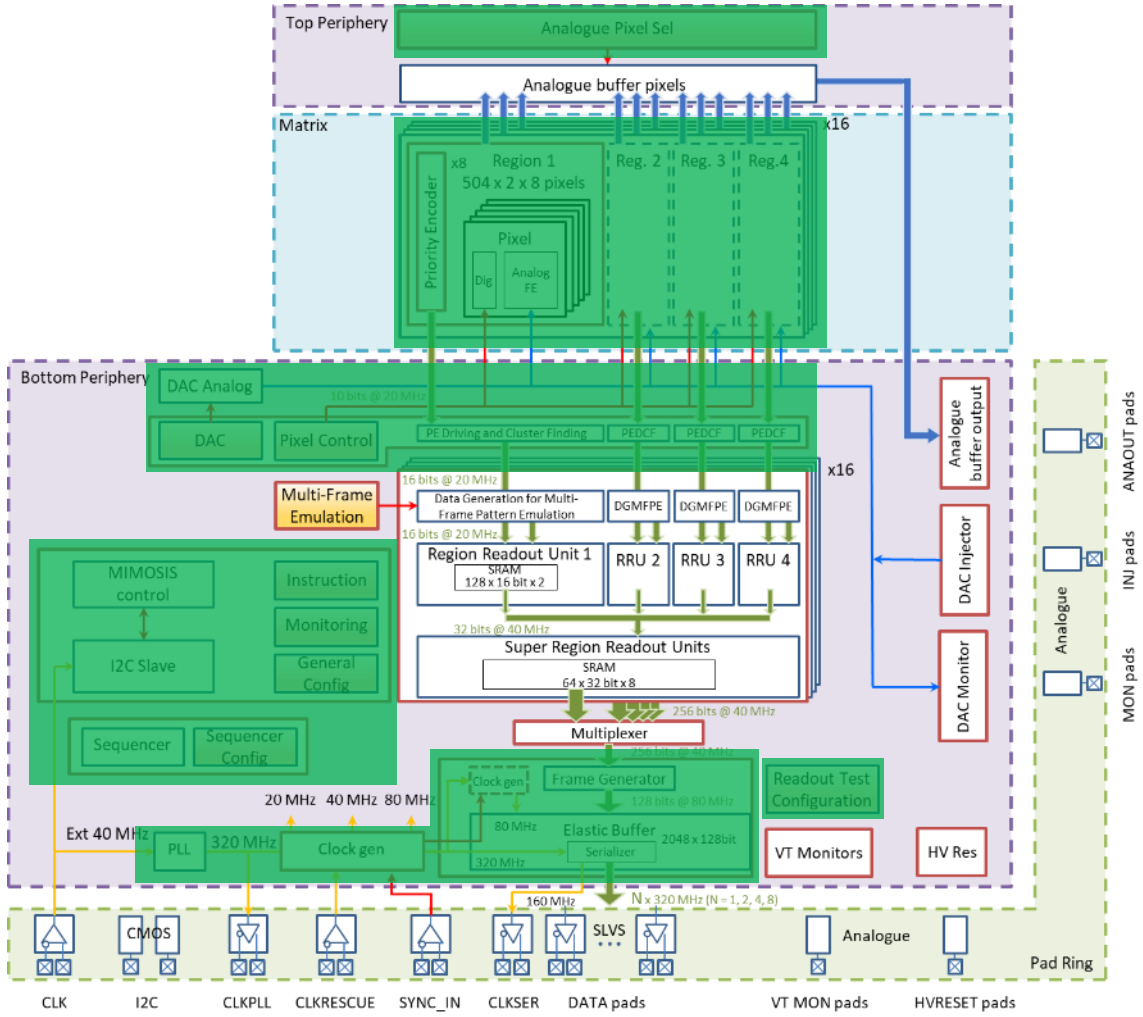


NIEL factor ~ 5 x 10^{-2}

MIMOSIS-2 – what was changed?

Reworked blocks in MIMOSIS-2

(F. Morel @ Mimosis sensor perspectives and next steps towards the CBM-MVD https://indico.gsi.de/event/15130/)

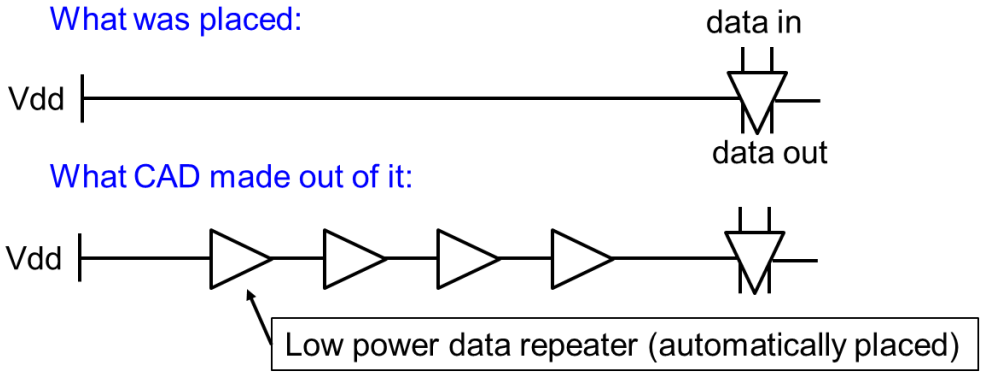


MIMOSIS-1 and MIMOSIS 2 follow the same outside specs but:

- Major features added.
- Majority of all blocks reworked.

⇒ High risk submission

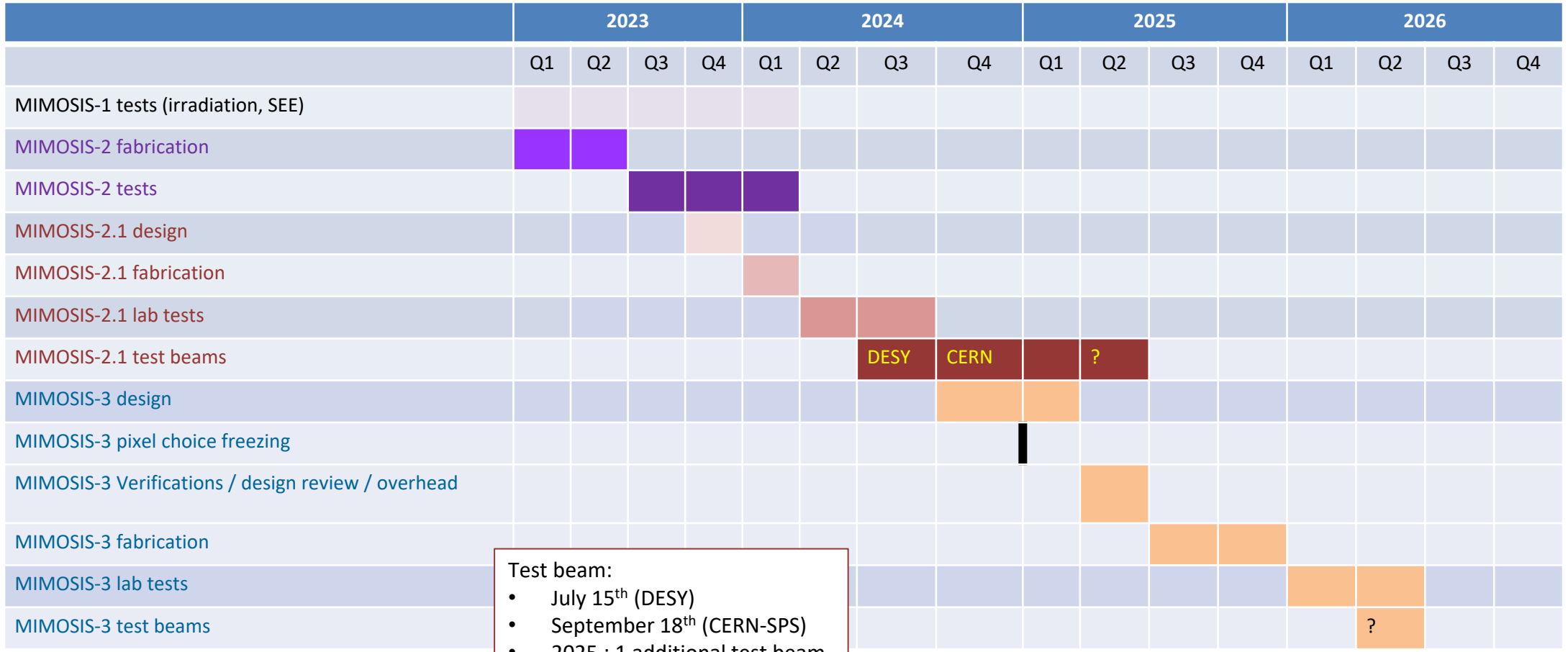
Bug example: Output driver powering issue:



Status Sept. 2023:

- 3 bugs spotted, fixes under evaluation.
- Resubmission required for full bug fix.
- Updated test plans accounting for MSIS-2 limits.

MIMOSIS calendar



Latch-up studies

Requirement for MVD:

- Must withstand LET< 35 MeV cm²/mg.
  (H. Darwish, PhD under preparation)

Test with MIMOSIS-1:

- Withstands LET=20 MeV cm²/mg.
- Limitation: dE/dx of Ca-ions used

Test with MIMOSIS-2 (Au ions):

- No LU for LET≲50 MeV cm²/mg.
- Some LU seen above.

=> MIMOSIS-2 meets requirements

Protection system for Latch-up
(1 fast electronic fuse/sensor)
likely not required.