Large Area Low-power Monolithic CMOS Tracking Detectors for future Higgs Factory Experiments

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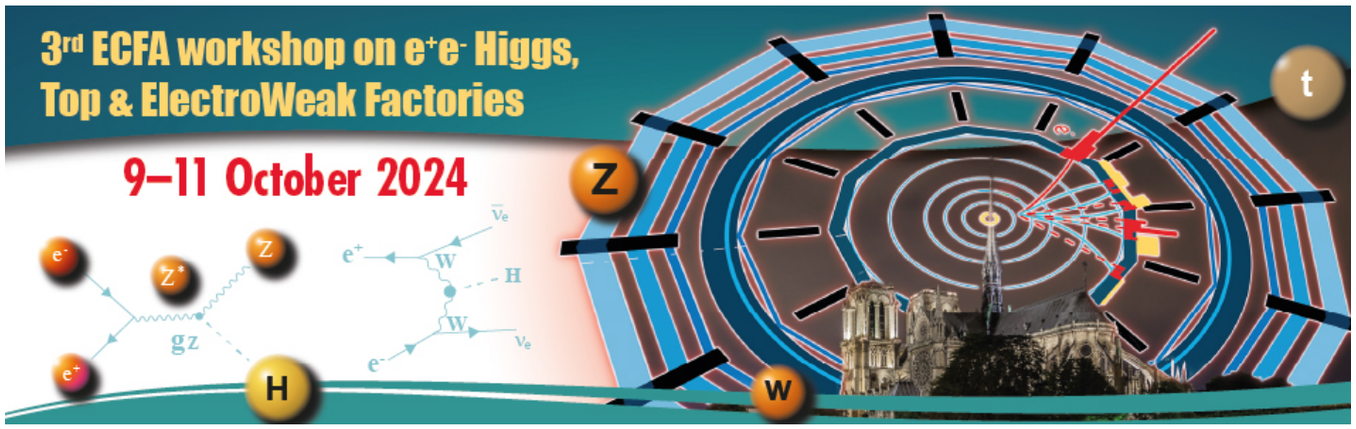
3rd ECFA Workshop on e+e- Higgs, Top & Electroweak Factories

9-Oct 2024

With contributions and inputs from colleagues in many institutes, especially

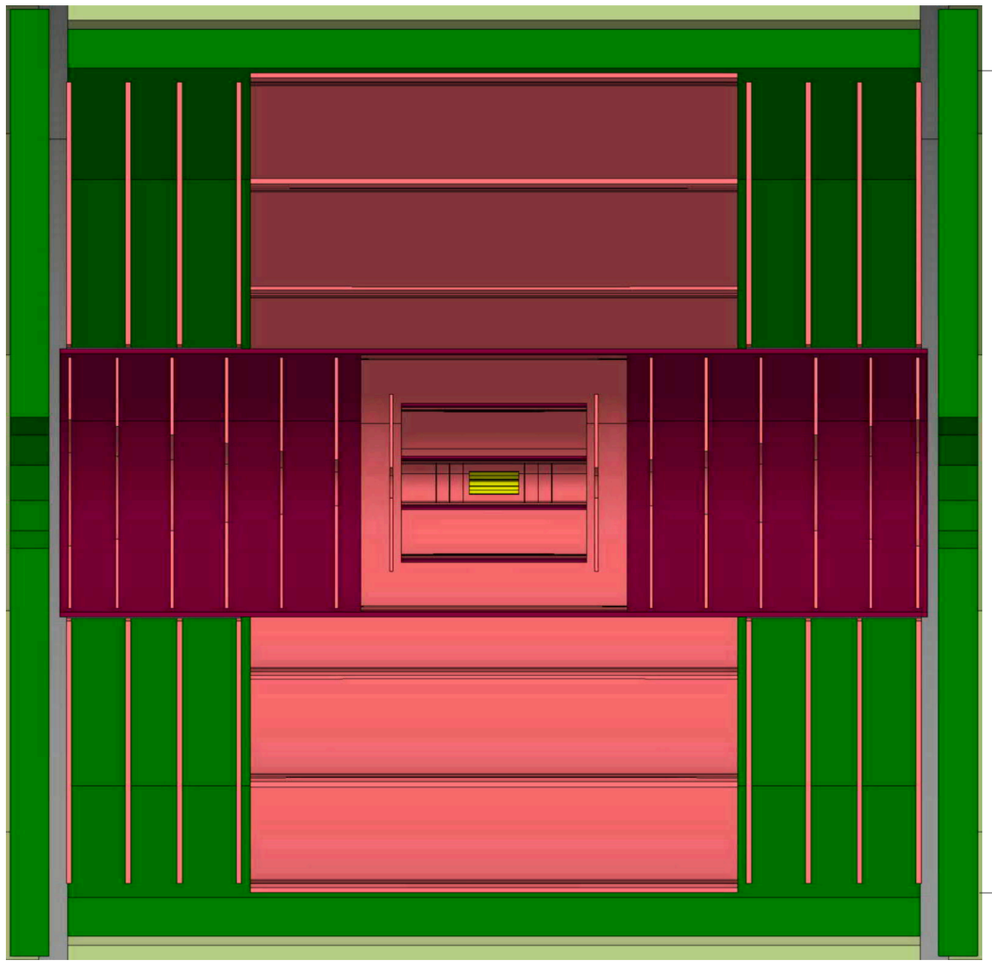
Bristol, Edinburgh, INFN Milan, IHEP, KIT, Lancaster, STFC RAL



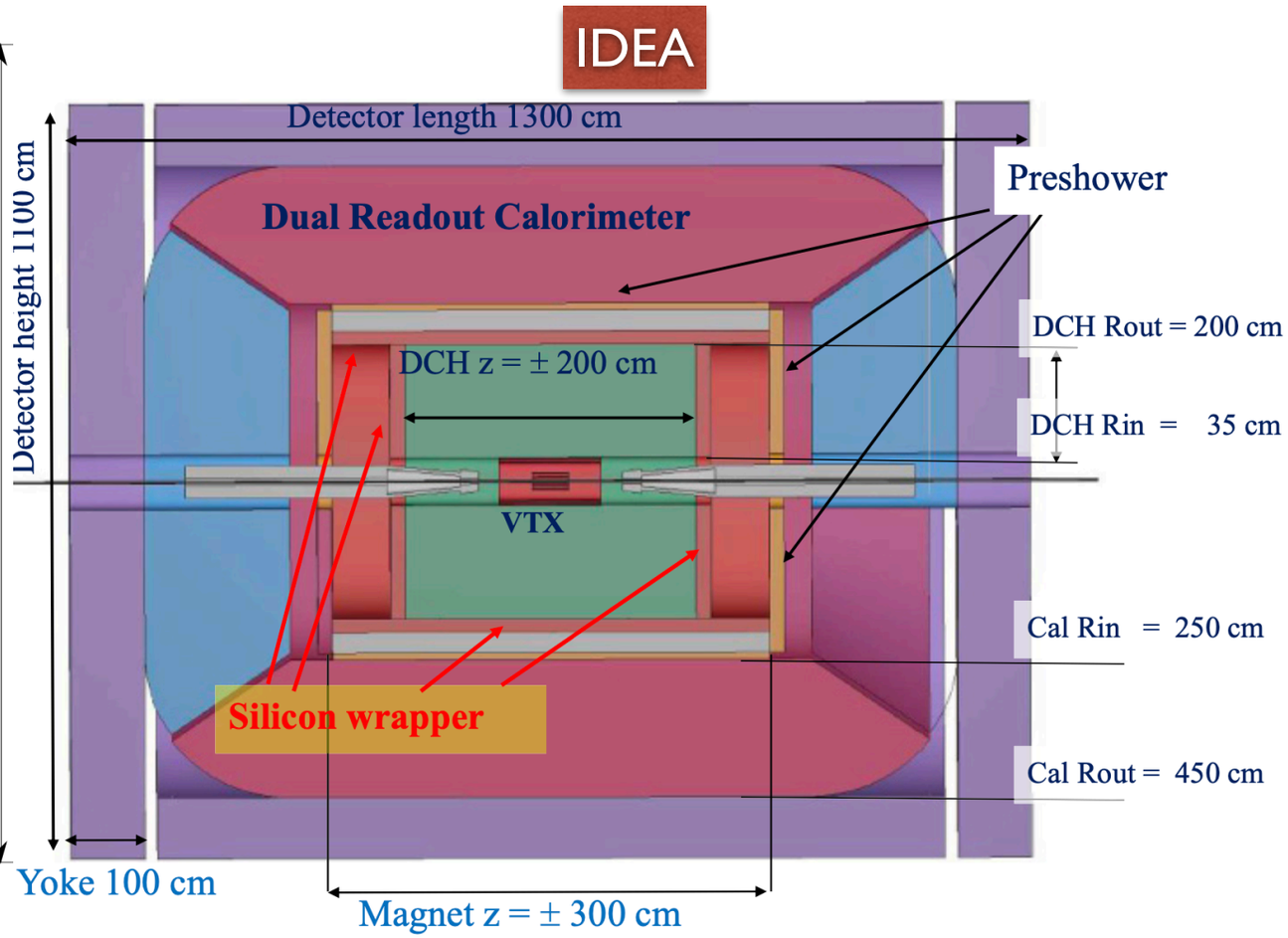
Setting the theme

- Future Higgs factory experiments typically require large tracking area O(100m^2), on the similar order as the HL-LHC experiments
  - Modest spatial resolution and radiation requirements for the middle/outer layers
  - Multiple scattering (material budget) limits the bulk of the tracking performances

CLD



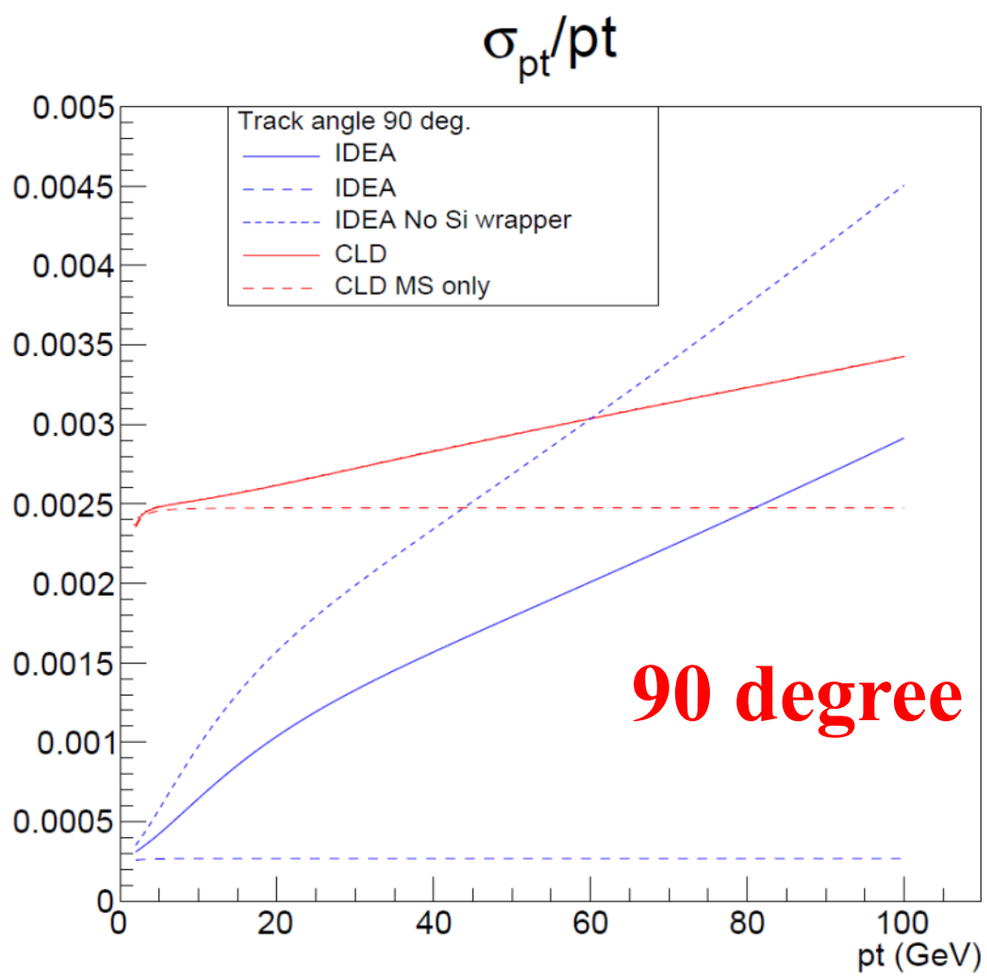
IDEA



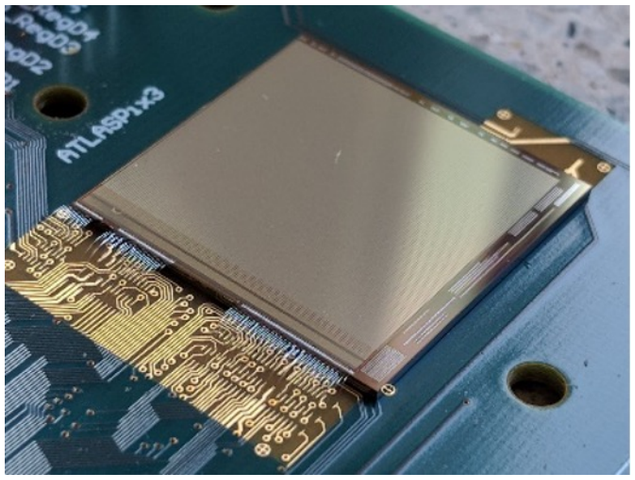
Vertex Tracker

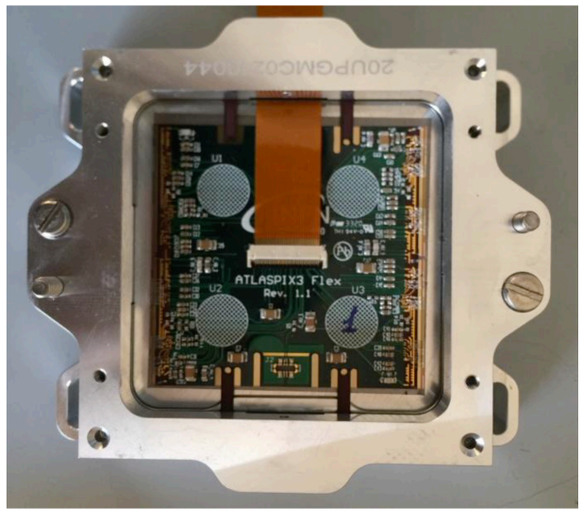
Large Area Tracker: case for the IDEA outer layer

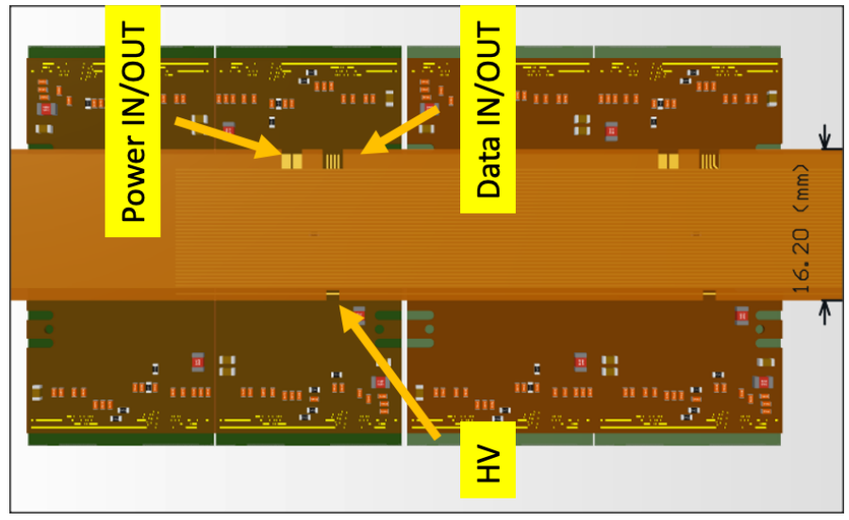
- Outer layer: precision silicon layer around the central tracker
  - Improve momentum resolution by providing additional measurements
  - Extend tracking coverage in the forward/ backward region
  - Covered area ~90 m2
- Significant impact on services and system readout
  - Need a technology suitable for large scale production (low cost and efficient assembly)
  - Limited space for services
  - Material budget is concern
- These need to be addressed during R&D together with sensor designs



HV-CMOS tracker - ATLASPix3 based prototyping



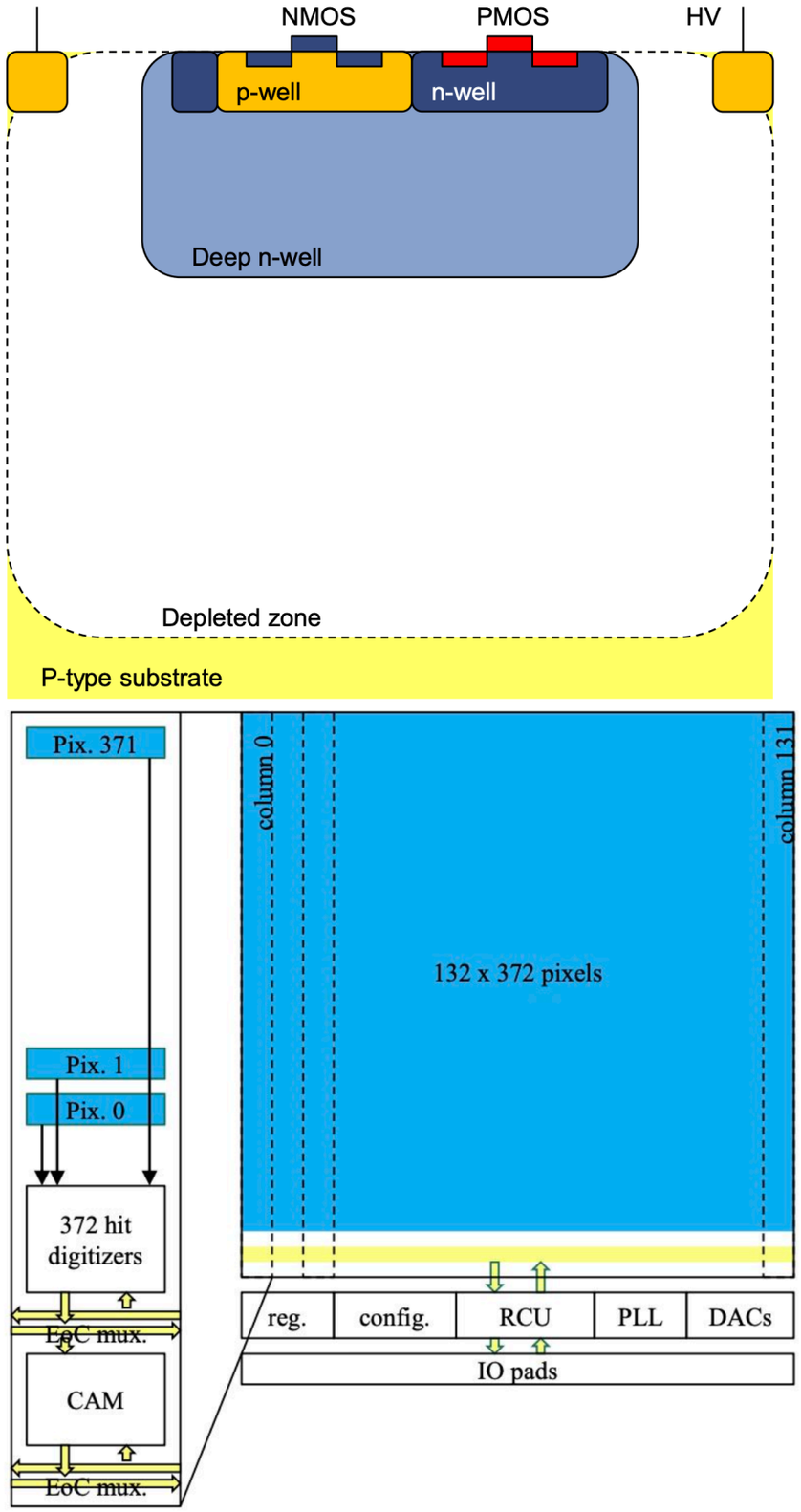




- Thanks to the recent progresses in several experiments, e.g. ATLAS ITk, ALICE ITS, mu3e, MAPS technology offers a promising solution for large area tracking
  - FCC-ee requires an order of magnitude larger in area than the state-of-the-art MAPS tracker
  - System level prototyping should start as early as possible, in parallel with new sensor R&D
- ATLASPix3 was developed for ATLAS ITk, now used widely as HV-CMOS demonstrator
  - A lot of synergies with the on-going ATLAS ITk integration and LHCb MightyTracker R&D
- Despite the large number of institutes involved, R&D resources are often very limited, majority of the work presented here are done by few postgraduate students and ECR
  - Riccardo Zanzottera (Milan), Fuat Ustuner (UoE), Lingxin Meng (Lancaster), Ruoshi Dong (KIT)

ATLASPix3/3.1 general features

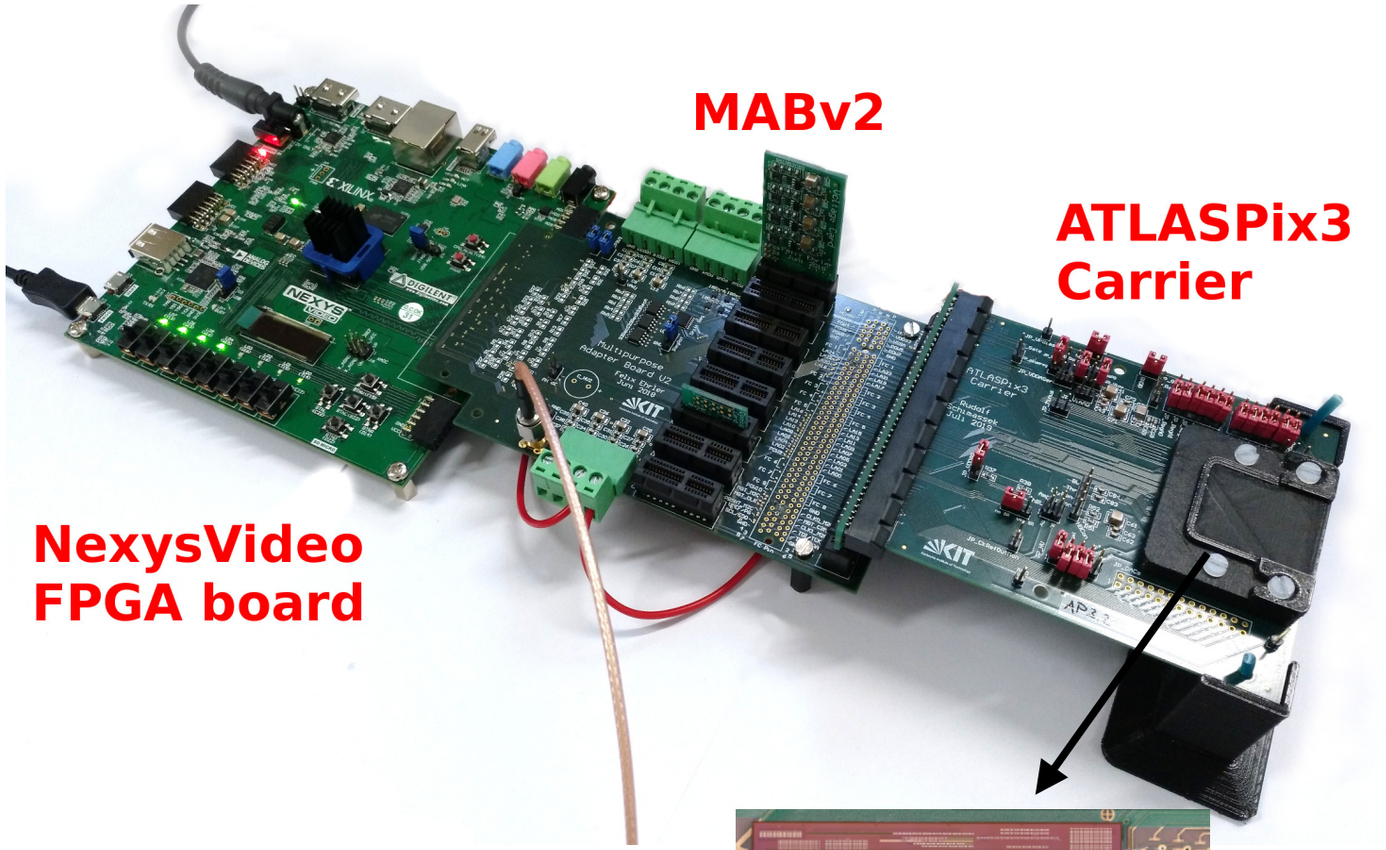
- AMS/TSI 180nm process, substrates 300 Ωcm
  - Breakdown (unirradiated): ~-65V
  - Full reticle size of 2.2 cm x 2.0 cm
    - Matrix size: 132 x 372
    - Pixel size: 50µm x 150µm
  - Individual amplifiers and threshold tuning circuits
    - Threshold can be tuned to 800e, with dispersion ~60e, noise ~ 70e
  - Digital part separated from the analog in the peripheral
  - Triggerless/Triggered readout
    - Data output: up to 1.28 Gbit/s 64b/66b (triggered), 1.6 Gbit/s 8b/10b (un-triggered)
  - 25ns time stamping
  - Good time resolution: ~4 ns (corrected)
  - Shunt/LDO (SLDO) regulators for Serial Powering
  - Power consumption 140 mW/cm²

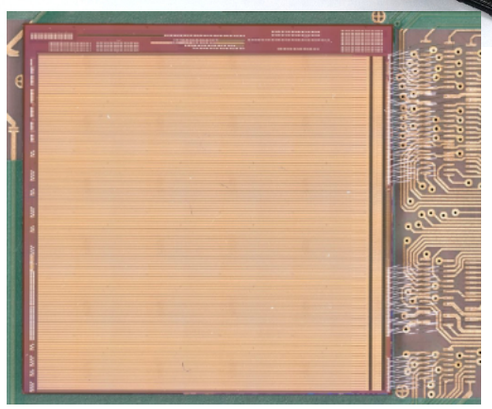


I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021 https://ieeexplore.ieee.org/document/9373986

ATLASPix3 - GECCO Readout System

- Readout system
  - Digilent Nexys Video FPGA board
  - GEneric Configuration and COntrol
  - Device carrier boards supporting:
    - Single chip card (SCC)
    - Multi-chip Telescope
    - Quad module
  - Qt-based software GUI

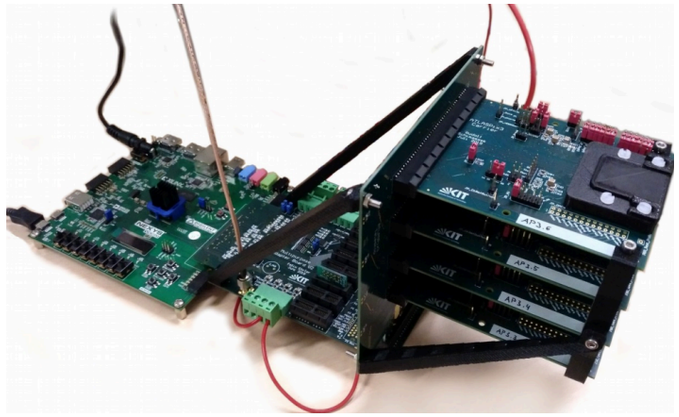


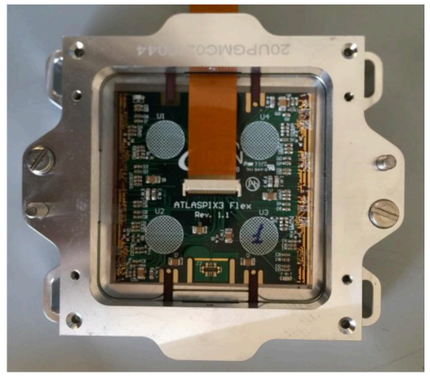


Summary of progress so far

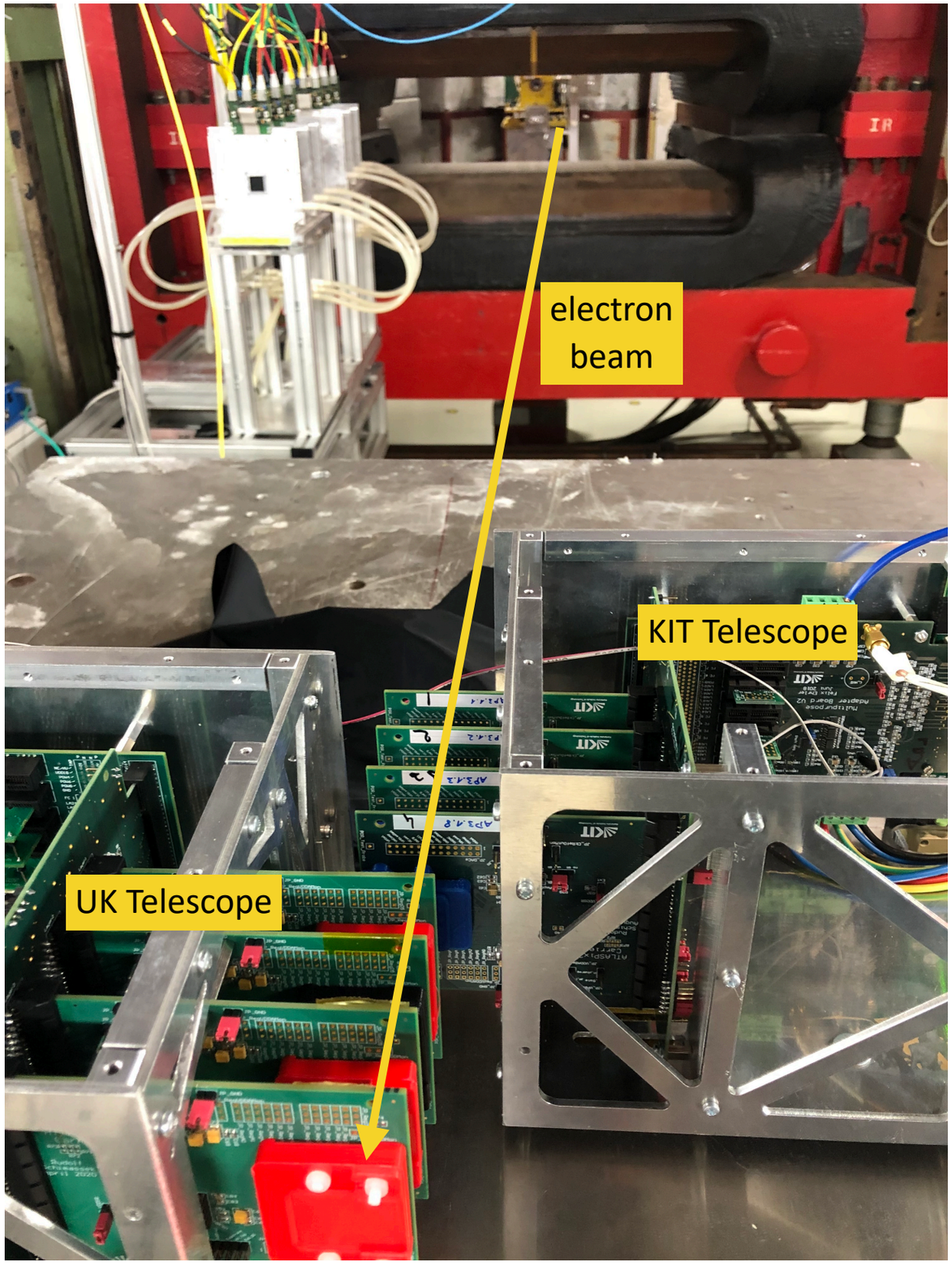
- 2 ATLASPix3.0 and 3 ATLASPix3.1 wafers diced (most thinned to 150um)
  - Joint production contributions: Edinburgh/Lancaster/KIT/Milan/RAL with the help from Heidelberg
- O(100) GECCO boards and single chip carriers produced in IHEP and distributed globally
  - Many institutes commissioned single chip lab test setup and electrical measurements
  - Supplied also to the other projects such as the LHCb MT upgrade
- ATLAS ITk pixel inspired quad-module has been developed
  - First version for ATLASPix3 has been manufactured and tested in lab and Testbeam
  - V2 quad-flex for ATLASPix3.1 (with functional Shunt-LDO) designed and 20 were produced in Sep-24
    - Ready to be assembled into modules end of 2024-25
- Two testbeam (DESY and CERN):
  - DESY: 2 telescopes, one quad
  - CERN (Sep 2024): triggered output together with calorimeter
- Preliminary mechanical support has been prototyped (not in this talk)

Telescope and DESY Test Beam

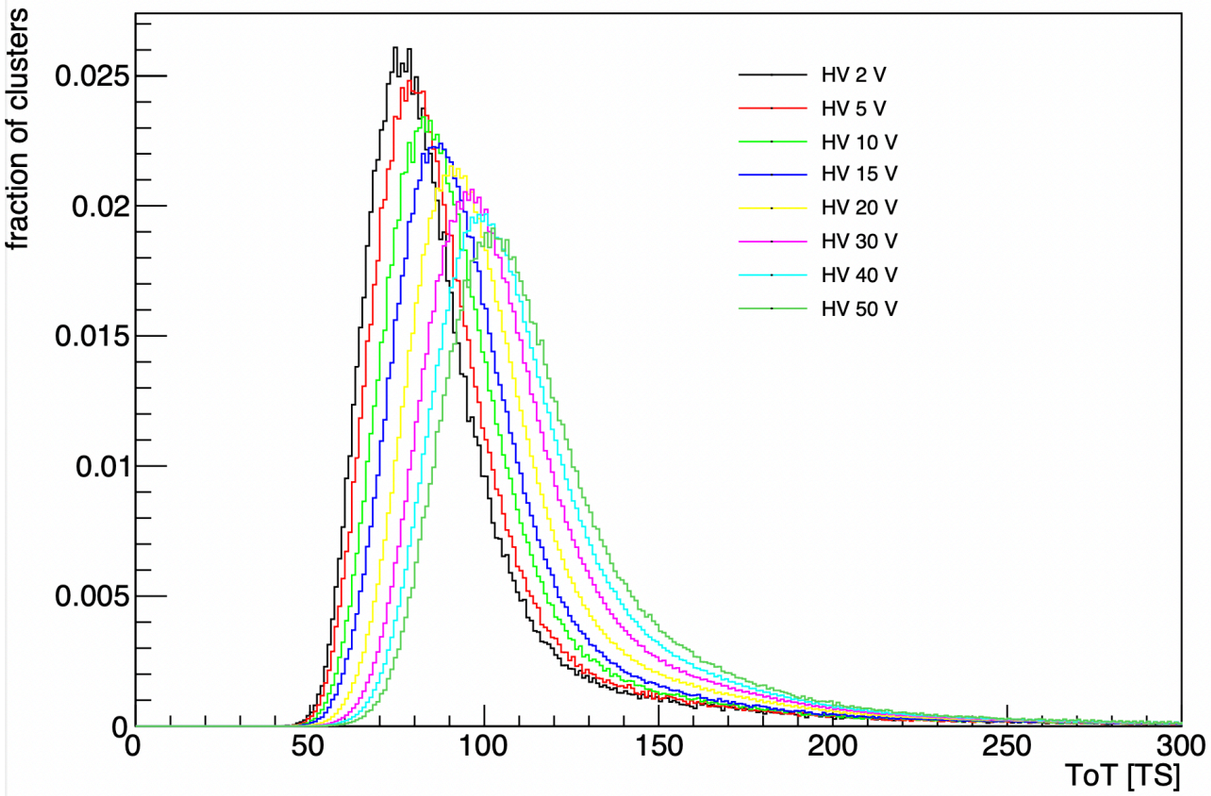


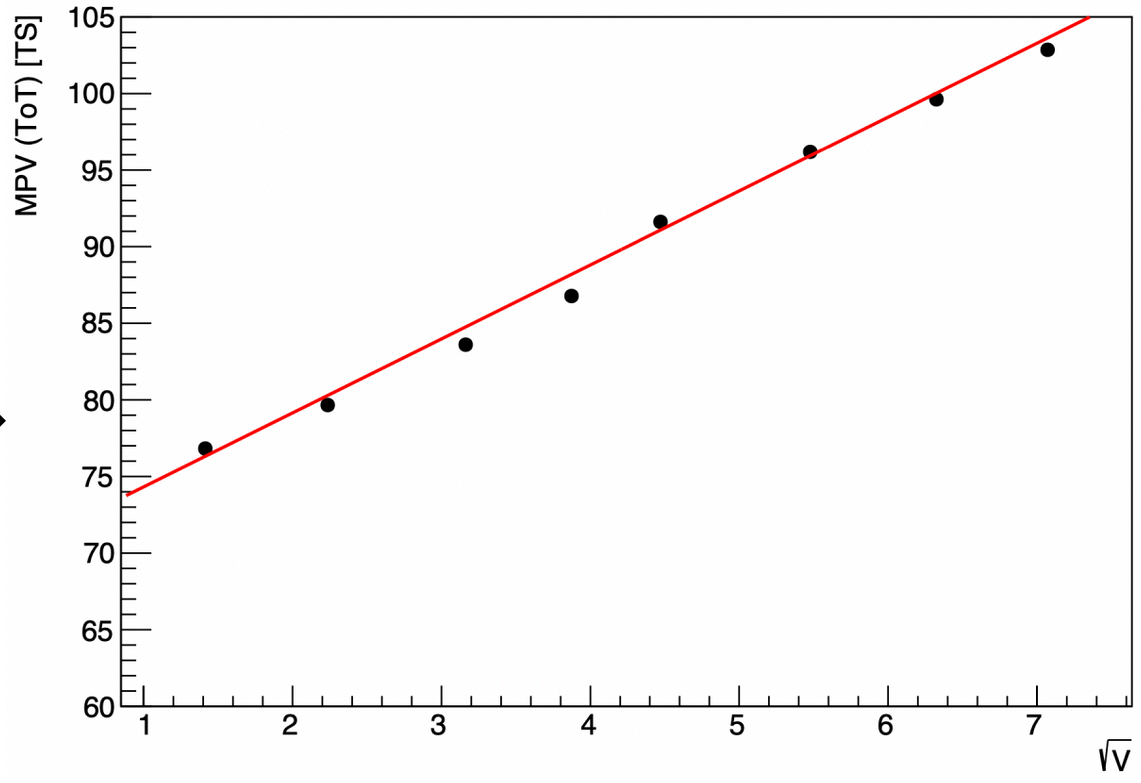


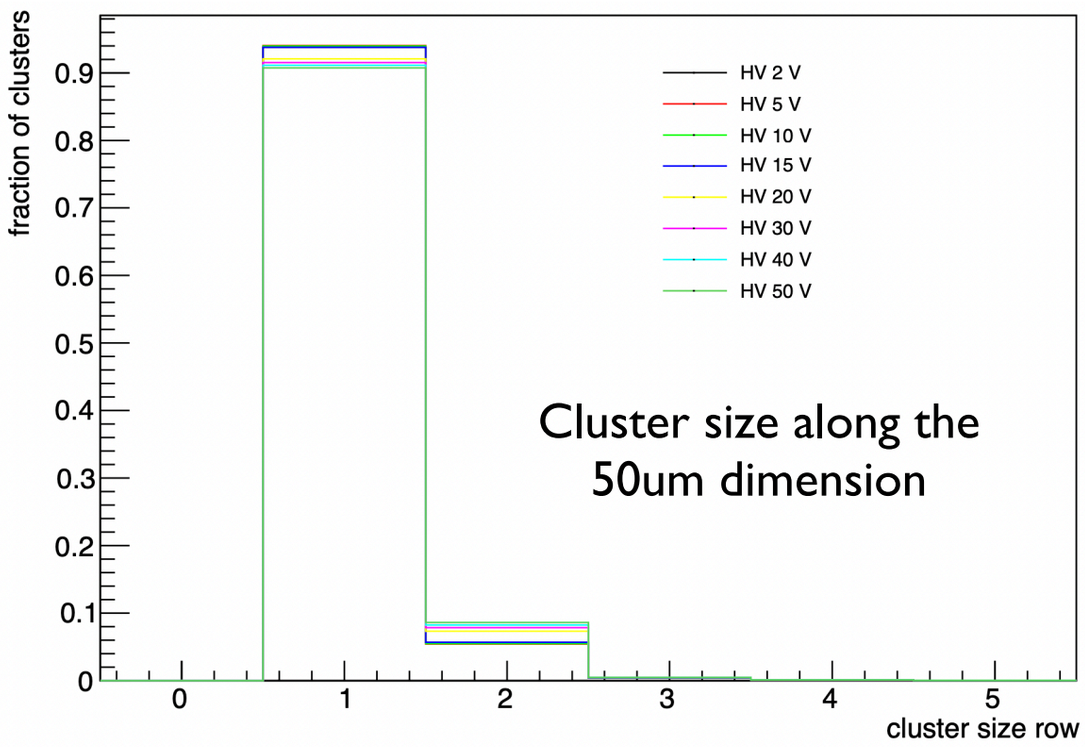
- Testbeam at DESY April 2022
- Two 4-layer telescopes and a quad tested
- Readout and reconstruction:
  - Hit driven readout
  - Reconstruction with Corryvreckan
  - Iterative alignment of the layers
  - Tracking through 3 or 4 layers
  - An arbitrary layer can function as DUT, here layer 3 is used as DUT



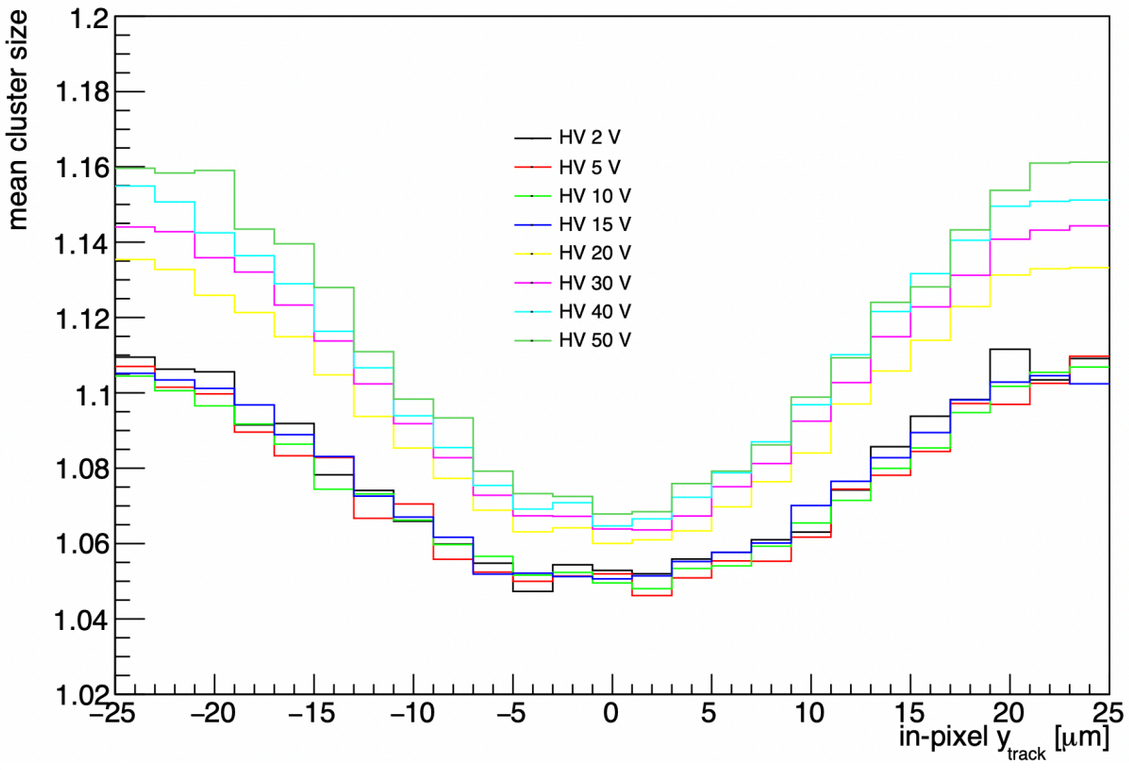
DESY Test Beam Analysis - ToT and Clusters



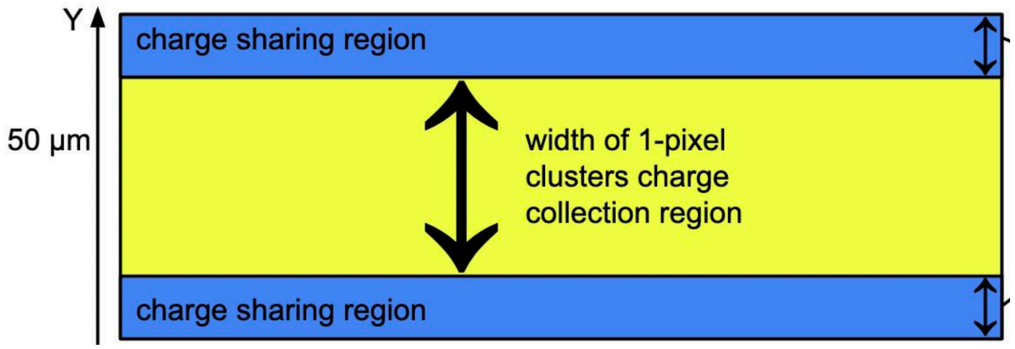




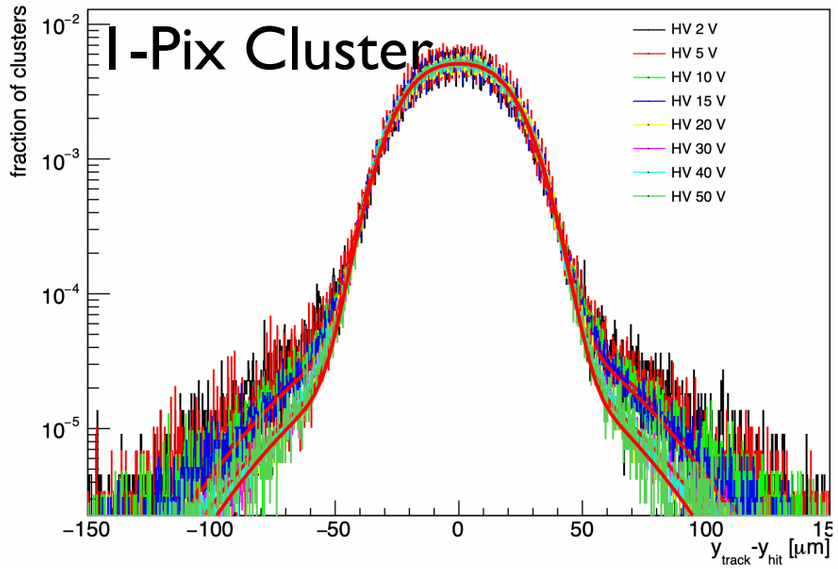
For HV>20V the region between pixels gets depleted

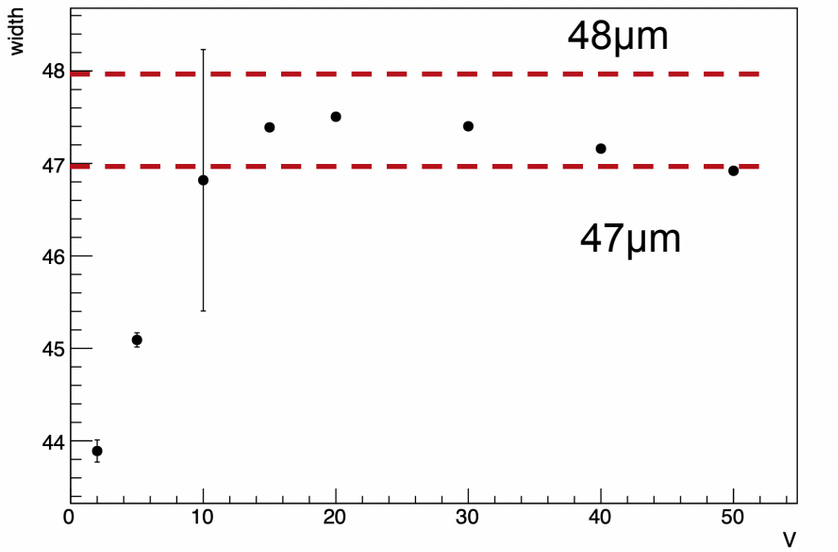


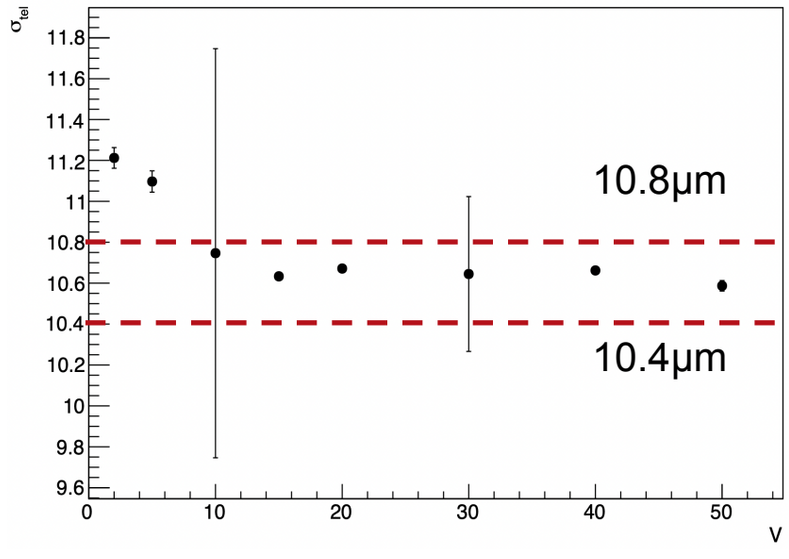
DESY TestBeam - Telescope resolution

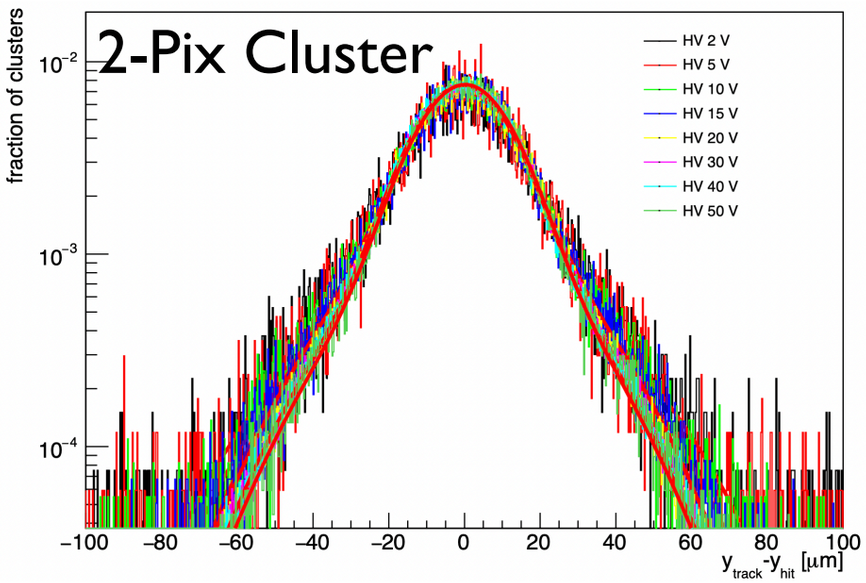


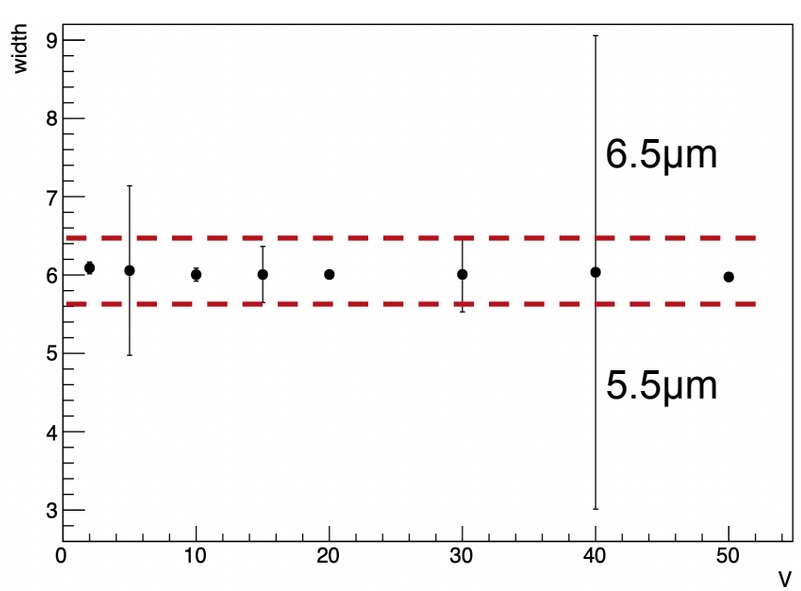
$$f(x) = [S(x|l,r,C)+G_{bkg}(x|\mu_{bkg},\sigma_{bkg})]*G_{tel}(x|\mu_{tel},\sigma_{tel})$$

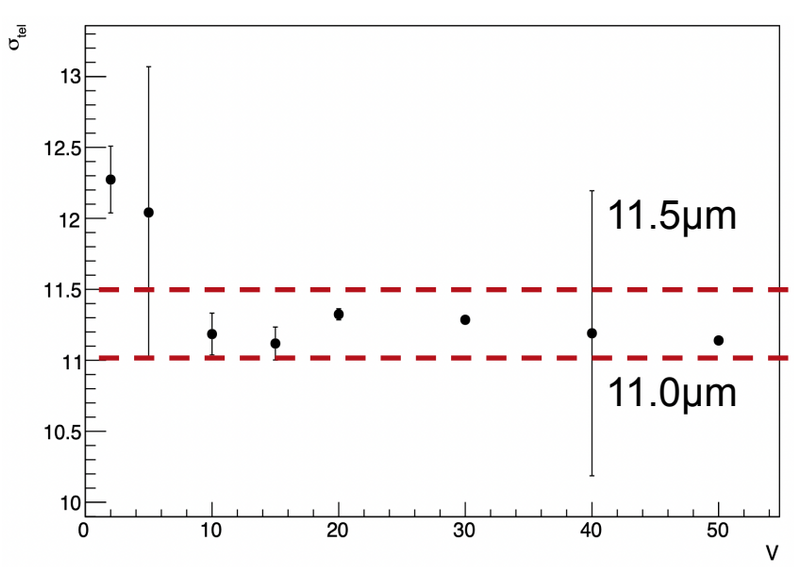






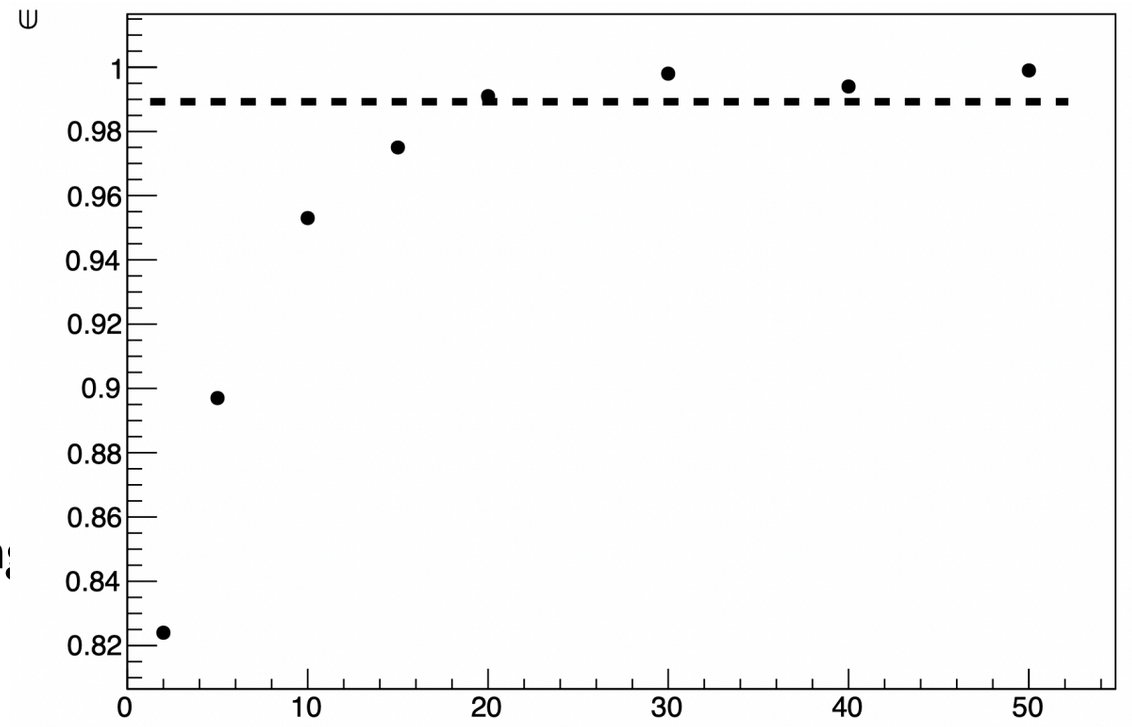


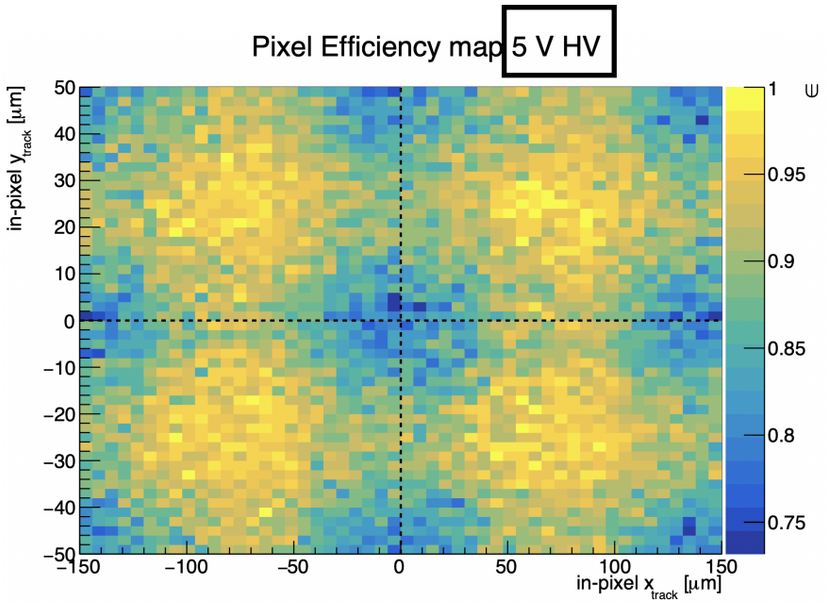


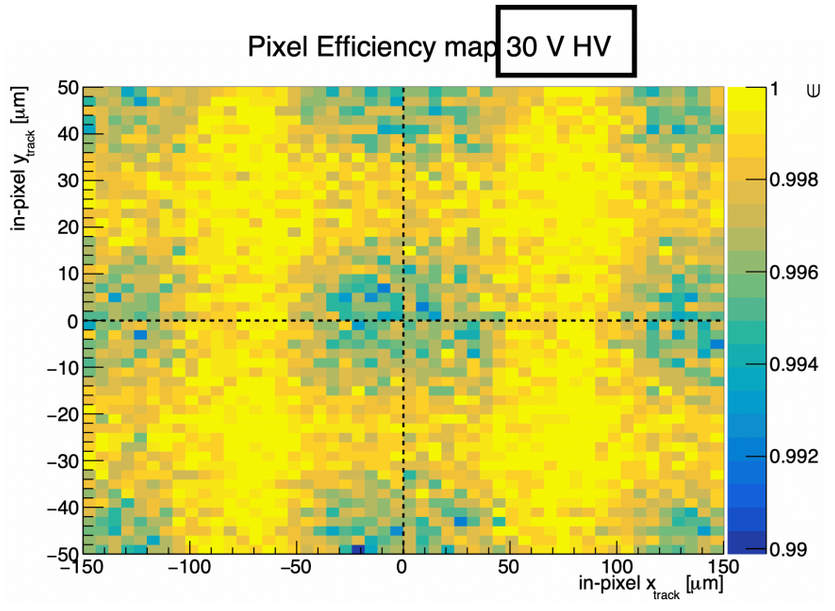


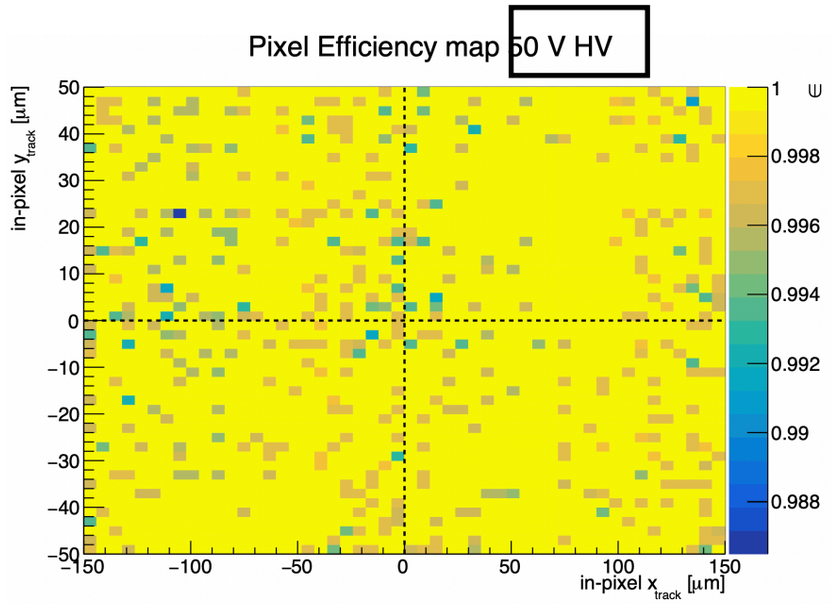
DESY TestBeam - Efficiency

- After 20 V
  - Overall efficiency > 99% achieved after 20V
  - Inefficiencies in the charging sharing regions recovered
  - This gives a relatively wide bias operational ran



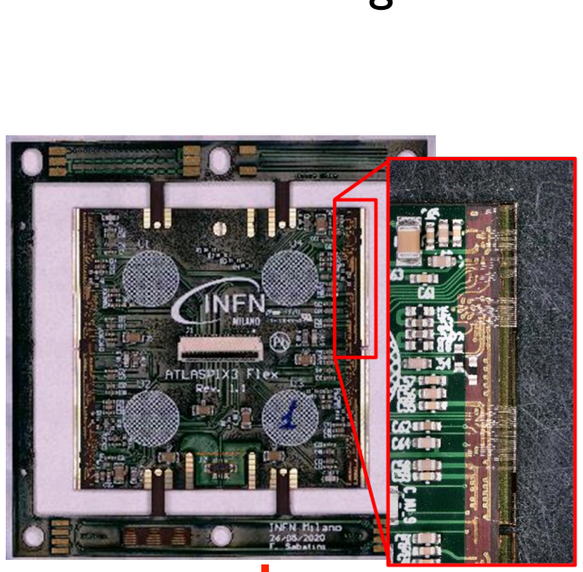


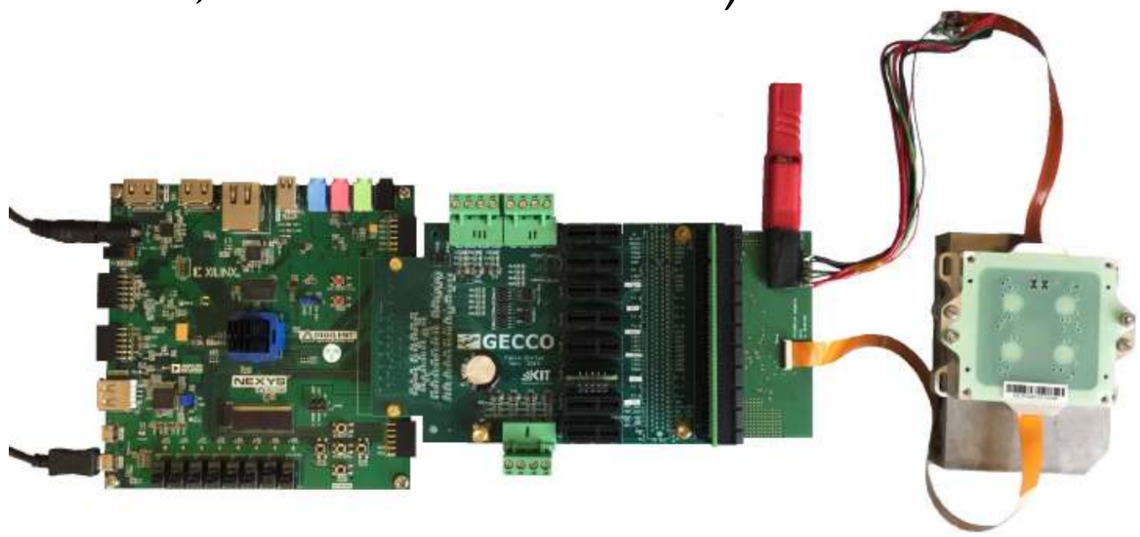


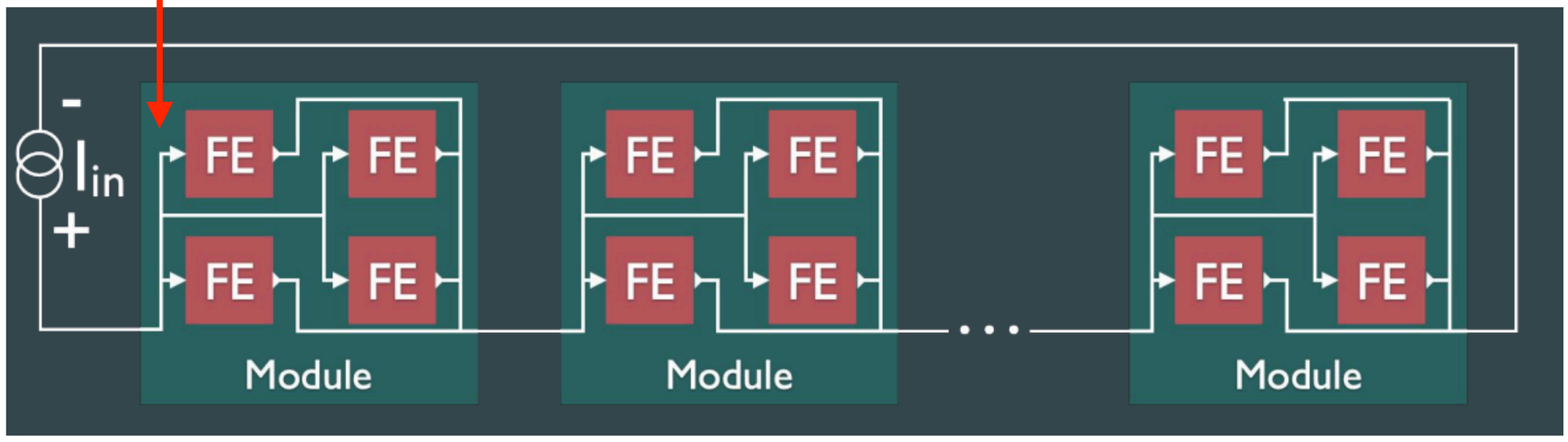


Quad module and Serial Powering (SP) Chain

- ATLAS ITk pixel detector inspired quad module and SP chain is being developed using ATLAPix3 for data aggregation and power distributions
  - 4 modules within a quad share data, and bias
  - Dedicated changes in flex, readout (hardware, firmware and software)



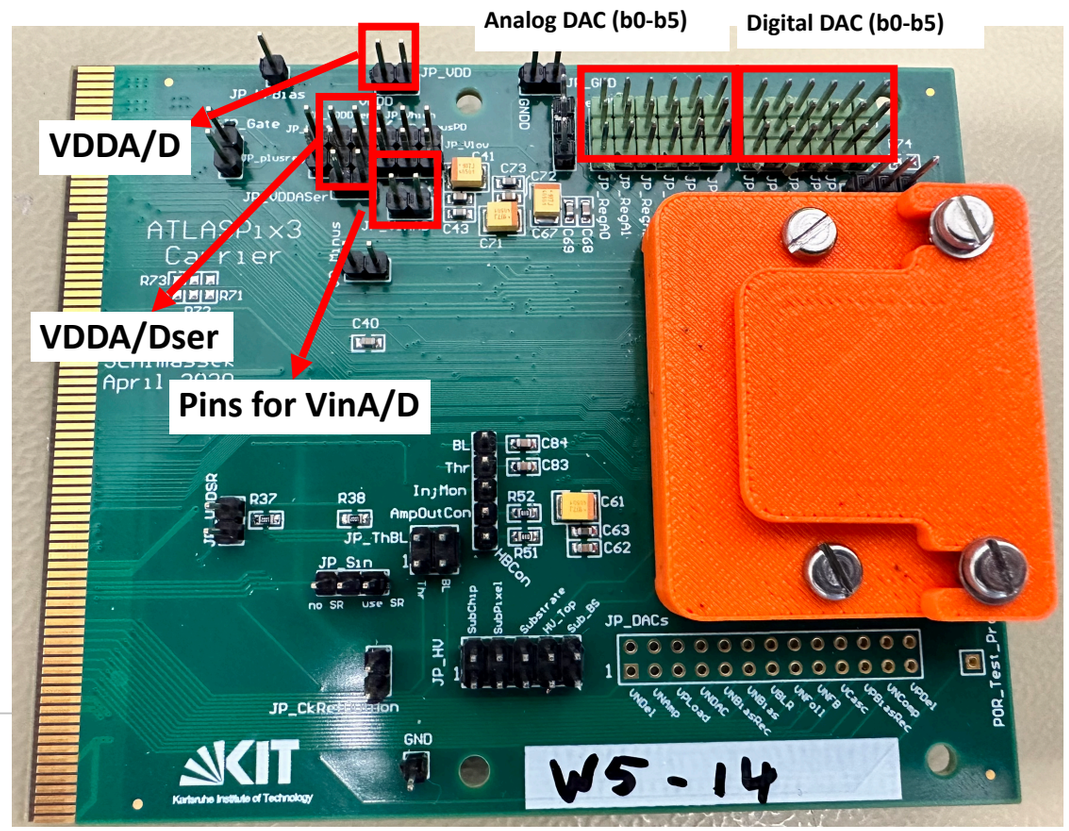


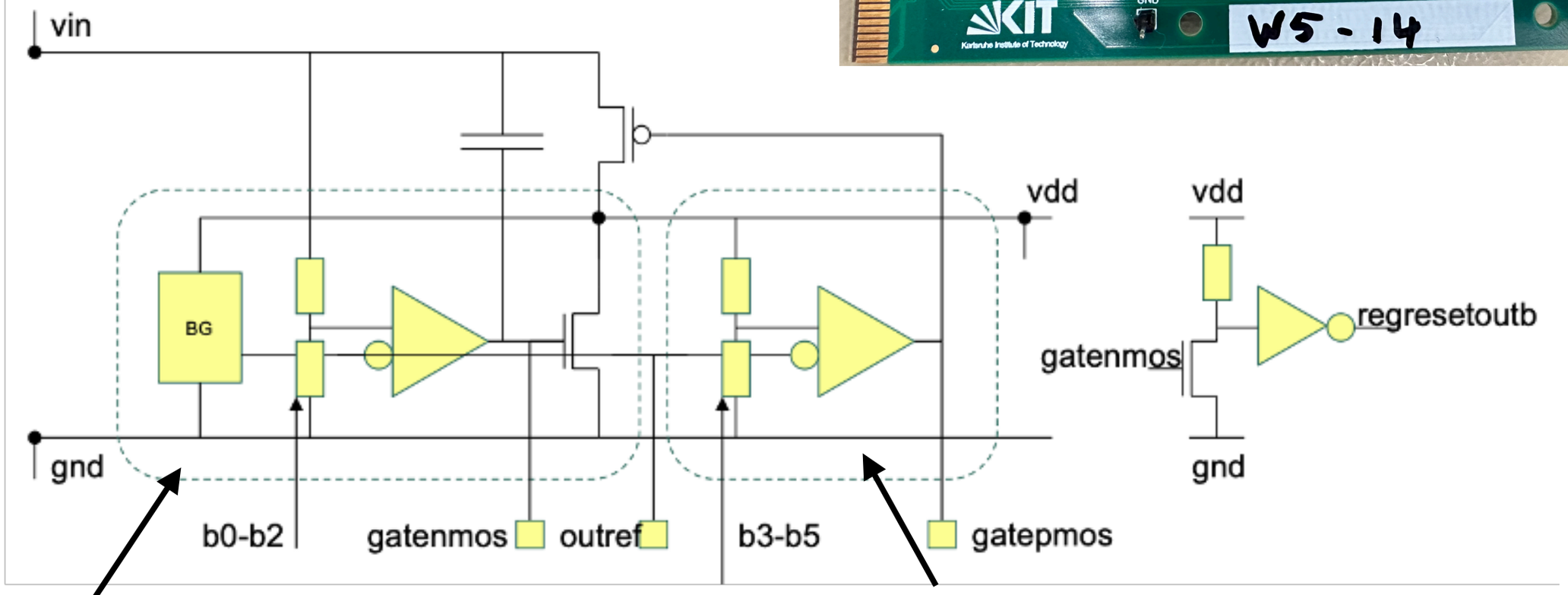


J. Chan, ATL-ITK-SLIDE-2022-674

ATLASPix3 SLDO features

- Two steps SLDO regulators for VDDD/A separately
  - 3 bits to tune threshold of shunt regulator
  - 3 bits to tune VDD
  - gatenmos, outref, gatepmos are for monitoring
  - regresetoutb can be used as power on reset
- This allows for constant current operation mode
  - Greatly simplified the operation power supply
  - Serial Powering chain of multi-quads



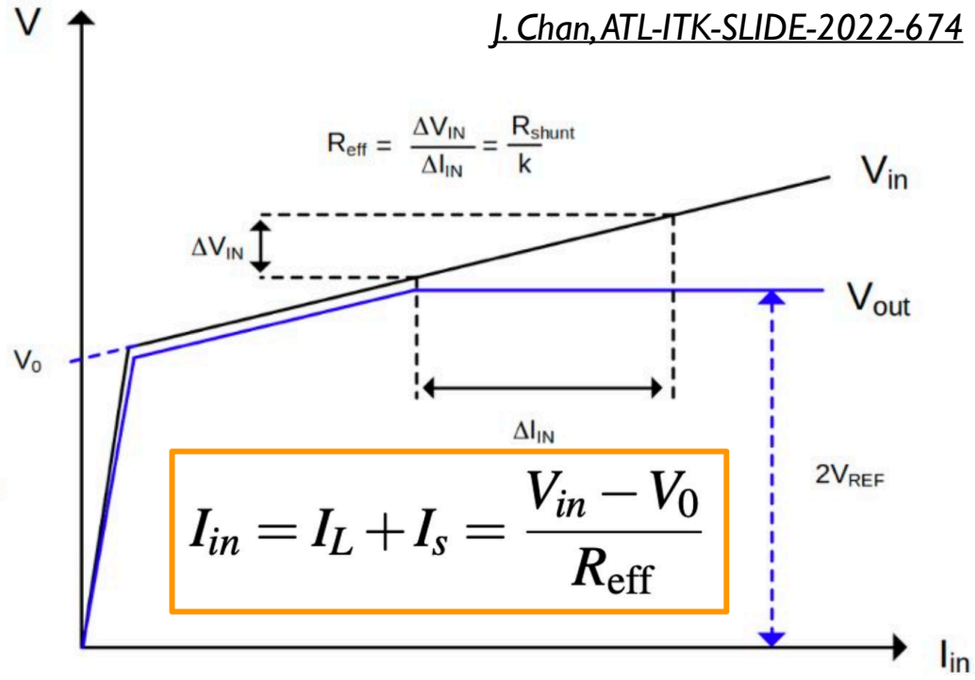


First Loop: Shunt regulation

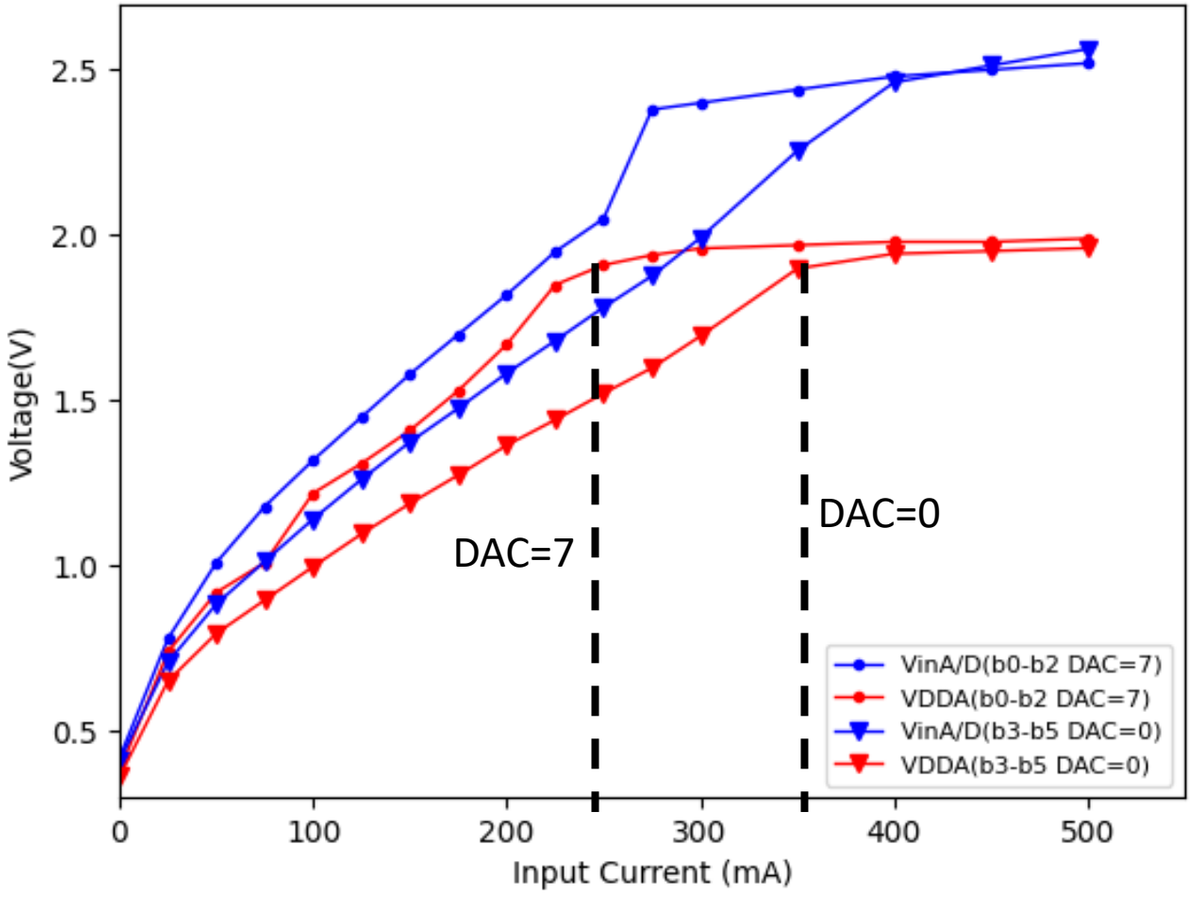
Second Loop:VDDD/A regulation

SLDO IV characterisations - single chip

- Current threshold can be tuned within ~50mA (measurements fluctuate a bit)
- Ohmic behaviour is verified after threshold
- Output Small tuneable range for the output



Analog Circuit, Chip W5-14 Regulator Turn-on Curve



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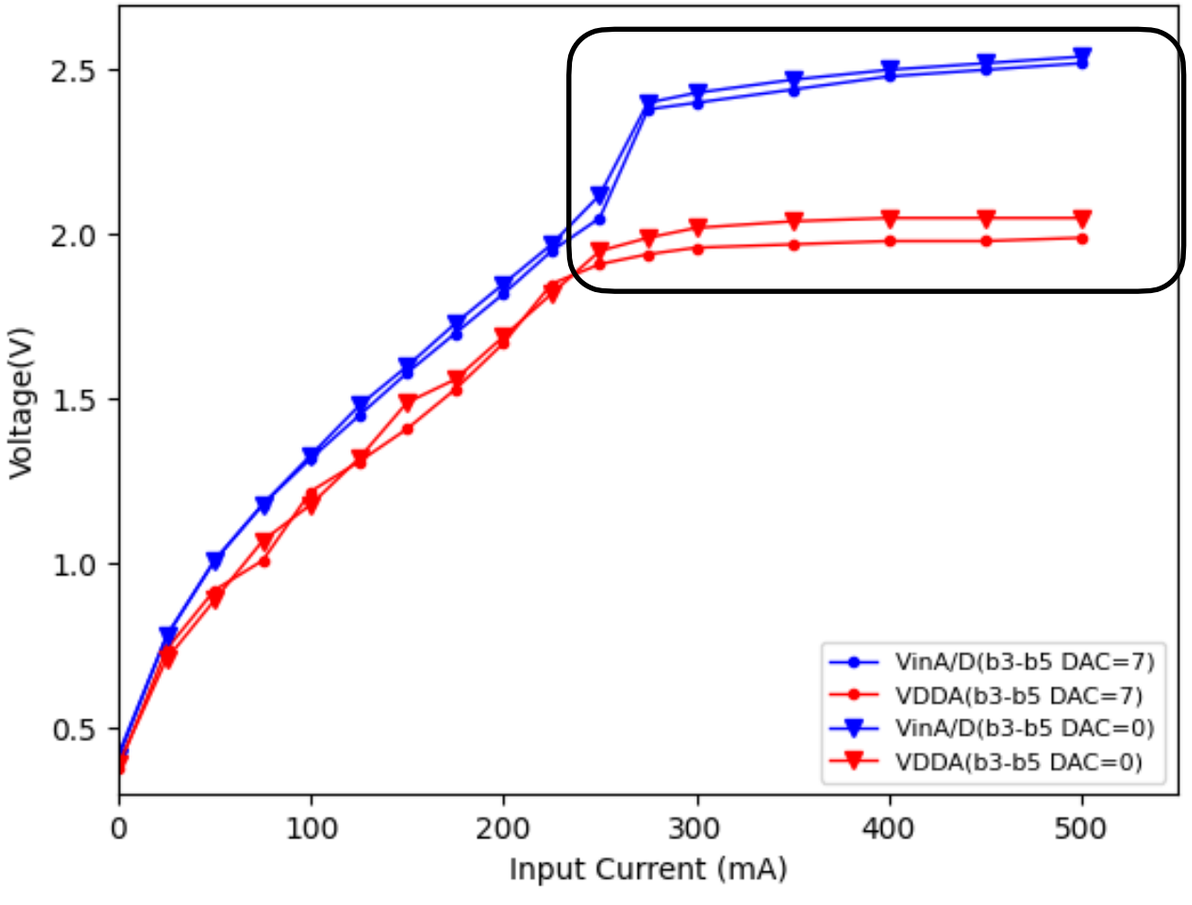
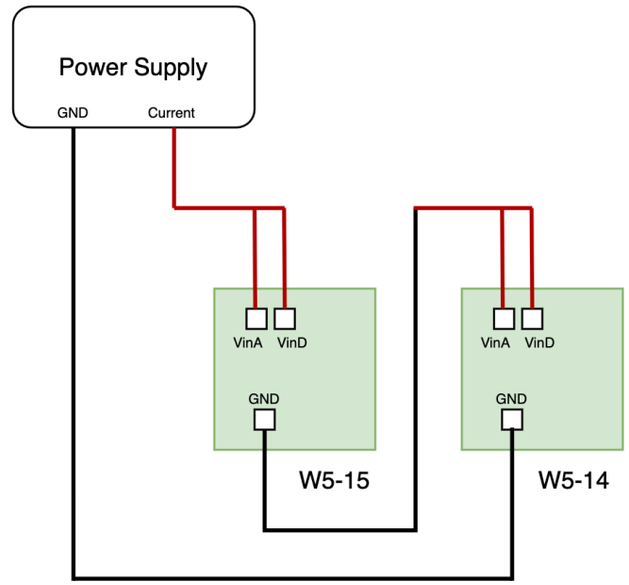
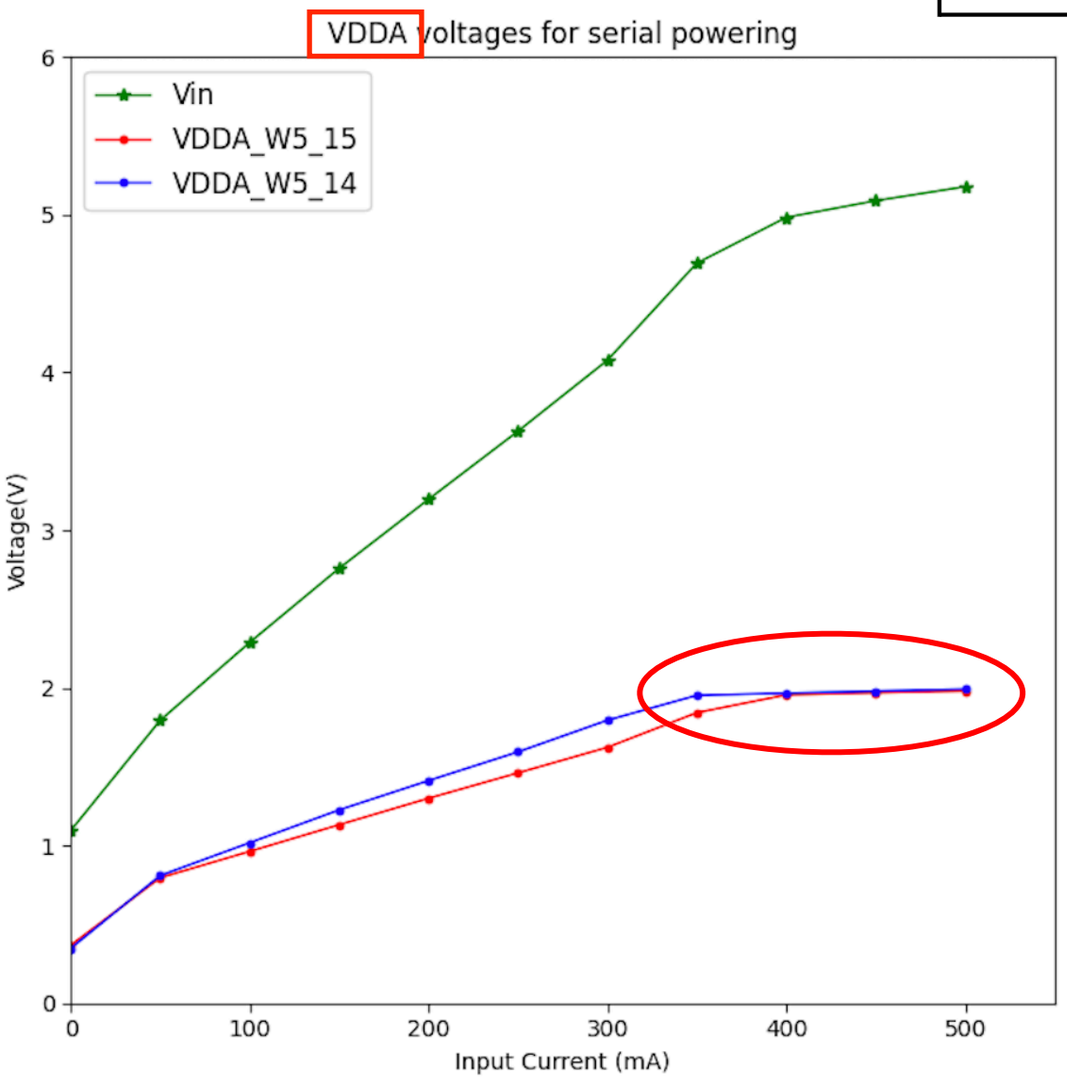
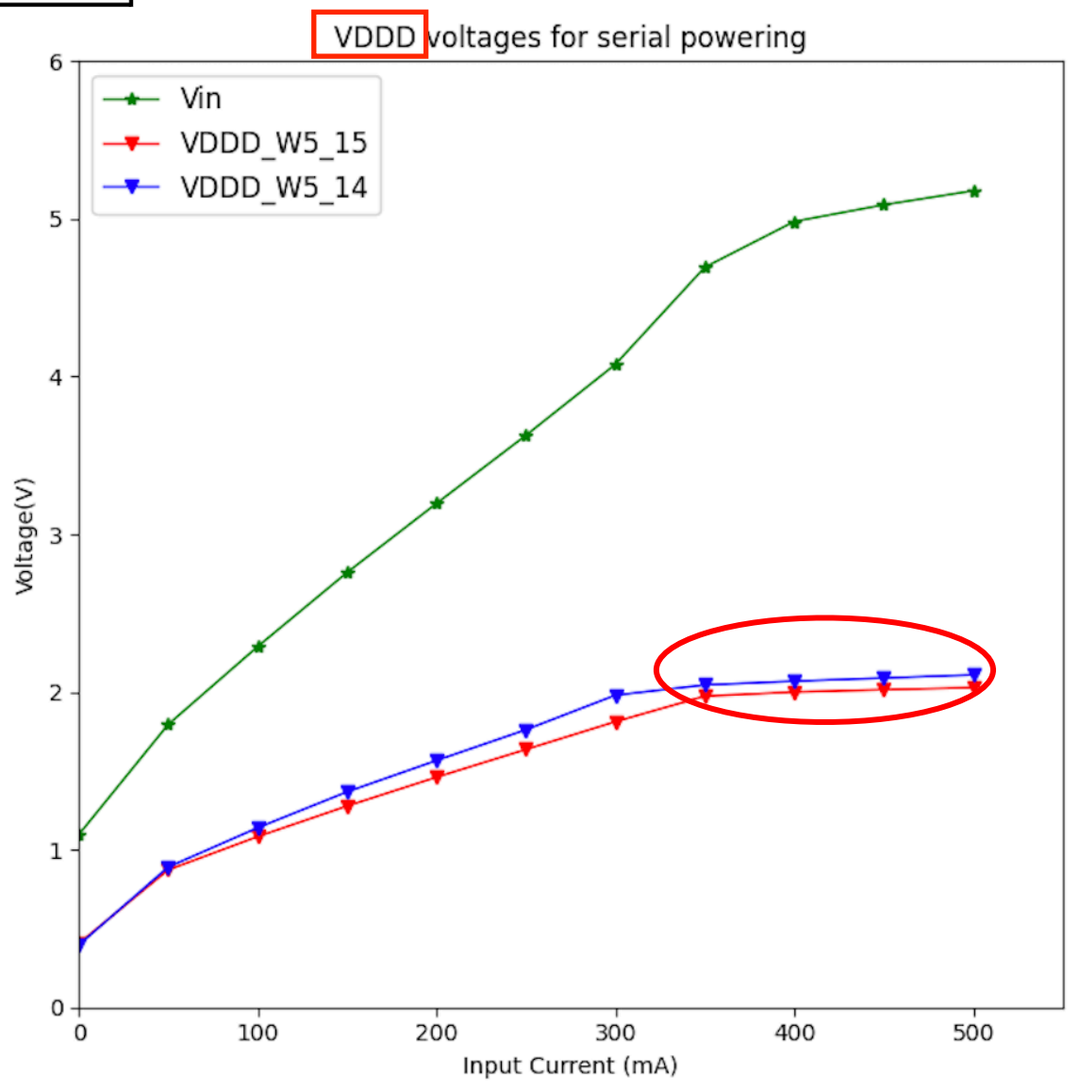


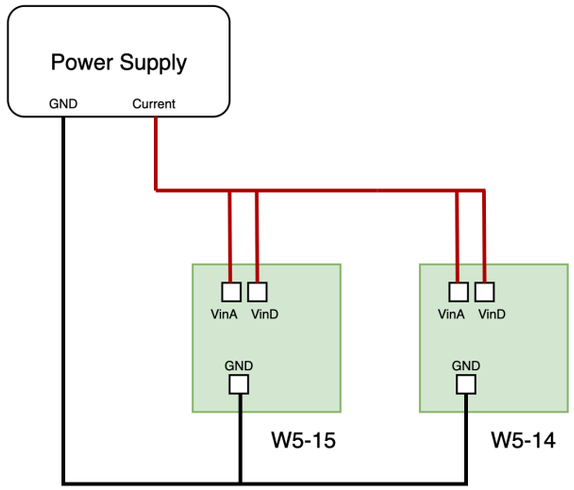
SLDO characterisation - Two chips in Serial

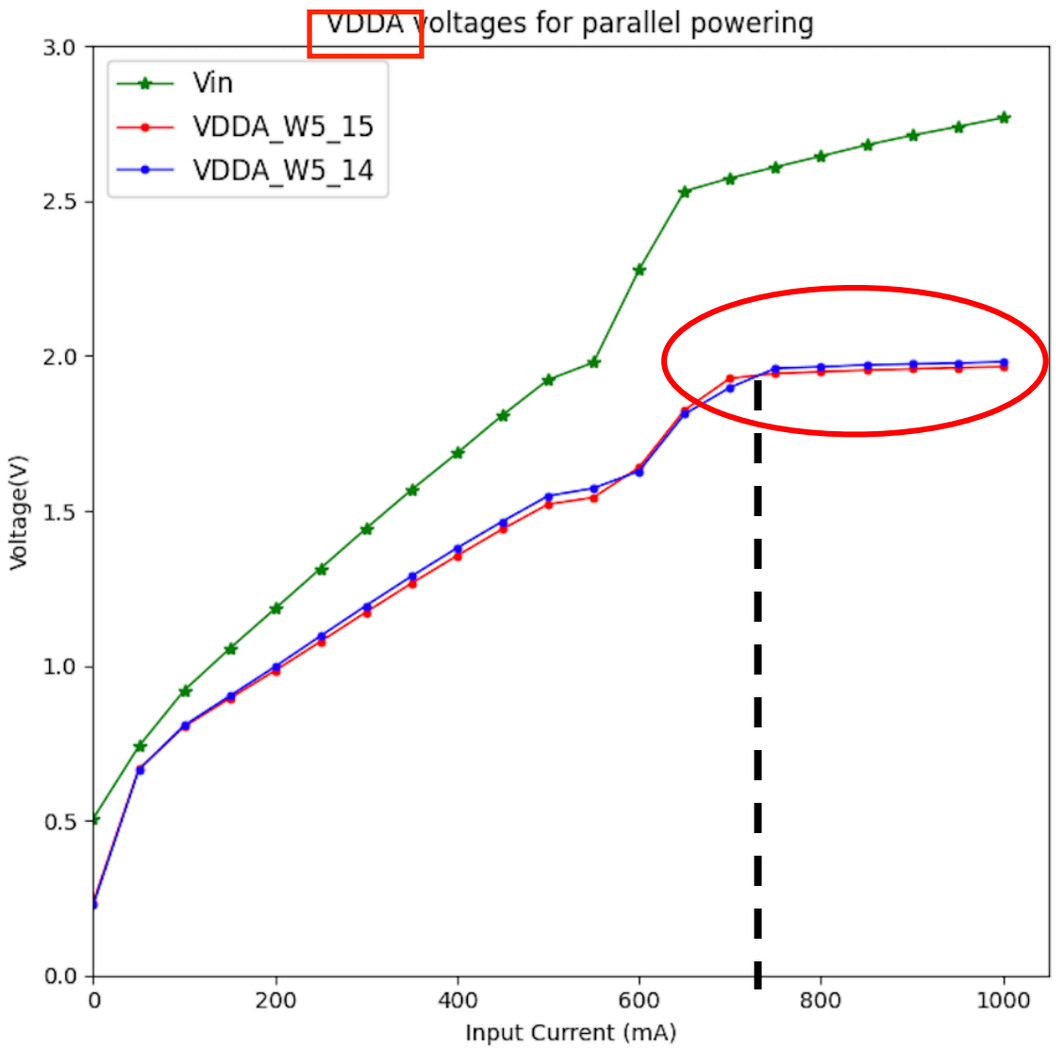


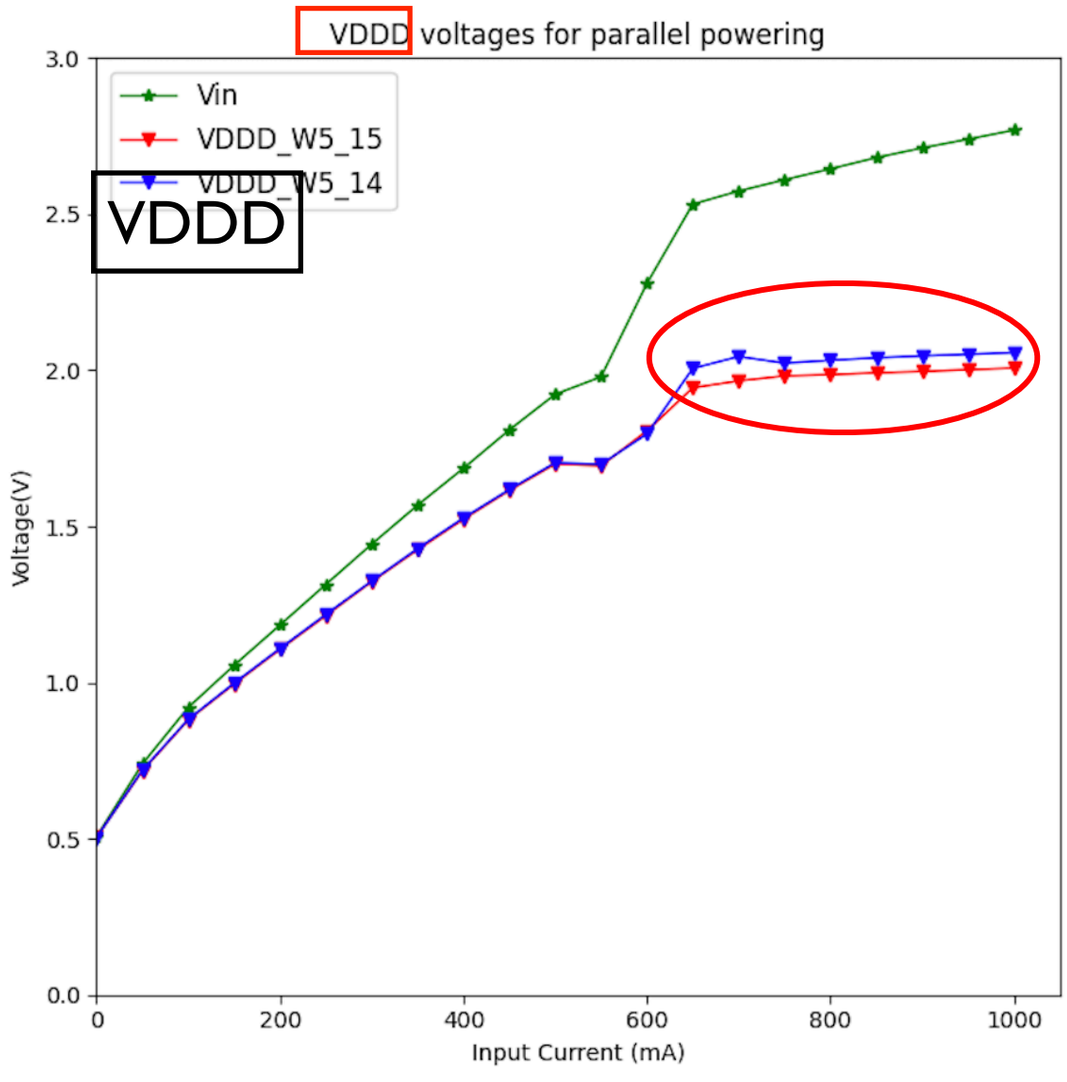




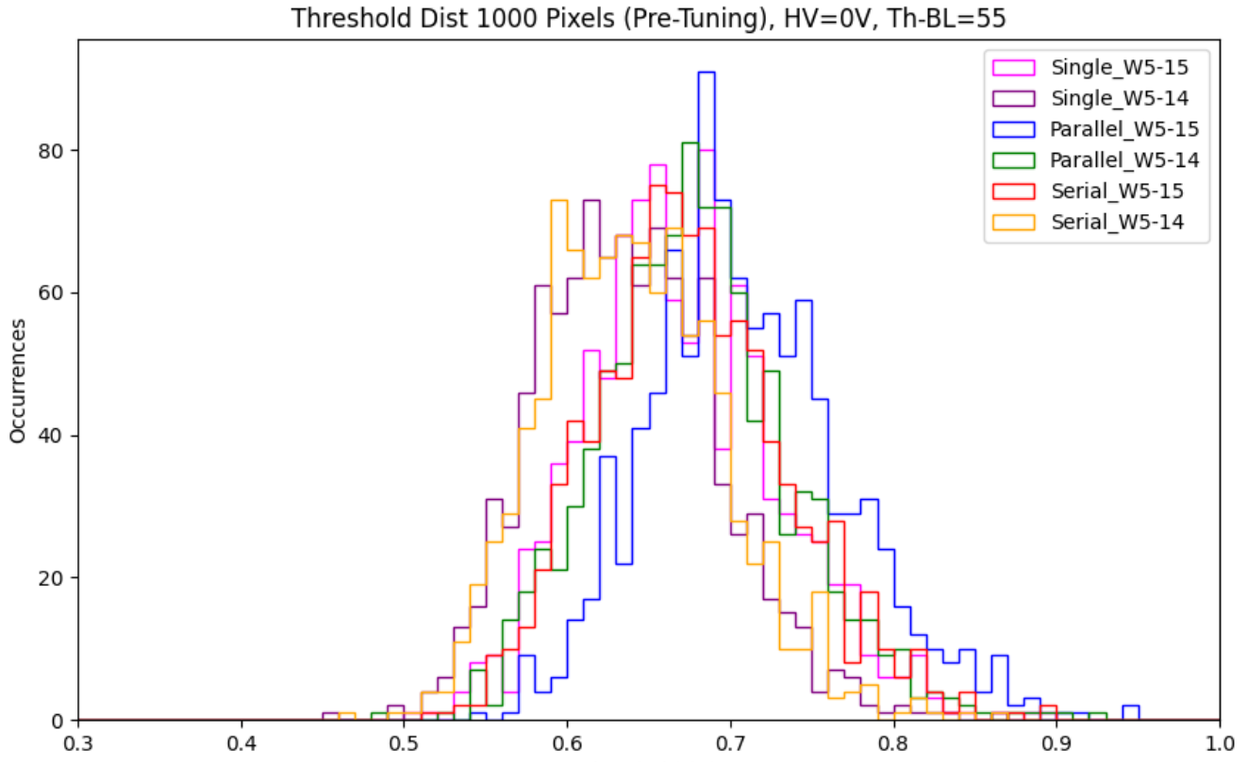
Shunt-LDO characterisation - Two chips in Parallel

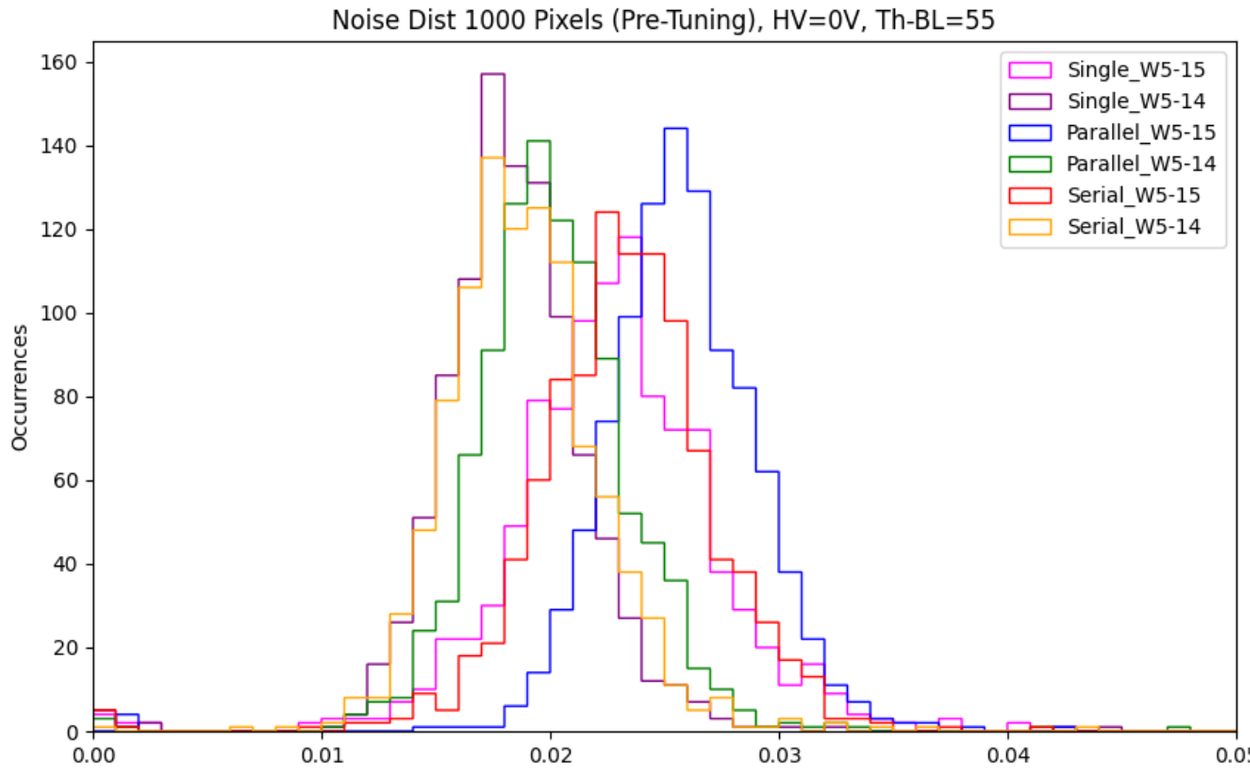






Multi-chip readout and characterisation



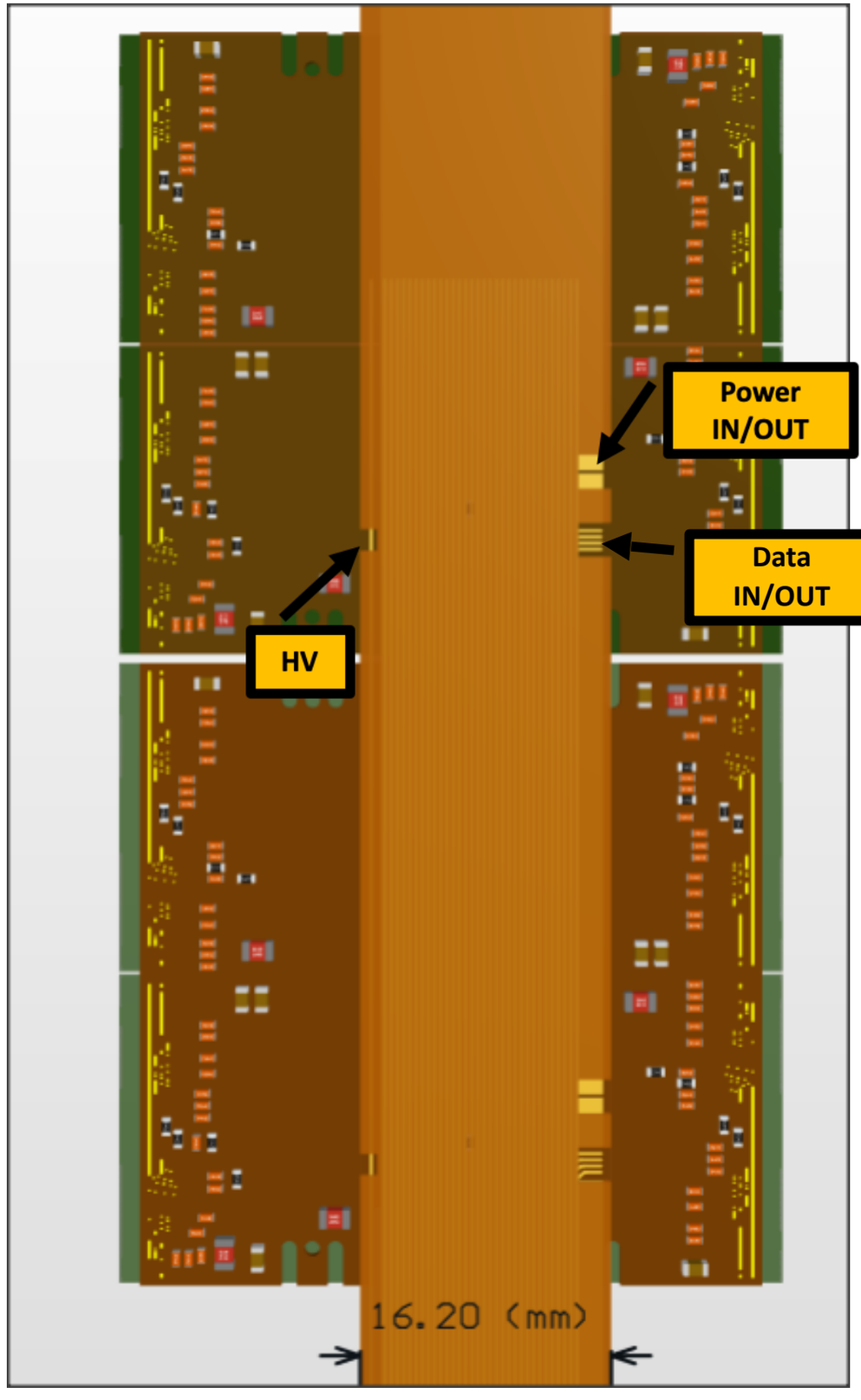


- Very minor degrading with the same thresholds when connected in parallel

	Constant Current Single		Constant Current Parallel Connection		Constant Current Serial Connection	
	Threshold (V)	Noise (V)	Threshold (V)	Noise (V)	Threshold (V)	Noise (V)
SCC (W5-15)	**0.670 ± 0.0591**	**0.0227 ± 0.00462**	0.710 ± 0.0613	0.0257 ± 0.00348	**0.676 ± 0.0593**	**0.0233 ± 0.00407**
SCC (W5-14)	**0.638 ± 0.0554**	**0.0184 ± 0.00341**	0.678 ± 0.0591	0.0202 ± 0.00408	**0.640 ± 0.0558**	**0.0189 ± 0.00341**

Quad-module → Stave electrical bus considerations

- Distribution of power and data along the stave
  - reducing power dissipation on the distribution lines
  - minimise the number of connections
- Read-out units
  - Multi-chip modules (example 2x2 quad modules)
    - Or large stitched detectors
  - Bias in parallel all sensors in a module
- Serial powering chain supplied by constant current
  - All biases are generated internally by SLDO and on-chip regulators
  - Chip-to-chip data transmissions: local data aggregation on module (not on APix3)
  - clock data recovery (not on APix3)
- Reduce material by developing PCB with Al as conductor



Summary and Next Steps

- ATLASPix3 has been used as HV-CMOS demonstrators beyond the original ITk upgrade
  - Ideal for the short-term R&D on multi-chip readout systems
- Presented here preliminary findings of APix3 based system prototyping
  - First quad module assembled and tested - big step towards large area application
  - Second quad module flex based on ATLASPix3.1 have been produced and ready to be assembled
  - Shunt-LDO has been verified at single chip and double-chip structure
  - Prototyping for mechanic and cooling are being pursued
- In the next 2-3 years we aim to finish the ATLASPix3.1 based system prototyping
  - Assembly and tests O(5) quad-modules, and integrate 2-3 quad-modules on a serial powered chain on top of a O(60cm) power bus (e.g. Al flex at CERN)
  - In parallel seek funds to continue to contribute to smaller scale MPW for sensor improvements (some earlier results indicate potential to reduce significantly the power consumption)
  - This project was presented at the first DRD3 collaboration week with proposal in preparation
- In the long-run, we plan to integrate this with other more sensor-driven projects and to explore synergies with other experiments (e.g. LHCb MT, EPIC)

In memory of

Dr Roy Lemmon
STFC Daresbury

Professor Max Klein
University of Liverpool

Professor Ian Shipsey FRS
University of Oxford

for their passion, contribution, vision in detector instrumentation, Higgs factory, and so much more

Backup slides

Selected resources and references

- Most recent talks
  - ICHEP2024, A. Andreazza, https://indico.cern.ch/event/1291157/contributions/5888449/attachments/2900792/5087168/20240720_IDEASiTracker.pdf
  - ICHEP 2024, R. Zanzottera, : https://indico.cern.ch/event/1291157/contributions/5888448/attachments/2900868/5087024/atlaspix3_ichep2024.pdf
  - 2nd ECFA Workshop on e+e- Higgs/Electroweak/top Factories, A. Andreazza: https://agenda.infn.it/event/34841/contributions/208326/attachments/111412/158979/20231012_SiDetectorsForIDEA.pdf
  - DRD3 collaboration week, https://indico.cern.ch/event/1402825/contributions/6002306/attachments/2879169/5043446/20240617_LargeAreaProposal.pdf

ATLASPix3.1new vs 3.0

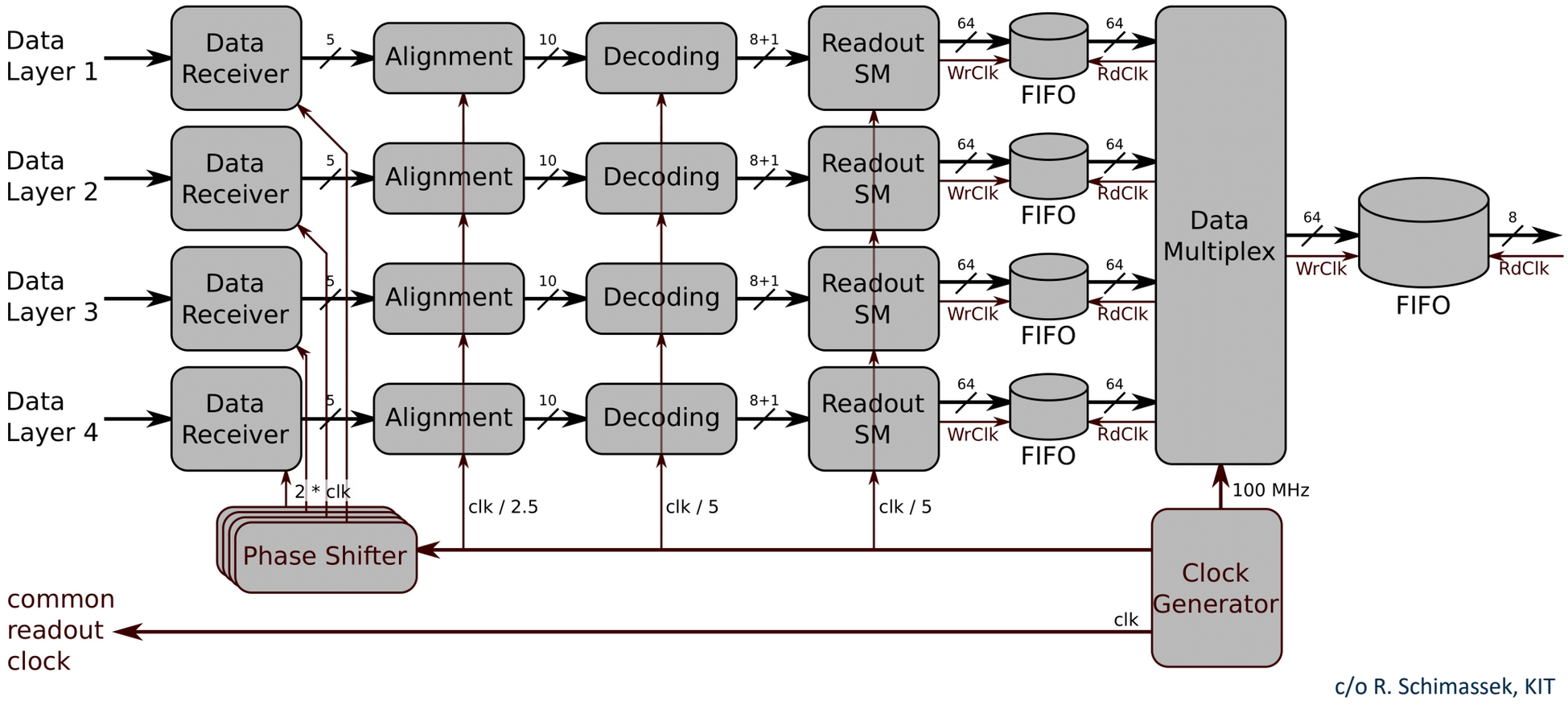
ATLASpix3.1

- ATLASpix3.1 submitted in December and delivered in February
- Redone masks for 8 Layers
- 12 wafers produced
- Reduced detector capacitance by replacing M2 shield with M3 shield (from about 250fF to 130fF)
- Modified design of the guard ring
  - Larger distance between DN and PW ring (see slides)
  - M1 ring disconnected from PW
  - Idea set substrate to -120V and M1 ring to -60V
- Added stability capacitor to the power regulator

Ivan Peric

Firm-/Software changes for quad

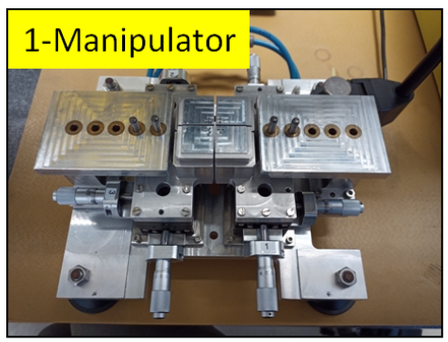
- Firmware:
  - Multiplication of the **elemental structure** for the single chip
- Software:
  - Configuration with SPI and CMD
  - Chips can be configured **simultaneously** or **individually**

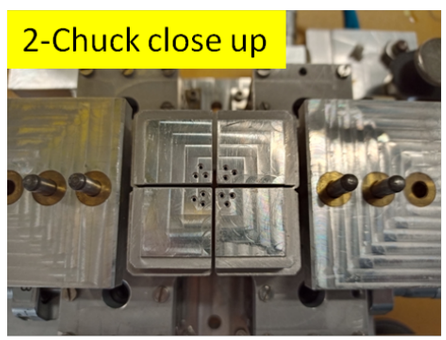


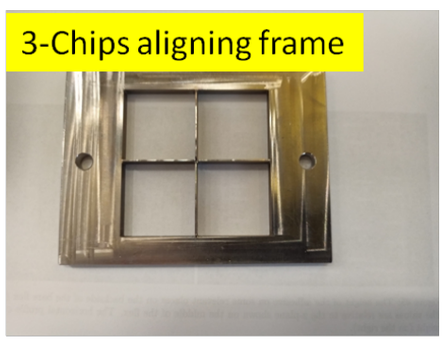
c/o R. Schimassek, KIT

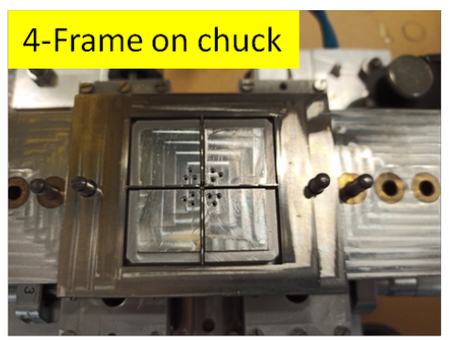
Assembly procedure

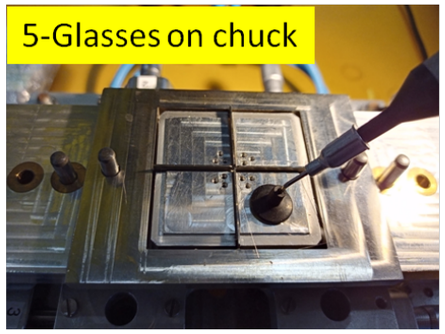
- Shown with **glass squares**: same procedure also used for real module assembly
- Gap between chip of **100 um ± 50 um** has been achieved

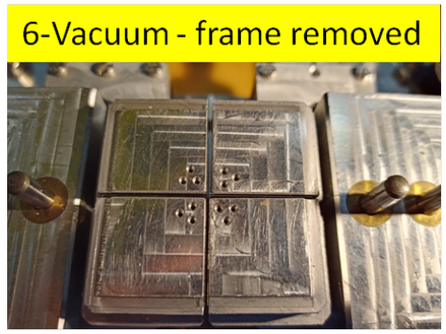


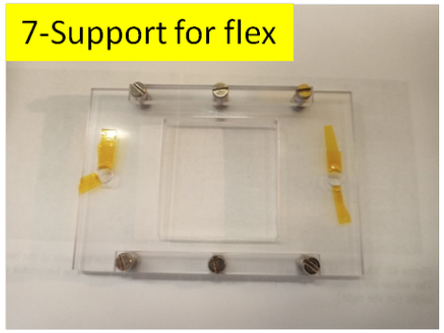


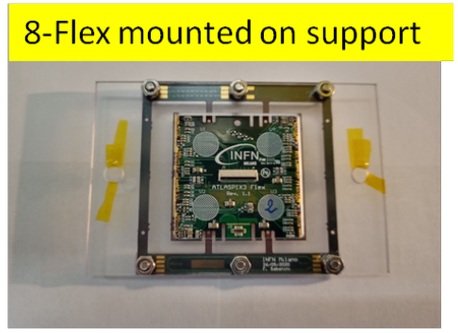


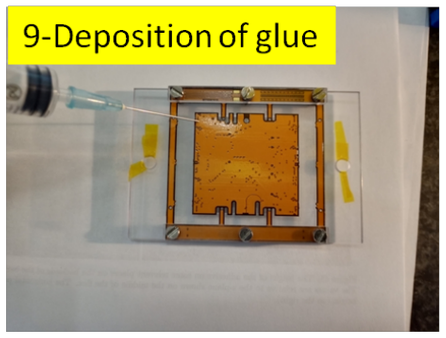


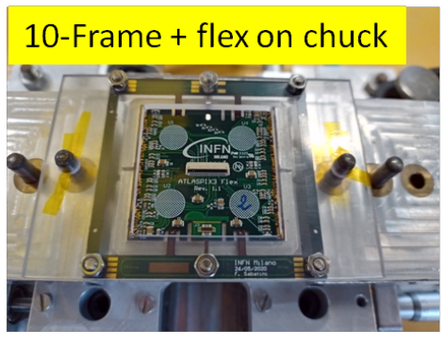


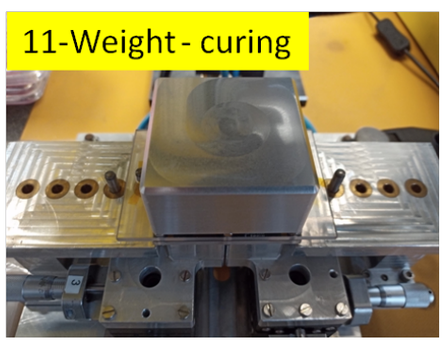


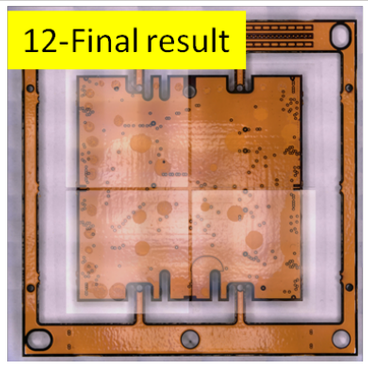






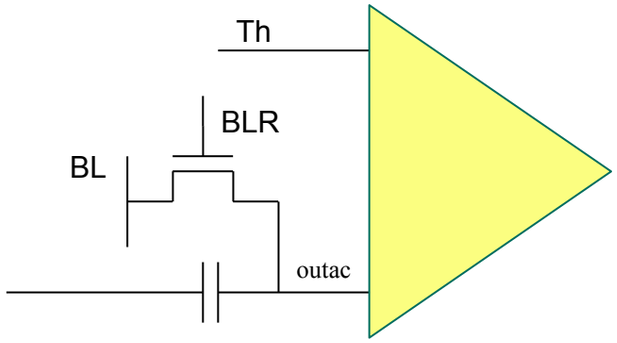


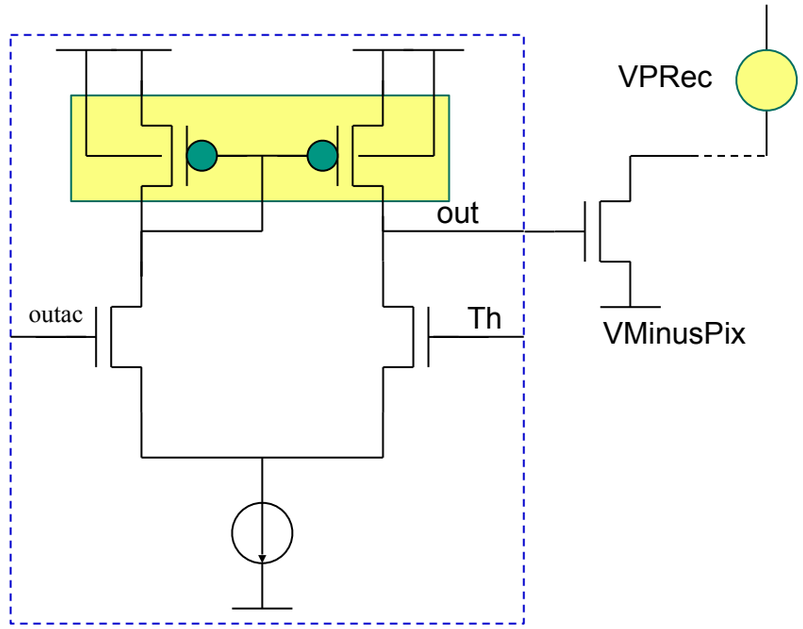


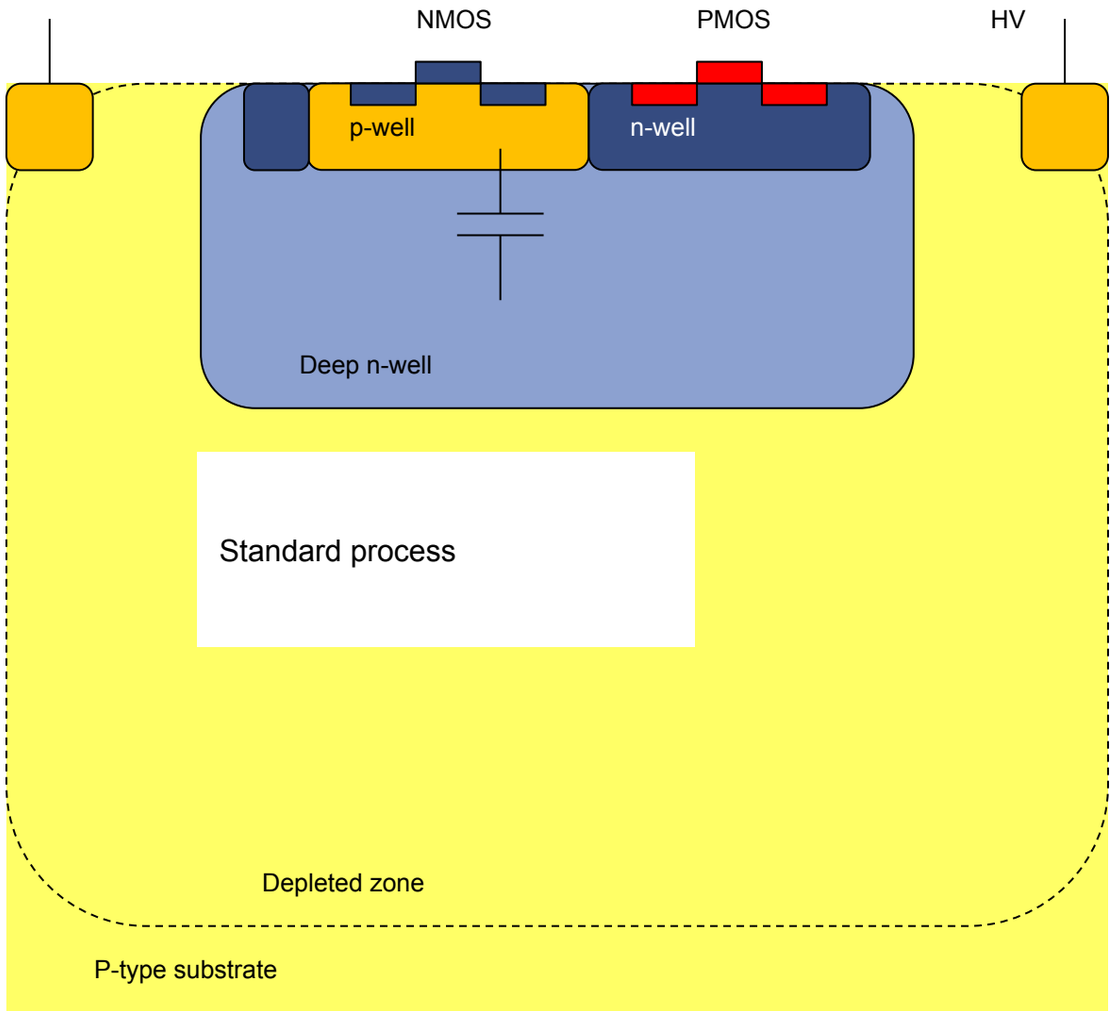


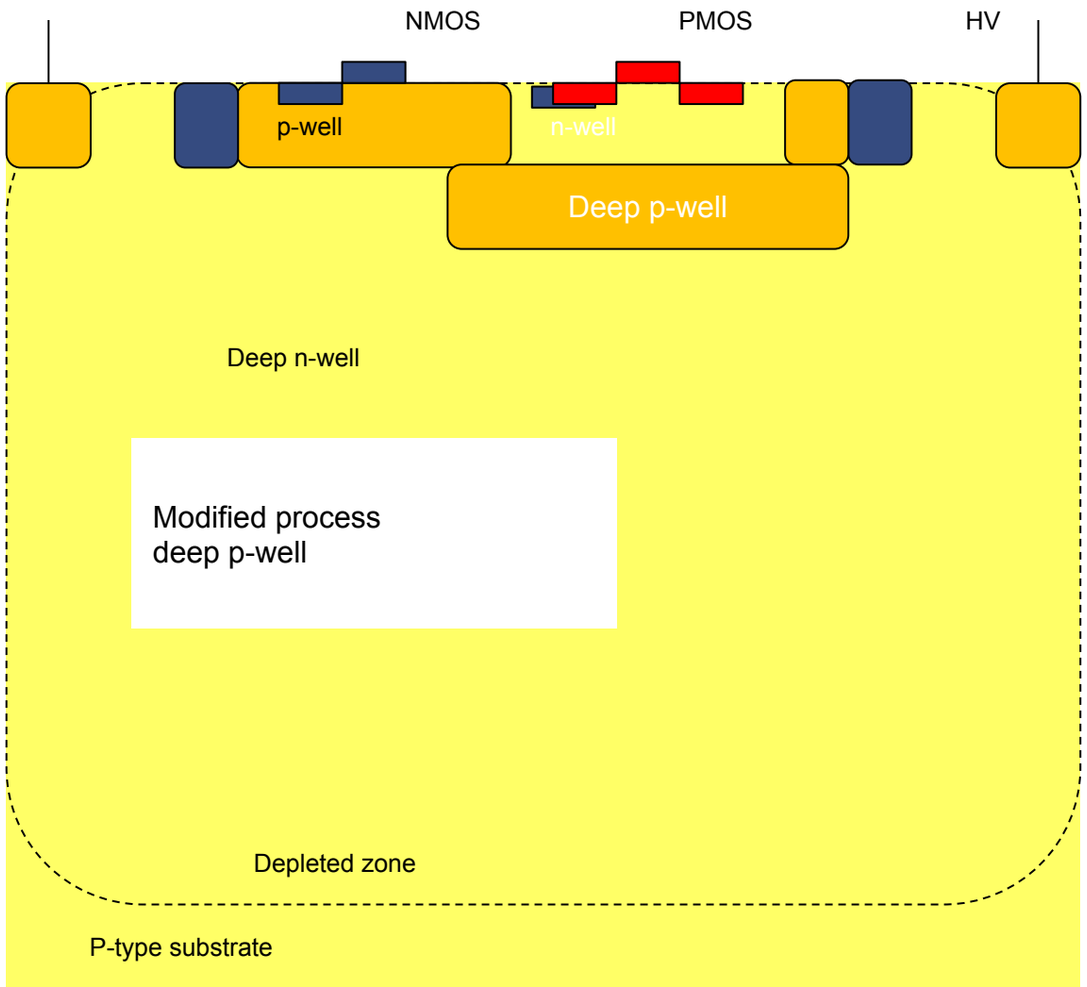
CMOS comparator

- Needs deep p-well
- Works with smaller bias current



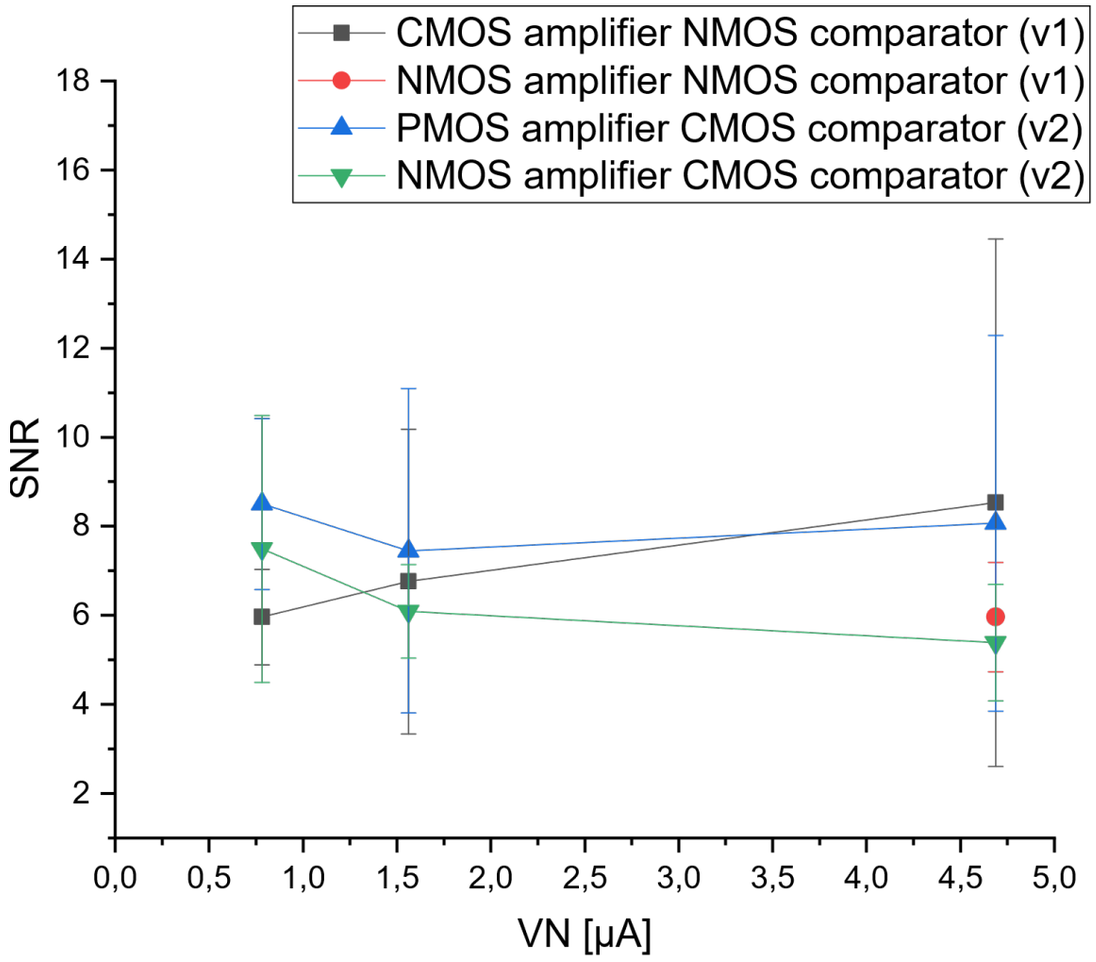


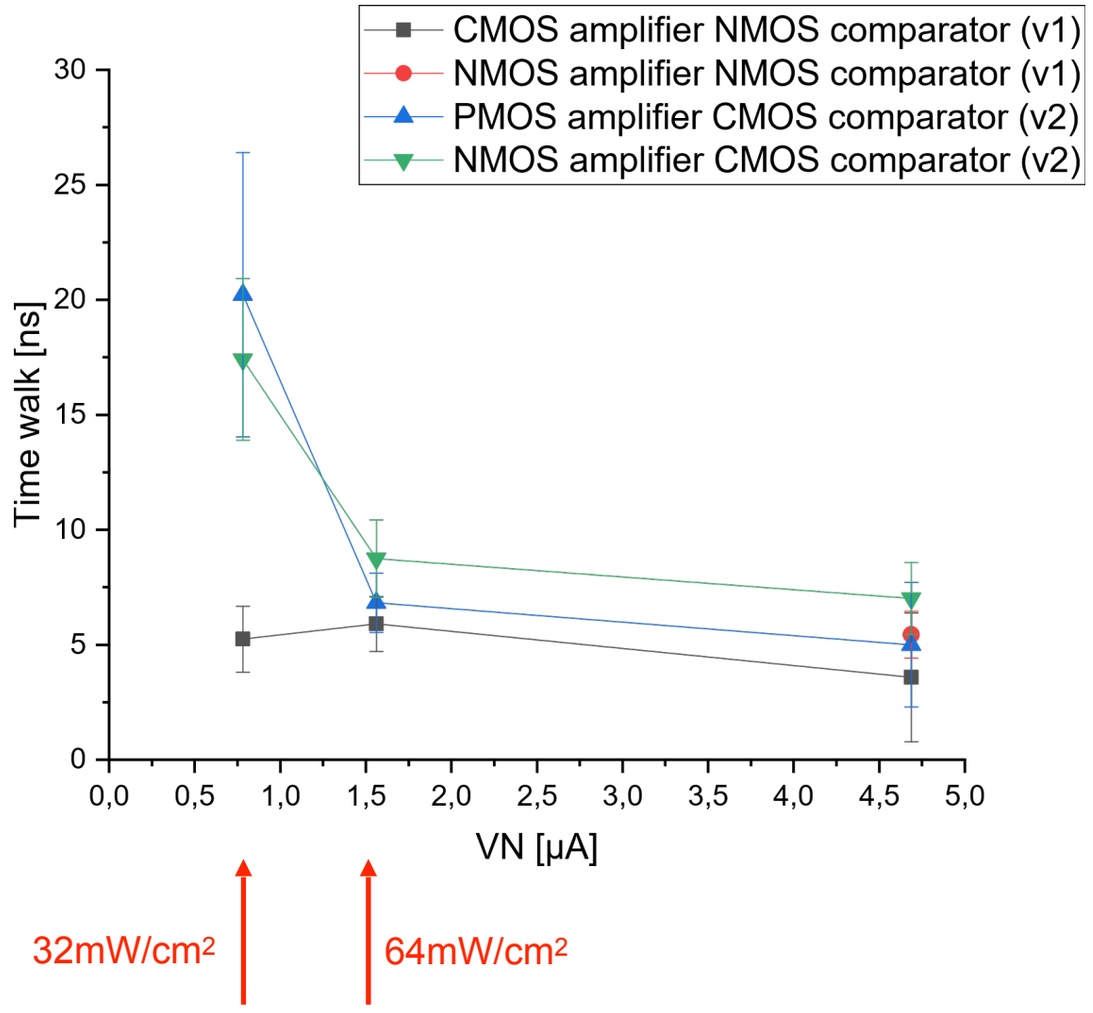




Preliminary measurements and implications

- Pixel matrices with three amplifier types have been operated with smallest possible threshold
- Signal to noise ratio (from ToT) and time walk for signals larger than 3200e have been measured
- CMOS amplifier has smallest time walk
- **Low power consumption is possible (up to factor of 4 reduction compared with ATLASPix3)**

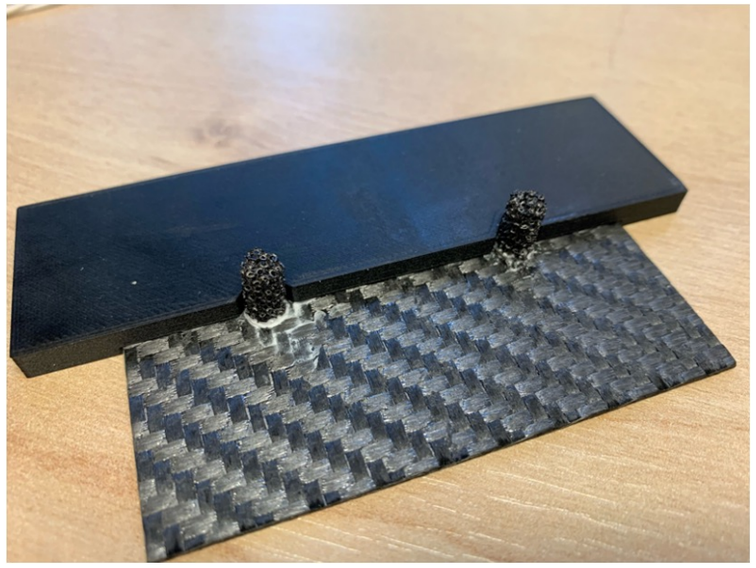


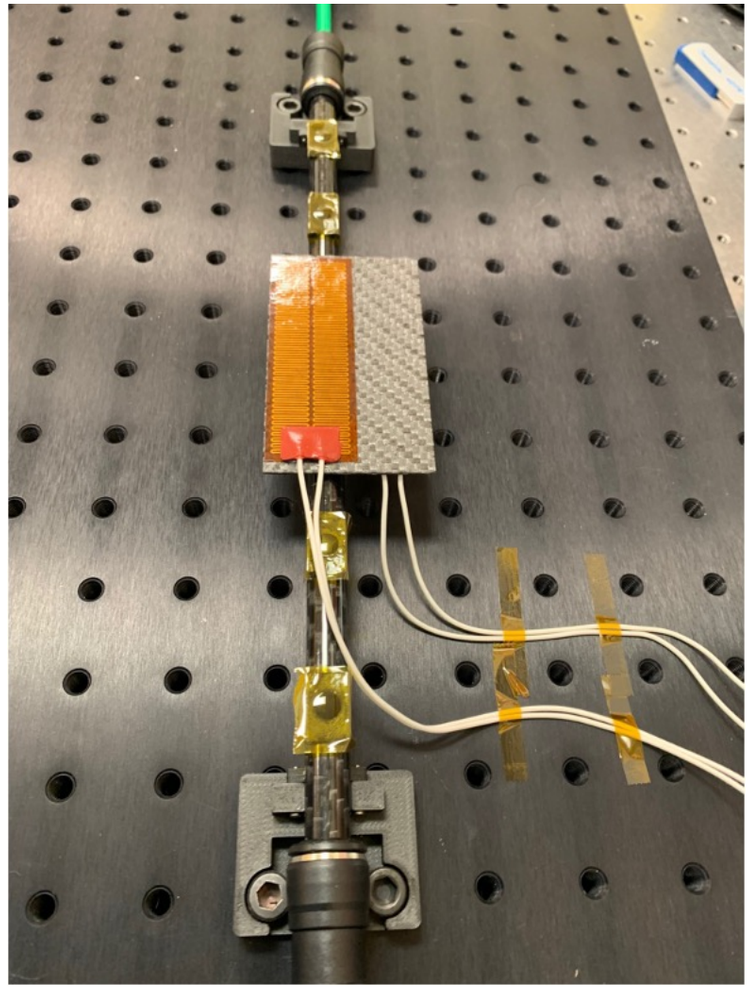


ATLASPIX3: 140mW/cm²

Pre-prototype thermal evaluations

Pre-prototype: Base attached to tube & heaters on





*First look: at 3.1W power (expected from 8cm*4cm area), temperature rise ~10 degrees w.r.t. CDA*

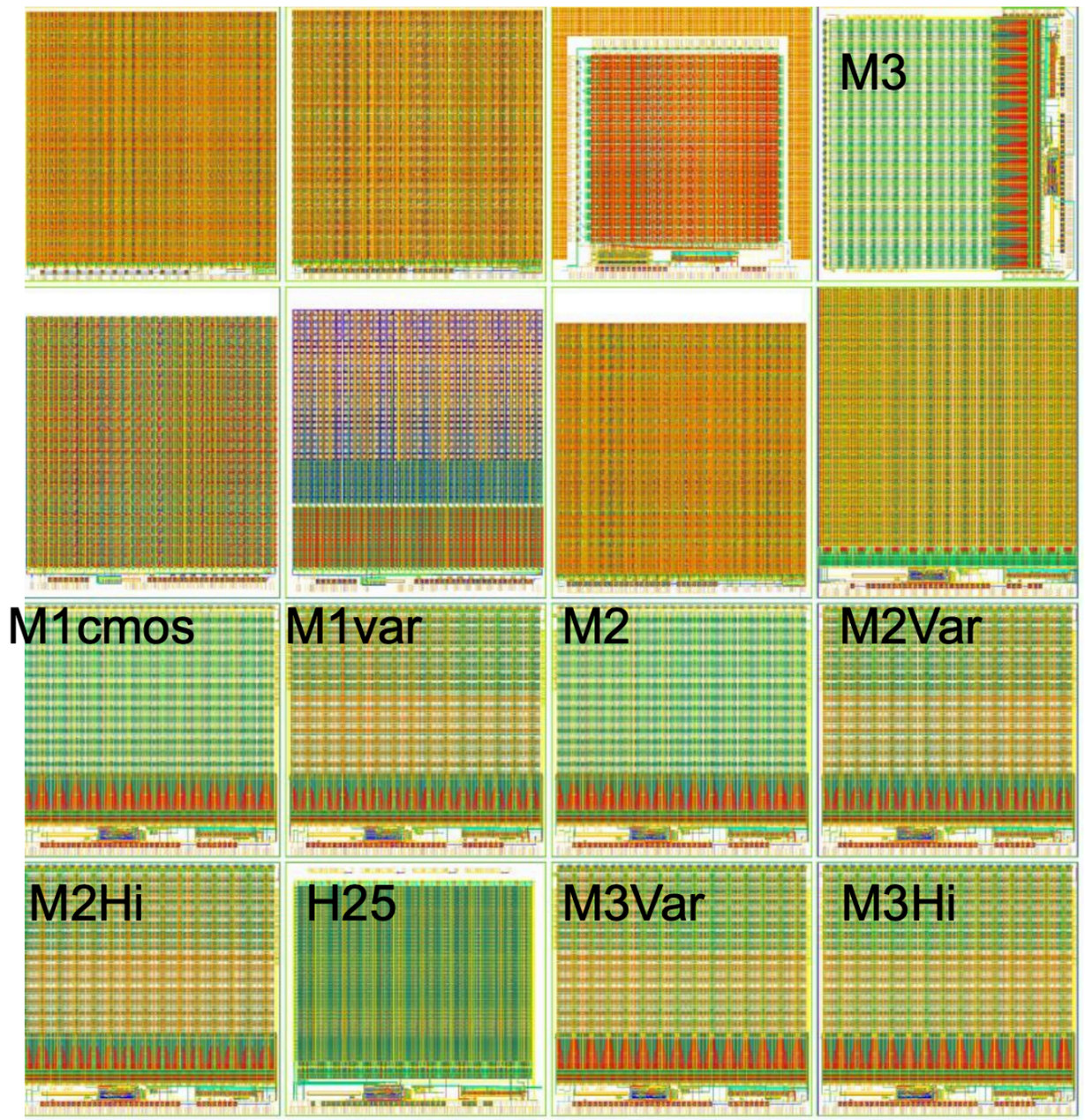
- Investigate performance of high-thermal conductivity (eg Allcomp) foams as a heat exchanger
  - Combination of large area and increased stream velocity through foam can lead to high efficiency
- Characterise performance (i.e. temperature rise vs power) for different flow velocities
- Develop FEA models simulating the fluid flow through foams

Liverpool

Improvements beyond ATLASPix3 (180nm)

Karlsruher Institut für Technologie

- Engineering run 2020 and 2021
  - TSI 180nm
  - Several designs for future electron colliders and DESY telescope upgrade (TELEPIX)
  - Pixel 25um ×165 um
- Improvements beyond ATLASPix3
  - Improved breakdown voltage by better design of guard ring (60V → 120V)
  - Reduction of power consumption by optimized amplifier and comparator designs



https://adl.ipe.kit.edu/english/26.php

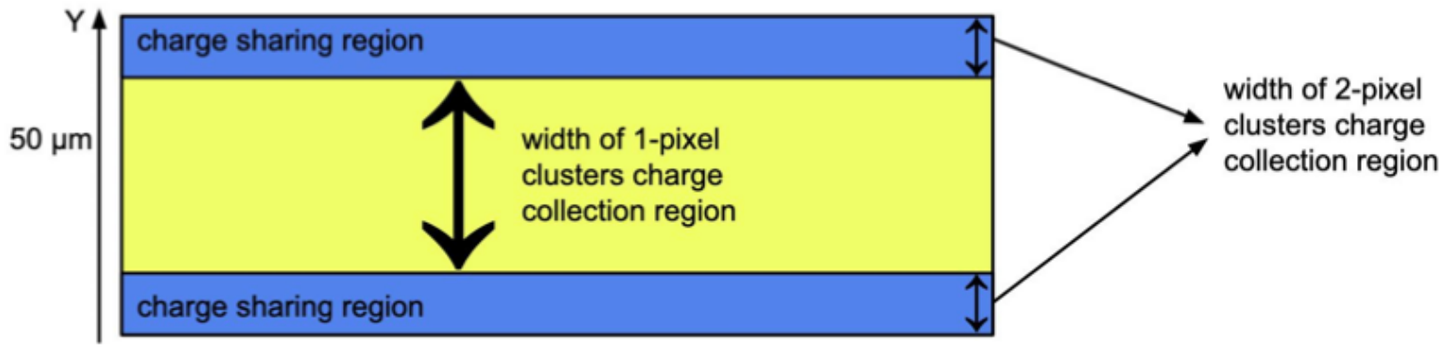
Improvements for sensors beyond ATLASPix3

Ivan Peric

- Options:
  - Different pixel sizes
  - Different amplifier types (NMOS and PMOS)
  - Different comparator types (NMOS, CMOS and distributed)
  - Different TDAC types (placed in pixels or in periphery)
- Fixed improvements versus ATLASPIX3
  - Hit buffer cell with time to digital converter (supports time resolution ~ 100ps), TDAC, differential receiver for distributed comparator
  - Possibility of daisy-chain readout – one chip acts as data collector for another
  - Possibility to bias pixel n-well with voltage higher than 1.8V, and to bias pixel p-well with voltage lower than 0. It reduces capacitance. Reduced capacitance means better time resolution for the same power consumption.
- PMOS amplifier has lower noise than the NMOS amplifier when the bias current is high (~10µA). It has better (smaller) time walk for threshold of nine sigma noise. PMOS amplifier is more suitable for larger pixels i.e. pixels with larger capacitance (larger than 150fF)
- NMOS amplifier has better time walk for nine sigma noise for small bias currents (~1µA). It is a good choice for small pixels with little capacitance. Some risk because NMOS has more flicker noise and because we have little experience with this amplifier type
- NMOS comparator is the standard comparator type we used so far. It has some disadvantages: rather high current consumption (~3µA), larger delay than CMOS comparator, need for additional bias voltage of 2.1V, output signal of reduced amplitude, it occupies large area and causes large detector capacitance
- CMOS comparator does not have the disadvantages of NMOS comparator, it is faster for the same current consumption, potentially more radiation tolerant, smaller. Disadvantage is that CMOS comparator needs additional deep p-well implant (iso-PMOS option). This implant will be produced by TSI for the first time – there is some risk that it does not work.
- Distributed comparator has only three transistors in the pixel and adds very little capacitive load. The receiver and TDAC are placed in the hit buffer at the periphery. It is fast, low power and does not require additional iso-PMOS. The disadvantage is that it requires two lines per pixel to connect it with the hit buffer. This is not a problem for pixels larger than 50µm x 150µm.
- TDAC can be placed in pixel but it adds detector capacitance. TDAC can also be placed at the periphery, in this case it makes periphery slightly larger

Testbeam Analysis - Resolution (1)

- **Resolution for 1-pixel and 2-pixels** (row projection) **clusters** in **precise Y direction** (50 μm pitch)
- Distribution of residuals in Y fitted with function $f(x) = [S(x|l,r,C)+G_{bkg}(x|\mu_{bkg},\sigma_{bkg})]*G_{tel}(x|\mu_{tel},\sigma_{tel})$ where
  - $S(x|l,r,C) = \begin{cases} C & l<x<r \\ 0 & elsewhere \end{cases}$ is a **top-hat function** describing the **charge collection region**
  - $G_{bkg}(x|\mu_{bkg},\sigma_{bkg})$ is a Gaussian background which accounts for tails in the resolution function, for example, due to δ-rays or bremsstrahlung
  - $G_{tel}(x|\mu_{tel},\sigma_{tel})$ is a Gaussian function which describes the **telescope resolution**



- width of the step-function $(l+r)$ and σ_{tel} extrapolated from fit to study their **variation with HV**