ÖAW AUSTRIAN ACADEMY OF SCIENCES

Towards detectors for HET factories

Electronics, mechanics, integration

Thomas Bergauer

11 Oct 2024

3rd ECFA workshop on e+e- Higgs, Top & ElectroWeak Factories

9–11 October 2024

Sorbonne Université, Campus des Cordeliers, Paris

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https://indico.in2p3.fr/e/ecfa2024

Administrative and Technical support team

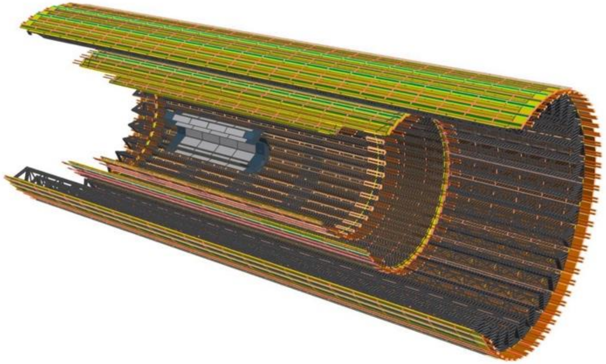
- Luc Petizon (IJCLab Orsay)
- Sylvaine Pieyre (LLR Palaiseau)
- Sarodia Vydelingum (APC Paris)

Vertex Detectors State of the Art

- **Belle II VTX upgrade** (2028-2030)
  - CDR May 2024 in Arxiv: [2406.19421]

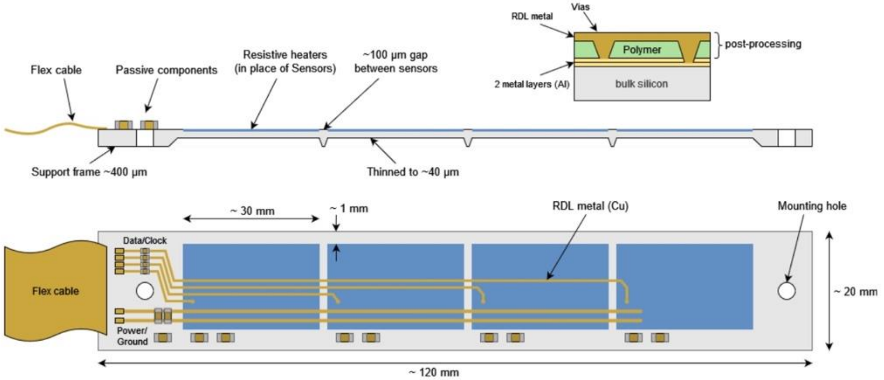
- Sensors: 180 nm modified Tower, 33µm pitch,
  - analog part based on TJ-Monopix2
  - Digital part adapted to fit Belle-II needs (10µs trigger latency, optional features of outer layers)
- iVTX ladders: 2 layers (14 and 22 mm radii) featuring an "all-silicon ladder" design: 0.2%X_0 per layer.
- Power 200 mW/cm^2

- Mechanics: ultra-light supports and air cooling
  - open-cell reticulated vitreous carbon (RVC) foams: 45 kg/m^3



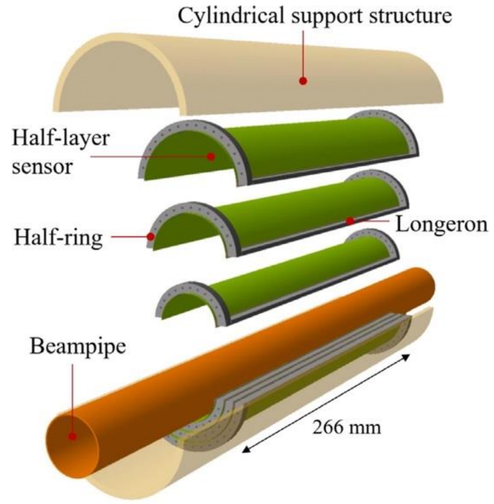
Pitch	33µm
Signal ToT	7 bits
Time stamping	50 to 100 ns
Fine time * stamping	~ 5 ns for hit rate < 10 MHz/cm^2
Hit rate max for 100% effi	120 MHz/cm^2
Trigger handling	30 kHz with 10 µs latency
Trigger * output	~10 ns resolution with low granularity
Power (with hit rate)	120 to 200 mW/cm^2 (1 to 120 MHz/cm^2)
Bandwidth	1 output 320 MHz

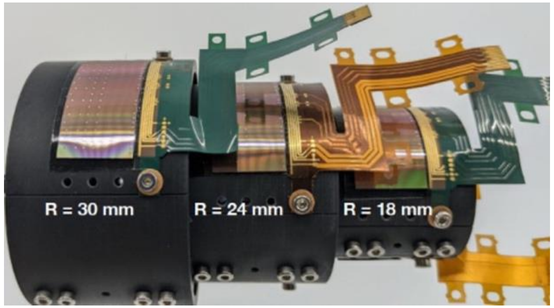
* optional features for outer layes

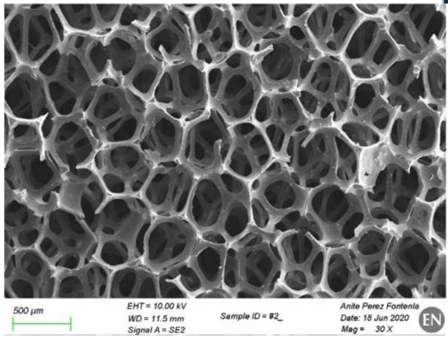


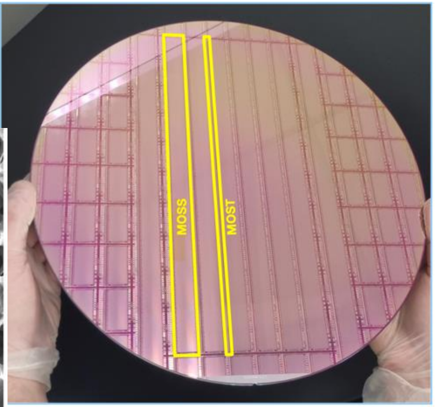
Vertex Detectors State of the Art

- **ALICE** ITS2 @ LS2 : 24k ALPIDE MAPS
- **ALICE** ITS3 @ LS3 (2028-2030):
  - TDR May 2024
- Sensors:
  - 180 nm Tower → 65 nm TPSCo
  - 200 mm wafer → 300 mm wafer diameter
  - Stitched sensors up to 100 x 260 mm
  - 50µm thinned results in 0.07 %X_0 per layer
  - Pitch 20µm; 40mW/cm^2 power dissipation
  - Pioneering bent sensors
- Mechanics: ultra-light supports and air cooling
  - open-cell reticulated vitreous carbon (RVC) foams: 45 kg/m^3









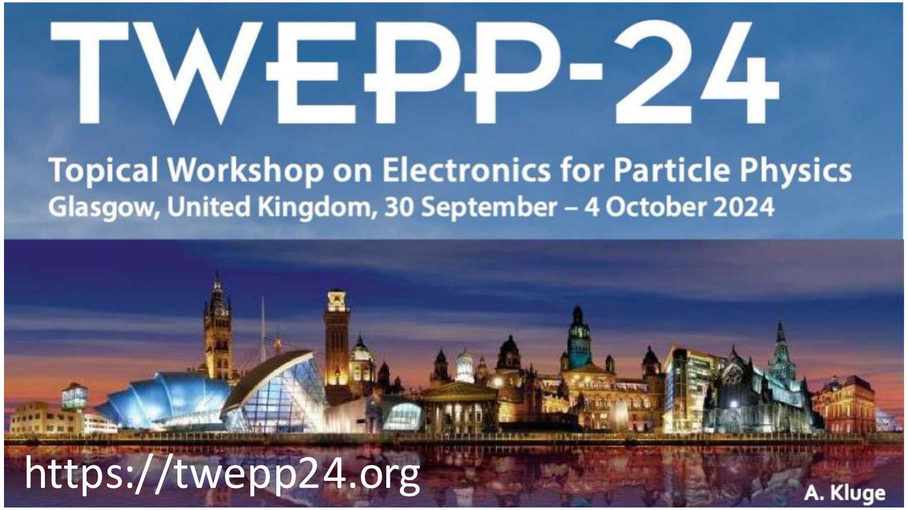
Where to start

Electronics:

- TWEPP Conference Series
- DRD7 Collaboration

Mechanics:

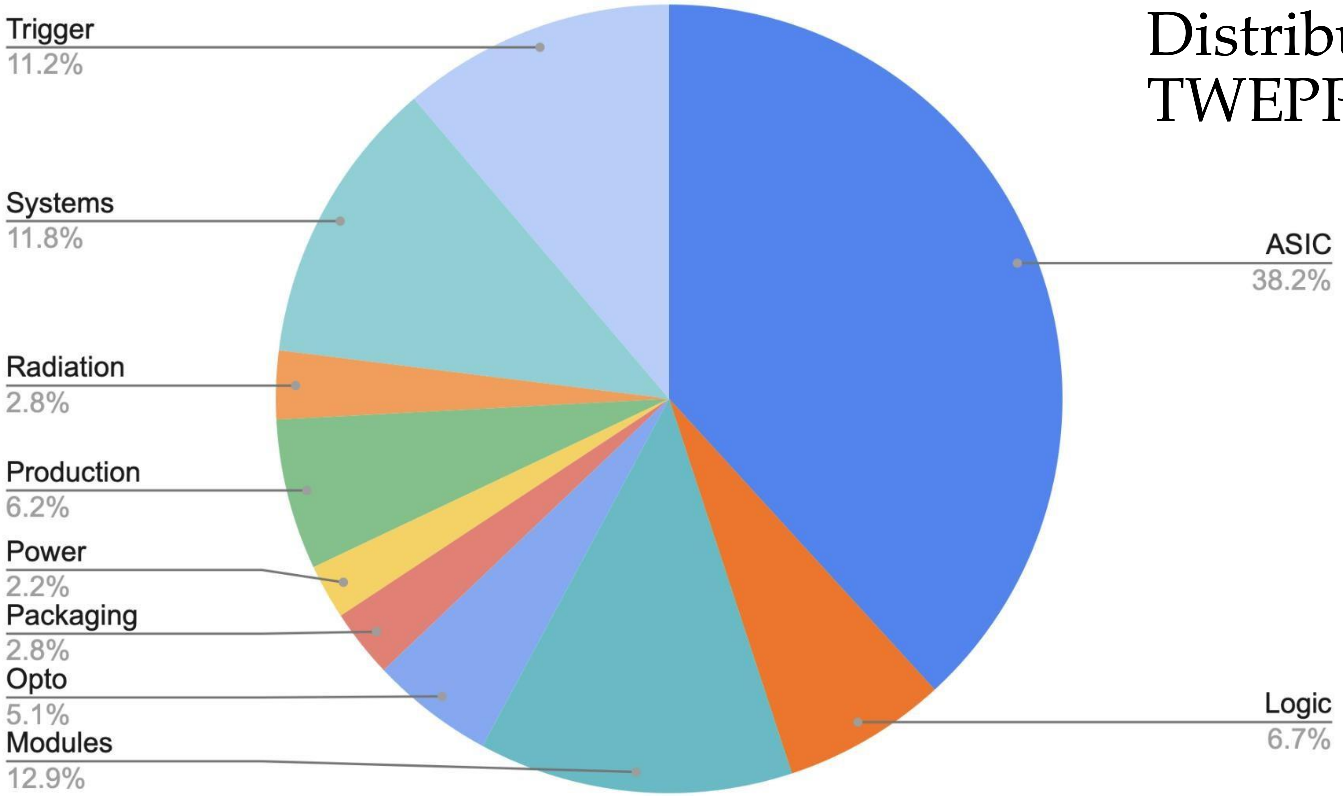
- Forum on tracker mechanics
- DRD8 collaboration t.b.d.



https://twepp24.org

https://indico.cern.ch/event/1336746/

Topics in Electronics

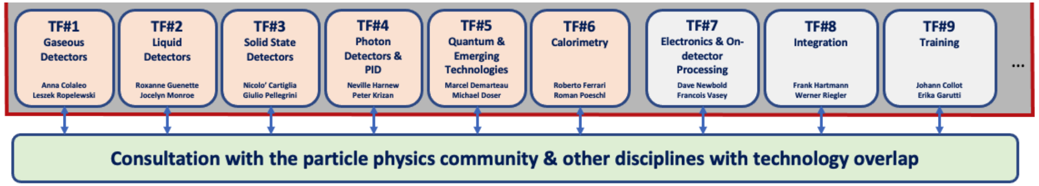


Distribution of topics at TWEPP24 workshop

ASIC includes both MAPS sensors and FE-ASICs

TRLs in Electronics and Mechanics

- Initially, during Roadmap process, electronics, integration and training were proposed as “orthogonal” topics, necessary for and acting as support for all other detector technologies
→ targeting **mid- to high TRLs**



TF#1 Gaseous Detectors
Anna Colaleo
Leszek Ropelewski

TF#2 Liquid Detectors
Roxanne Guenette
Jocelyn Monroe

TF#3 Solid State Detectors
Nicolo’ Cartiglia
Giulio Pellegrini

TF#4 Photon Detectors & PID
Neville Harnew
Peter Krizan

TF#5 Quantum & Emerging Technologies
Marcel Demarteau
Michael Doser

TF#6 Calorimetry
Roberto Ferrari
Roman Poeschl

TF#7 Electronics & On-detector Processing
Dave Newbold
Francois Vasey

TF#8 Integration
Frank Hartmann
Werner Riegler

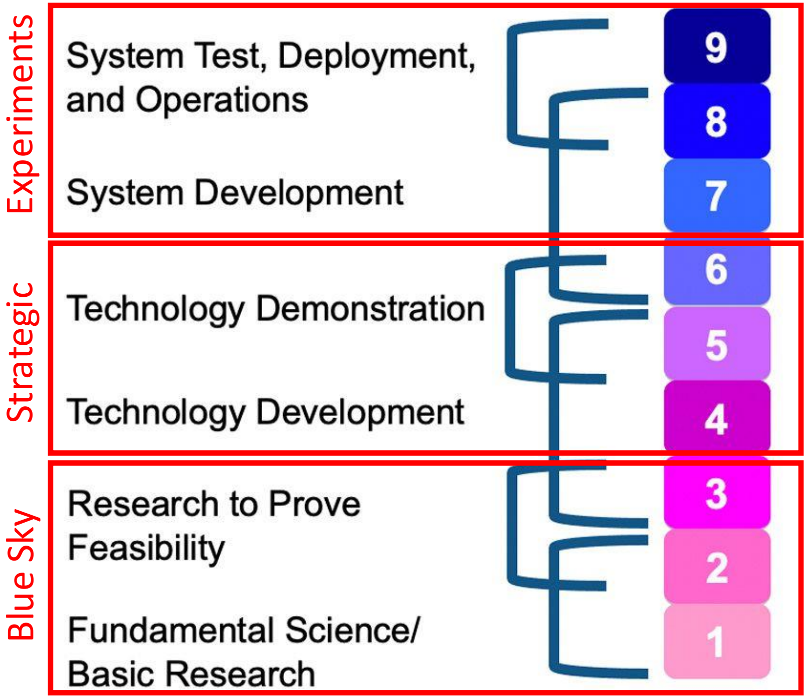
TF#9 Training
Johann Collot
Erika Garutti

...

Consultation with the particle physics community & other disciplines with technology overlap

- However, if we look into the DRDTs for TF7 and 8 in the Roadmap, the topics are actually targeting **much lower TRLs**

Technology Readiness Levels (TRLs) 1-9:
Method for estimating the maturity of technologies



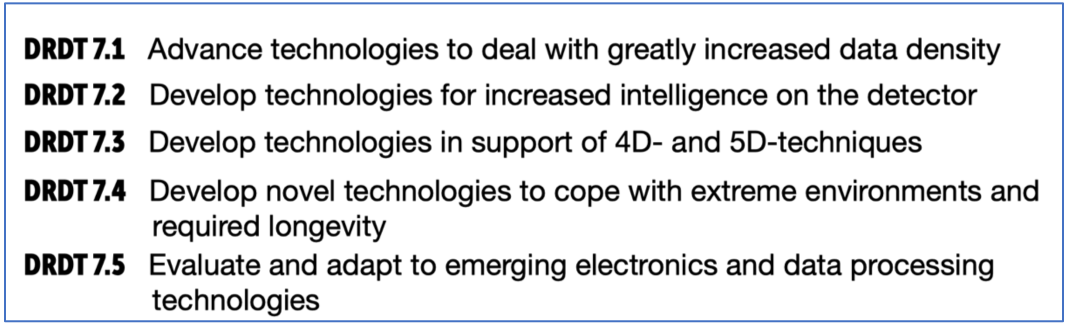
Experiments
9
System Test, Deployment, and Operations
8
System Development
7

Strategic
6
Technology Demonstration
5
Technology Development
4

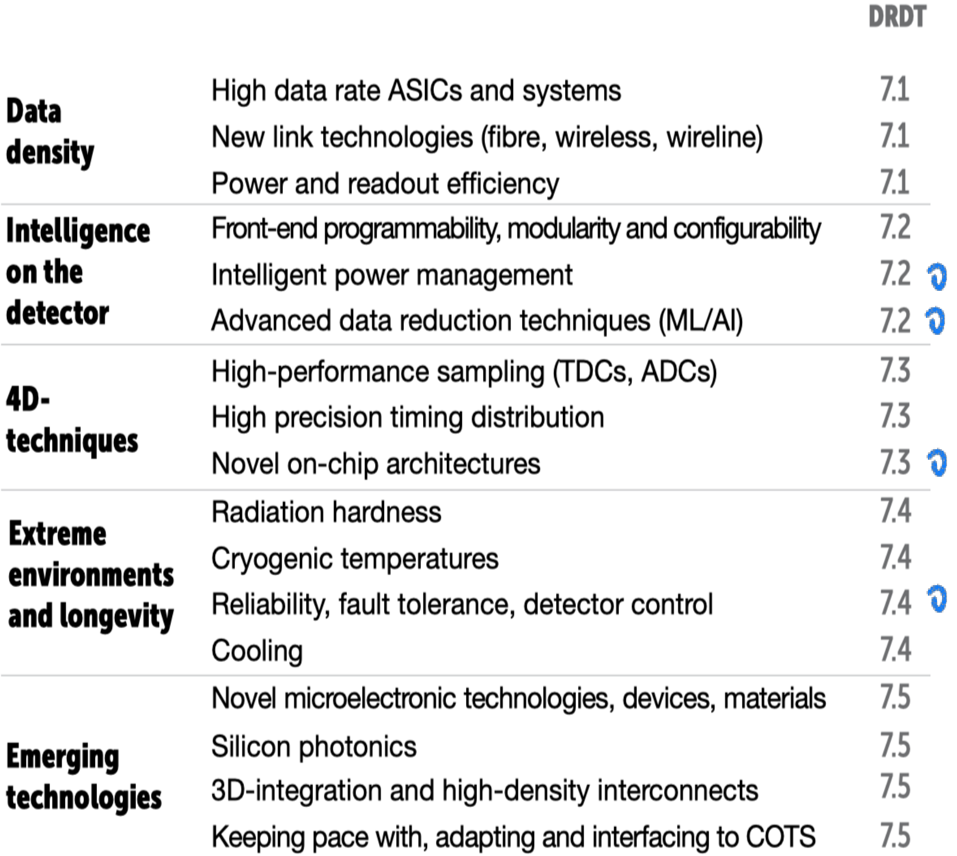
Blue Sky
3
Research to Prove Feasibility
2
Fundamental Science/ Basic Research
1

Topics on Electronics

- High-level DRD Themes (below) and detailed list of topics from “detector readiness matrix” (right)



DRDT 7.1	Advance technologies to deal with greatly increased data density
DRDT 7.2	Develop technologies for increased intelligence on the detector
DRDT 7.3	Develop technologies in support of 4D- and 5D-techniques
DRDT 7.4	Develop novel technologies to cope with extreme environments and required longevity
DRDT 7.5	Evaluate and adapt to emerging electronics and data processing technologies

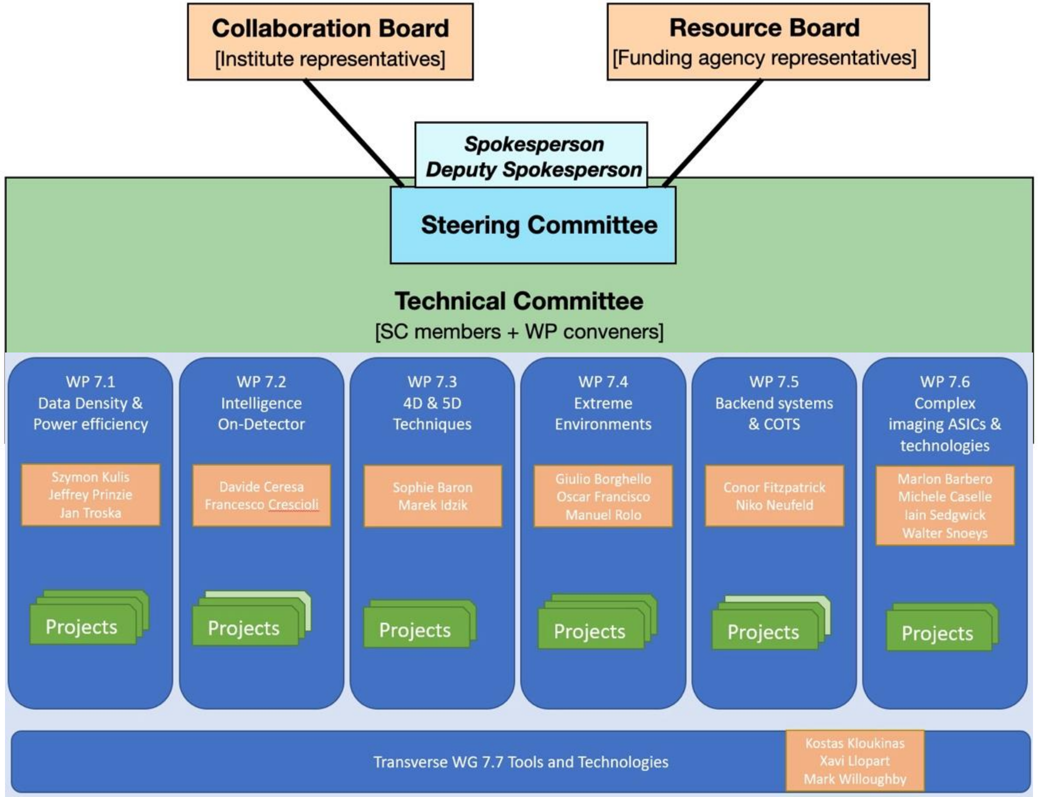


		DRDT	
Data density	High data rate ASICs and systems	7.1	
	New link technologies (fibre, wireless, wireline)	7.1	
	Power and readout efficiency	7.1	
Intelligence on the detector	Front-end programmability, modularity and configurability	7.2	
	Intelligent power management	7.2	↻
	Advanced data reduction techniques (ML/AI)	7.2	↻
4D-techniques	High-performance sampling (TDCs, ADCs)	7.3	
	High precision timing distribution	7.3	
	Novel on-chip architectures	7.3	↻
Extreme environments and longevity	Radiation hardness	7.4	
	Cryogenic temperatures	7.4	
	Reliability, fault tolerance, detector control	7.4	↻
	Cooling	7.4	
Emerging technologies	Novel microelectronic technologies, devices, materials	7.5	
	Silicon photonics	7.5	
	3D-integration and high-density interconnects	7.5	
	Keeping pace with, adapting and interfacing to COTS	7.5	

↻ Currently not explicitly covered by projects in DRD7

DRD7 Collaboration: Electronics

- Objectives: Carry out strategic R&D in electronics, fulfilling DRDTs, Coordinate cross-European access to technologies, tools and knowledge, Interface with other DRDs
  - No orthogonal "Service-Provider" for other DRDs
- Full proposal submitted to DRDC by 21 May 2024; approved in June 2024 DRDC and RB meetings
- Organization:
  - 19 countries, 68 institutes with ~110 FTE contributors (224 people) ; around 180 "observers"
  - 1st workshop in March 2023
    2nd workshop in Sept. 2023;
    3rd workshop 9-10 Sept 2024



Collaboration Board
[Institute representatives]

Resource Board
[Funding agency representatives]

Spokesperson
Deputy Spokesperson

Steering Committee

Technical Committee
[SC members + WP conveners]

WP 7.1
Data Density & Power efficiency
Szymon Kulis
Jeffrey Prinzie
Jan Troska
Projects

WP 7.2
Intelligence On-Detector
Davide Ceresa
Francesco Crescioli
Projects

WP 7.3
4D & 5D Techniques
Sophie Baron
Marek Idzik
Projects

WP 7.4
Extreme Environments
Giulio Borghello
Oscar Francisco
Manuel Rolo
Projects

WP 7.5
Backend systems & COTS
Conor Fitzpatrick
Niko Neufeld
Projects

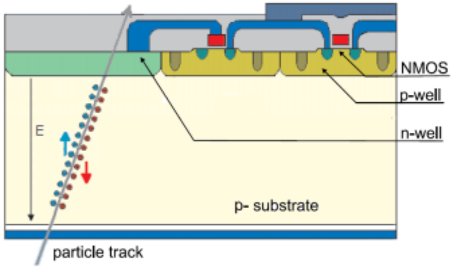
WP 7.6
Complex imaging ASICs & technologies
Marlon Barbero
Michele Caselle
Iain Sedgwick
Walter Snoeys
Projects

Transverse WG 7.7 Tools and Technologies
Kostas Kloukinas
Xavi Llopart
Mark Willoughby

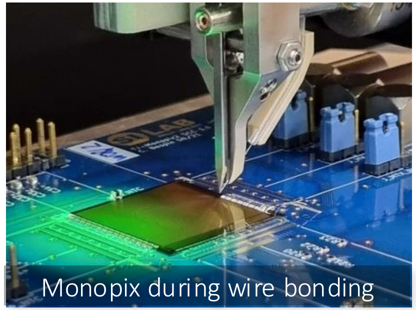
R&D Topics in Electronics

- **MAPS** and “**normal**” **FE-ASICs**
- **Opto**electronics & analog/digital links
- **Packaging** & Interconnects
- **Power**, Grounding & Shielding
- **Radiation**-Tolerant Components & Systems
- Programmable **Logic**: FPGA, System-on-chip
  - Design & Verification Tools & Methods
- PCB, **module** & component design
- **System** design, description & operation
- **Trigger** & Timing Distribution

Imaging ASICs: (D)MAPS

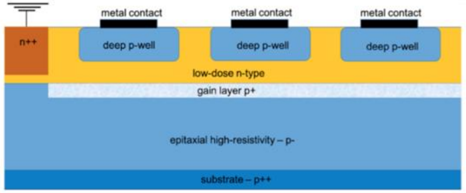


- Monolithic Hybrid pixel detectors unify Sensor and CMOS electronics
  - High resistivity substrate and HV-compatible process allow depletion
  - Large vs. small collection electrode
- Mixed-mode design
  - **Analog-on-top**; now **Digital-on-top** is preferred due to better simulation/verification possibilities



Monopix during wire bonding

- Dependency on a few Foundries, eg.:
  - **Tower(Jazz) 180 nm → TPSCo 65 nm**
    - More than 10 years experience in HEP
      Customization to increase radiation hardness
    - 180 nm used in ALPIDE (ALICE ITS2) in running experiment, but also MALTA, Monopix, MIMOSIS, OBELIX (Belle-II),..
    - 65 nm for ITS3 and FCC-ee projects (with stitching)
    - Access organized by and via CERN
  - **LFoundry** 110 nm and 150 nm: INFN-ARCADIA, RD50-MPW



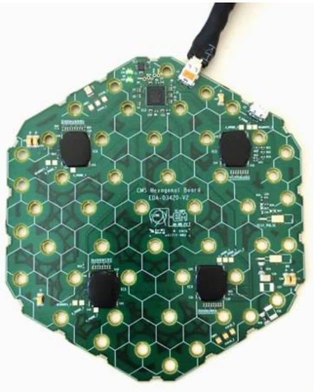
A. Apresyan (FNAL) Monolithic AC-LGAD

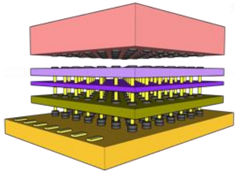
ASICs

- Several additional foundries available via [Europractice]
- “Opensource“ PDK: Skywater 130 nm via efabless
- Direct foundry contact in the US

- ASICs for different purposes in both analog and digital domain:
  - FE-readout of hybrid pixel sensors: mixed mode RD53A, ECON-T & ECON-D for CMS HGCal (CERN/FNAL), HGROC (Omega)
  - LGAD-readout: analog FAST3 (UMC 110 nm, INFN Torino), ETROC for CMS ETL (FNAL)
  - BE-ASIC: digital lp-gpt (CERN)
  - DC-DC converter, e.g. FEAST2 (CERN)

Only large labs seem to be capable of developing ASICs





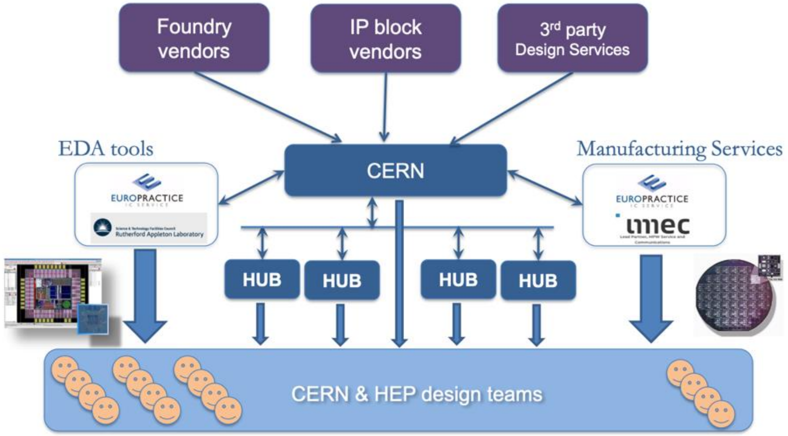
LGAD - 2x2 matrix wire-bonded to the input of the ASIC

Transverse Tools & Technologies

- Chip development is a major undertaking
  - Becomes more and more complex with smaller nodes and more complex technologies
  - HEP needs specific “3-way NDA” for design sharing
  - Challenges in design, verification and foundry submission
  - Facilitate collaborative work across different institutions
  - Shared IP blocks and Test Systems
  - Biggest challenge: maintain long-term engineers

- Different stakeholders:
  - Europractice IC and Software services
  - CERN ASIC Support https://asicsupport.web.cern.ch
  - EP R&D WP5 developments
  - DRD7.7 „Hub-based structure“
  - Expertise in many institutions

DRD7 WP7



Foundry vendors

IP block vendors

3rd party Design Services

EDA tools

CERN

Manufacturing Services

HUB

HUB

HUB

HUB

CERN & HEP design teams

Kostas Kloukinas

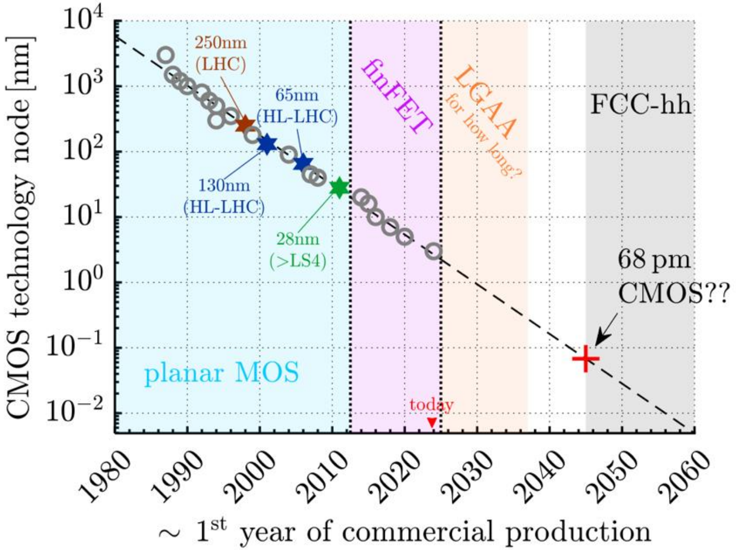
Extreme Environments

- Radiation Resistance of Advanced (<65nm) CMOS Nodes: TID, NIEL, SEE
  - First studies on 65nm in 2012 → chip prod in 65nm (now)
  - 65 nm -> 28 nm pixel sensor readout

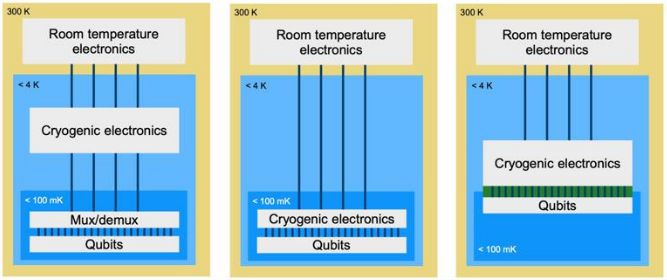
10 years

- Cryogenic ASICs
  - Device modeling: development of ”cold” Process Design Kits (PDKs),
  - Design and characterization of mixed-signal CMOS IP blocks
  - Demonstrator chips in TSMC 28nm for photon detection in (LAr, LXe) noble liquid experiments, quantum computing and sensing
  - temperature corners at 165-87-77-4K

lateral gate-all-around-device



G. Borghello



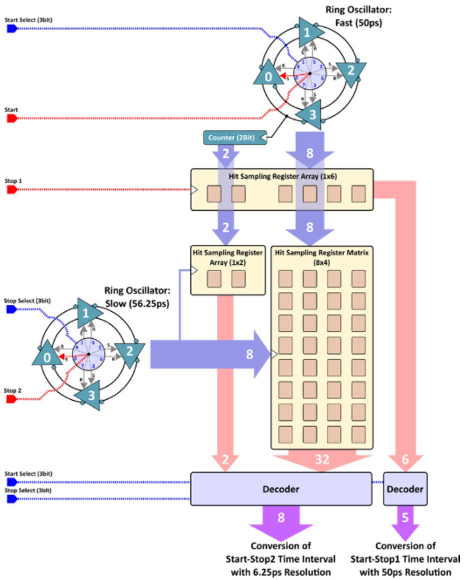
IP Blocks for 4D & 5D Techniques

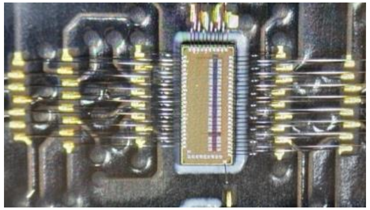
- 4D: spatial plus timing
- 5D: adding energy deposition measm.

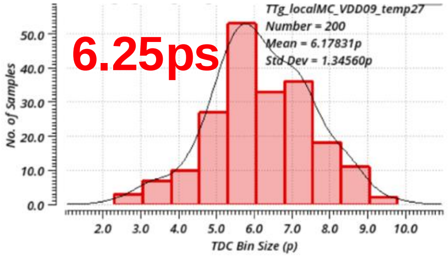
- Develop common IP blocks for high-performance sampling (TDC, ADC)
  - Vernier TDC with ring buffers
  - 6.25ps TDC timing

- Timing Distribution Techniques
  - Study phase determinism of various FPGAs
  - ASIC for Phase Monitoring and Phase Shifting

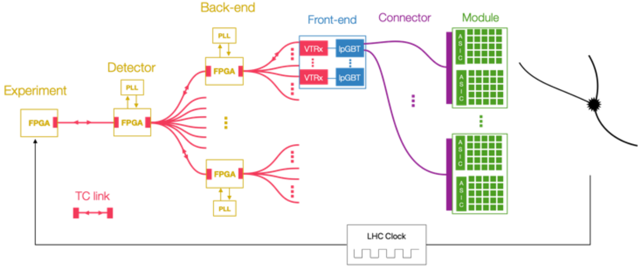
SLAC 28nm TDC ASIC :







J. Mendez (SLAC)



Intelligence on Detector

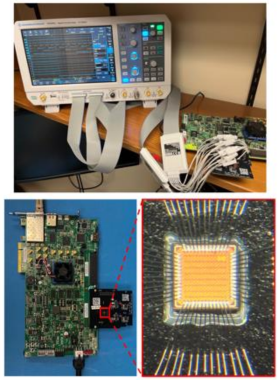
Front-end programmability, modularity and reconfigurability must be enhanced to allow fewer, more versatile front-end electronics

- embedded FPGA: Programmable Logic Array IP
  - openFPGA or FABulous
  - Including reprogrammable ML algorithms into FE
- Radiation Tolerant RISC-V SoC
  - RISC-V: royalty-free open logic architecture, supported by European Chips Act
  - Radiation hardening by spatial redundancy: (TMR, DMR), instruction replay or checkpoint recovery

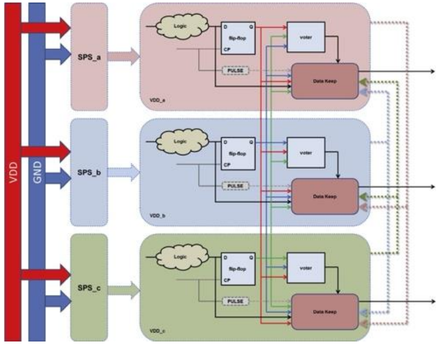
FABULOUS
eFPGAs made easy

J. Gonski

28nm eFPGA Test Setup



RISC-V®

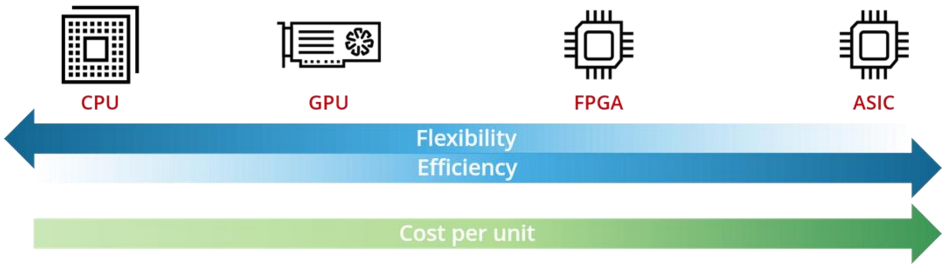


V. Petrovic et al.

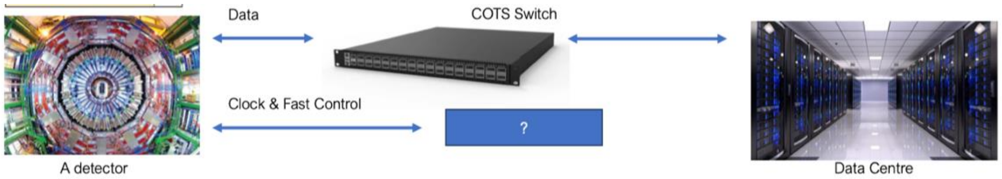
Backend Systems and COTS

Commercial off-the-shelf

- Keeping pace & adapting of COTS computing (CPUs, GPGPUs, FPGAs, AI)
  - We're (usually) not the target market
  - It takes time and effort to develop for general purpose technologies
  - Technology evolution is fast but hard to predict



- Lower radiation levels opens the door to increasing the complexity of Front-End electronics (RISC -V based processors, RAMs and SoC in the Front-End)
  - directly communicate with COTS back-end hardware
  - 100Gb Ethernet-based link

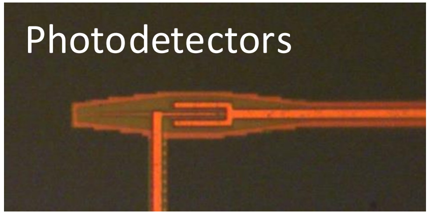


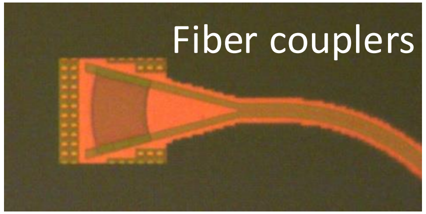
S. Baron

Data Density & Powering

Challenge: More channels and more bits per sample, higher data rates, less mass and power.

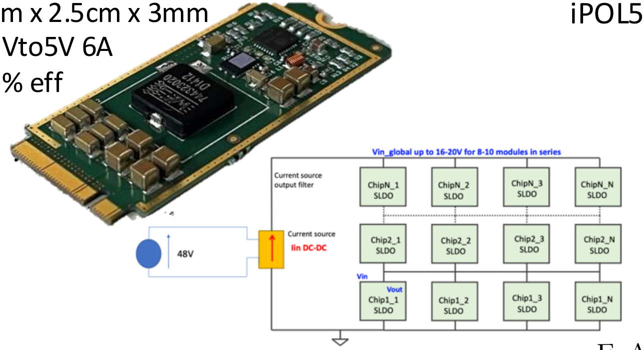
- Silicon Photonics Transceivers: Light-manipulating structures are patterned (deep UV lithography) on Silicon
  - 100 Gb/s per fibre optical readout with 2.5 Gb/s control optical link operating at a BER of 10^{-12}.
  - Radiation tolerance up to 10^{16} particles/cm^2 and 10 MGy.
- Develop power distribution schemes and their voltage/current regulators.
  - DC/DC converters, e.g. bPOL48V from 48V to 5V and iPOL5V, an IP block in 28 nm
  - Survey of Gallium Nitride (GaN) for e.g. serial powering
- Wireless technology
  - Multi-hop data transmission between inner detector layers



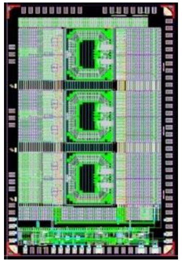


J. Troska

5cm x 2.5cm x 3mm
48Vto5V 6A
85% eff

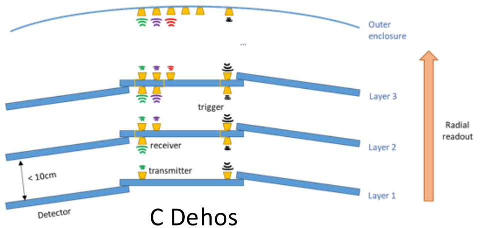


iPOL5V



S. Michelis

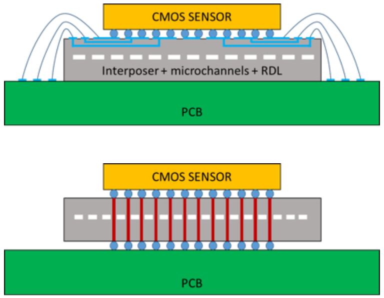
F. Arteche

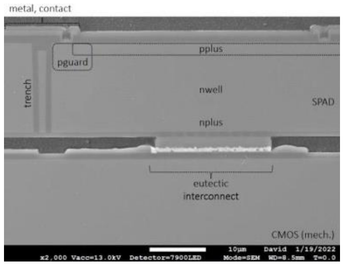


C Dehos

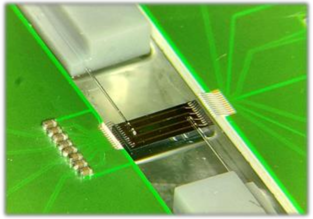
3D Integration

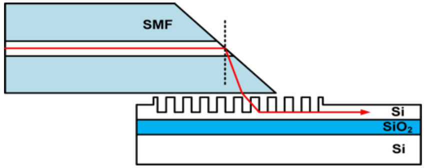
- „3D integration“ of chiplets through a combination of
  - Through-silicon-vias (TSV), redistribution layers (RDL)
  - Sensor, FE-electronics, memory, processing, even Silicon Photonics
- Different technologies under evaluation/development
  - Laser drilled through silicon vias, maskless process for wafer and single die
  - Anisotropic conductive films

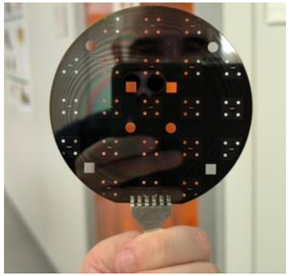


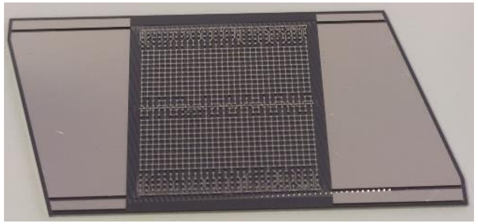


Sherbrooke/TRIUMF







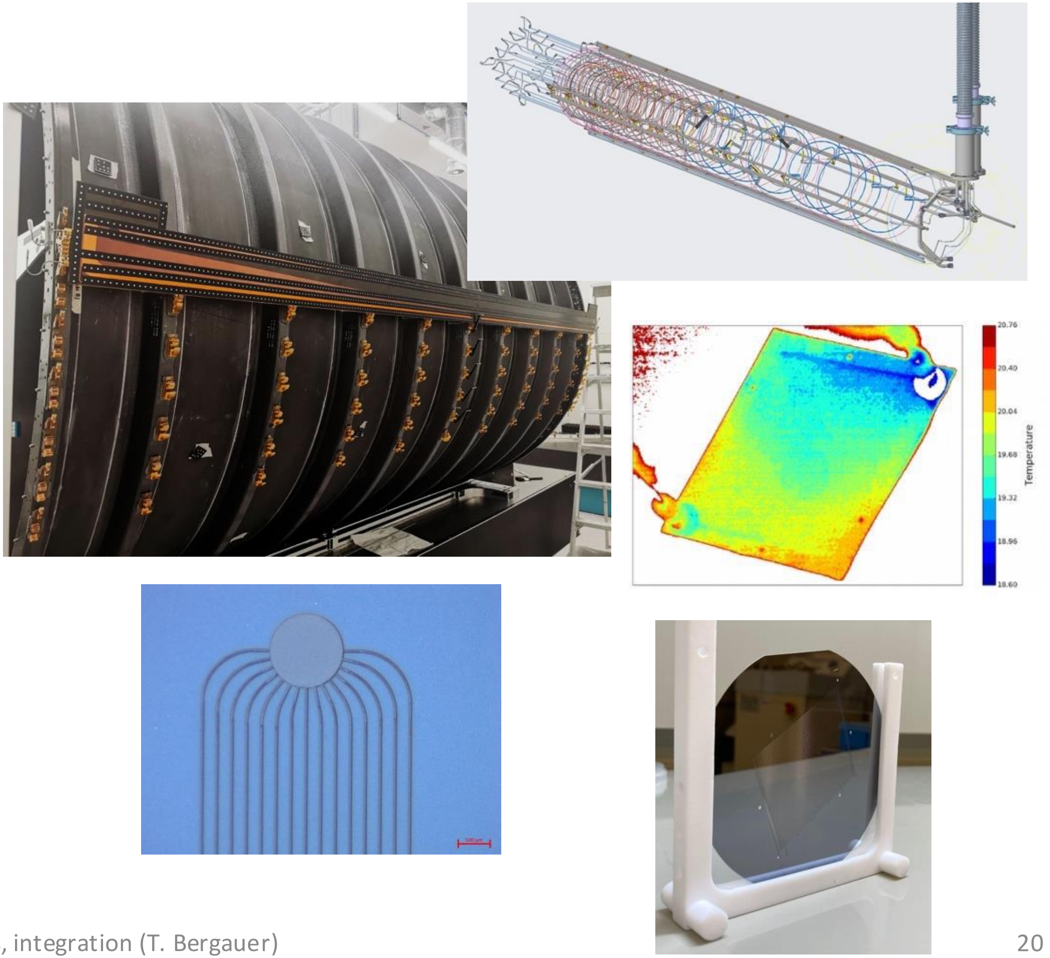


M. Ullan

Mechanics, Cooling, Integration

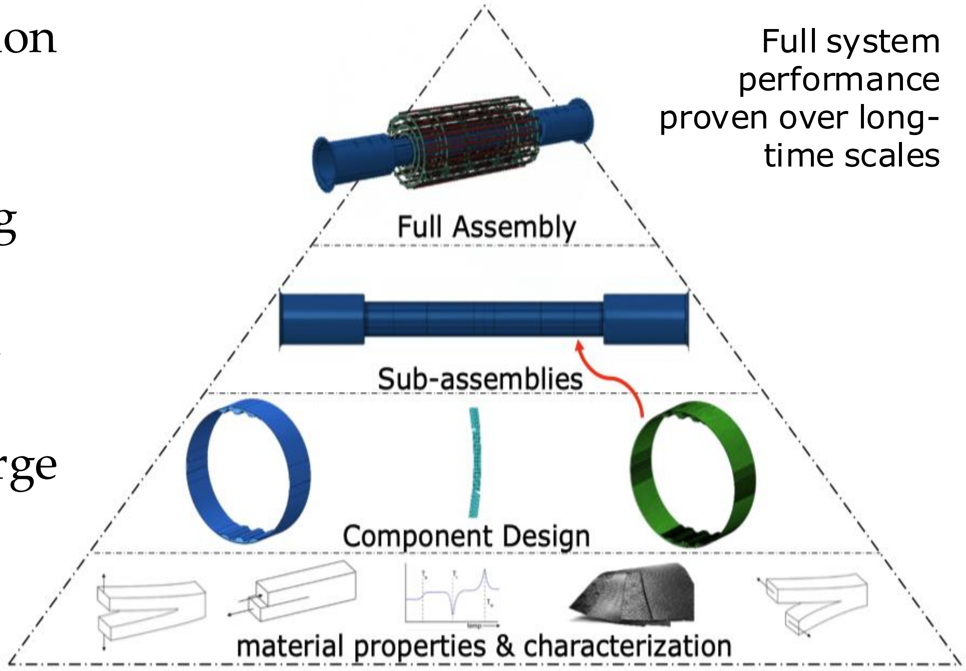
Topics in Mechanics

- Mechanics
  - Advanced Composites, e.g. reinforced CF foams
  - Thermal management
  - Support structures, Metrology
- Cooling:
  - Airflow cooling
  - Evaporative CO_2 and single-phase systems
  - Microchannel cooling in Si
  - Cooling tubes: welding, materials
- Tools: Finite element analysis



Low Mass Mechanics

- Novel materials for structural and thermal management applications, including qualification for operation in harsh environments
  - Radiation, heat, CTE,….
- Advanced manufacturing techniques, including additive manufacturing; 3D printing
- Support structures of composite materials with embedded thin-walled pipes;
- Modular, scalable designs for detectors with large surface areas
  - Standardized interfaces
- Vacuum-tight composite structures
  - Replacements for beam pipes

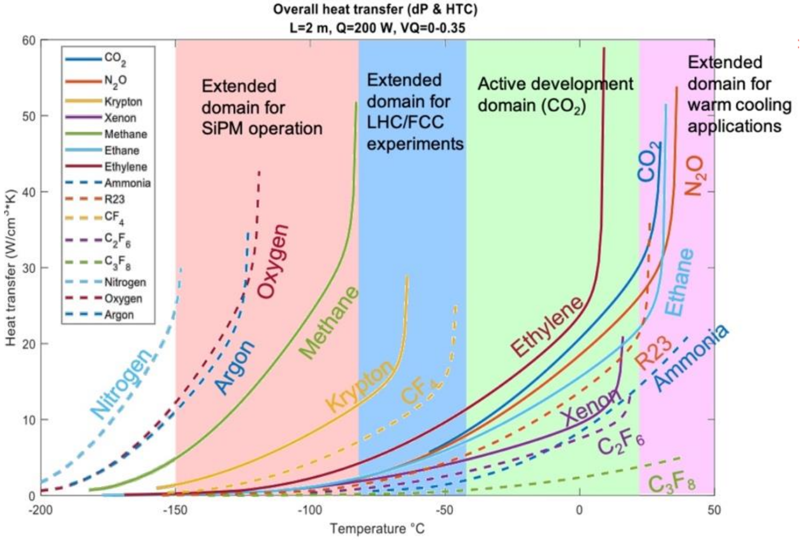


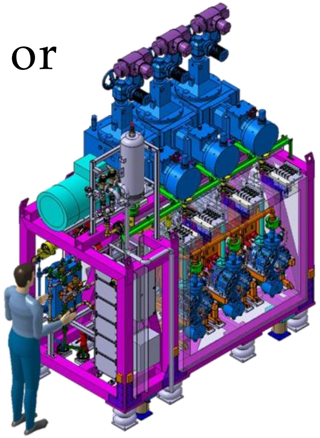
Full system performance proven over long-time scales

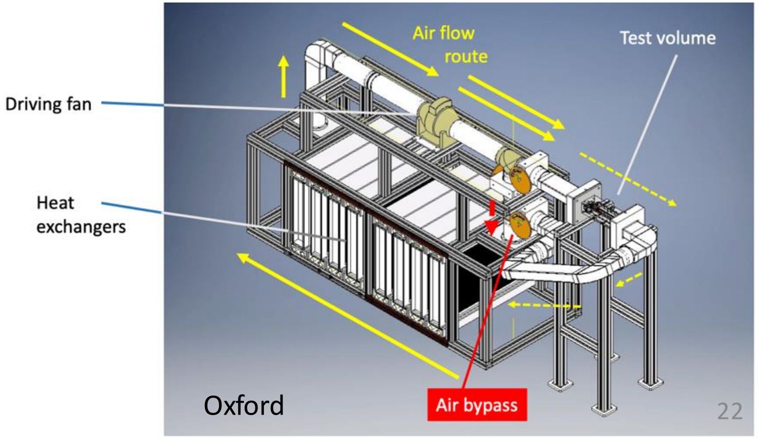
J. Hicks – FTDM 2021

Cooling

- Evaporative and liquid cooling for both low and warm temperatures
  - based on **eco-friendly** refrigerants and new cycles
  - Gas cooling solutions for detectors, including flow design and heat
  - E.g. Krypton: the CO_2 for colder temperatures
- Gas Cooling for warm low-power detectors (Typical lepton colliders)
- Integrated cooling circuits, such as silicon or ceramic substrates with embedded microchannels
  - Connection technologies for cooling circuits, including leak repair methods
- Instrumentation, including flow measurements for gases and liquids.

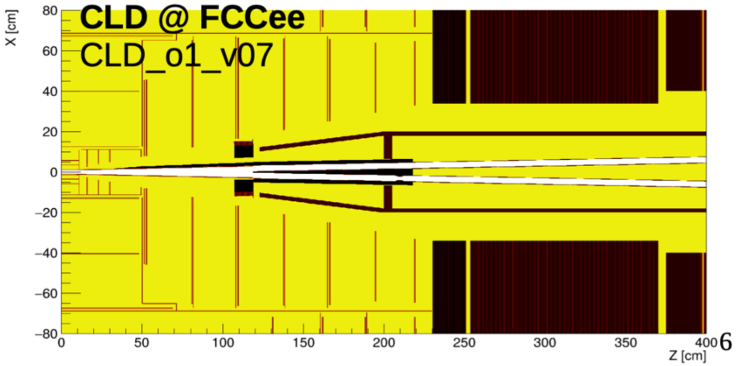




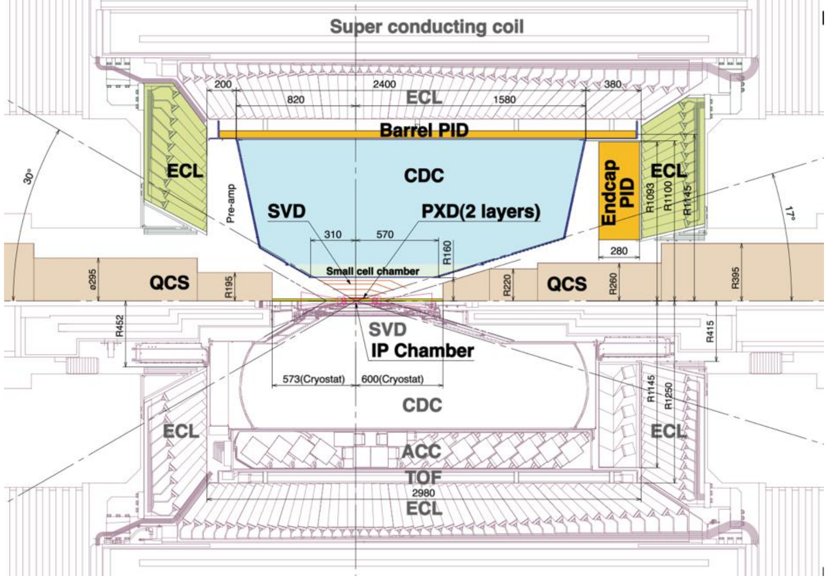


Integration

- Machine-Detector Interface is significantly different @ ILC and FCC-ee
    - Very similar to Belle-II, where QCS (final focusing magnet) is 60cm away from IP
- Installation and fast access for maintenance of vertex detector need to be considered



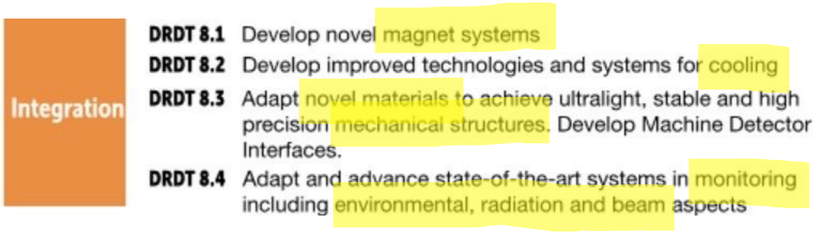
Daniel Jeans



Status of DRD8 Collaboration

- Initial TF convenors from ECFA Roadmap process did not continue as proposal preparation team
- New proponents had to be searched for, which were found by the group around the “Forum on Tracker Mechanics” workshop organizers
  - Burkhard Schmidt (CERN), Andreas Mussgiller (DESY) and others

- Community survey resulted in an interest in going forward
- Community Meeting on December 6, 2023
- LoI by end of February 2024 with the **aim to write a full proposal by the end of this year**
  - LoI does not cover all DRDTs, as they are quite diverse
  - Focus on vertex detector mechanics and cooling
  - 22 institutes in 7 countries, 32 FTE at the moment

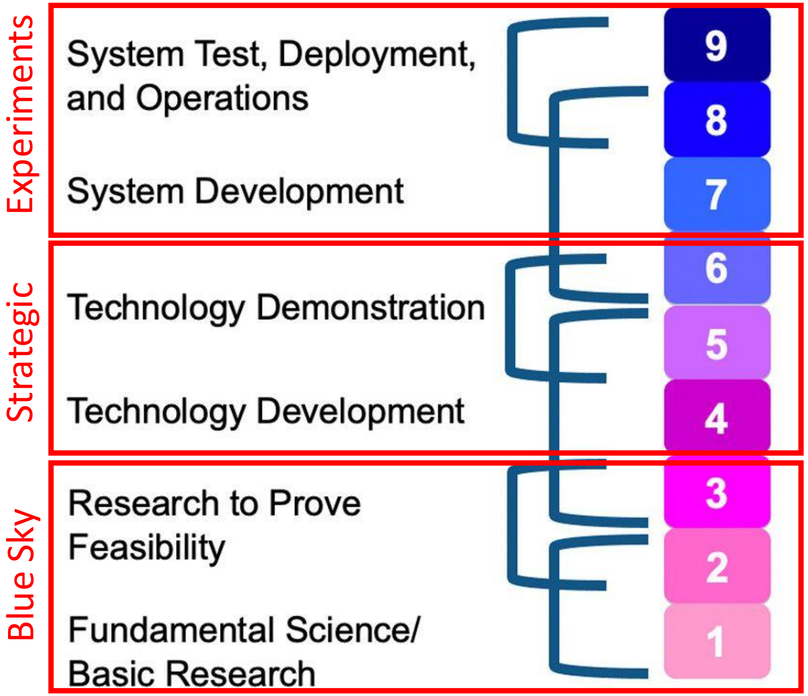


Integration	**DRDT 8.1**	Develop novel magnet systems
	DRDT 8.2	Develop improved technologies and systems for cooling
	DRDT 8.3	Adapt novel materials to achieve ultralight, stable and high precision mechanical structures. Develop Machine Detector Interfaces.
	DRDT 8.4	Adapt and advance state-of-the-art systems in monitoring including environmental, radiation and beam aspects

Summary

- Electronics and Mechanics R&D are twofold relevant:
  - In the **R&D phase of an experiment** to pave the way to technologies with long lead times (addressing low TRLs)
    - DRD7 and DRD8 collaborations addressing these needs
  - At the **TDR/EDR phase**, when the actual implementation is getting concrete (high TRL)
- Catching up with industrial developments is a challenge, especially in the microelectronics and ASIC domains
  - Complexity & costs are constantly increasing
  - Organizing the community efficiently is essential

Technology Readiness Levels (TRLs) 1-9:
Method for estimating the maturity of technologies



Experiments
System Test, Deployment, and Operations
System Development
9
8
7

Strategic
Technology Demonstration
Technology Development
6
5
4

Blue Sky
Research to Prove Feasibility
Fundamental Science/ Basic Research
3
2
1


VIENNA
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19-23 MAY
FCC WEEK
2025

19 to 23 May 2025


VCI
VIENNA CONFERENCE ON INSTRUMENTATION

THE 17th
VIENNA CONFERENCE
ON INSTRUMENTATION
17 – 21 FEBRUARY 2025

SCIENTIFIC TOPICS

New Detector Developments in
- Particle Physics
- Astro-particle Physics
- Nuclear Physics
- Quantum Sensing
- Medicine and Biology

Associated detector electronics
and detector specific software

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http://vci2025.hephy.at

Abstract submission deadline: 20 Oct. 2024

The End.

Thank you for your attention