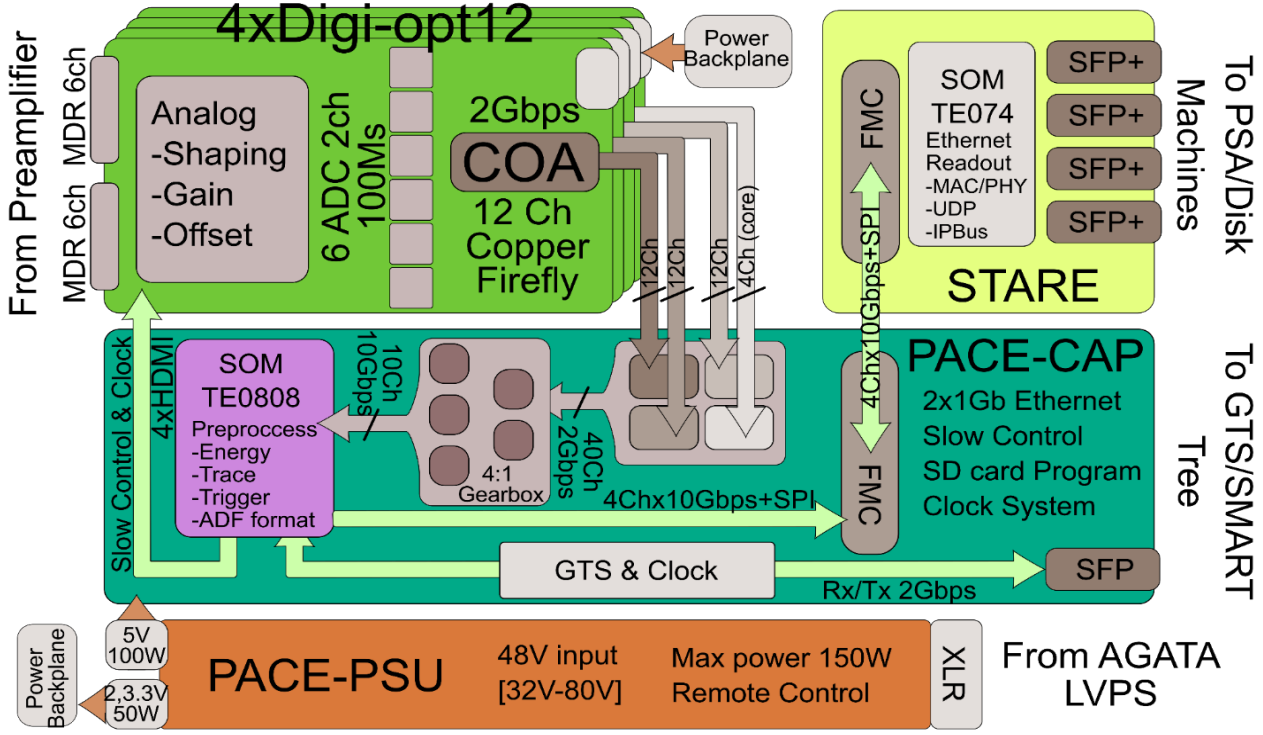
The AGATA Front-end Electronics for the Phase 2 and beyond

A. Gadea (IFIC-CSIC, Spain)

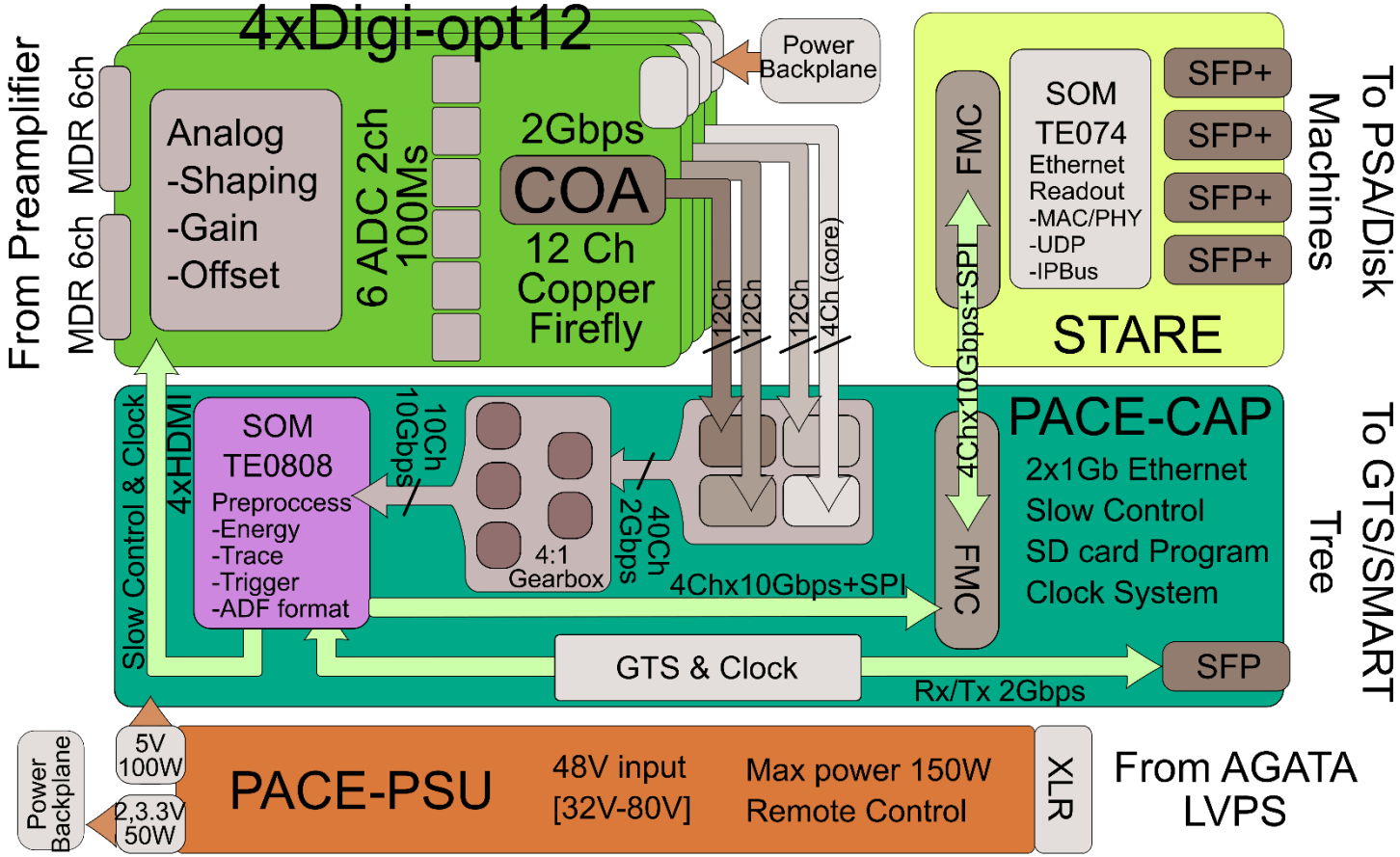


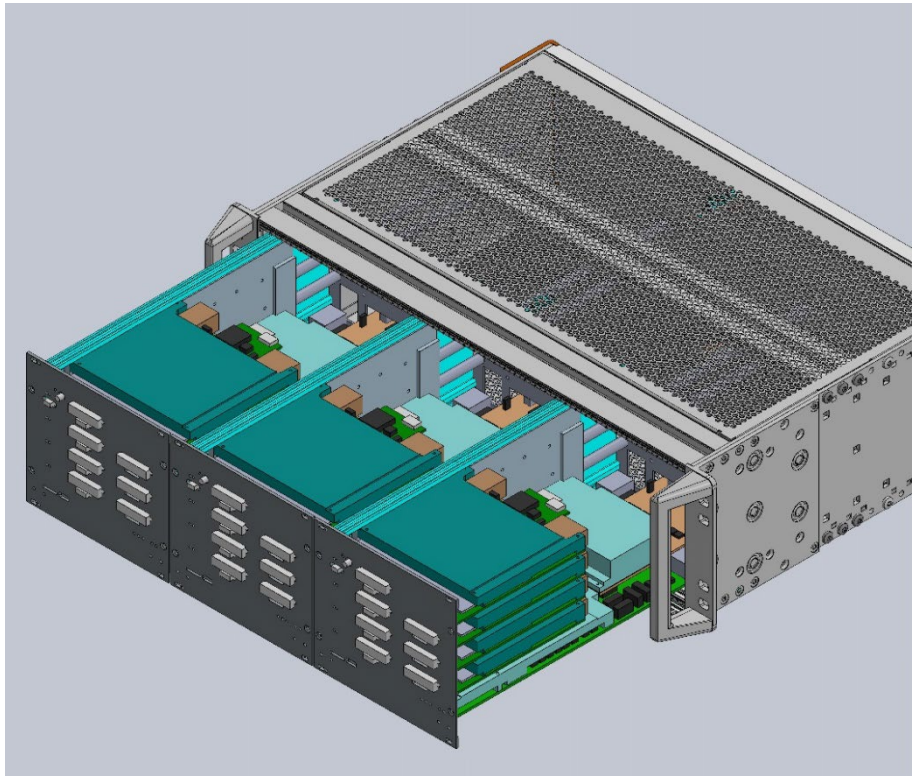
4th AGATA-GRETINA/GRETA collaboration meeting

November 20-22, 2024, ANL, USA

Phase 2 Electronics

AGATA phase 2 advancements in front-end electronics. *European Physical Journal A*, 59 (2023) 133.





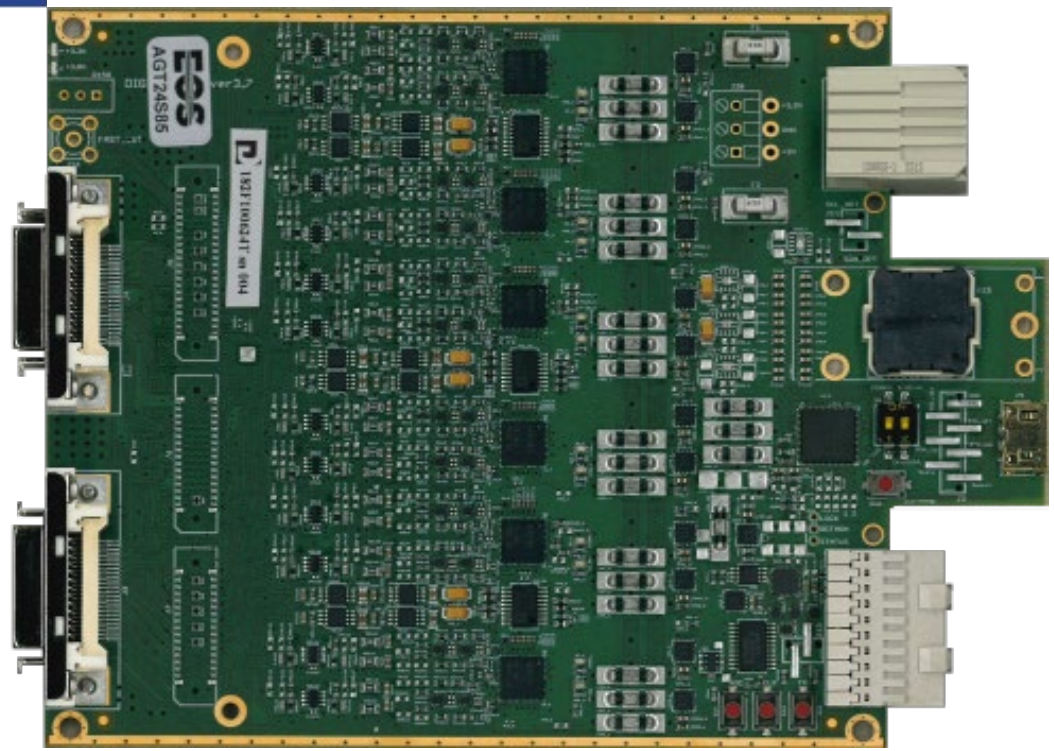
Follows the principles of the previous AGATA front-end electronics: Independent digitizer and pre-processing electronics for each capsule, only “connected” through the Global Trigger and Synchronization system.

The motivation to design a new electronics

- In the earlier versions of the AGATA electronics the samples transfer done with several (7 for phase 0 and 4 for Phase 1) 60 m to 100 m long 12-fold optical fibers.
- Obsolete critical components in the previous versions of the pre-processing electronics will not be present.
- The introduction of commercial mezzanines as main building blocks, improves production yield, reduces development time and facilitates maintenance.
- Avoiding customized point-to point data transfer after pre-processing: avoids customized interfaces and allows flexibility in the architecture of the Data Flow and processing server farms improving the rate capabilities.
- Improvements in the data transmission rates will allow the implementation software triggers in addition to the hardware GTS and SMART Trigger Processors.
- Pre-processing FPGA resources, presently used at < 50% level (except for the memory blocks, used at ≈ 80% level), allowing improvements in the preprocessing algorithms.
- The new Digi-Opt12 sampling board include improvements in the signal-to-noise quality and remove obsolete fundamental components and reduce power consumption.
- Extended monitoring for the input samples and for the pre-processing signals.

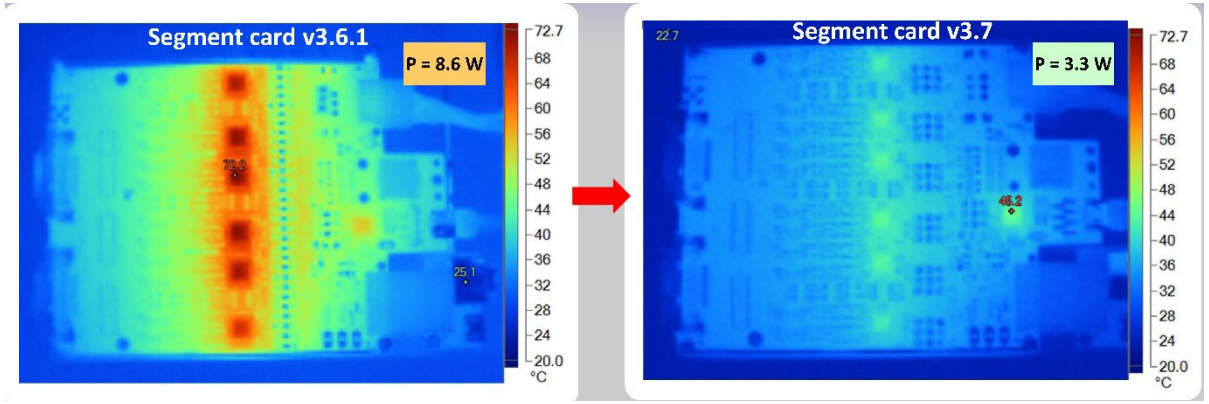
Implementation: DIGI-OPT12 v3.7

Alberto Pullia and Stefano Capra, INFN - Milano University of Milano



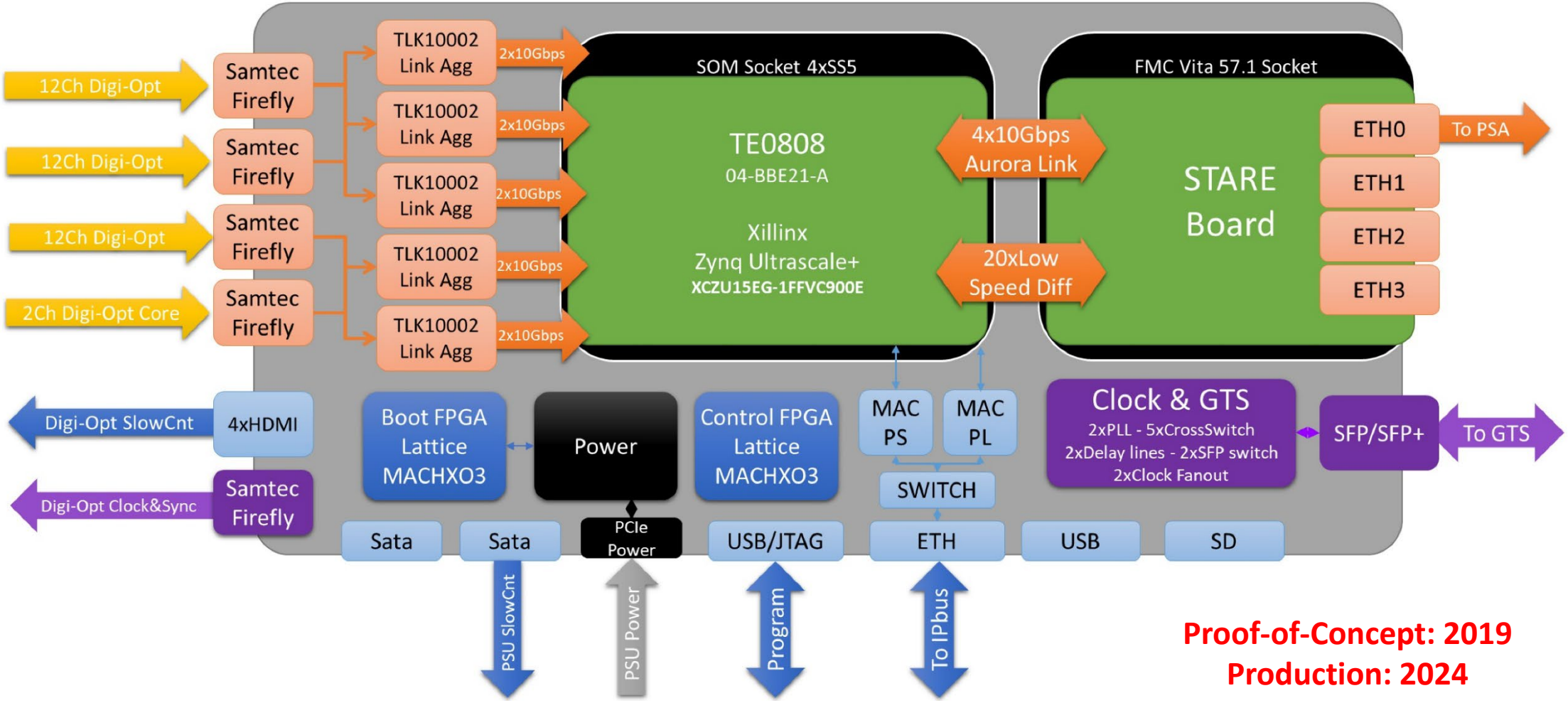
- Card redesign for ADC32J44 Dual-Channel, 14-Bit, 100-MSPS ADC's with JESD204B Interface.
- Two boards Segment & Core versions
- New design of signal conditioning stage
- Production yield: 94.6% after repairs 100%
- ~50% lower power consumption
- Includes as well low noise LTC6247 opamp that allows to reach σ = 1.5 LSB i.e. ENOB = 11.6

Input from pre-amplifiers by 10m MDR cables
Requires 1 backplane with power distribution and 1 backplane with the 100 MHz clock distribution.
FireFly copper cable readout at 2Gbps



Pre-processing block diagram

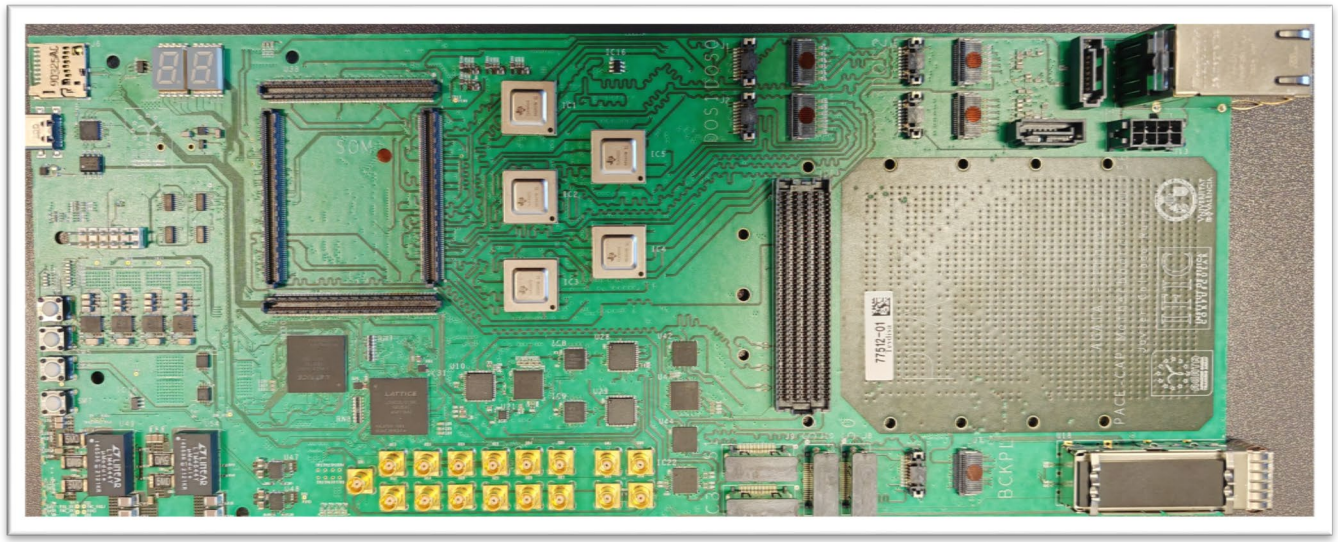
J.Collado, V.Gonzalez, IFIC – CSIC and ETSE University of Valencia
N. Karkour X. Lafay et al., IJCLab, Orsay France and the AGATA FEE W.G.
Slow Control & monitoring Scope Ch. Bonnin, IPHC Strasbourg



Proof-of-Concept: 2019
Production: 2024

Implementation: Pre-processing board PACE

J.Collado, V.Gonzalez, IFIC – CSIC and ETSE University of Valencia

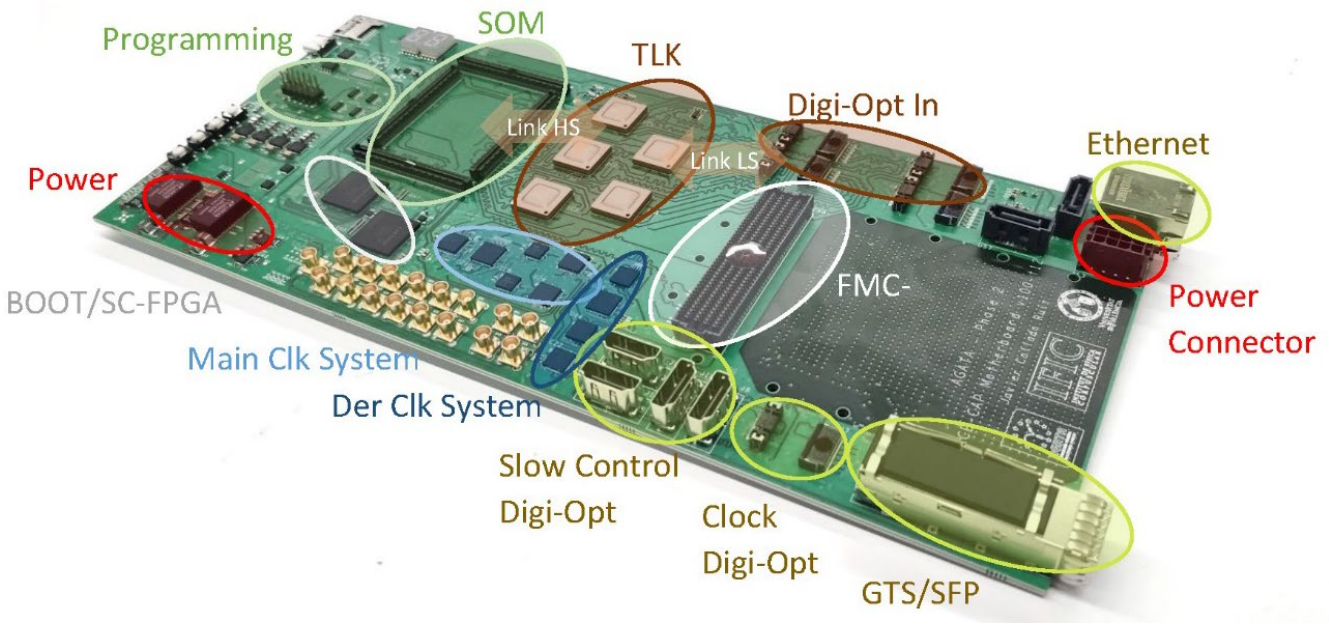


- Read-out the DIGI-OPT12 boards through FireFly
- Time Domain Multiplexing link aggregation (IDM) concept built in the receiver section implemented with TLK10002 (TI).
- IDM allows to use more efficiently the FPGA Transceivers .
- Global Trigger and Synchronization is fully supported (GTS or SMART).
- The link provides a common clock to all the system that is cleaned and fine-tuned during the alignment protocol in the PACE Clock & GTS hardware section.
- Following the pre-processing on the SOM FPGA, all the events validated by the GTS second level trigger, are readout via the Ethernet STARE board, plugged into the FMC Vita 57.1

With a SoM TE0808-05-BBE81-E
by Trenz Electronics based on the
AMD Zynq™ UltraScale+™
XCZU15EG-1FFVC900E
(746,550 Logic Cells and 24 transceivers)
with 4 GByte DDR4

Implementation: Pre-processing board PACE

J.Collado, V.Gonzalez, IFIC – CSIC and ETSE University of Valencia



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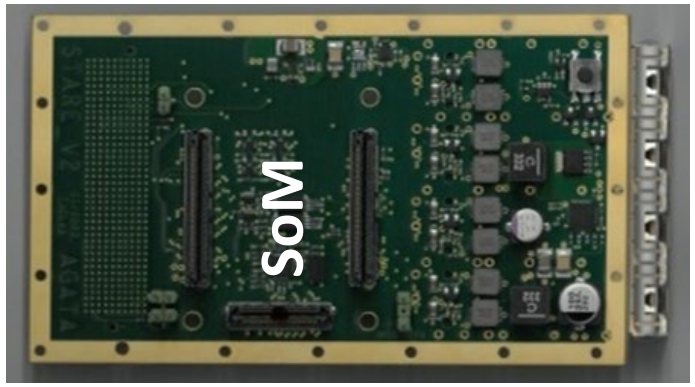
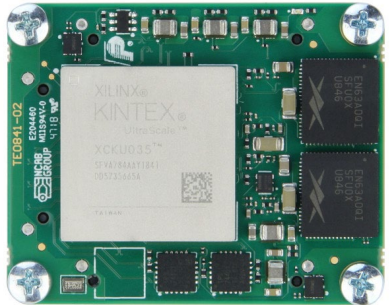
Implementation: Ethernet board STARE

N. Karkour X. Lafay et al., IJCLab, Orsay France



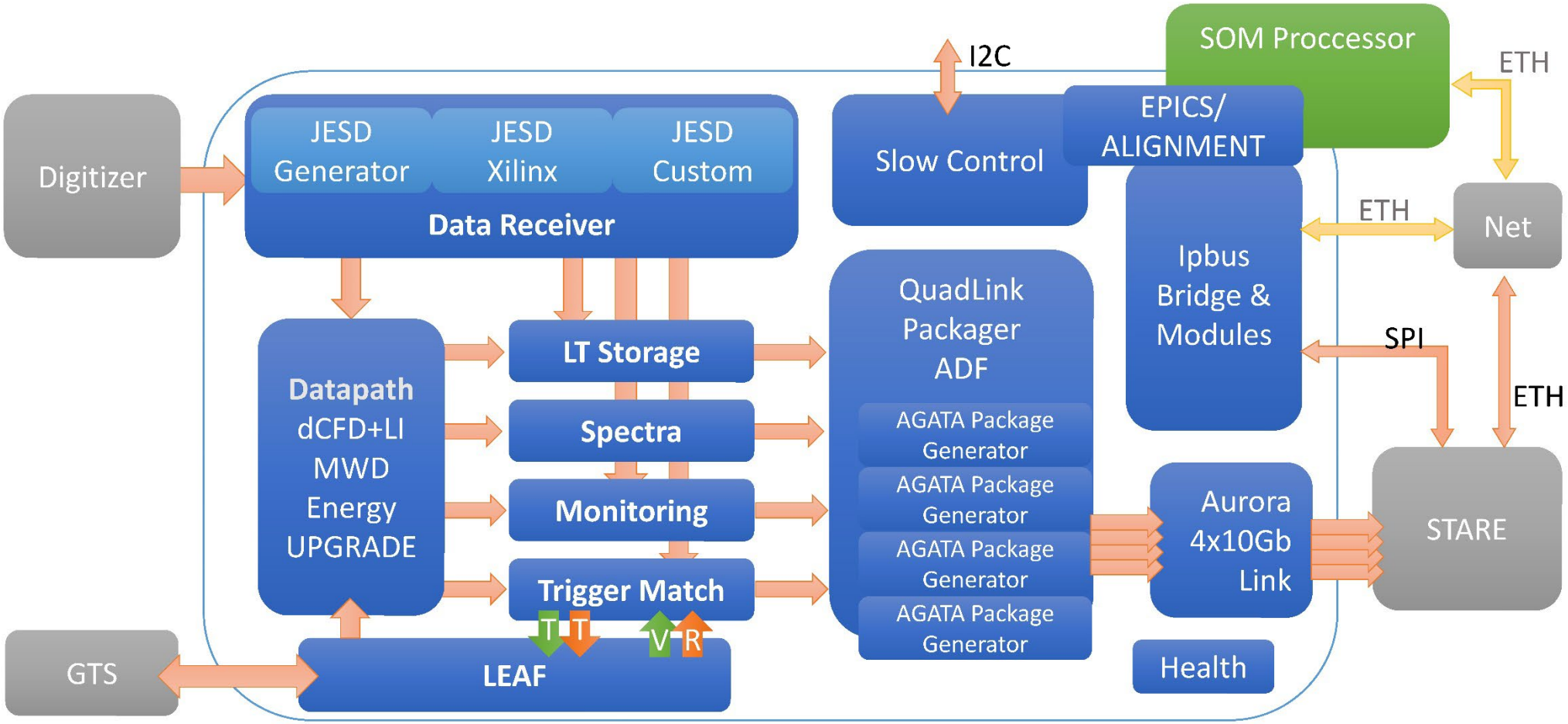


With a SoM TE0841-03-41I31-A
by Trenz Electronics based on the
AMD Kintex™ UltraScale™
XCKU040-1SFVA784I FPGA (530,250 Logic Cells and 8 transceivers)
with 4 GByte DDR4

- The STARE board is a FMC mezzanine to be mounted on PACE pre-processing
- Its function is to do the readout using fast Ethernet protocol at high bandwidth.
- The STARE mezzanine compiles the generated data from the PACE over a Xilinx AXI stream AURORA interface, using up to 4 independent 10 Gbps transceiver lines.
- Each line data is formatted to be transferred through 4 independent 10 Gbps transceivers to servers or computer farm using UDP protocol. Each of the 4 UDP channels can send data to several different servers.
- The STARE module is equipped with external memory to allow re-transmission of any packages not correctly received by the HTC server farm.

Firmware for the Pre-processing board PACE

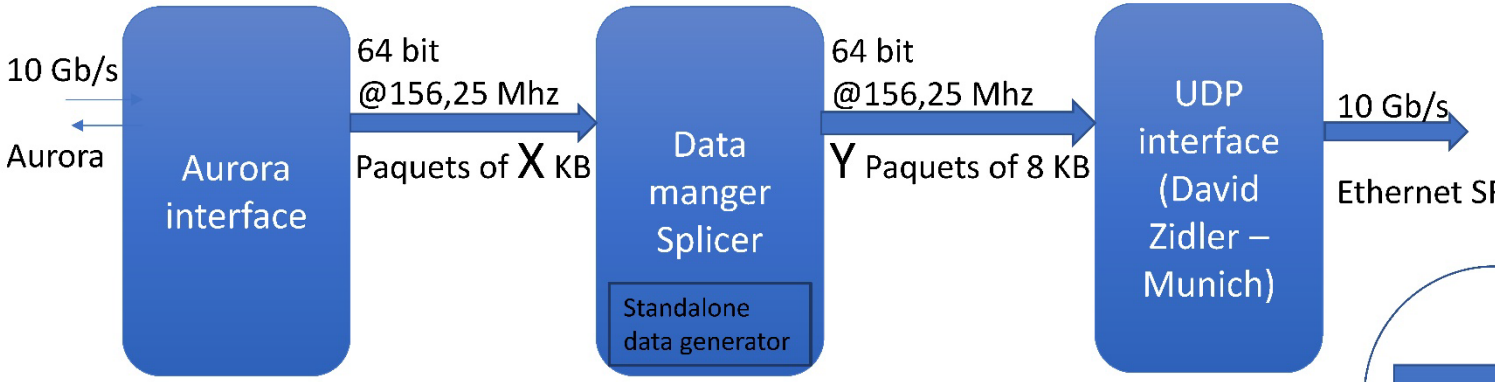
J.Collado, V.Gonzalez, IFIC – CSIC and ETSE University of Valencia, Spain



All firmware modules existing. Required revision of the GTS Leaf, and the AGATA Package generator.
Migration to the Global Trigger and Synchronization SMART system foreseen in Phase 2.
New Energy evaluation algorithm developed by M. Kogimtzis, STFC, UK

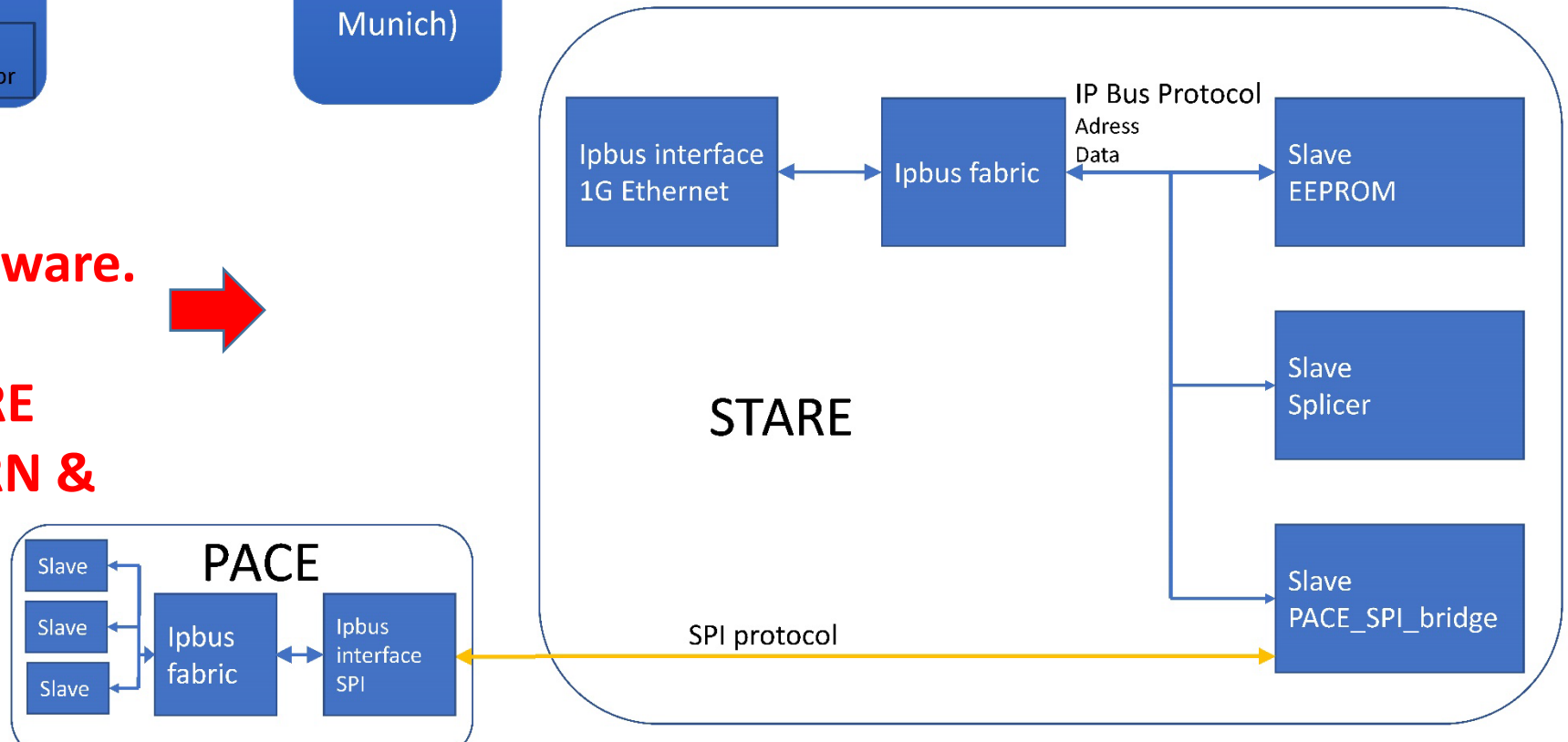
Firmware for the Ethernet board STARE

N. Karkour X. Lafay et al., IJCLab, Orsay France



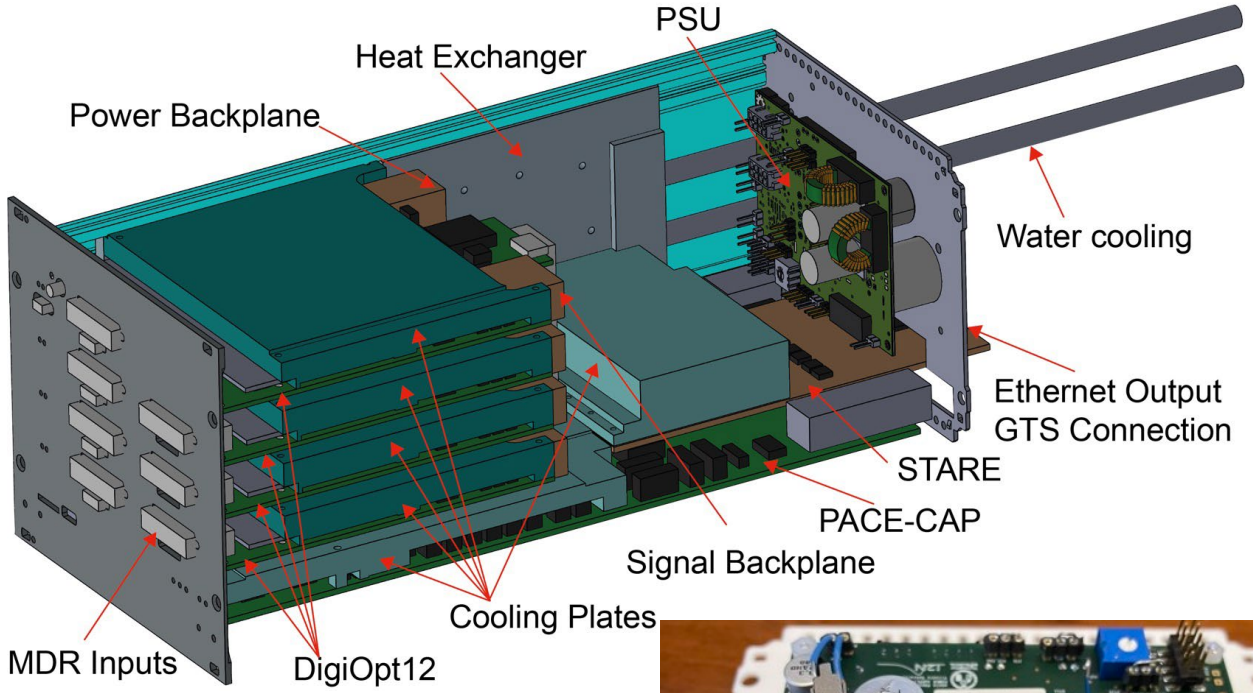
Data Path Firmware with UDP in the future RUDP

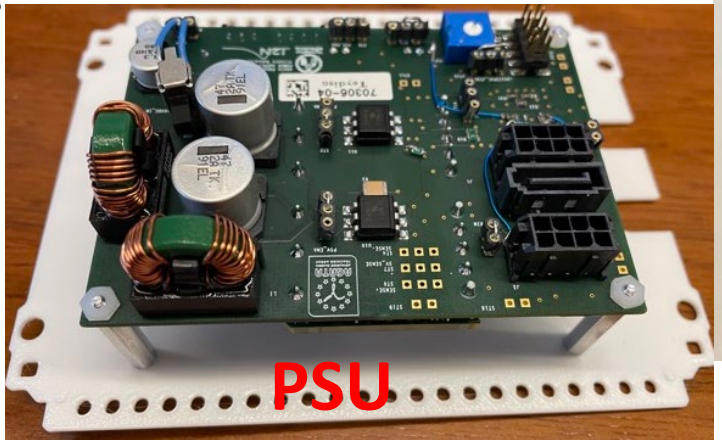
IPbus Master/Slave Firmware. Presently IPbus control performed through STARE IP_Bus SlowControl (CERN & LPSC Grenoble)



Implementation: mechanics and PSU

V.Gonzalez, ETSE University of Valencia





Schedule for the Completion and Production of the Phase 2 Electronics

DIGIOPT12 (V3.6, V3.7, V3.71)

80 channels (3 Segments + 1 Core) produced or under production

STARE Ethernet Interface board

135 STARE boards + Spares Already produced

PACE Pre-Processing Board

70 PACE Ordered, delivery scheduled early 2025

PACE Pre-processing firmware

95% completed ongoing final formatting and GTS still to test

STARE Data transfer Firmware

Completed a production version with UDP protocol working stable

RUDP version under discussion

Outlook: AGATA Electronics beyond Phase 2

R&D Starting for the AGATA Front-End Electronics beyond Phase 2: based on the Digital – Preamplifier concept.

- **Cryogenic ASIC developments (Uni Milano, INFN, CNRS, CEA, GANIL)**
  Low-noise, analog, cryogenic ASIC pre-amplifiers.
  Designing cryogenic ASICS requires to realize and characterize series of single components and small circuit structures in order to build cryogenic models.
  The goal is the realization and characterization of monolithic cryogenic pre-amplifiers for anode or cathode electrode signals
- **Low-Power, Low-Noise Digitizers for cryogenic ASIC readout. (Uni. Valencia, Uni. Milano, INFN)**
  The goal is a low power ADC board, with target performance ENOB of 12 bits at 100 MHz.
  Commercial FADCs IC with such performance and 100mW per channel exists.
  The ADC should include the JESD240 protocol and serial outputs to make use of PACE.
- **Interconnection and Cyostat development for the Digital Preamplifier. (CNRS, Uni.Cologne)**
  The Digital Preamplifier concept requires developments in the AGATA cryostat including the interconnection between the Digital-preamplifier ASIC and the warm Digitizer board.

Acknowledgements

Thanks to the AGATA Front-End Electronics Working Group

&

the Data Processing Working Group (Data Acquisition and Control)

The new Global Trigger and Synchronization System SMART is being developed by G. Wittwer et al., GANIL, France

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