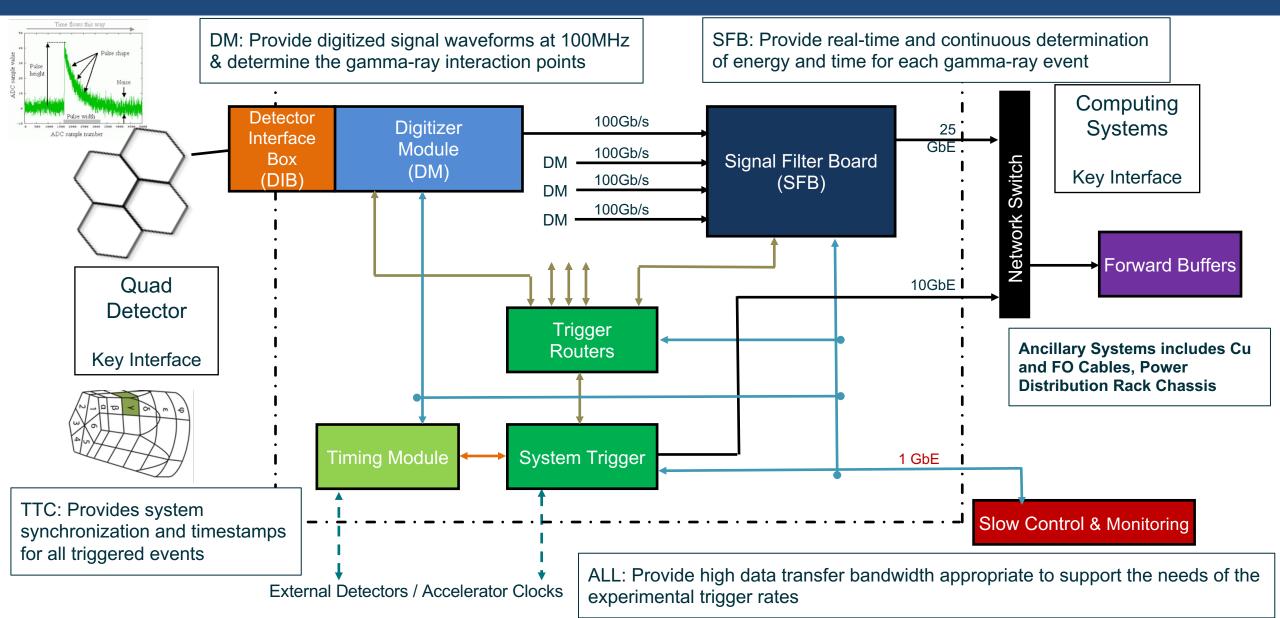
GRETA Electronics





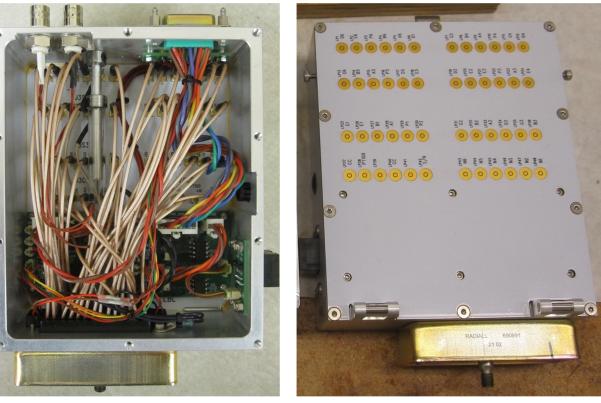
Electronics Scope and Key Capabilities



Detector Interface Box

- Interface between Detector and Digitizer Module
- Routes Power to the Detector, Temperature monitor, Analog Core Contact output

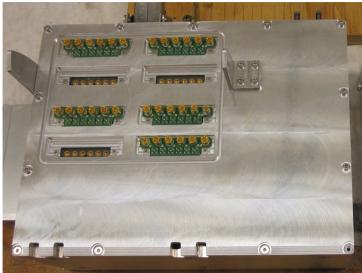




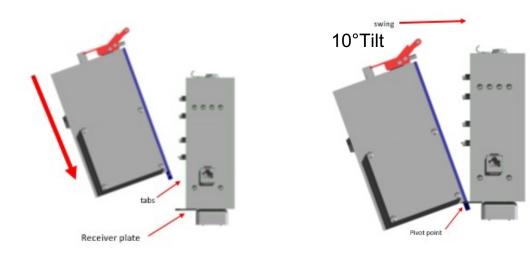
Digitizer Module

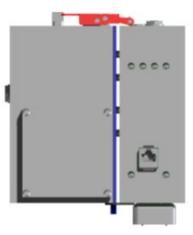
- Digitize the detector signals and streams them to the Signal Filter Board
- 40 (36 segments + 4 gain ranges for the core contact, all LTC2194) 100MHz 16-bit digitizers, selected to minimize integral and differential non-linearity) – organized on 3x12channel segment boards and a CC board
- 300 MHz CC ADC for triggering (fast timing signal) outputs trigger primitives (TS of LEDs) to the trigger system
- Receives 48-bit global clock from the timing system
- 100 Mb data output (10 x 10Gb) on proprietary protocol over 16-strand MTP fiber cable – all ADC data + metadata (e.g. TS) is streamed from the DM units
- 10 Gb control link allows "scope mode" computer-based oscilloscope capability
- Cooled by dedicated glycol cooling loop via cooling block

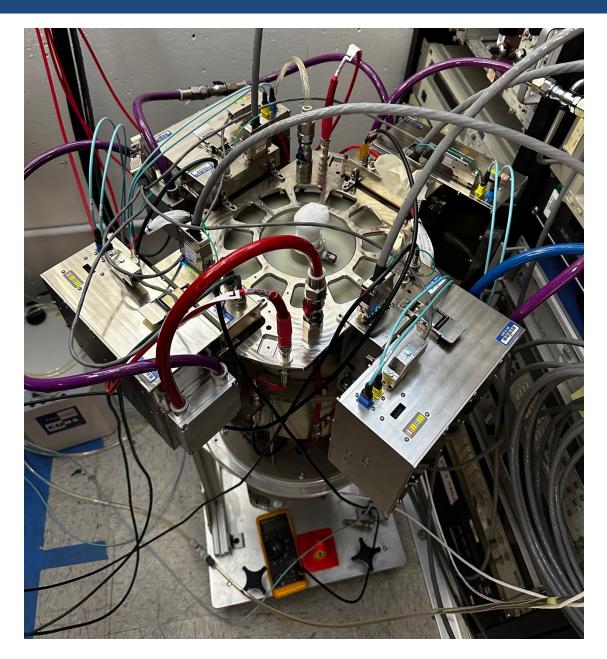




Digitizer Module Installation Scheme

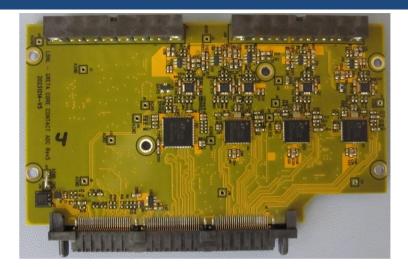


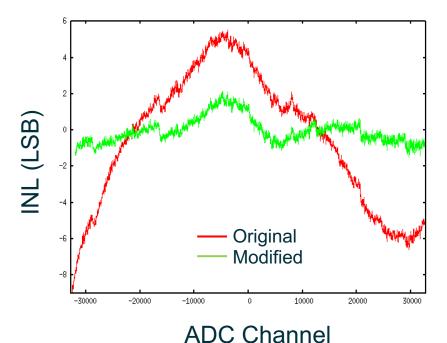




Digitizer Module – Core Contact Board

- Discovered an integral linearity issue on the core contact board
 - Anti-alias filter
 - Input impedance change for out of range ADC channels
 - Intra ADC crosstalk for out of range ADC channels
- Core contact is digitized in 5 ADC channels
 - 4x Data Acquisition with different gains
 - 1x Fast trigger ADC
- Redesigned board
 - Added input buffer amplifier
 - Added additional ADC chip (chip use single channel)
- INL significantly improved
 - Original (+5.3,-6.3 LSB) (red trace)
 - Modified (+1.8,-1.2 LSB) (green trace)
 - Spec <= +/- 2 LSB



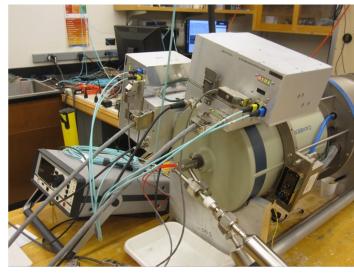


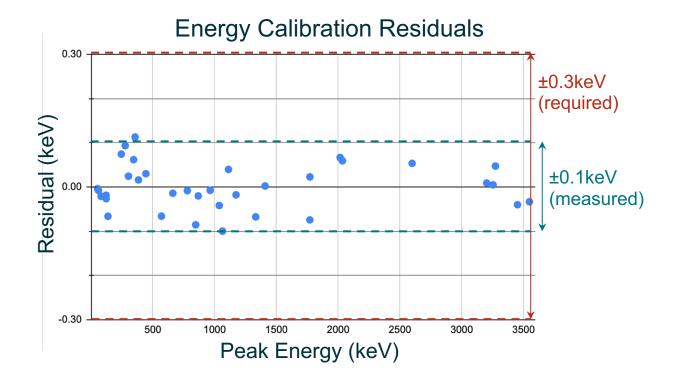
Digitizer Module Core Contact Performance

Energy Resolution

Peak (@ rate)	FWHM [keV]	Req. [keV]
60 keV (1 kHz)	1.361±0.001	<= 1.4
1332 keV (1 kHz)	2.314±0.006	<= 2.5
1332 keV (50 kHz)	3.08±0.01	<= 3.5

Measurements carried out with production hardware and firmware (including SFB)





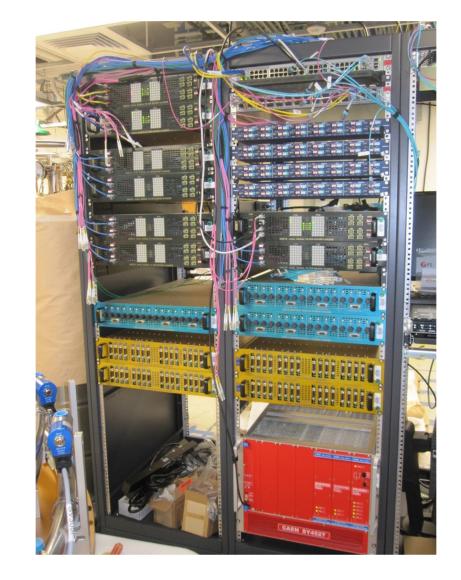
Measured: ± 0.1 keV Spec: ± 0.3 keV (over 10 MeV)

- Testing also confirms that the Digitizer Module meets temperature stability requirements
 - Gain is stable to <= 0.03% across full range over 12
 - hours, or $\pm 2^{\circ}$ C temperature change

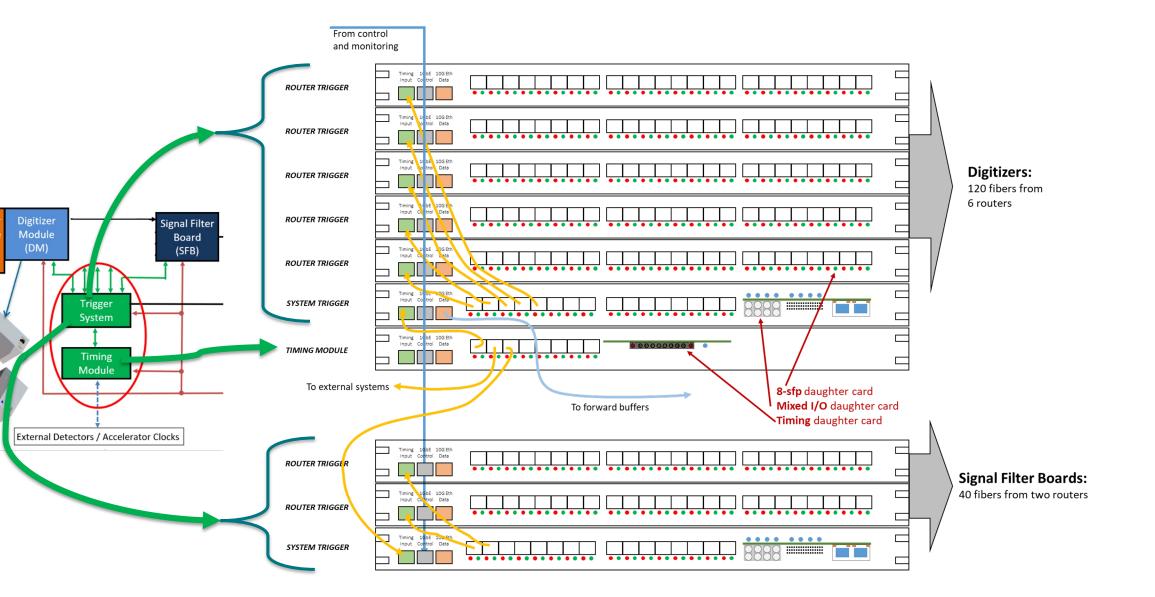
Signal Filter Board

- Receives detector ADC data, runs digital filter to extract energy and timing information and select waveform snippets
- On trigger validations, routes the data to the forward buffer with compressed waveforms as UDP datagrams (25 Gb interface)
- Based on off-the-shelf Hi-Tech FPGA board with Xilinx Virtex Ultrascale FPGA
- One FPGA per Quad module; packed as 2u units serving two Quads





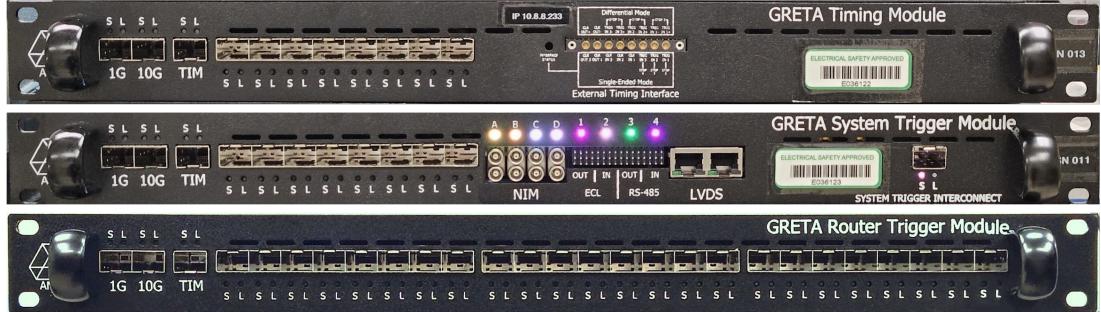
System Components – Trigger System Detail



System Components – Module Overview

One design, 3 configurations using 4 FMC plug in cards:

- Timing Module: Provides the source of clock throughout the system, as well as clock interface for external detectors.
- System Trigger Module: Distributes clock from timing master to the routers and provides trigger logic for SFB and Digitizer systems. Also provides trigger diagnostics and summary data via its 10GBPS Ethernet interface
- Router Trigger Module: Provides fanout of timing and trigger to the digitizer and SFB endpoints. Also
 provides aggregation of event information being sent back to the system trigger from the endpoints



Ancillary Systems

- Digitizer Module Power Supplies
 - TDK Lambda power supplies 4 Quads in 2u chassis
- Cable Breakout Chassis
 - Receive and distribute LV from CAEN modules; provide interlocks and AC power for fans and LN bayonet heater
- Detector HV (and LV)
 - CAEN HV and LV cards, individually floating HV channels
- Custom fiber plant
 - Includes custom fiber breakout units (passive) and spider cables

