Développements de techniques d'interconnexion sans masques pour détecteurs à pixel

G. Calderini
LPNHE Paris

Outline

In this presentation I will talk mainly of recent development in the field of sensor-readout pixel interconnections

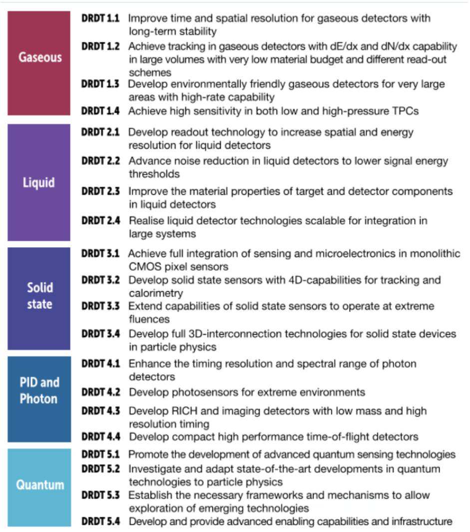
I will deal in particular with Anisotropic Conductive Films (ACF) and Anisotropic Conductive Pastes (ACP), with results coming from a few projects (AIDAInnova, future DRD3 Collaboration)

Since there has been the first Collaboration Meeting of DRD3 last week at CERN, I will also give a short report a few general topics about the DRD3/WG7 https://indico.cern.ch/event/1402825/

Jerome plans to give a more general summary of the DRD3 meeting in his presentation

ECFA Detector R&D Themes

These themes, identified in the Roadmap, are **critical** to achieve the science programme outlined in the ESPP (The European Strategy for Particle Physics) and are **derived from the technological challenges** that need to be overcome for the scientific potential of the future facilities.



Gaseous	**DRDT 1.1**	Improve time and spatial resolution for gaseous detectors with long-term stability
	DRDT 1.2	Achieve tracking in gaseous detectors with dE/dx and dN/dx capability in large volumes with very low material budget and different read-out schemes
	DRDT 1.3	Develop environmentally friendly gaseous detectors for very large areas with high-rate capability
	DRDT 1.4	Achieve high sensitivity in both low and high-pressure TPCs
Liquid	**DRDT 2.1**	Develop readout technology to increase spatial and energy resolution for liquid detectors
	DRDT 2.2	Advance noise reduction in liquid detectors to lower signal energy thresholds
	DRDT 2.3	Improve the material properties of target and detector components in liquid detectors
	DRDT 2.4	Realise liquid detector technologies scalable for integration in large systems
Solid state	**DRDT 3.1**	Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors
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	DRDT 3.3	Extend capabilities of solid state sensors to operate at extreme fluences
	DRDT 3.4	Develop full 3D-interconnection technologies for solid state devices in particle physics
PID and Photon	**DRDT 4.1**	Enhance the timing resolution and spectral range of photon detectors
	DRDT 4.2	Develop photosensors for extreme environments
	DRDT 4.3	Develop RICH and imaging detectors with low mass and high resolution timing
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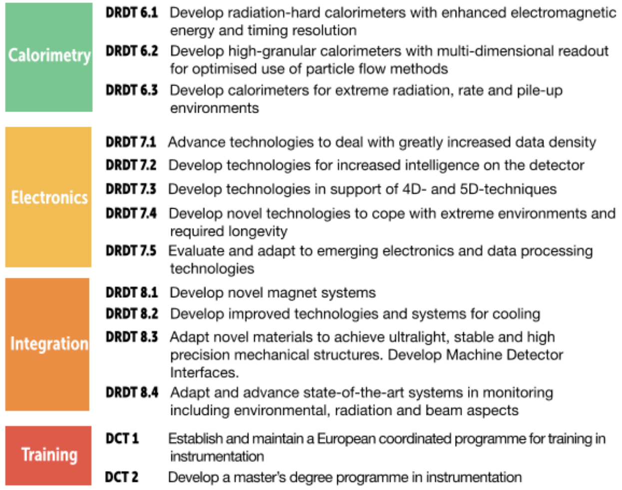
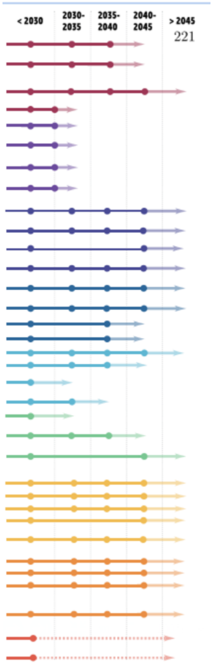
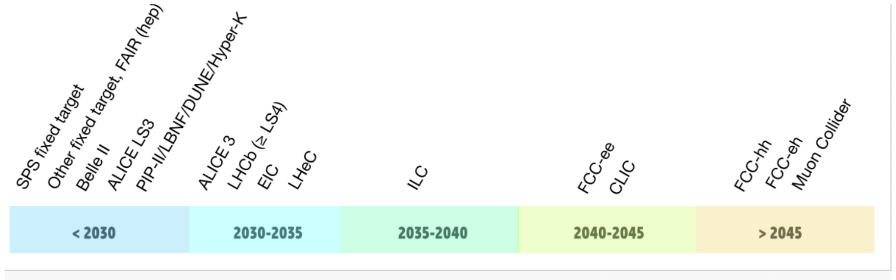
Quantum	**DRDT 5.1**	Promote the development of advanced quantum sensing technologies
	DRDT 5.2	Investigate and adapt state-of-the-art developments in quantum technologies to particle physics
	DRDT 5.3	Establish the necessary frameworks and mechanisms to allow exploration of emerging technologies
	DRDT 5.4	Develop and provide advanced enabling capabilities and infrastructure



Calorimetry	**DRDT 6.1**	Develop radiation-hard calorimeters with enhanced electromagnetic energy and timing resolution
	DRDT 6.2	Develop high-granular calorimeters with multi-dimensional readout for optimised use of particle flow methods
	DRDT 6.3	Develop calorimeters for extreme radiation, rate and pile-up environments
Electronics	**DRDT 7.1**	Advance technologies to deal with greatly increased data density
	DRDT 7.2	Develop technologies for increased intelligence on the detector
	DRDT 7.3	Develop technologies in support of 4D- and 5D-techniques
	DRDT 7.4	Develop novel technologies to cope with extreme environments and required longevity
	DRDT 7.5	Evaluate and adapt to emerging electronics and data processing technologies
Integration	**DRDT 8.1**	Develop novel magnet systems
	DRDT 8.2	Develop improved technologies and systems for cooling
	DRDT 8.3	Adapt novel materials to achieve ultralight, stable and high precision mechanical structures. Develop Machine Detector Interfaces.
	DRDT 8.4	Adapt and advance state-of-the-art systems in monitoring including environmental, radiation and beam aspects
Training	**DCT 1**	Establish and maintain a European coordinated programme for training in instrumentation
	DCT 2	Develop a master's degree programme in instrumentation





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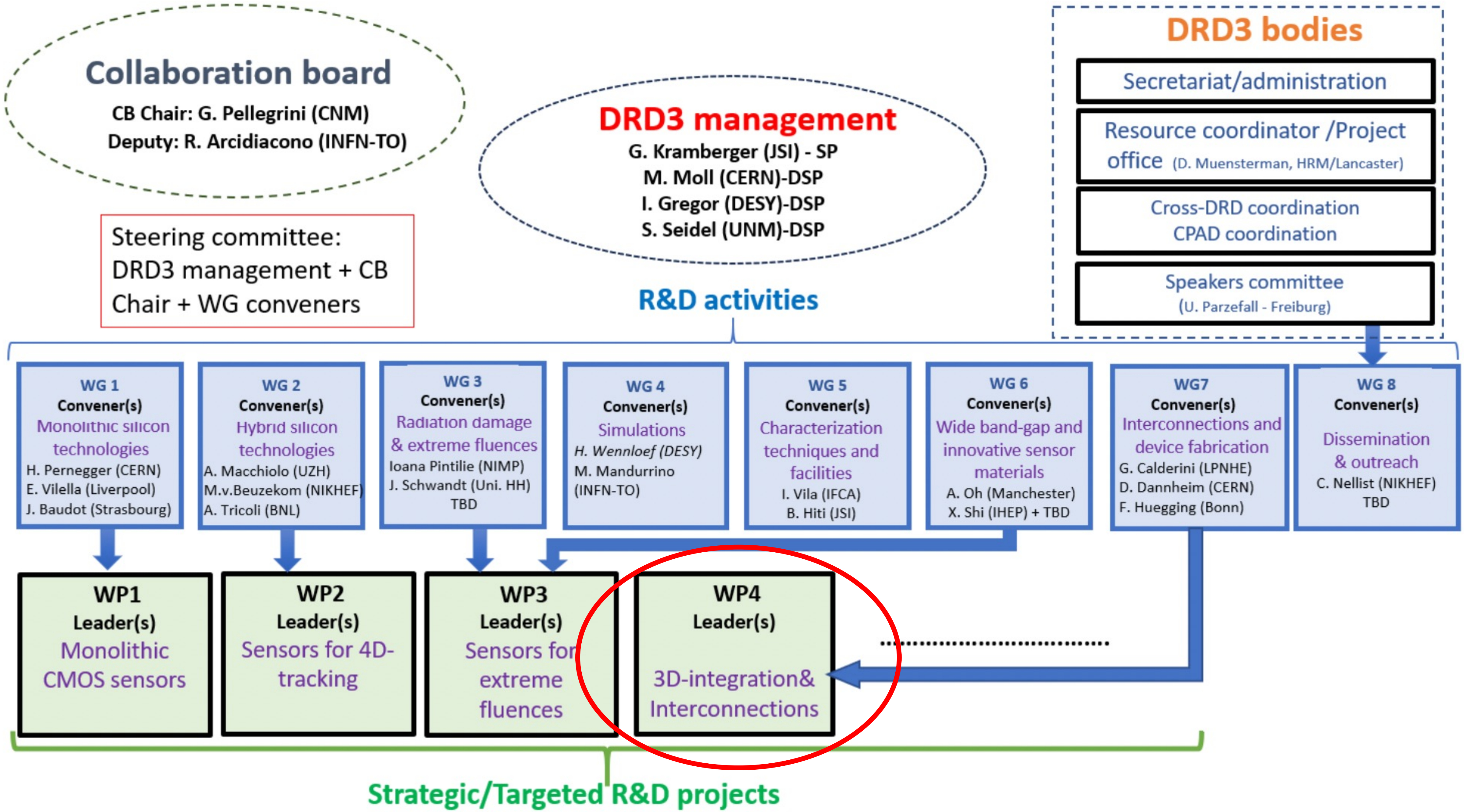

Collaboration board

CB Chair: G. Pellegrini (CNM)
Deputy: R. Arcidiacono (INFN-TO)

Steering committee:
DRD3 management + CB Chair + WG conveners

DRD3 management

G. Kramberger (JSI) - SP
M. Moll (CERN)-DSP
I. Gregor (DESY)-DSP
S. Seidel (UNM)-DSP

DRD3 bodies

- Secretariat/administration
- Resource coordinator /Project office (D. Muensterman, HRM/Lancaster)
- Cross-DRD coordination CPAD coordination
- Speakers committee (U. Parzefall - Freiburg)

R&D activities

WG 1
Convener(s)
Monolithic silicon technologies
H. Pernegger (CERN)
E. Vilella (Liverpool)
J. Baudot (Strasbourg)

WG 2
Convener(s)
Hybrid silicon technologies
A. Macchiolo (UZH)
M.v.Beuzekom (NIKHEF)
A. Tricoli (BNL)

WG 3
Convener(s)
Radiation damage & extreme fluences
Ioana Pintilie (NIMP)
J. Schwandt (Uni. HH)
TBD

WG 4
Convener(s)
Simulations
H. Wennloef (DESY)
M. Mandurrino (INFN-TO)

WG 5
Convener(s)
Characterization techniques and facilities
I. Vila (IFCA)
B. Hiti (JSI)

WG 6
Convener(s)
Wide band-gap and innovative sensor materials
A. Oh (Manchester)
X. Shi (IHEP) + TBD

WG7
Convener(s)
Interconnections and device fabrication
G. Calderini (LPNHE)
D. Dannheim (CERN)
F. Huegging (Bonn)

WG 8
Convener(s)
Dissemination & outreach
C. Nellist (NIKHEF)
TBD

WP1
Leader(s)
Monolithic CMOS sensors

WP2
Leader(s)
Sensors for 4D-tracking

WP3
Leader(s)
Sensors for extreme fluences

WP4
Leader(s)
3D-integration& Interconnections

……………………………

Strategic/Targeted R&D projects

DRD3/WP7

35 groups expressed interest in this WG in questionnaire circulated last year

18 submitted now specific EoI centered on activities; process till open

We identified four main axes of research

- Maskless processes and fast interconnections for testing

  RG 7.1: Yield consolidation for fast interconnection technologies

  RG 7.2: Demonstration of in-house process for single dies and pixel interconnections for a range of pitches (down to < 30 µm)

- Improved classical flip-chip technologies for process accessible to labs

  RG 7.3: Development of post-processing for classical bumping interconnection

  Bump-bonding techniques for small pitch

- Multi-chip and module interconnections (flexes)

  RG 7.3: Development of post-processing for classical bumping interconnection

  Validation of demonstrator modules (test beam, radiation hardness)

- 3D integration

  RG 7.4: Development of wafer-to-wafer approach in presently advanced interconnection

  RG 7.5: Development of VIAS in multi-tier sensor/front-end assemblies

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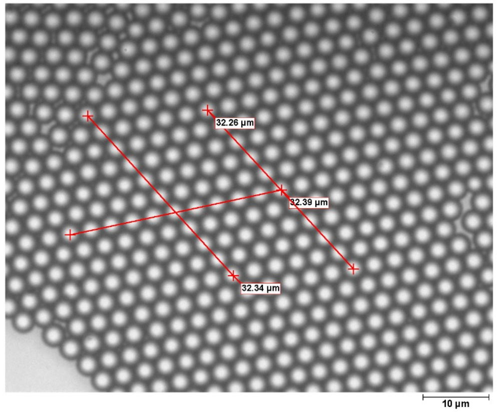
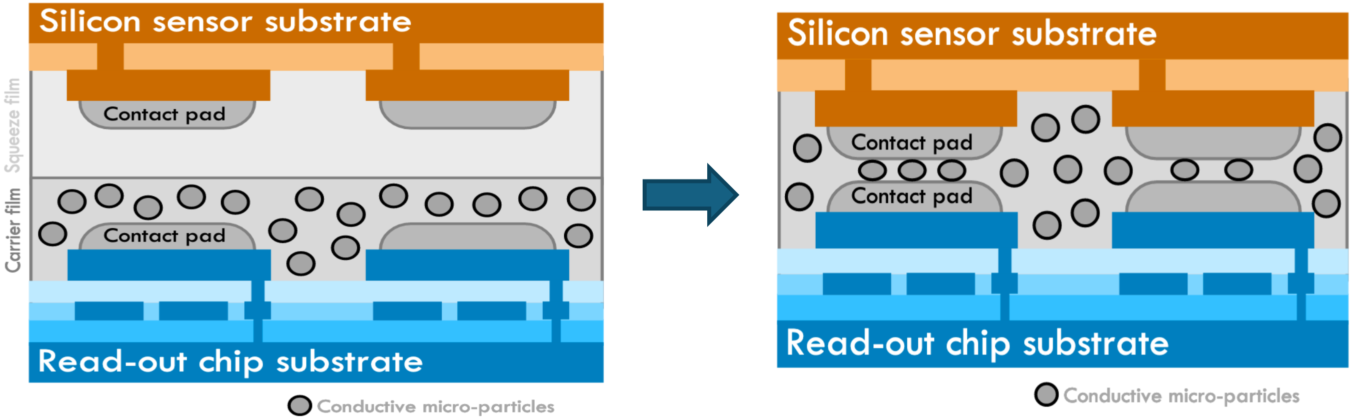
Maskless interconnections: anisotropic conductive films (ACF)

Anisotropic conductive films can be used as interconnection technique

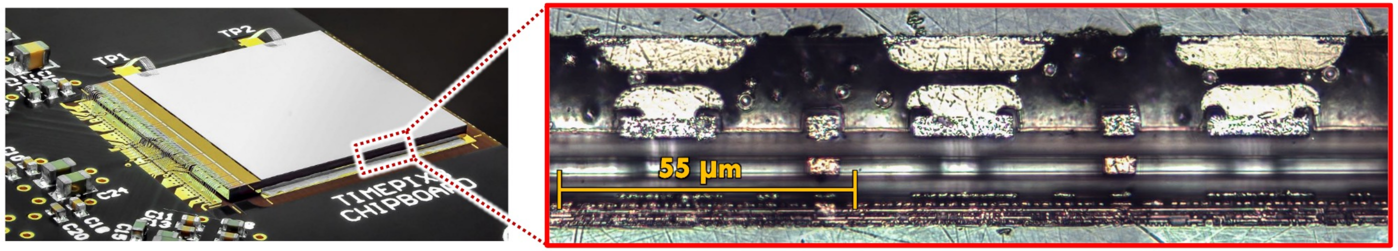
Application potentially important also from the cost point of view, bump represent a significant fraction of the hybridization cost of pixel modules





UBM is still required to obtain the particle adhesion, but it is a wet chemical deposition of Ni and Au (maskless process, low cost)

CERN has done a lot of progress on ACF and is trying to develop in-house deposition



M. Vicente, D. Dannheim et al.

Collaboration CERN EP-RD/LPNHE/UniGE/ Compart financed inside AIDAInnova WP in hybrid detectors

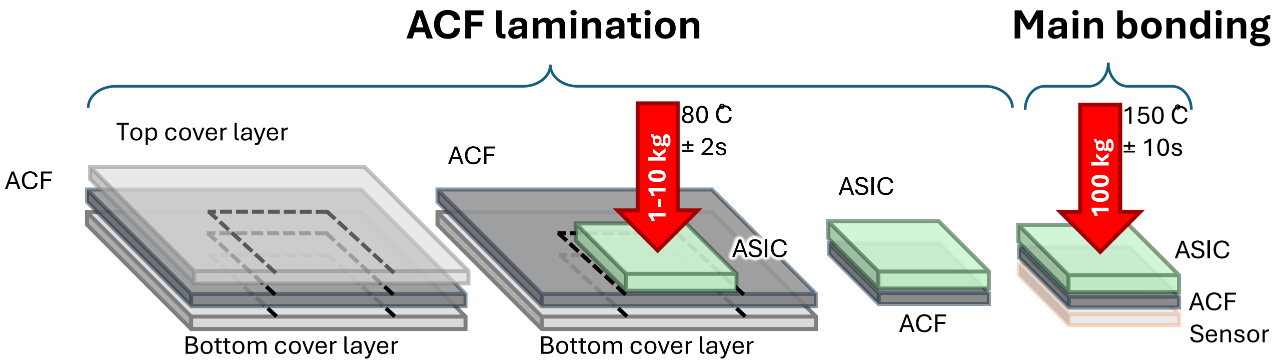
https://indico.cern.ch/event/1307202/contributions/5498740/attachments/2822534/4929452/240319_ACA_AIDAinnova%20Ahmet%20LALE%202.pdf

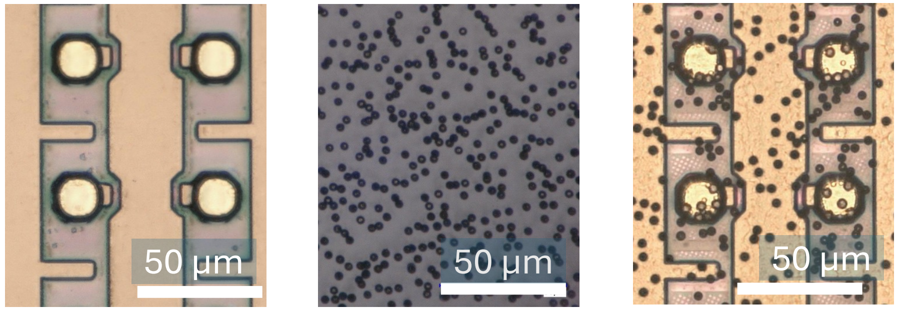
Anisotropic Conductive Adhesive (ACA) Bonding

UNIVERSITÉ
DE GENÈVE
FACULTÈ DES SCIENCES

- ACA connection done at Geneva University using semi-automatic flip-chip bonder
  - Precise temperature, pressure and alignment control
  - Heating <u>up to 400 ℃</u> and force applied by bonding arm <u>up to 100 kgf</u>
  - Available for bonding with **ACF/ACP**
- ACF bonding has two steps – lamination and bonding
  - Pressure applied to displace and compress particles
  - Epoxy cures at 150 ºC for a few seconds only

SET ACCµRA100
10 years old

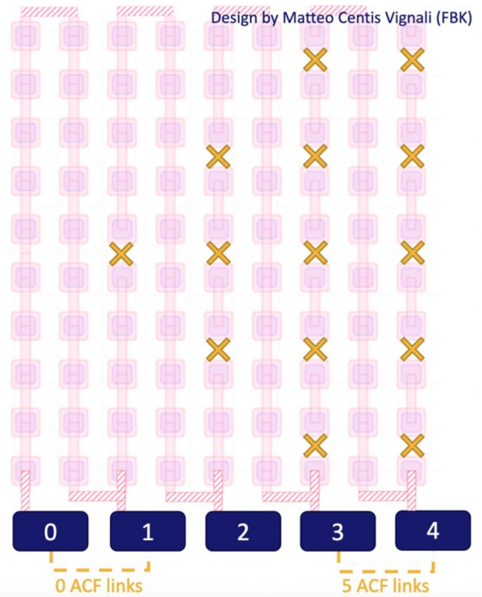


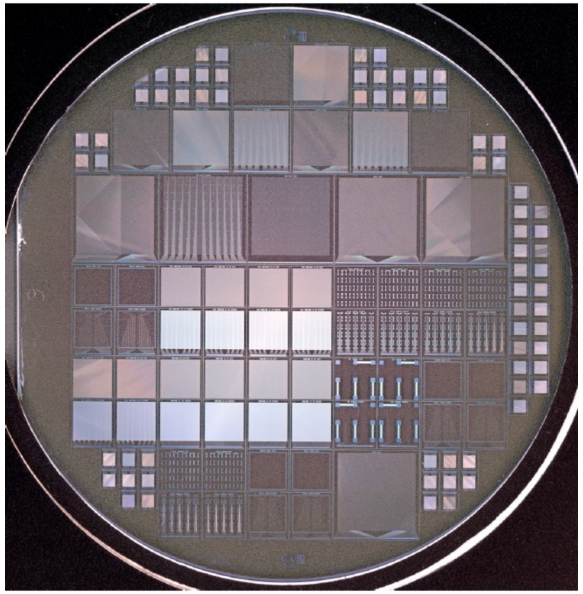


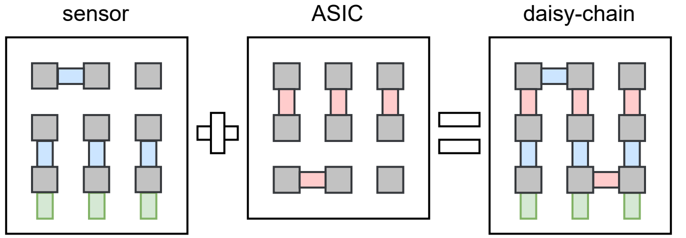
Mateus Vicente

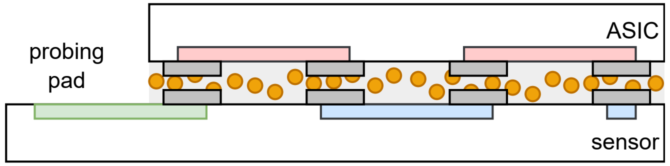
Dedicated daisy-chain studies – design

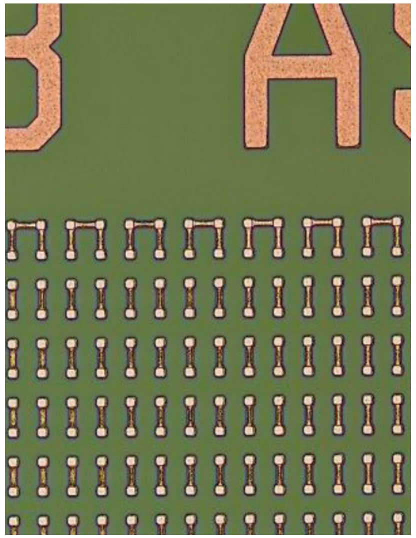
- Daisy-chain 6” quartz wafer with 625 μm thickness to characterize ACF/ACP performance
- Study of ACA interconnection properties
  - Low-pitch and large-pitch reliability
  - Different device size
  - Resistance measurements
  - Mechanical analysis







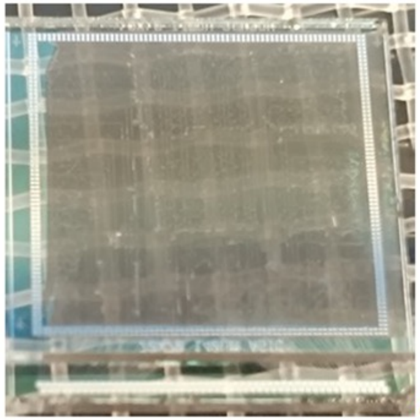




	pitch	size in mm	connections	per wafer	type	diceable
160x160 20um	20 um	3.2 x 3.2	25600	36	grid	no
CLICpix2	25 um	3.2 x 3.2	16384	34	grid	no
400x400 25um	25 um	20 x 20	640000	5	grid	yes
Timepix3	55 um	14 x 14	65536	4	grid	no
Timepix3 islands	55 um	14 x 14	65536	4	grid	no
RD53	50 um	20 x 20	160000	4	grid	no
RD53 islands	50 um	20 x 20	160000	2	grid	no
70x70 140um	140 um	20 x 20	2112	3	peripheral	yes
10x10 1000um	1000 um	20 x 20	400	3	grid	yes
3x3 4500um	4500 um	20 x 20	36	1	grid	yes

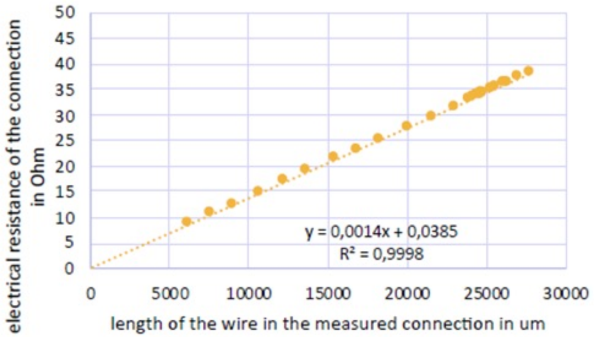
Dedicated daisy-chain studies – bonding

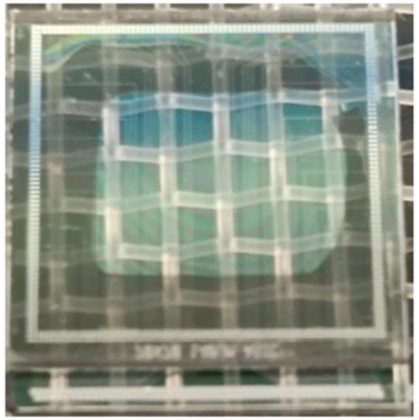
- Different ACA type bonding
  - Peripheral structure (2 rows, 140 µm pitch), used two types of ACF and one ACP
  - Consistent results, resistance less than 5 Ω per chain (8-9 connections)



3 µm particles

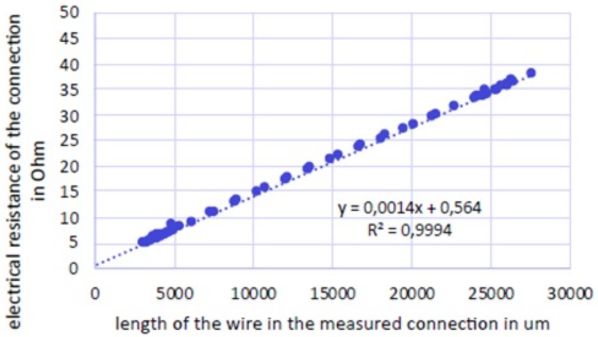
18 µm ACF – resistance measurement

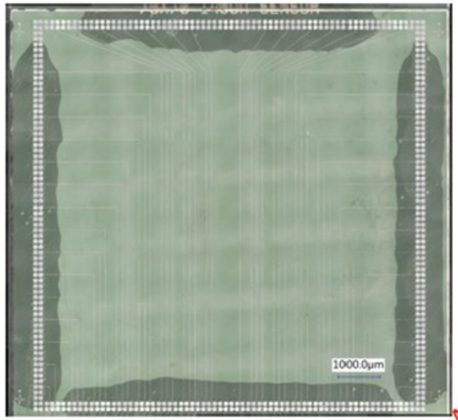




3 µm particles

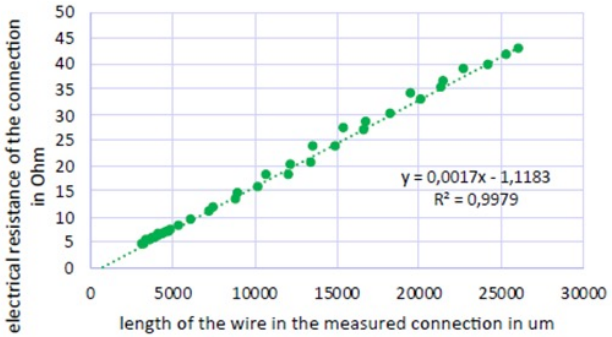
14 µm ACF – resistance measurement





4 µm particles

ACP – resistance measurement



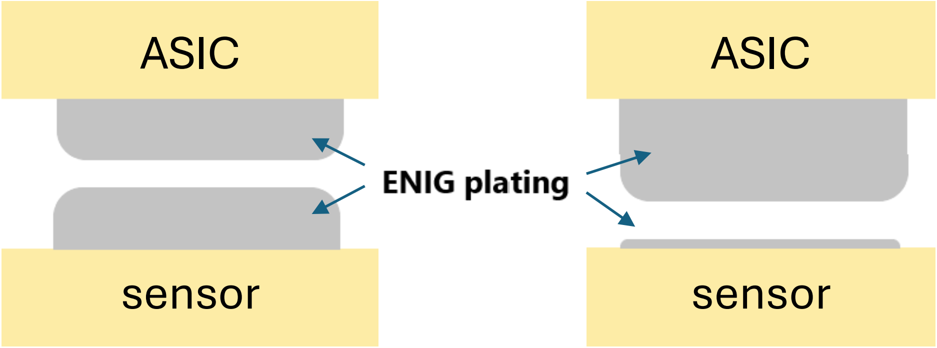
Peter Svihra

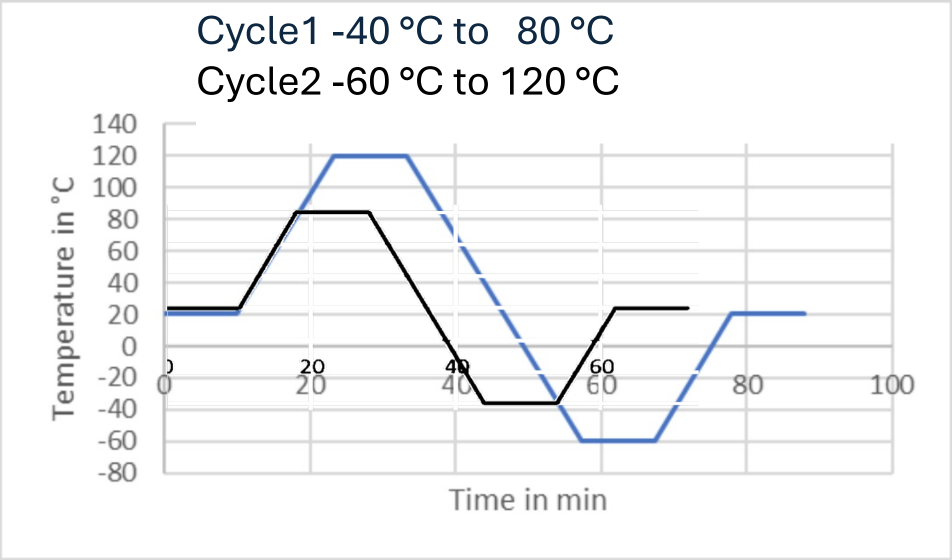
Dedicated daisy-chain studies – stability

Study of performance after thermal cycling

- <u>10x10 pixels with 1 mm pitch</u>
- ACP bonded
- 3 different test suites x 2 plating types x 2 devices
  - 20x thermal-cycled
  - 4-wire measurements

- *Only 9 of 100 connections tested on each device*
  <u>–> 108 tested total</u> (out of 1200)
- 3 missing connections after bonding, 2 died in Cycle1 and 3 in Cycle2
- Resistance worsened by **0.2 Ω** and **0.7 Ω** after each set of cycles

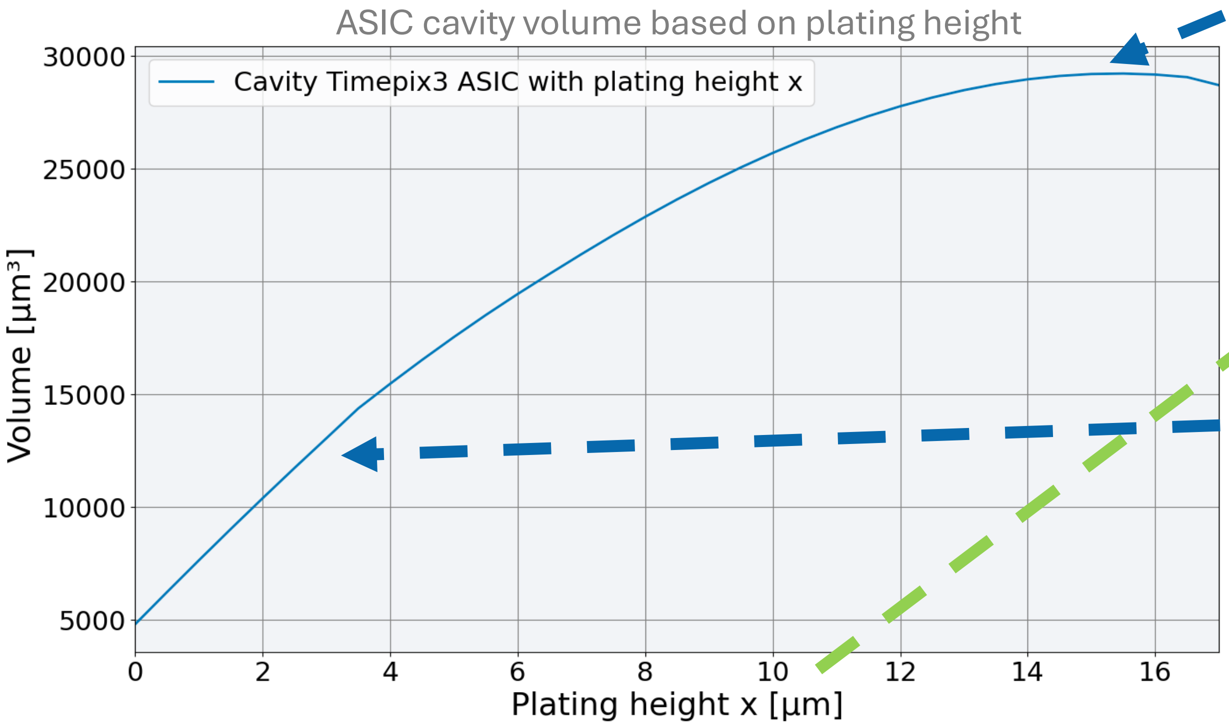


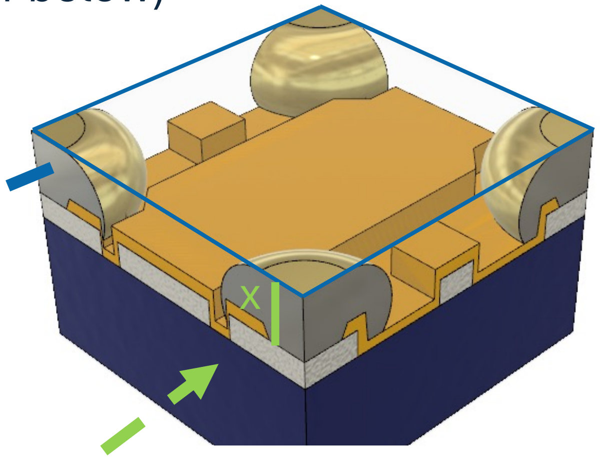

Cycle1 -40 °C to 80 °C
Cycle2 -60 °C to 120 °C

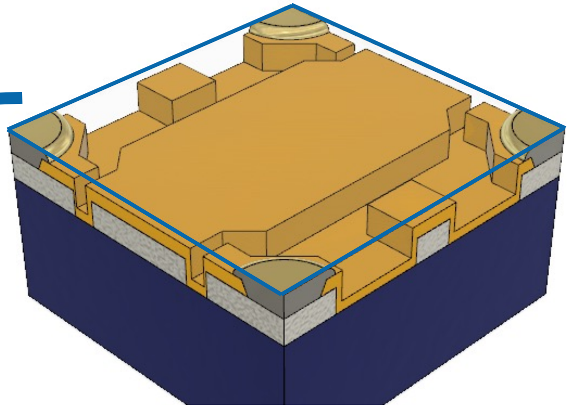
Evaluation with real chip: Timepix3

Need for sufficiently large cavity volume between sensor and ASIC after bonding to fit excess adhesive

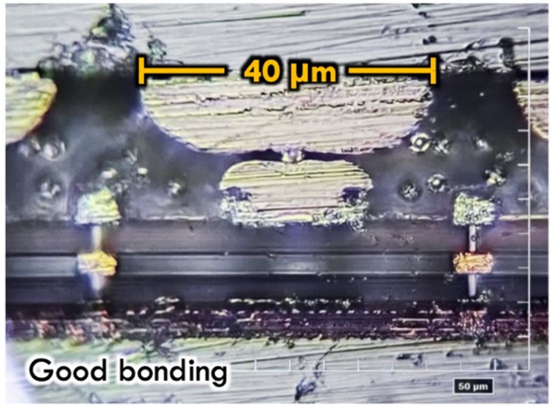
- Problem for small-pitch structures (such as 55 µm pitch or below)
- **Volume** directly related to plating height **x**
- Developed approximate model for calculation



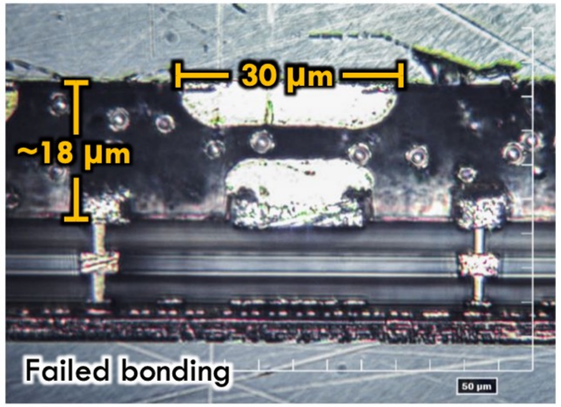




Timepix3 assembly w/ re-worked pad

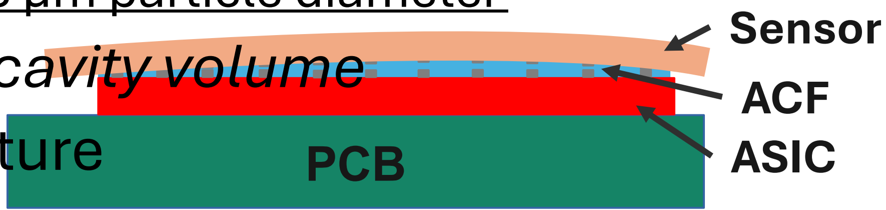


Timepix3 assembly w/ original ENEPIG

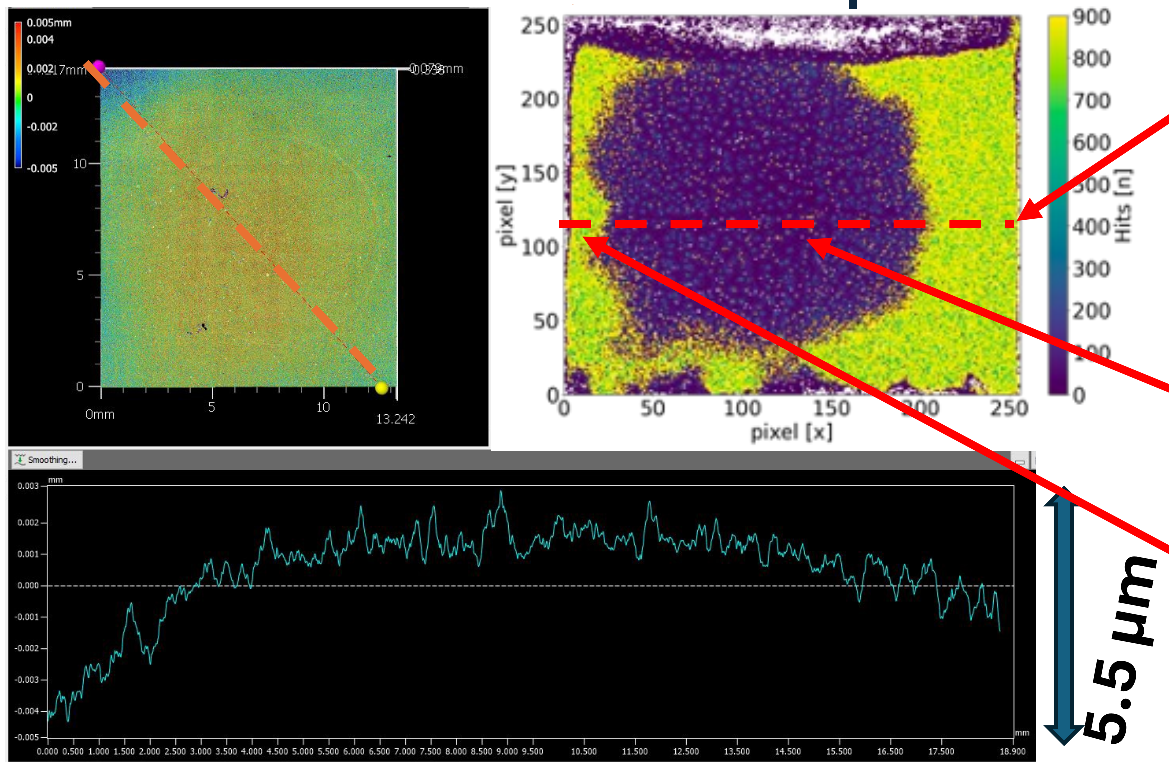


Evaluation with real chip: Timepix3

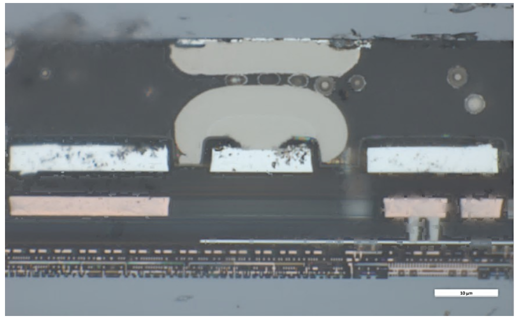
- Evaluation of different ACF thickness (18 µm vs 14 µm), both with 3 µm particle diameter
  - Bent due to *insufficient bonding pressure* or *plating cavity volume*
  - Plan to use higher force flip-chip machine in near future

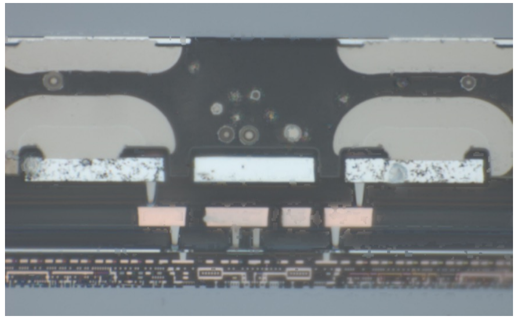


ACF 18 µm



Right	**(1.54 ± 0.20) µm**
Centre	**(3.67 ± 0.19) µm**
Left	**(3.63 ± 0.10) µm**

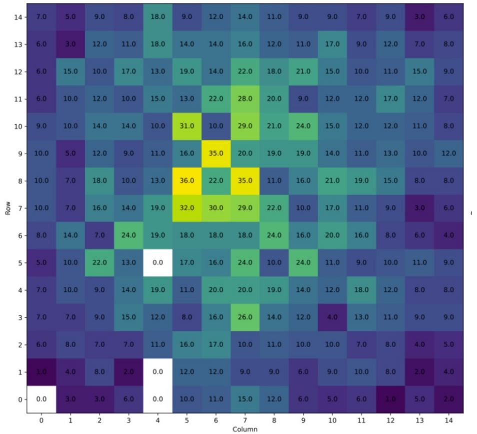




Other projects and applications

ALTIROC2/3

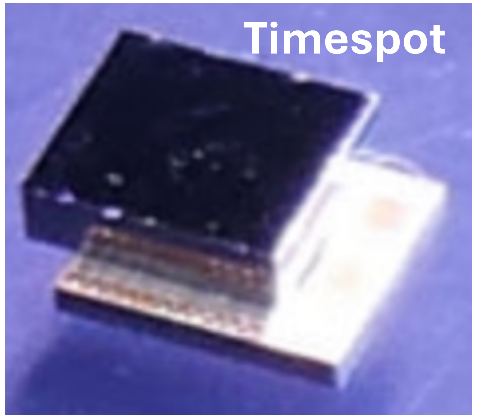
- 15x15 pixels, 1300 µm pitch
- LGAD sensor
    - ACP with 10 µm particles
    - **98.2% yield**
    - *Tested by A. Wang (USTC)*



ALTIROC2 response

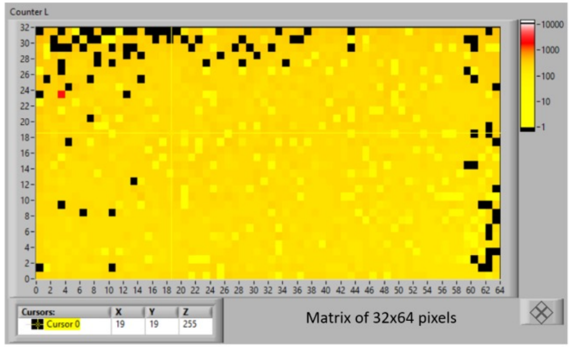
Timespot

- 32x32 pixels, 55 µm pitch
- Si 3D trench sensor
    - ACF 18 µm thick
    - **… to be tested …**
    - *Provided by A. Loi (INFN)*



SPHIRD

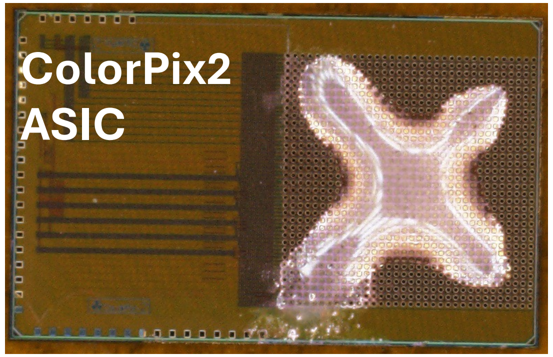
- 32x64 pixels, 50 µm pitch
- Si planar sensor
    - ACF 14 µm thick
    - **85% yield**
      (+7% weak response)
    - *Tested by M. Ruat (ESRF)*
- **CZT** sensor 2 mm thick
    - NCP
    - **… to be tested …**



SPHIRD Si response

ColorPix2

- 32x32 pixels, 70 µm pitch
- **CZT** sensor 1.8 mm thick
    - NCP
    - **around 70% first yield** *(el. tests then failed)*
    - *Tested by J. Jirsa (FNSPE CTU)*



Anisotropic conductive films (ACF/ACP): outlook and plans

- Optimisation of bonding parameters
  - Bonding pressure, time, temperature
  - Variation of adhesives (films/pastes; conductive/non-conductive; particle densities, …)
- More stability testing of daisy-chain structures
  - Radiation hardness, electrical properties, mechanical strength, …
- Already linked to multiple projects
  - Expanding with testing of functional assemblies by us and partners
- Need for an improved flip-chip machine
  - Brings potential to reflow (such as Timepix4 Cu pillars) as well as higher force

Advancement in flip-chip techniques

Different technological level

This needs today RTO or industry

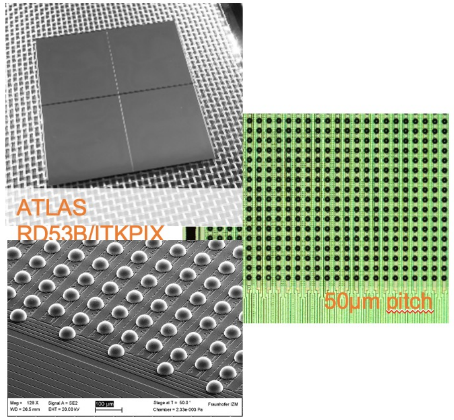
Vendors busy with upgrade productions

Move part of process to laboratories

Different features from different technologies can address specific complex issues

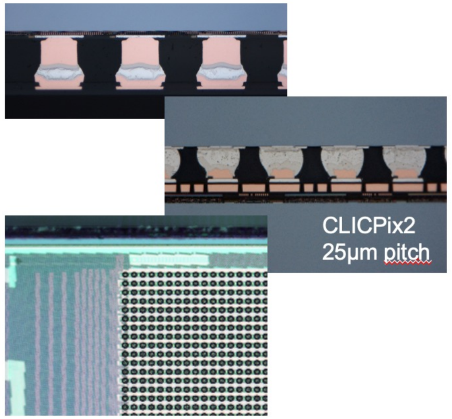
- small pitch
- process-temperature constraint
- electrical properties (current, C)
- connection flow (wafer-wafer, device-wafer)

Fine pitch bumping



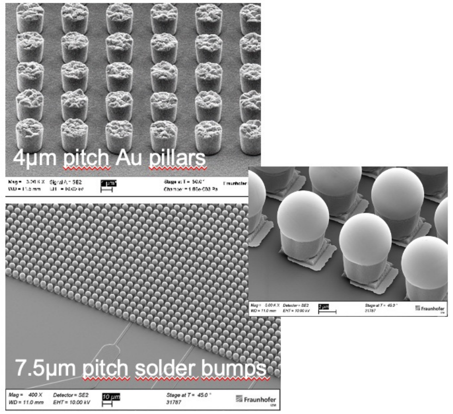
- Pitch 100…50µm
- Bump size: 50…25µm
- Material: Solder bumps, pillar bumps with solder cap

µ-bumping



- Pitch 50…20µm
- Bump size: 25…12µm
- Material: Solder bumps, pillar bumps

Sub-10µ-pitch



- Pitch 10…2 µm
- Bump size: 6…1µm
- Material: pillar bumps, metal pins

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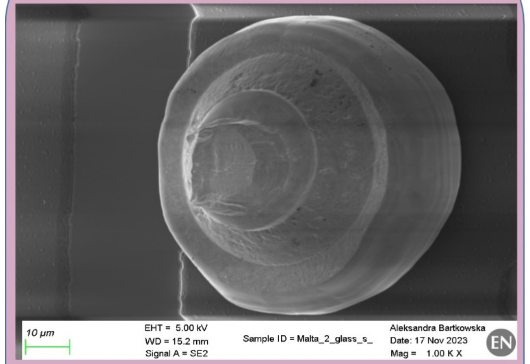
T. Fritzsch, Fraunhofer IZM

Gold stud and nanowires

Gold studs



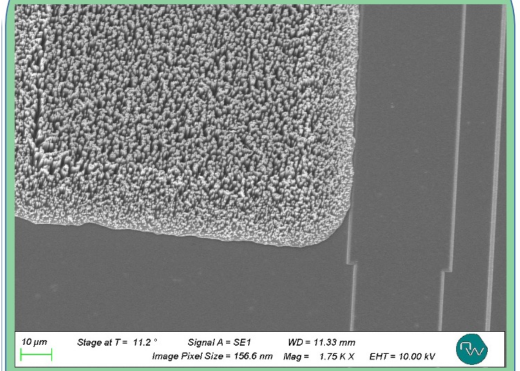
- **Individual** pad selectable
- **Touch before** bond possible
- **No mask** needed

Gold stud can be deposited with standard wire bonding machine with ball-bonding head

Does not require masks but deposition is done through the bonding program

Flip-chip is then achieved by compression, but assembly often achieved through glue

Nanowires (NW)



- **Low** resistance and parasitic
- **Glue-free** process available
- **Chip** and **wafer** level

Nanowires are grown on pads

Low-resistance

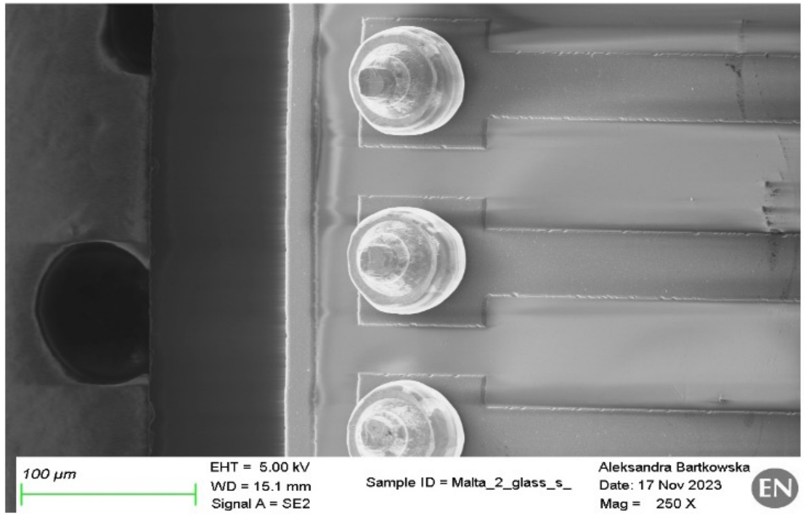
Flip-chip is then achieved by compression; no glue mandatory but can be used

Techniques adaptable to both sensor-to-chip and flex interconnection

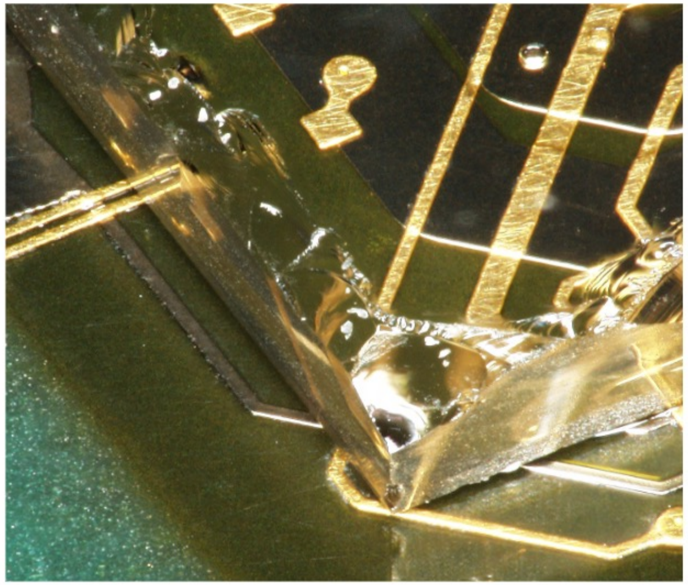
Abhi Sharma

Gold studs

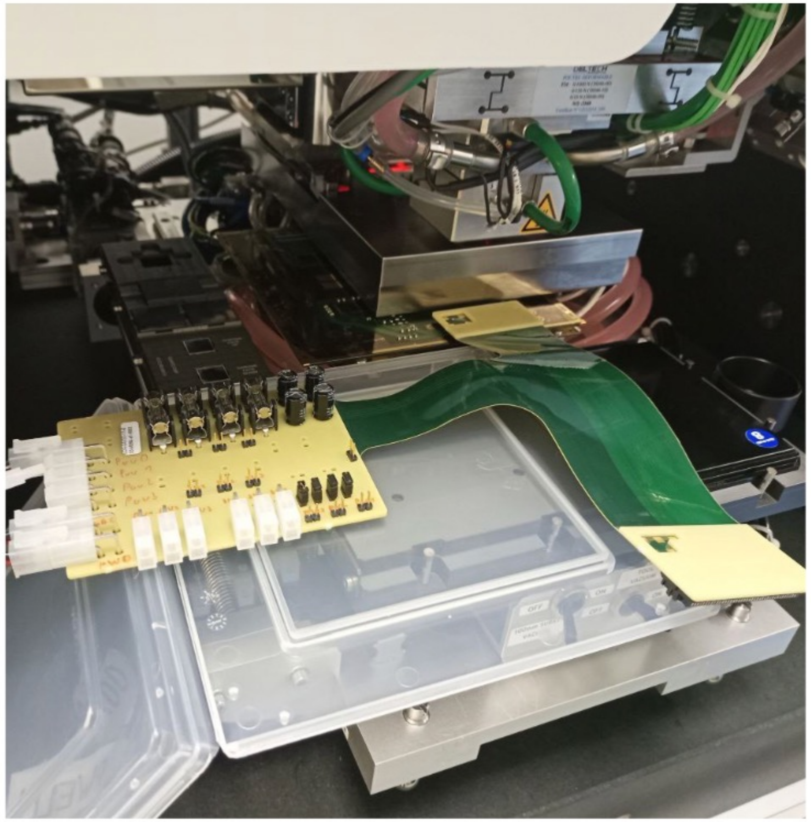
- **Individual pad** selection possible on application phase
- **Successful bonding** of test structures and MALTA2 sensors onto flex
- Verified **in situ pre-bonding verification**
- Bonded using **epoxy under-fill** Araldite 2011



Gold studs with flat head on test structure

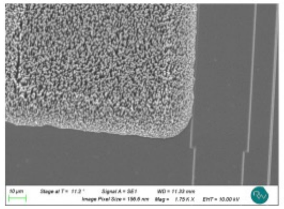


Test structure connected to flex using gold studs

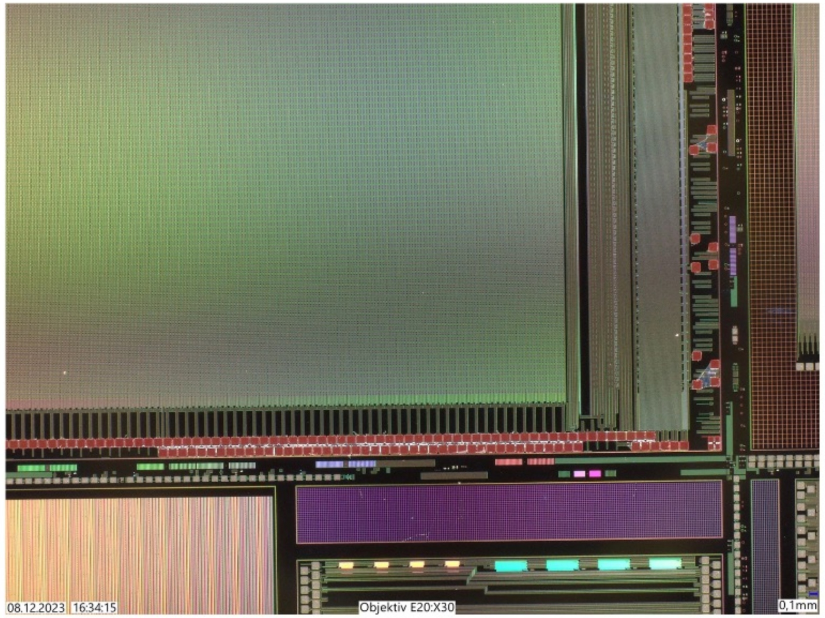


In situ pre-bond verification

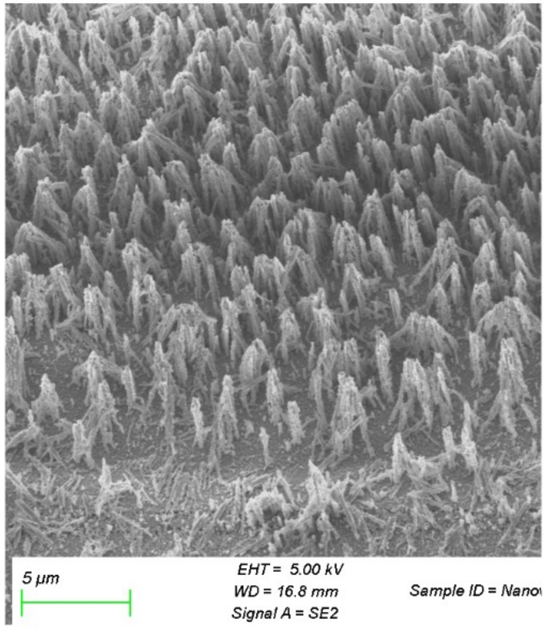
Nano-wires deposited on wafers



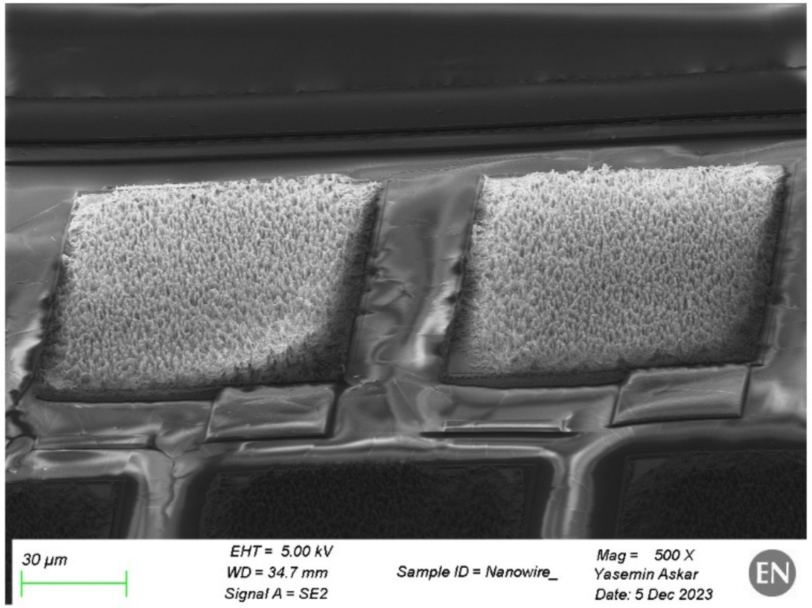
- MALTA2 **wafers** processed (88µm x 88µm aluminum pads with 32µm spacing)
- Currently **>90% pads** with perfect coverage, pads with **partial coverage that are still bond able** – no impact on MALTA2 performance
- Possible to **probe wired pads** with probe-card



Wafer scale wire deposition

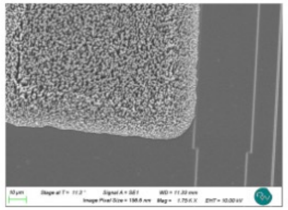


Close view

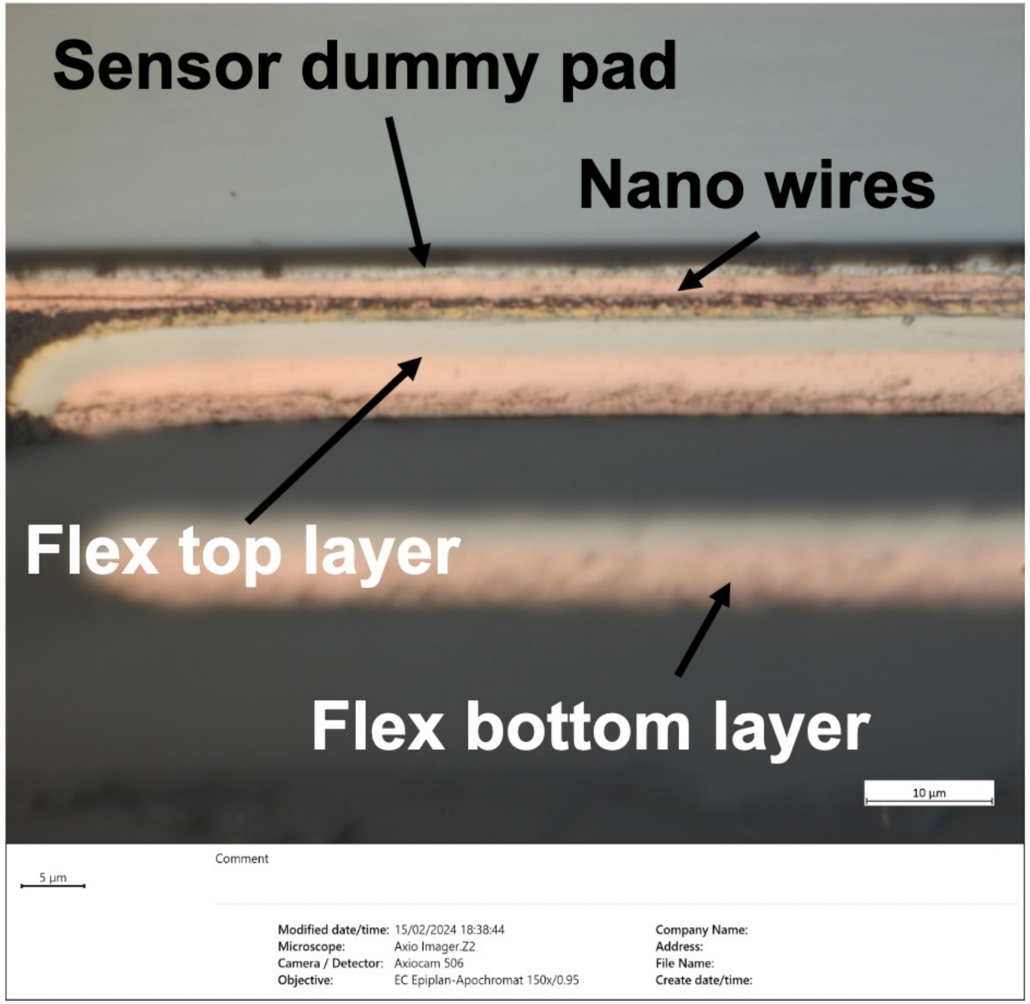


Nano-wires on chip pads

Nano-wire bonding of a chip on flex



- Successful **bonding** of nano-wired MALTA2 pads onto flex PCB pads using the **glue assisted process**
- Practically every **non-conductive glue** can be used for the bonding process



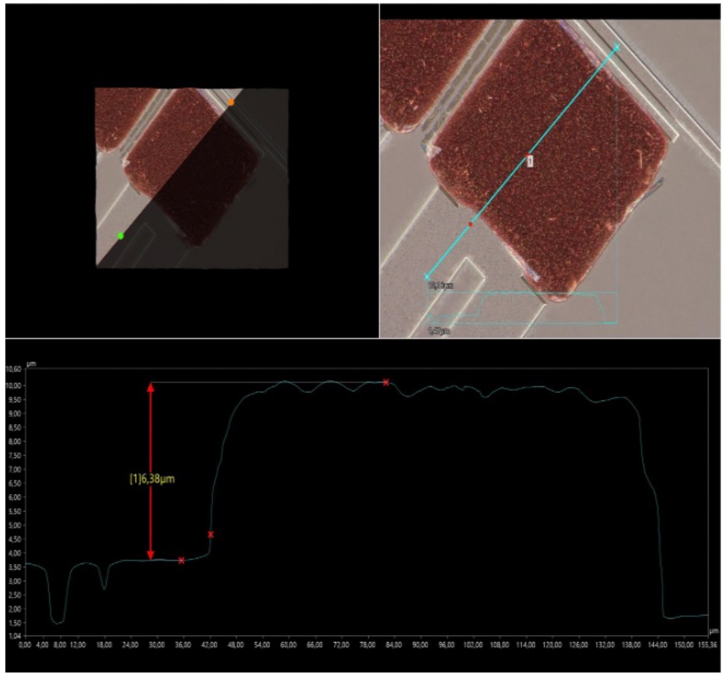
Comment

Modified date/time: 15/02/2024 18:38:44
Microscope: Axio Imager.Z2
Camera / Detector: Axiocam 506
Objective: EC Epiplan-Apochromat 150x/0.95

Company Name:
Address:
File Name:
Create date/time:

<u>Different bonding options:</u>

- **Sintering** (glue-free)
- **Cold welding** (glue-free)
- **Glue supported**



Wafer-to-wafer bonding and 3D interconnections

- Want to reduce mass, i.e. thickness of pixel detectors as much as possible while keeping the benefits of the hybrid approach:
  - Separate development and optimization of sensors and FE electronics allowing for best performance of FE electronic and sensor.
  - Fine pitch interconnection between FE and sensor pixel with a pitch down to ~20µm.
  - Thinning of FE and sensor parts to the minimum.
  - Can benefit from active CMOS sensor development by integrating some electronic already into the sensor

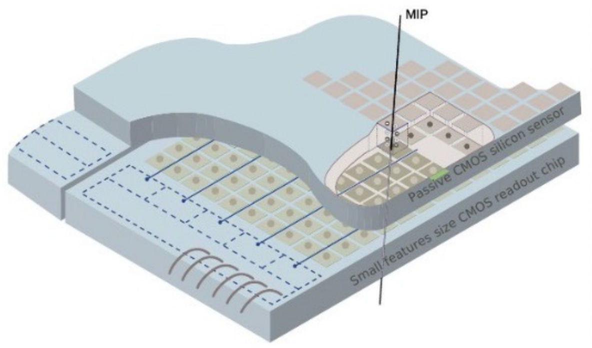
→ Target is the development of ultra-thin hybrid pixel detectors based on:

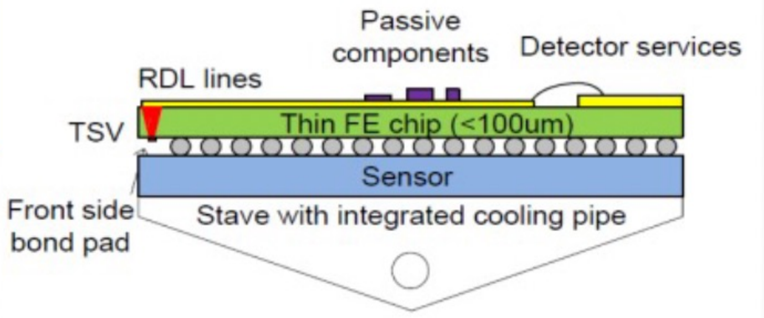
  - 50 – 100 µm thick pixel sensor on 200 (300) mm CMOS wafers
  - ~20 µm thick pixel FE chip thickness on 200 (300) mm CMOS

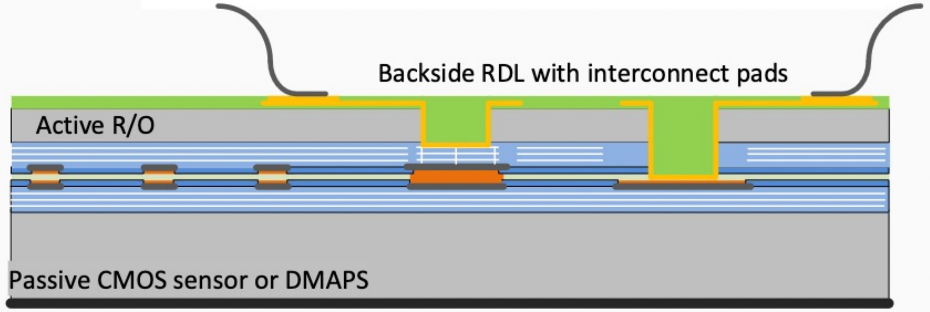
Standard hybrid pixel module:
150 µm FE & 150 µm sensor
2013 (ATLAS IBL & ITk)

TSV hybrid pixel module:
80 -100 µm FE & 150 µm sensor
2019 (AIDA 2020 proof of concept)

Ultra thin hybrid pixel module:
~20 µm FE &
50 -100 µm sensor
2025 (future tracking detector, esp. in innermost layers)



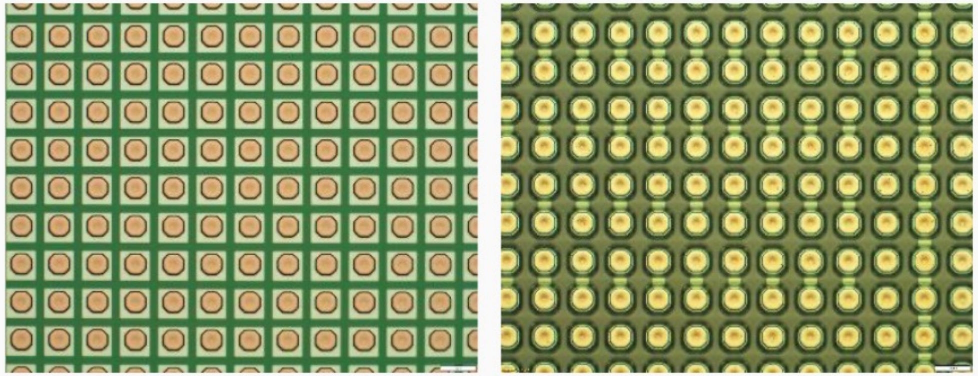




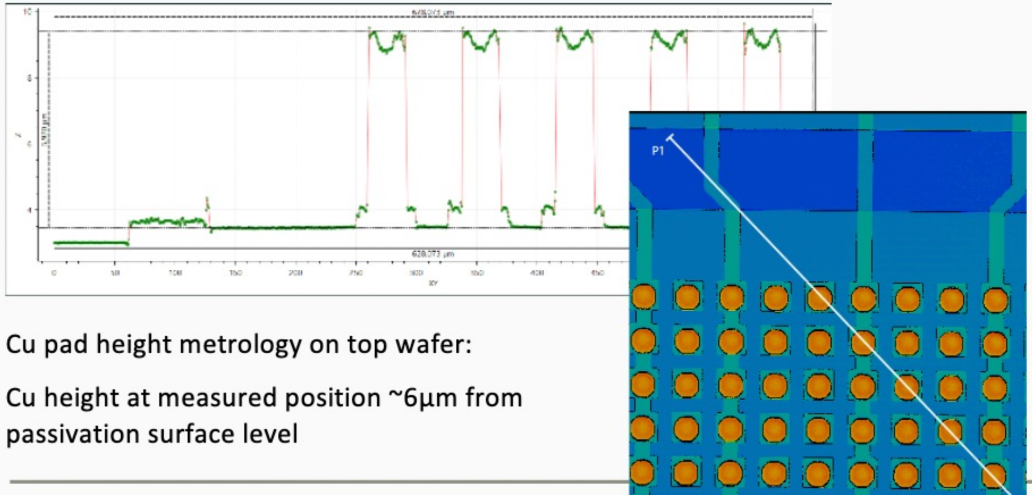
Fabian Huegging

Tests with dummy wafers

TOP wafer: Cu UBM pad and patterned polymer layer



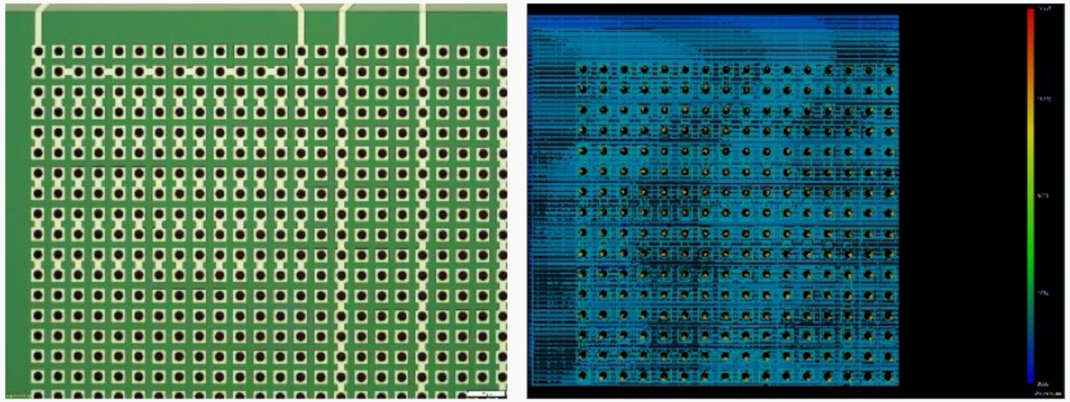
Cu-UBM pad wafer without (left) and with polymer bond layer (right)

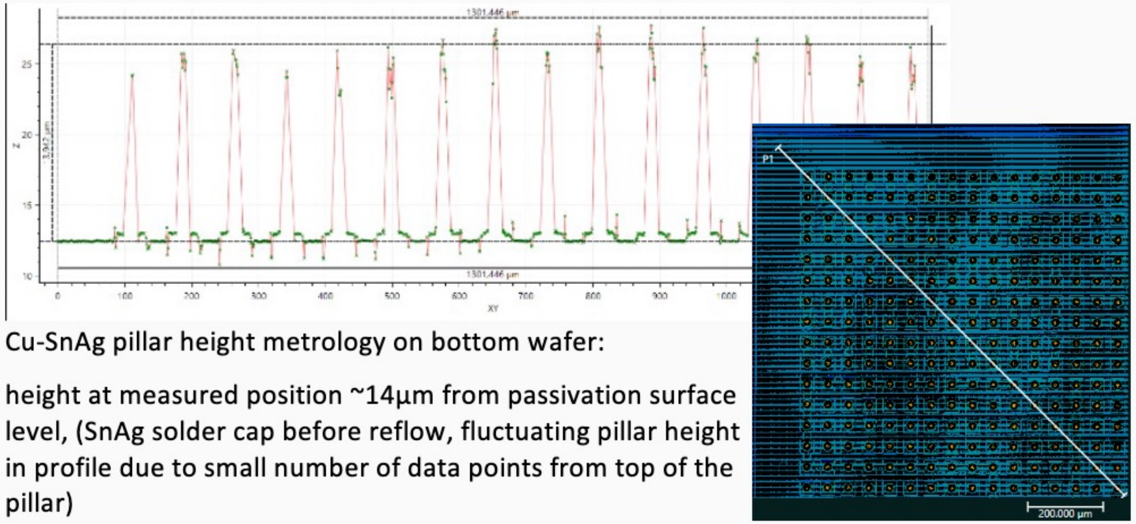


Cu pad height metrology on top wafer:

Cu height at measured position ~6µm from passivation surface level

BOTTOM wafer: Cu-SnAg pillar





Cu-SnAg pillar height metrology on bottom wafer:

height at measured position ~14µm from passivation surface level, (SnAg solder cap before reflow, fluctuating pillar height in profile due to small number of data points from top of the pillar)

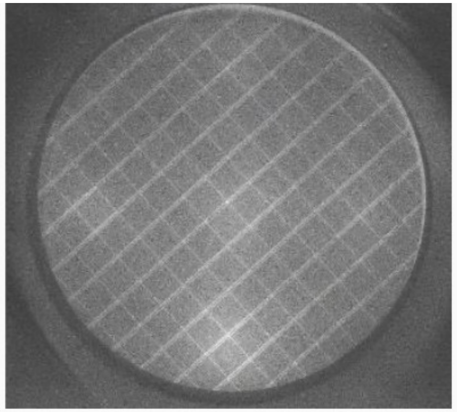
First attempts with real wafers

Bonding process evaluation using daisy-chain-test wafer:

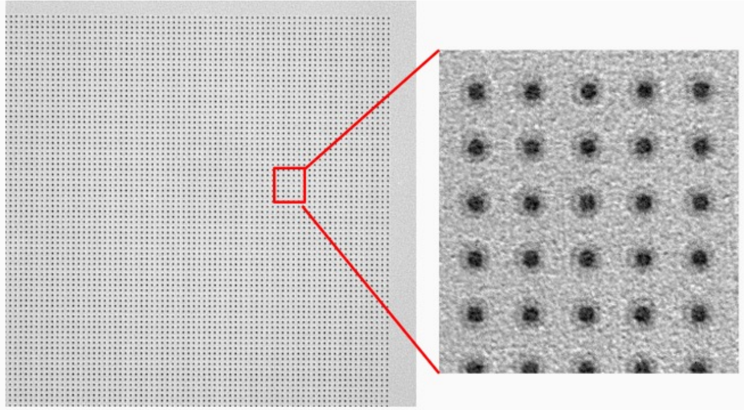
TOP wafer: UBM pad and patterned polymer layer
BOTTOM wafer: Cu-SnAg pillar

Preliminary Process Results:

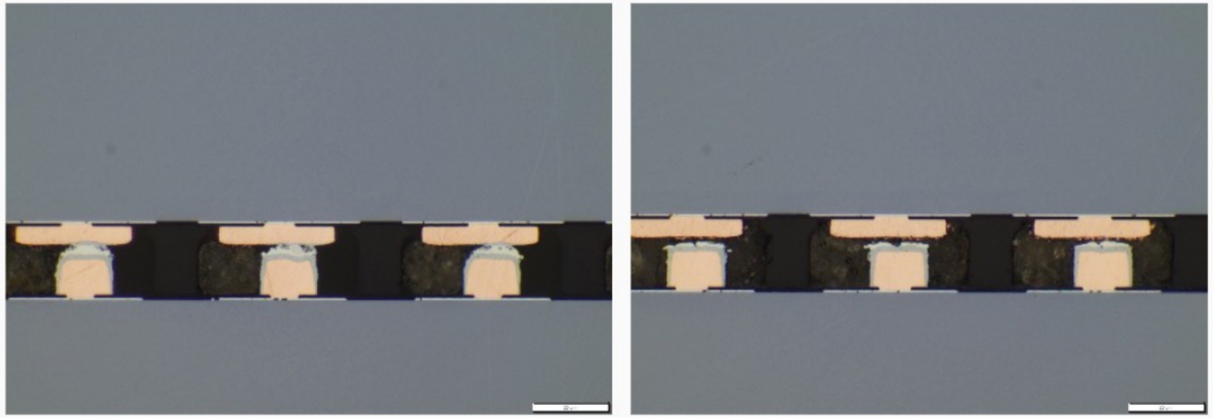
- Process evaluated for 20µm polymer layer thickness, measured bond layer thickness: 21µm (+/- 0.5µm across the wafer)
- Pillar height: 13…15µm (as plated) (tolerances across the wafer)
  Cu pad height: 5.5µm (+/- 0.5µm across the wafer)
- Thinning of top wafer to 80µm thickness possible
- Dicing of wafer stack possible
- Low adhesion between top and bottom chip after dicing (chips can be easily de-bonded)
- Large area solder transfer from CuSnAg-pillar (bottom chip) to Cu pad (top chip) visible after top chip debonding but some pillars are not connected to Cu pads (see cross section)



Full wafer IR image, details are to small for bond layer characterization



X-ray inspection of bonded chips: UBM pads - medium gray, pillar - dark gray; UBM and pillar are different in size



cross section after wafer to wafer bonding:
Left: slightly connected pillars, solder transfer to Cu pad (top) visible
Right: gap between pillar and pad, no solder transfer to Cu pad (top) visible

Interplay with DRD7 in 3D integration

Via industry/RTOs
it will profit of commercial drive

Stack to match digital/analog
many reasons to do so

Could allow complex communication between different connected devices

Allow to contact/power/read a lower layer through an upper one

Multi-tier, mixed-technology

Interface with DRD7

- Multi-tier electronics-oriented (example: optical connections) will go more in DRD7
- Vertical integration sensor-oriented (example: vias to reach FE chips) will go in DRD3

Participate to DRD3 !

If you have interest for any of the activities covered by DRD3 (see also Jerome's review) don't hesitate to contact the conveners of the corresponding WG!

(or me / Jerome / Auguste / Marlon, and we will point you to the relevant persons)

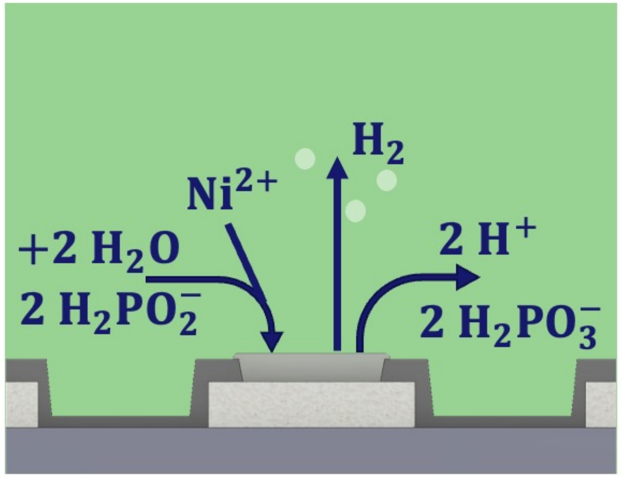
Backup

Electroless Nickel Immersion Gold (ENIG)

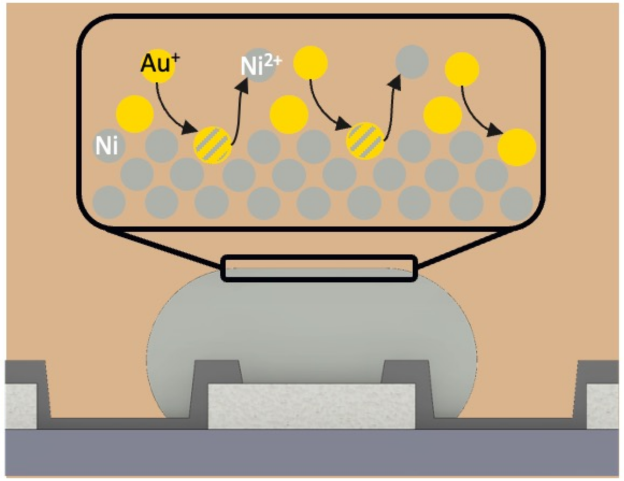
- Electroless Nickel
  - Self-catalytic reaction on pad surface
  - Performed on aluminium (activated surface) or on previous nickel deposits in a nickel bath
- Immersion Gold
  - Corrosion protection, very thin layer (< 1 µm)

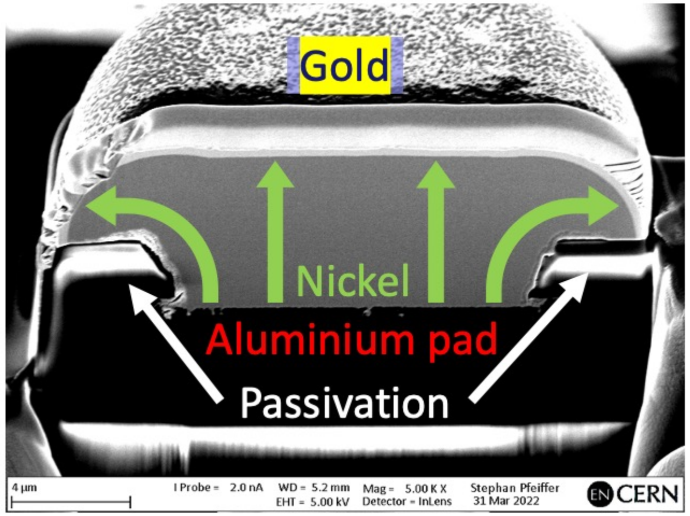
- Ongoing optimisation of the process in EP-DT Micro-Pattern Technologies lab
  - Cleaning, oxide removal, nickel bath stability,…
  - Optimisation performed for different pad topologies

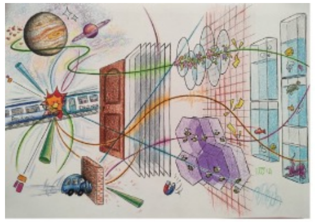
Electroless Nickel



Immersion Gold







Expressions of Interest

DRD3

Group	Contact	Ongoing work / topics of interest	Maskless	classical processes	2.5D integr. / modules	3D integration	FTE
ANL	Jessica Metcalfe	technologies for large-scale tracking devices	☐	☐	☐	☐	
Bonn University*	Fabian Hügging, Jochen Dingfelder	fine-pitch (<50 um) bonding; W2W bonding; in-house hybridisation	☑	☑	☐	☑	1 Staff + 1 Stud./Postdoc/Techn.
CERN*	Dominik Dannheim	In-house plating and hybridisation; compact module studies (including silicon photonics integration)	☑	☐	☑	☐	2.5 Res. + 2 Stud.
FBK	Giovanni Paternoster	3d-integration and interconnection of BSI-SiPMs for NUV/VUV; mask and mask-less UBM; W2W temporary bonding; chip-level solder-ball bonding >50 um; wafer-level micro bumps/pillars <50 um; in-house maskless interconnects	☑	☑	☑	☑	1 Staff
Fraunhofer IZM*	Thomas Fritzsch	hybridisation with <=25 um pitch; W2W bonding; wafer-level packaging; single-chip bump bonding for R&D	☐	☑	☐	☑	1 Staff
Geneva University*	Mateus Vicente	In-house flip-chip bonding: gold studs, ACP/ACF, Cu pillars; chip-to-flex	☑	☐	☑	☐	
IMB-CNM-CSIC	Miguel Ullán	RDL, TSV, interposers	☐	☑	☑	☐	0.5 Res.
INFN Bari	Giovanni Francesco Ciani	interconnection between bent sensors; stacking of several CMOS sensors for full 3d tracking	☐	☐	☑	☐	0.5 Res. + 0.5 Stud.
INFN Cagliari	Adriano Lai	in-house single-die hybridisation with innovative bonding techniques such as ACF/ACP	☑	☐	☐	☐	
INFN Firenze	Giacomo Sguazzoni, Giovanni Passaleva	Novel interconnection techniques for future applications	☑	☐	☑	☐	0.5 Res. + 0.5 Stud.
INFN Milano	Gianluca Alimonti	Indium bump bonding; in-house die-to-die and die-to-PCB bonding; hybridisation of RSD; multi-chip systems on PCB/bus tape	☑	☑	☑	☐	
INFN Trieste	Giacomo Contin	interconnects for bent and ultrathin chips (ALICE ITS3); aerosol jet printing for RDL and contactless interconnects; TSV and wafer-to-wafer for 3D stacking	☐	☐	☐	☑	3 Res. + 1 Stud.
IPHC Strasbourg	Maciej Kachel	3D integration; small pitch (<10 um) interconnection	☐	☑	☐	☑	0.1 Staff
IP2I Lyon	Didier Contardo	wafer-to-wafer interconnect demonstrator	☐	☐	☐	☑	0.6 Physicist + 2.8 Tec
KIT Karlsruhe	Michele Caselle	in-house flip chip, gold studs, TSV processing, RDL	☑	☐	☑	☐	0.5 Staff + 1 Stud.
LPNHE Paris	Giovanni Calderini	interconnects: ACF, ACP, gold studs; characterisation techniques and devices; reliability testing; new interconnection techniques / scalability	☑	☐	☐	☐	1.5 Res. + 1 Stud. + 1 Techn.
MPG Halbleiterlabor*	Ladislav Andricek, Jelena Ninkovic	direct wafer bonding; 3D/2.5D systems with micro-channel cooling; W2W/C2W bonding	☐	☑	☑	☑	1 Staff + 2 Stud./Postdoc/Techn.
NIKHEF	Martin Fransen	high-frequency ASIC to module integration (RDL, TSV), wire bonding	☐	☐	☑	☐	0.2 Staff
ORNL	Mathieu Benoit	in-house interconnect for hybridisation and module building: single-chip bumping, UBM, bonding; gold studs, ACP/ACF, Cu pillars; chip-to-flex, chip-to-interposer; interposer fabrication	☑	☐	☑	☐	1 Staff + 1 Stud./Postdoc/Techn.
*groups presenting at DRD3 workshop June 2024							**~30 FTE in total**