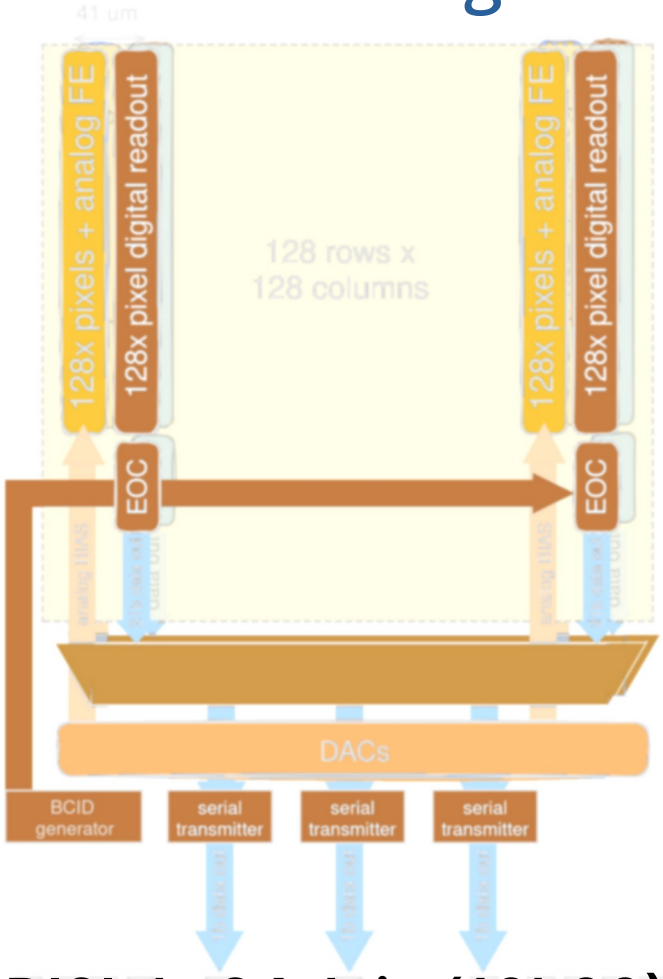
Development of a Monolithic CMOS sensor readout architecture for Ion tracking and identification



Réunion du GDR DI2I du 24 Juin (10h00) au 26 Juin
IJCLab - Orsay

Low energy range ion tracking and identification

Context:
development of a MAPS for particle identification as well as precision tracking

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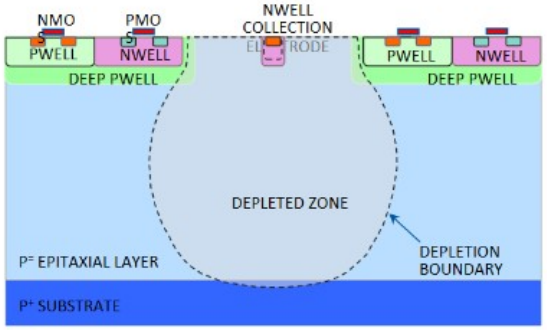
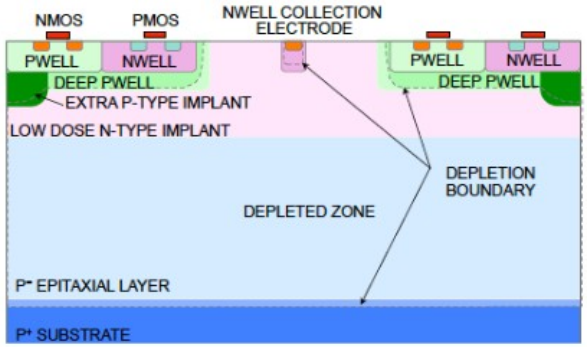
Charge collection: basic facts

Here on small collection node





- Fixed amount of charge generated by ionization in sensitive layer limited by substrate
  => all of it is collected over a cluster of pixels
- In **standard** process, **partial depletion**
  => charges move by diffusion and drift
  => sizeable charge sharing
- In **modified** process, close to or **complete depletion** (sometimes called DepletedMAPS)
  => drift strongly dominates
  => low charge sharing

Jérôme Baudot - Review on MAPS R&D - FTCF workshop 2024/01/15 8

Monolithic Active Pixel Sensor:
silicon detector where electronics and sensor share the same technological process

Low energy range ion tracking and identification

Context:
development of a MAPS for particle identification as well as precision tracking

Measurement of momentum (deflection in magnetic field) and energy loss (ionization, excitation) can be used for Particle Identification

- minimization of multiple scattering:
  low material budget
- particle identification:
  precision tracking system + energy loss measurement

Possible applications: ion fragmentation cross section measurements for hadrontherapy treatments improvement

Sensors providing as output the signal amplitude of fired pixels, would allow measurement per particle and greatly increase identification capabilities

MAPS with E measurement would simplify the system (no need of additional detectors)
MAPS advantages:

- low material budget
- small pixel pitch
- standard CMOS technology

The origin: the TIIMM project

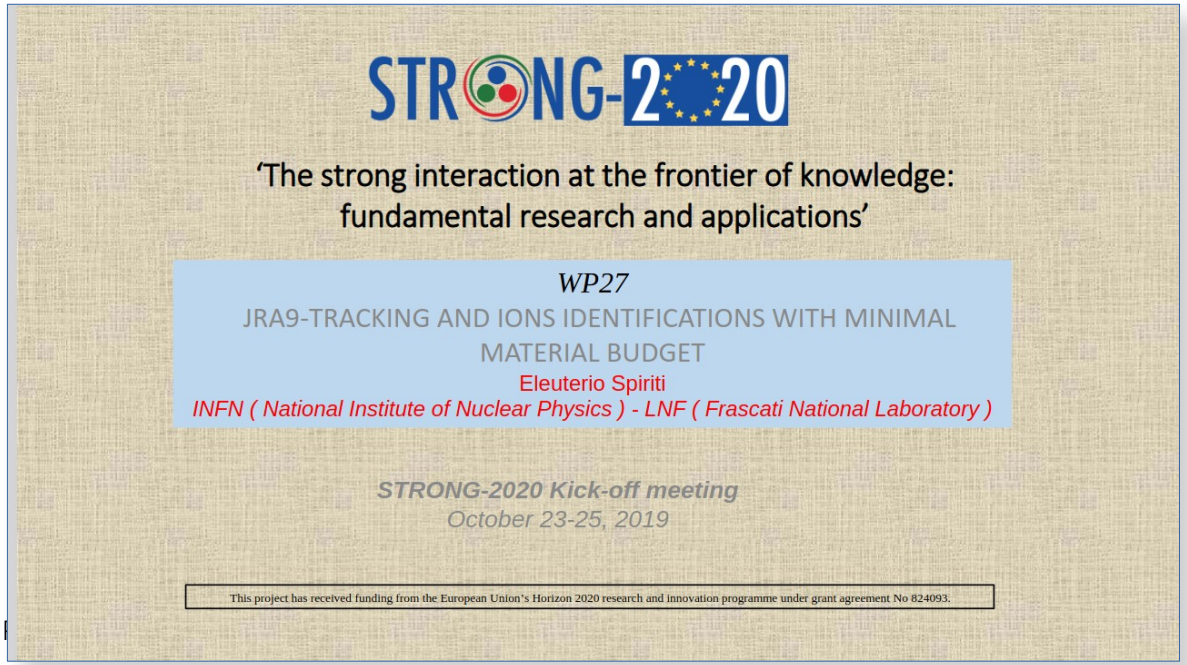
In the framework of the STRONG 2020 EU project the Joint Research Activity group Tracking and Ions Identification with Minimal Material budget (JRA9 TIIMM) develops a depleted MAPS detector using a modified TowerJazz 180nm process.

The target is a depleted MAPS for position and energy meaurements aiming at :

- position resolution better than 10um
- output signal amplitude of the fired pixels (energy loss measurements for particle identification)
- large input dynamics
- low material budget

5 prototypes realised and tested

- different sensing layer variants



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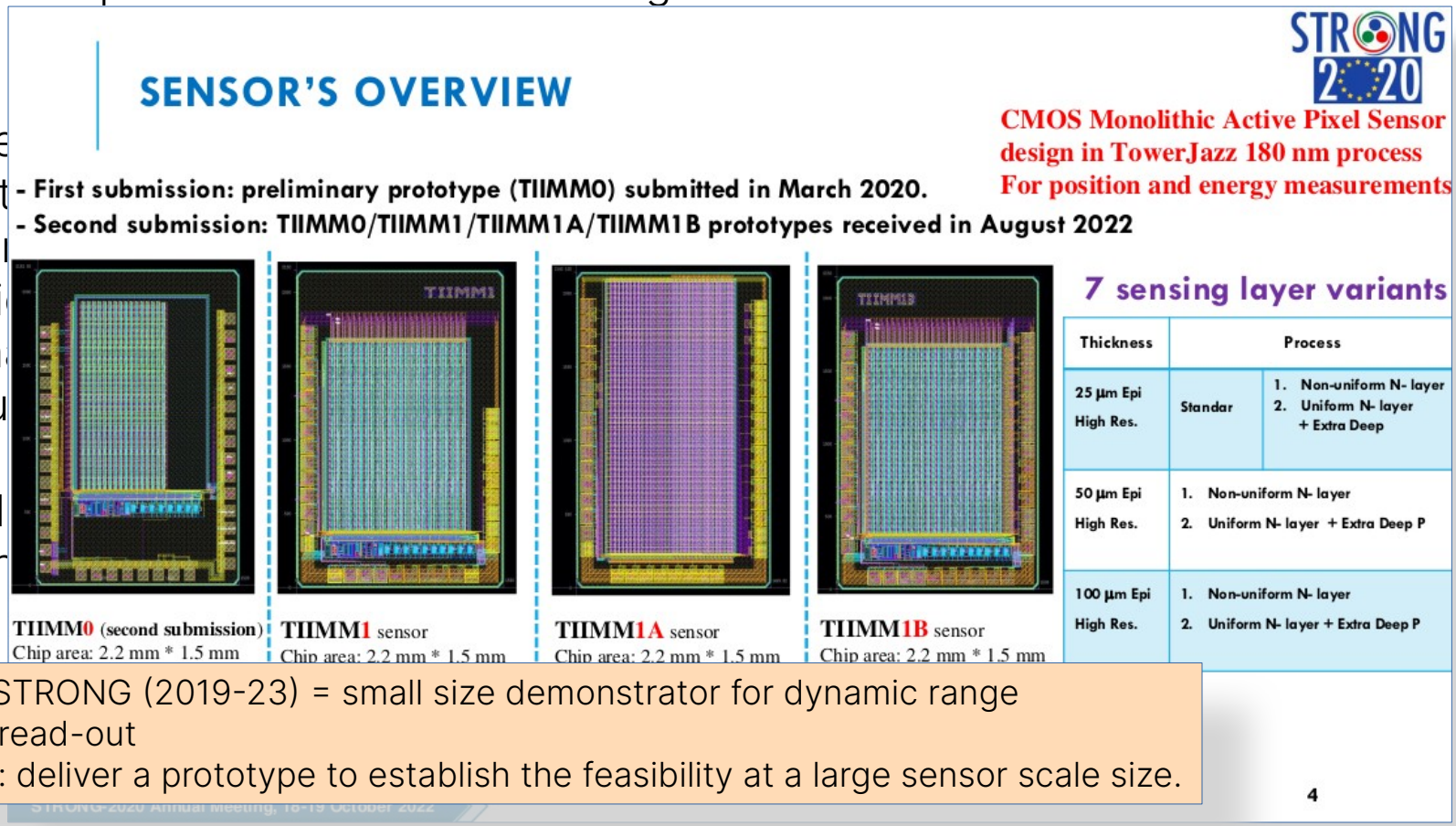

Goal within EU-STRONG (2019-23) = small size demonstrator for dynamic range
- no large scale read-out
TIIMM goal zero: deliver a prototype to establish the feasibility at a large sensor scale size.

The origin: the TIIMM project

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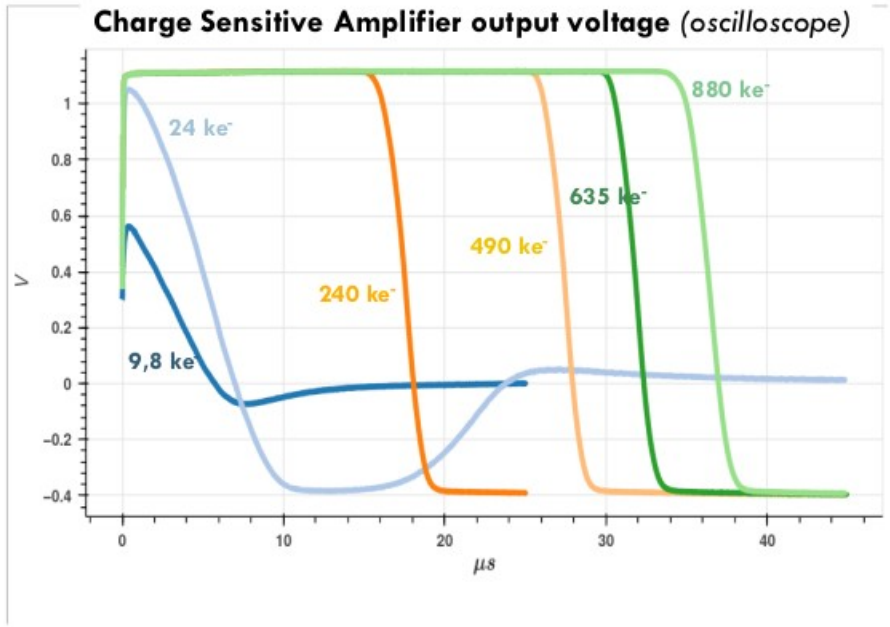
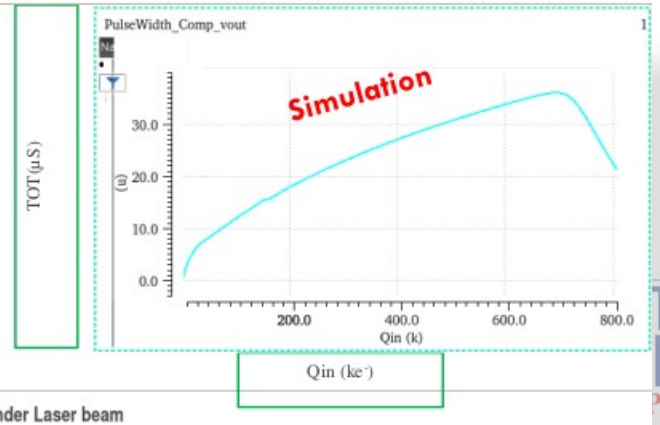
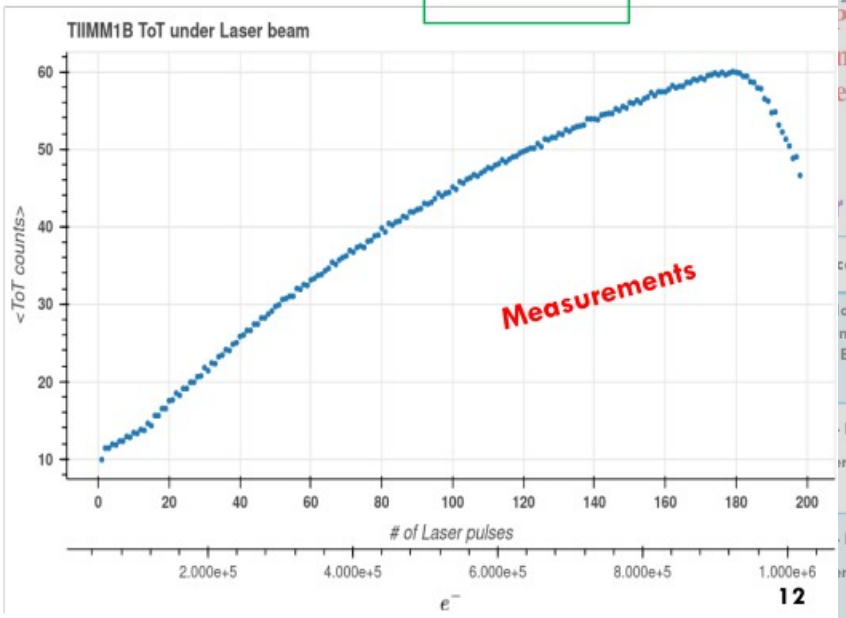
TIIMM1B – FIRST LASER TESTS ENERGY LOSS MEASUREMENT (SINGLE PIXEL TOT)







Range of measured charges on single pixel: ~ [500e⁻ , 900Ke⁻]

STRONG-2020 Annual Meeting, 18-19 October 2022

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- large input dynamics (1:10^5)
- low material budget

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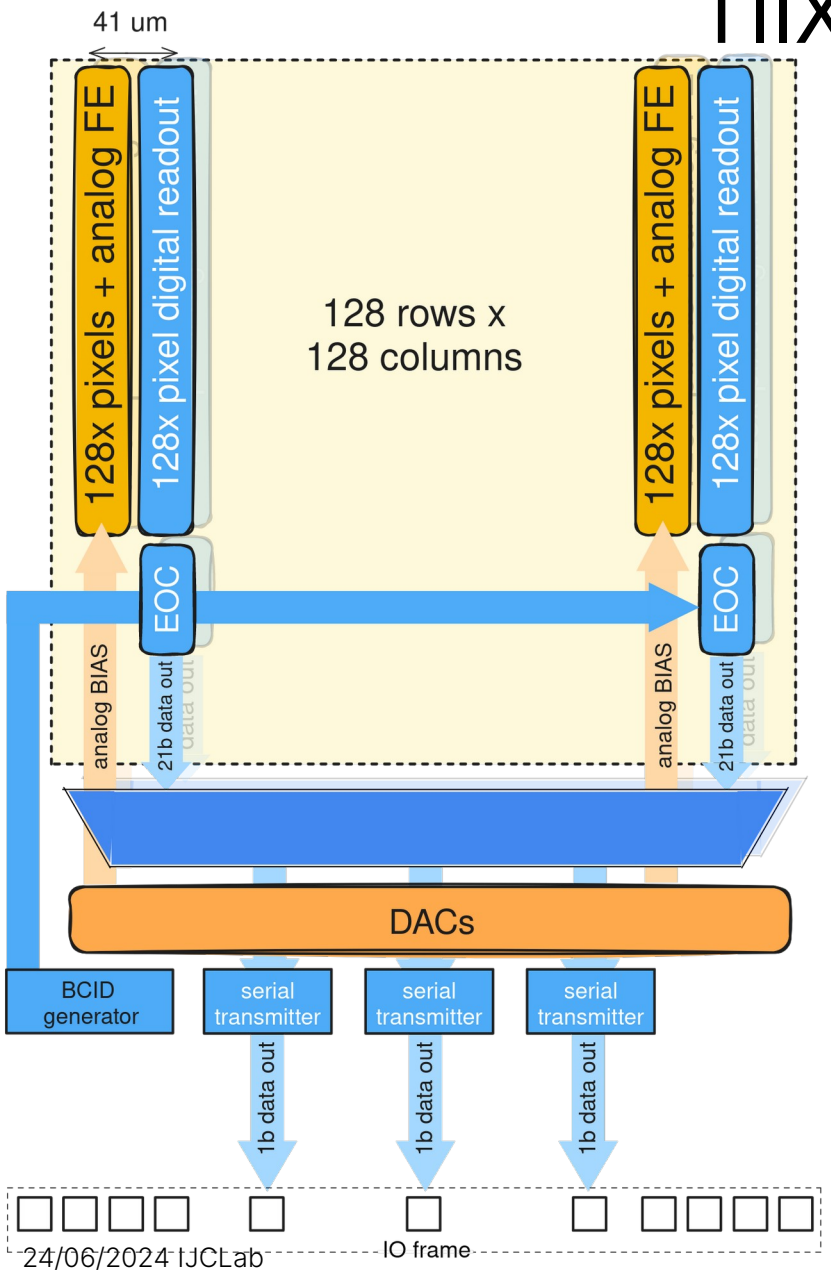
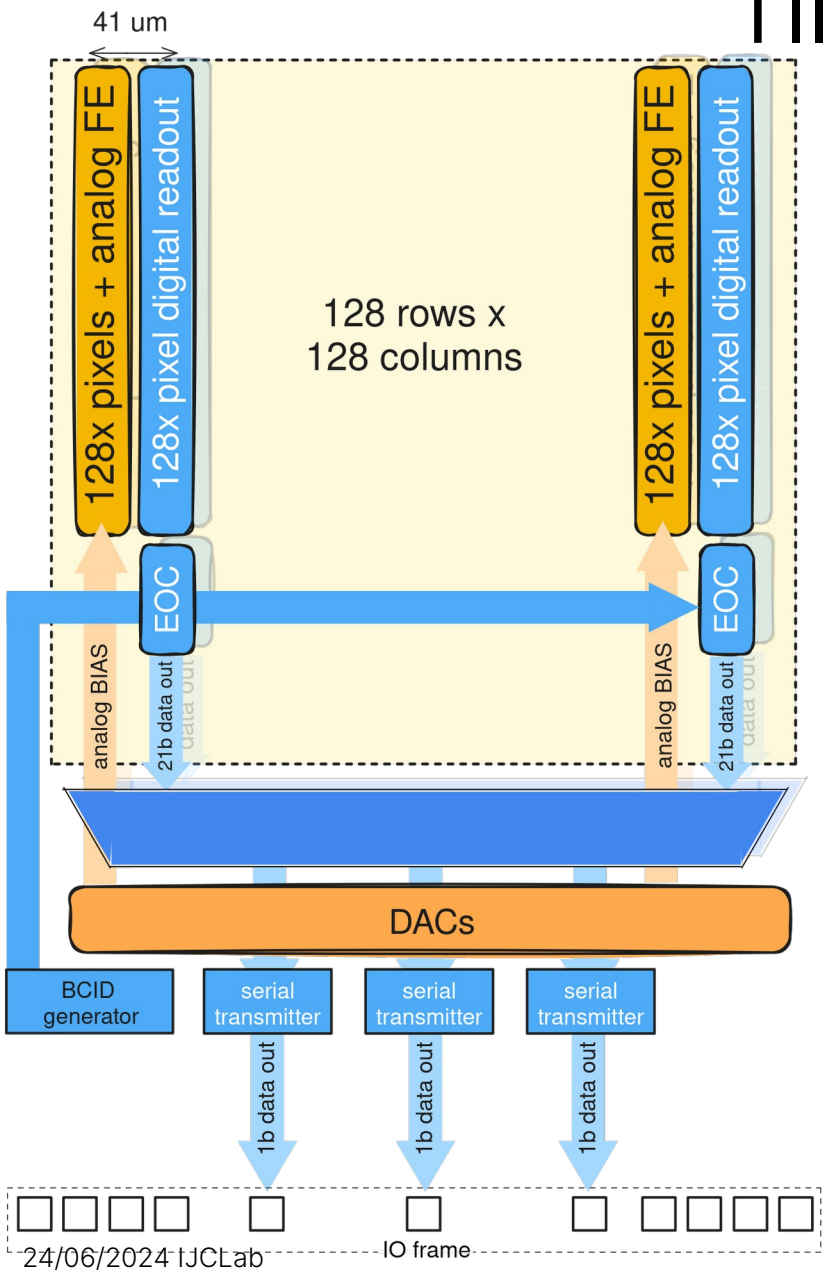
Possibility to extend the development :
combine the pixel front-end developed within TIIMM with a faster scalable matrix digital read-out

TIIX specifications



- Max surface = 6,3 × 5,4 mm2
- Max pitch 45 × 45 um
- 128 rows (scalable to 512) – 96 columns
- CMOS Technology: TJ 180 nm with 25um epilayer and modified process.
- Standard cell-based digital design
- Qin between 1k e- and ~ 800 ke- (FE dynamic range)
- Digital on Top conception flow
- Max Hit rate = 1 kHz/cm2
- Max Frame rate = 5kHz
- Output (serial data) frequency = 160 MHz

TIIX architecture



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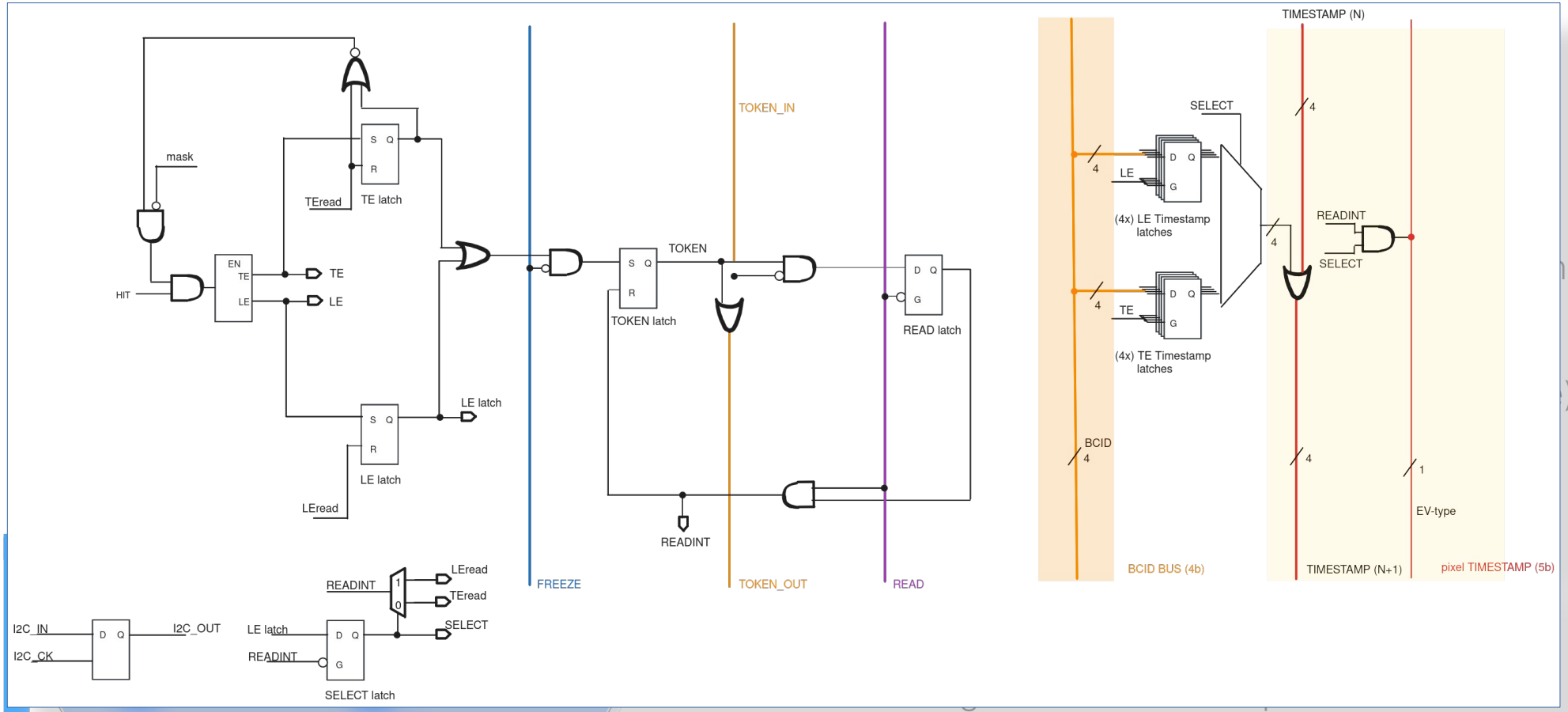
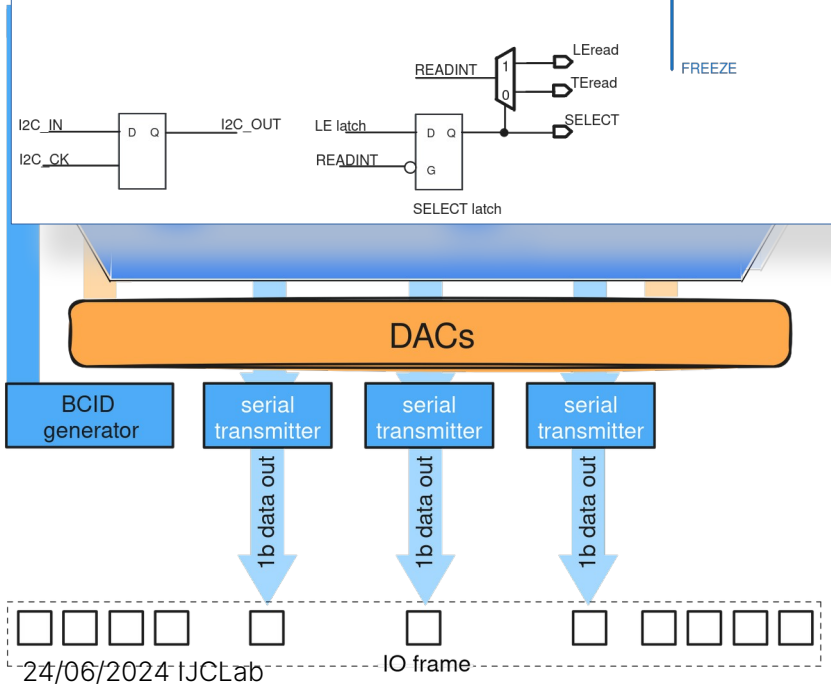
Goal: (faster) scalable matrix digital read-out

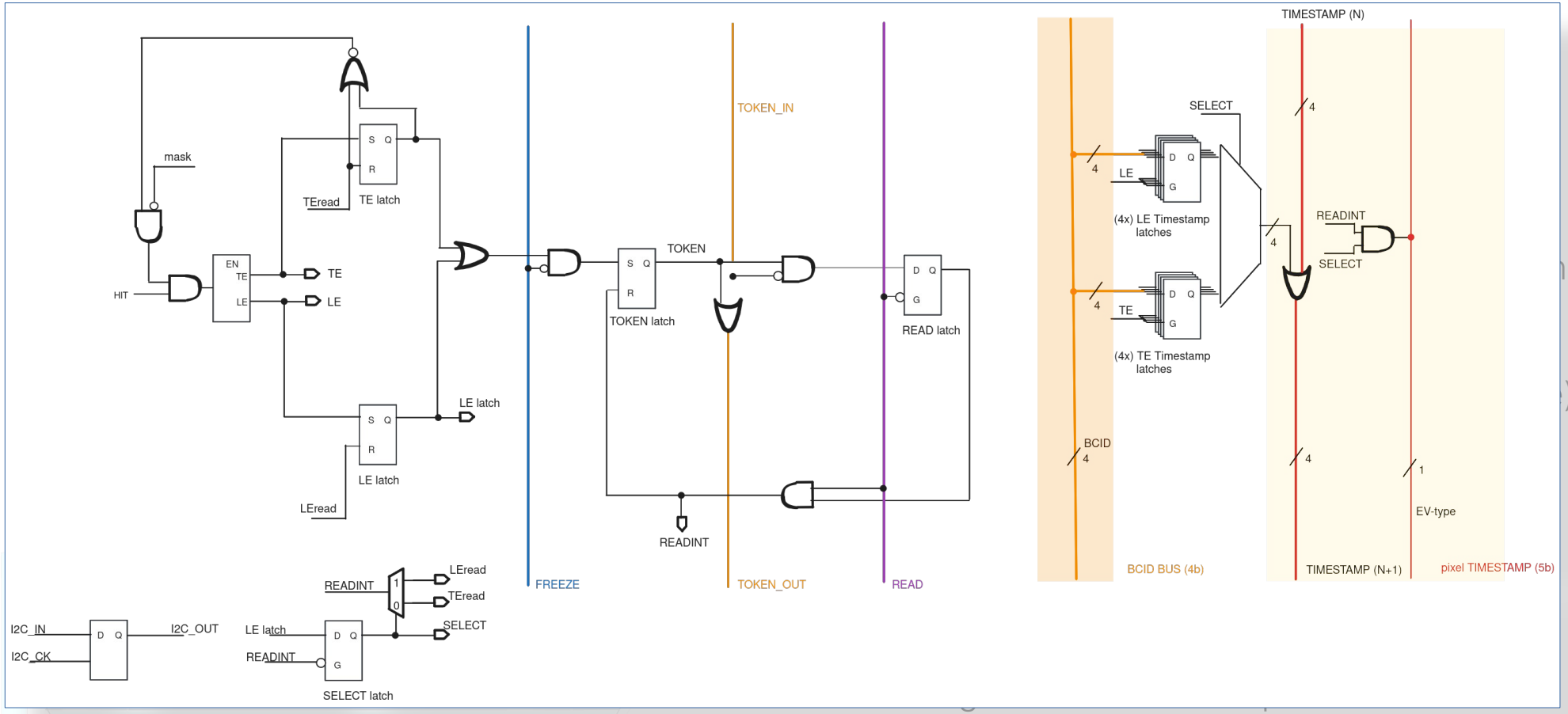
- Pixel matrix organised in 128 independent columns (128 pixels each)
- Digital read-out unit at each pixel





(128 pixels each)

- Digital read-out unit at each pixel



(128 pixels each)

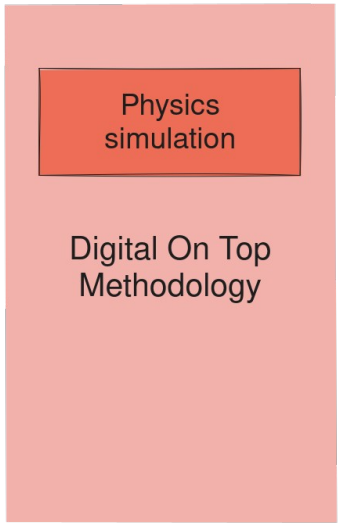
- Digital read-out unit at each pixel

- ToT: a 4b timestamp in pixel memory at each leading or trailing front generated by the pixel front-end comparator
  - 10b extension at the EOC level: the 10b timestamp is provided wrt a selectable clock frequency (40/20 MHz)
  - the full ToT is calculated off-chip: only the TE and LE timestamps are serialized by the three 160Mbps output links
- Pixel data are asynchronously read at the bottom of each column when they are present (data-driven readout)
  - fixed top-to-bottom priority (column drain architecture *a la* MONOPIX)

Design methodology

Design methodology

- SW simulation framework based on python scripts
- Parametric physics efficiency simulator with event generation



Design methodology

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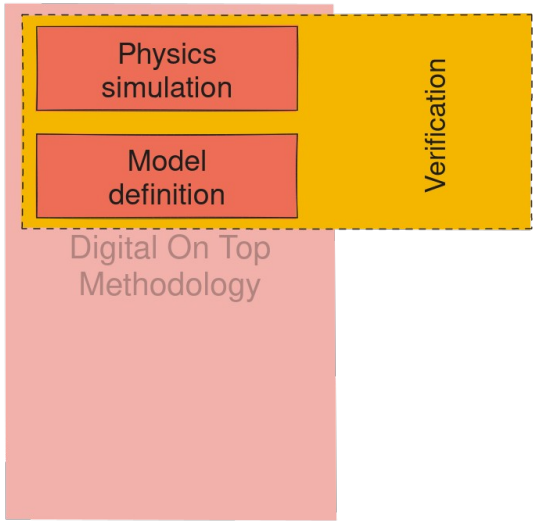
- Pixels hits ToT generation and functional architecture simulation testbench

flexible generation of input stimulus data, from sensor simulations (with given constrained random distributions enabling designers to test alternative and extreme cases)



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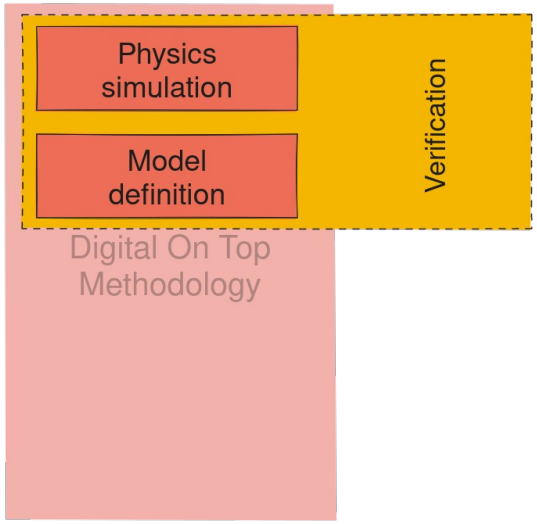

System Verilog model description

- SV is an extensions to Verilog
- system-level design and verification

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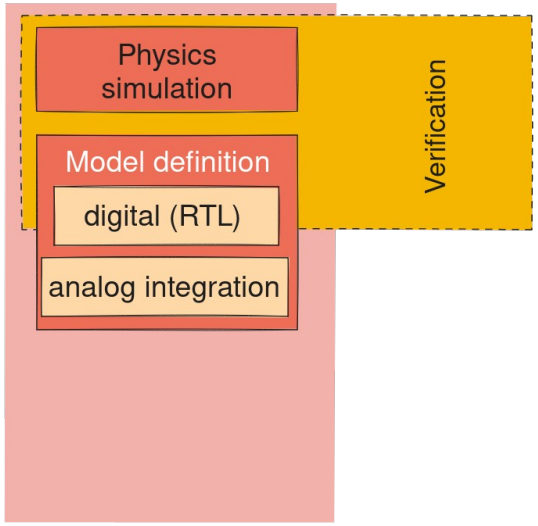

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Analog parts integrated ad SV level

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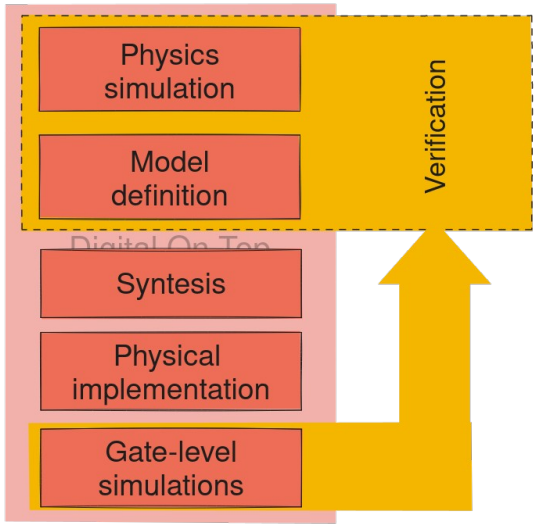

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Automated verification: capability of predicting expected chip outputs

Two strategies:
- verification methodology (UVM)
- System Verilog Assertions

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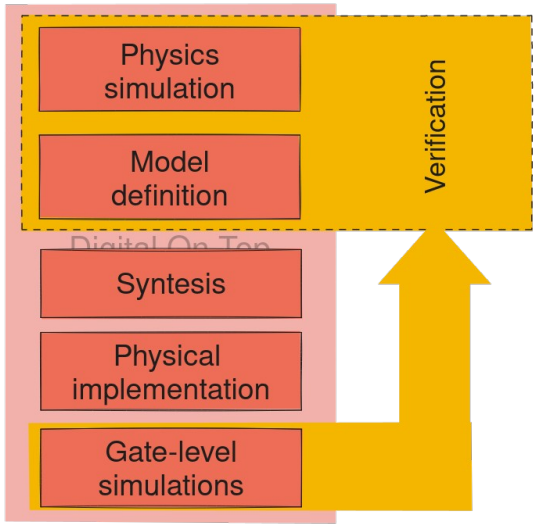

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System Verilog model description
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Verification is the most time-consuming part of the design !

Conclusion

- TIIX aims at combining the pixel front-end developed within TIIMM with a faster scalable matrix digital read-out
  - active pixel matrix is 128×128 pixels with a 41um pitch
  - the architecture should be scalable up to 512×512 pixels at the same pitch
- the proposed readout architecture uses a token passing mechanism along each column (column drain readout as in MONOPIX)
- TIIX pixel FE input dynamic is very large: a 10b ToT is used at chip level
  - the ToT information is not calculated inside the chip
  - the LE (leading edge) and TE (trailing edge) timestamps are serialized with 10b precision
- the timestamp clock frequency could be scaled down from 40MHz to 20MHz
- data are serialized via three LVDS links at a fixed 160Mbps speed

The design submission is currently scheduled for november 2024