# IDROGEN : un système d'acquisition haut débit synchronisé par un nœud WhiteRabbit amélioré

# The collaboration

- **IJCLab**
  - Hardware : Daniel Charlet
  - Firmware : Eric Plaige, Antoine Back, Cédric Esnault, D.Charlet
  - Software : Monique Taurigna, Chafik Cheikali, A.Back, Christelle Soulet
  - Test : Cédric Esnault, Daniel Charlet
- **Paris Observatory**
- **SYRTE**
  - Clock expertise and qualification : Paul-Eric Pottie
  - Hardware : Michel lours
- **Obs Nancay**
  - Firmware : Cédric Viou

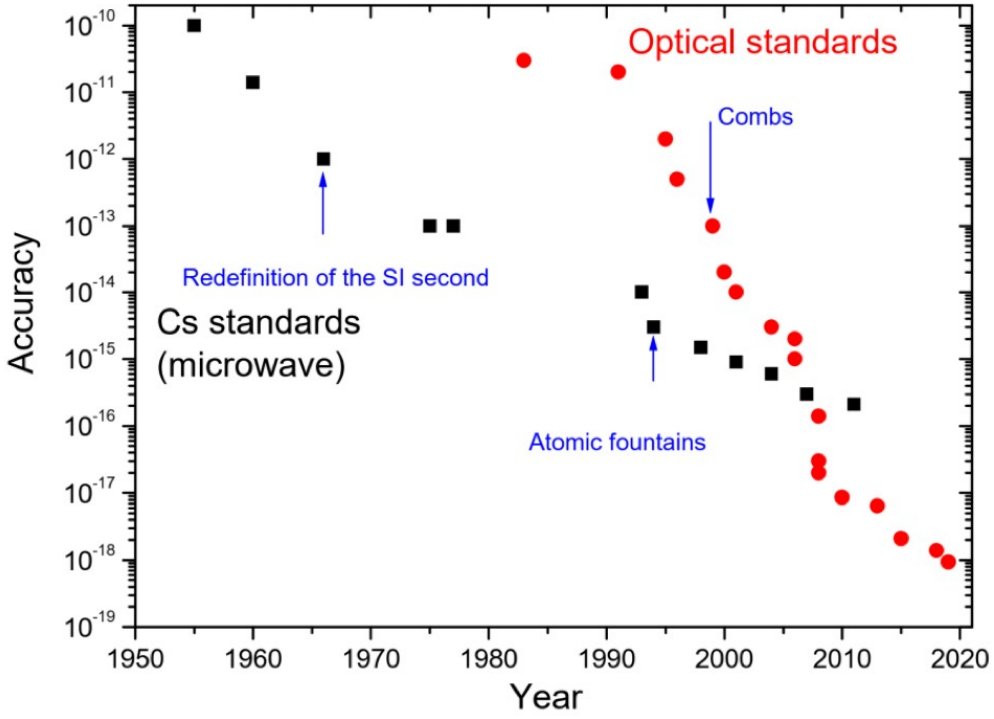
l'Observatoire de Paris | SYRTE

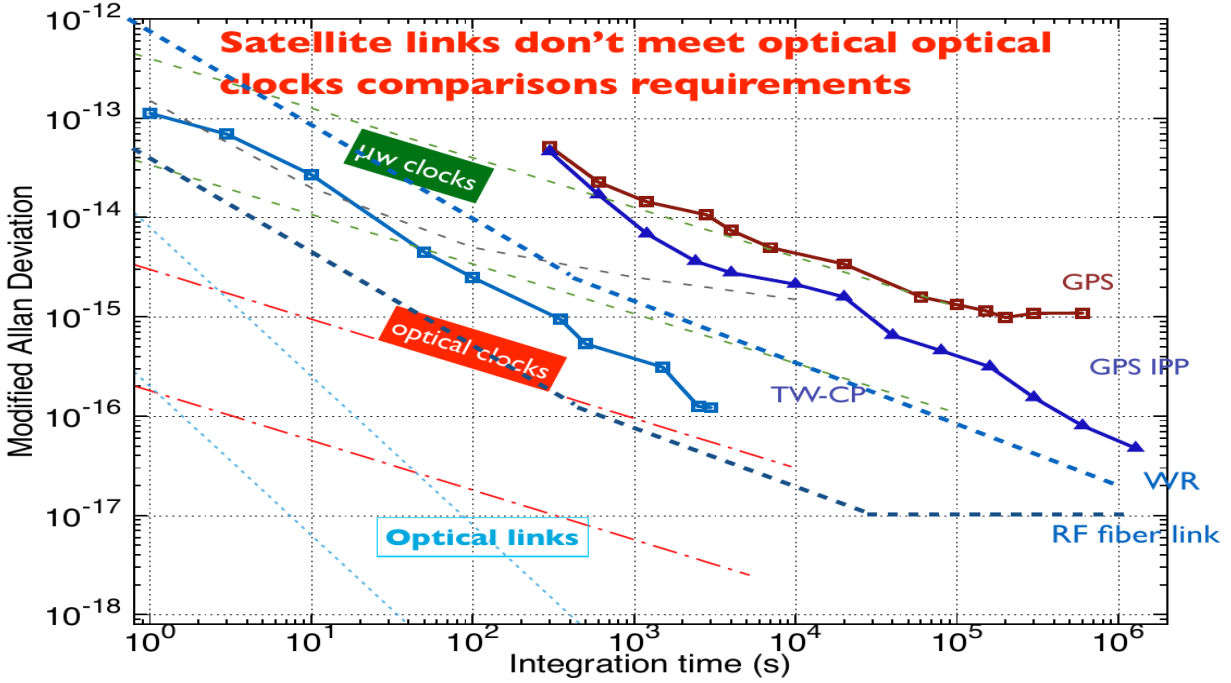
Systèmes de Référence Temps-Espace

Station de Radioastronomie de Nançay

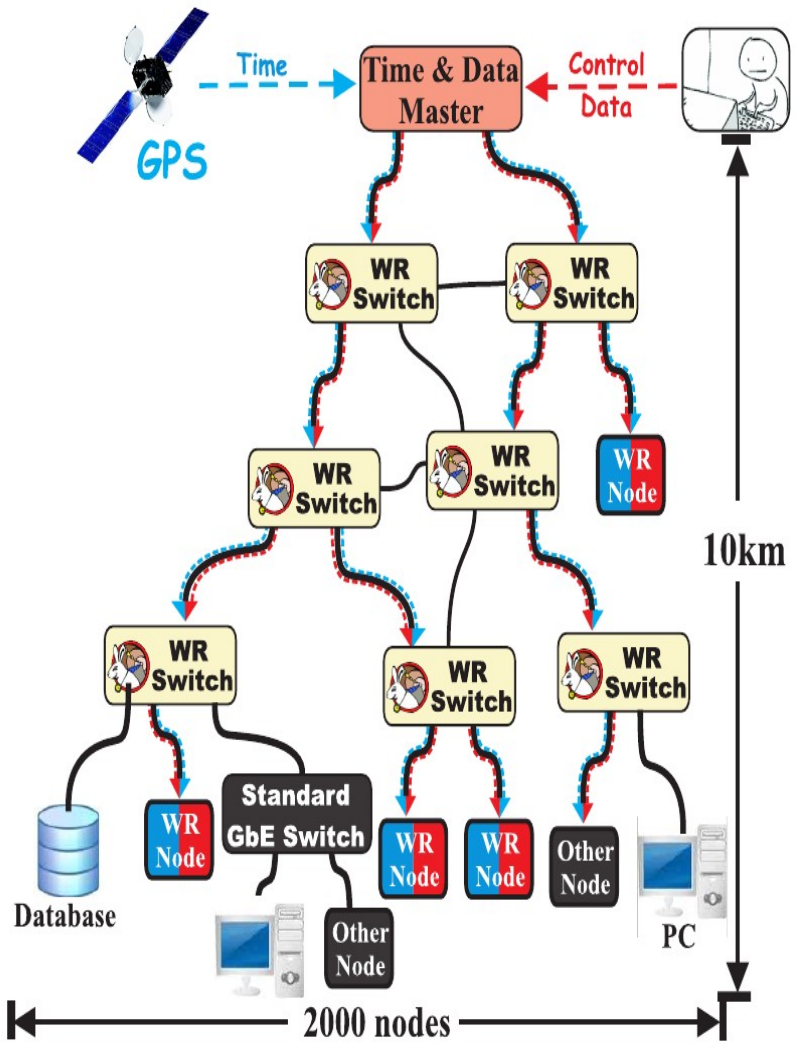
# Clock and time distribution performance

- Drastic improvement in clock performance



# White Rabbit principle : Enhanced Ethernet




- An extension of Ethernet which provides :
  - Synchronous mode (Syn-E) – common clock for physical layer in entire network, allowing for precise time and frequency transfer
  - Deterministic routing latency – a guarantee that packet transmission delay between two stations will never exceed a certain boundary.
- Technology overview
  - Precision Time Protocole (IEEE1588)
  - Synchronous Ethernet
  - DDMTD Phase tracking (Digital Dual Mixer Domain) …

# WHITE RABBIT PERFORMANCES POSITIONING

Wide user community

Best performance

| System | accuracy | Note |
|---|---|---|
| GPS | 10ns -200ns | Propagation in non-stationary disruptive environment. Problem of the multi-way. |
| GPS-IPPP | 2 – 3 ns | Resolution of phase ambiguities using RIMEX data. More complex implementation |
| On the shelf WR switch without calibration | 500ps - 100ns | Tested with WR switch SAFRAN in master configuration |
| On the shelf WR switch with calibration | 200ps – 2 ns | Tested with WR switch SAFRAN in master configuration |
| IDROGEN enhanced WR node | 13 ps | Tested with WR switch SAFRAN in grand master configuration |
| IDROGEN enhanced WR node | 1 ps | 2 IDROGEN boards on the WR switch configured in Grand Master and synchronized by T+ REFIMEVE fiber from Paris Observatory (SYRTE) |
| In development : IDROGEN & external functions | < ps | Aim of T+REFIMEVE |

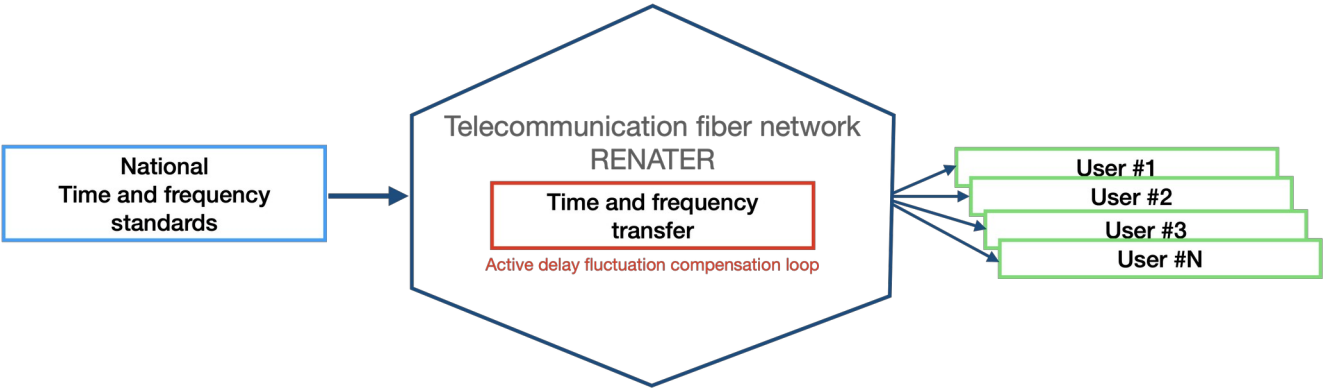
# T+REFIMEVE

## REFIMEVE : Network Metrological fiber with European vocation

**Concept** : Dissemination of time-frequency references by optical fiber

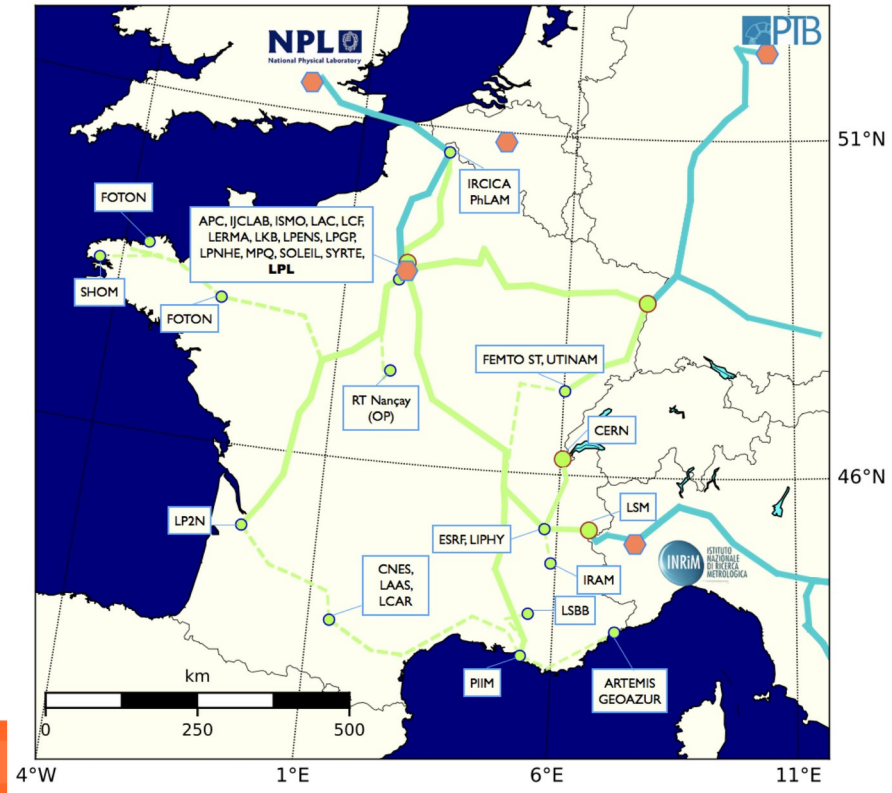
**Reponsabilities** : LPL & SYRTE for deployment and optical reference

IJCLab & SYRTE for timing




Signal to be provided by T-REFIMEVE

| | | Stability or relative stab. @1s | Stability or relative stab. @1day | Uncertainty | |
|---|---|---|---|---|---|
| | | | | routine | dedicated |
| Radiofrequency | 1st pillar - 10 MHz (White Rabbit)* | 1,00E-12 | 1,00E-15 | 1,00E-14 | 1,00E-15 |
| | 2nd pillar - 1 GHz | 1,00E-13 | 3,00E-16 | 1,00E-14 | 2,00E-16 |
| Time | 1st pillar (White Rabbit)* | 1 ns | 1 ns | 10 ns | 10 ns |
| | 2nd pillar | 20-50 ps | 500 ps | 10 ns | 2ns to 100ps§ |
| Optical frequency (194,5 THz/1542 nm) | Today | 1,00E-15 | 3,00E-16 | 1,00E-14 | 2,00E-17 |
| | Expected progress in 5 years | 1,00E-16 | 2,00E-17 | 1,00E-14 | 1,00E-18 |



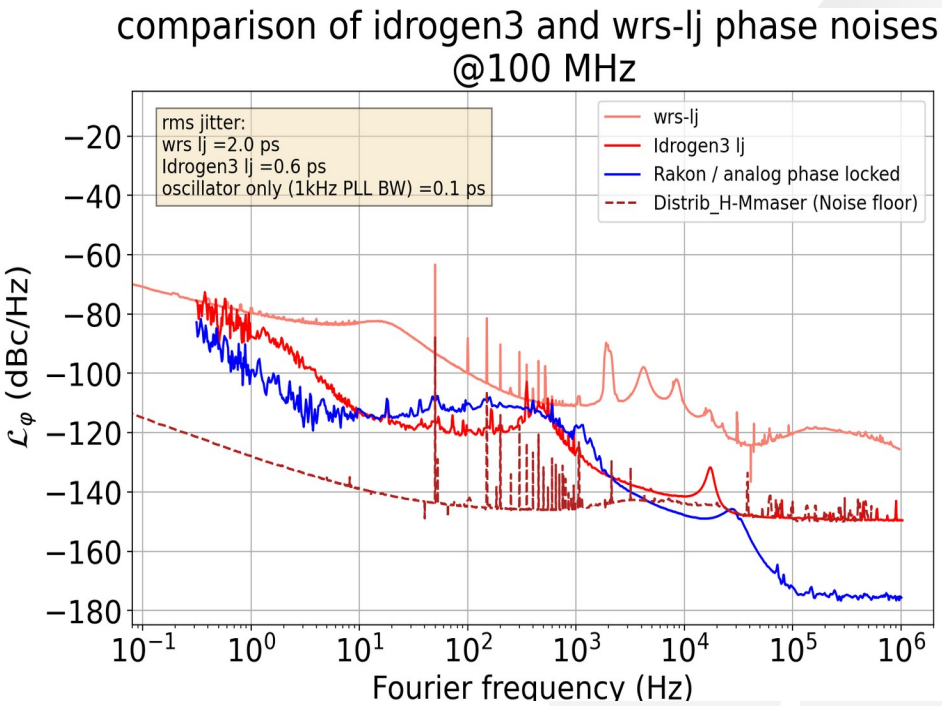
# Current WR projects:

- R&T TIMED
- IDROGEN board
- FMC ADC
- PICMIC project
- New-COMET project
- Master Oscillator

# WR RESEARCH & TECHNOLOGY : TIMED

- 5 Laboratories , 2 institutes (IN2P3 & INSU)
- Schedule : 3 years + 1 (require for 2024)
- Budget : 60K€
- Goals : WR capability extensions :
  - xTCA crate implementation
  - WR implementation simplification
  - WR FPGA external functions integration
  - WR enhancements (High stability frequencies)
- Contributions :
  - LPC Caen : Performance evaluation of a commercial crate controller including a WR switch
  - LPSC : Custom development of a crate controller including a WR switch
  - LP2IB : WR external VCXO (controlled oscillator) integration
  - IJCLab : WR simplification & enhancements,
  - IJClab accelerator department & KEK accelerator: Master oscillator distribution
  - Observatoire de Paris : WR enhancements

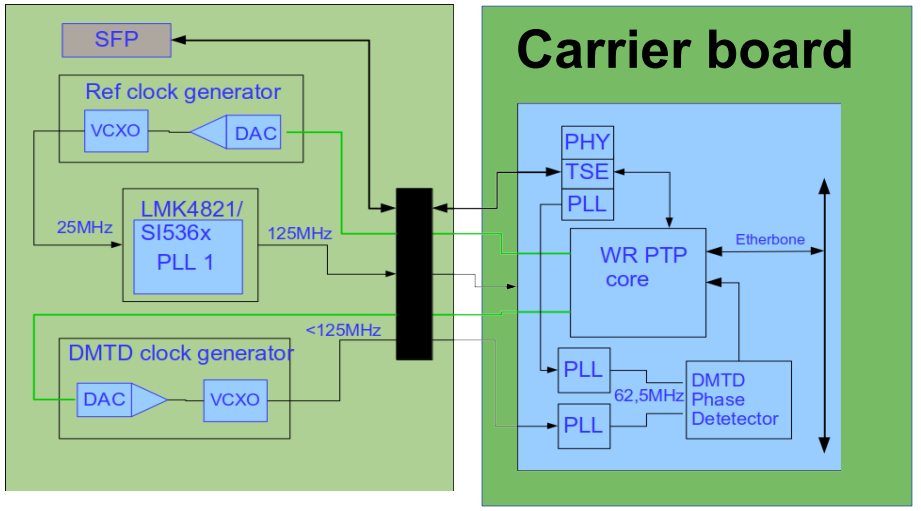
# R & T TIMED : Increasing performances

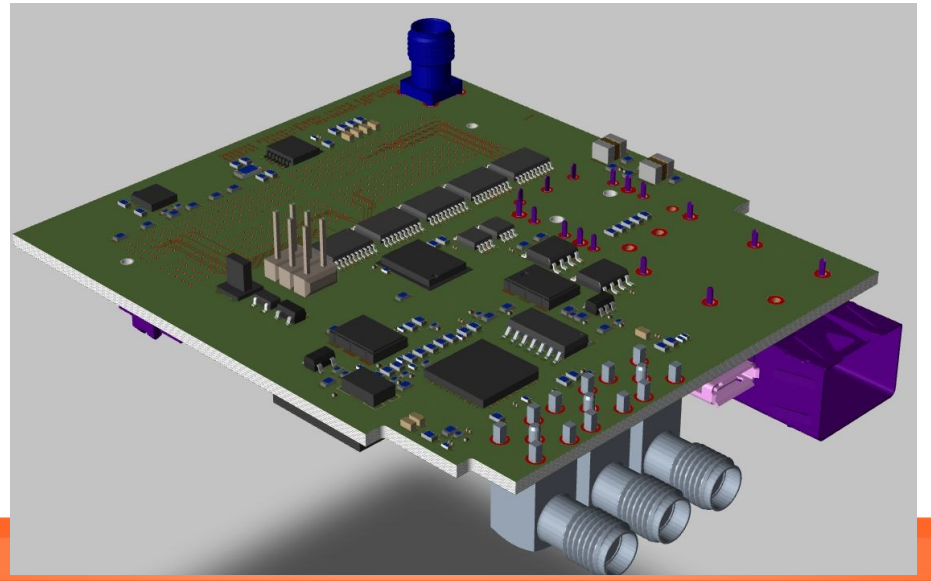



Preliminary results
Measurements made at SYRTE by P.-E. Pottie

- Current phase noise : 0,6 ps RMS
  - PLL (LMK04828) bandwidth optimized
  - Components upgrading
- Target phase noise : < 100fs
  - Soft PLL modification
  - Gain integrator optimization (Tunable by slow control system)
- Target phase noise <10fs
  - Modification of WR principle
  - Change current DDMTD system by optical phase measurement

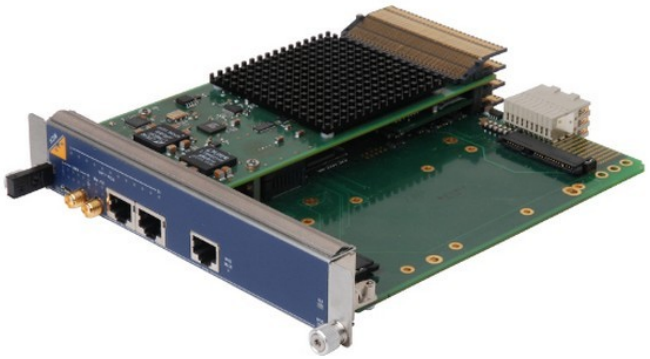
# WR development boards : FMC_PLL



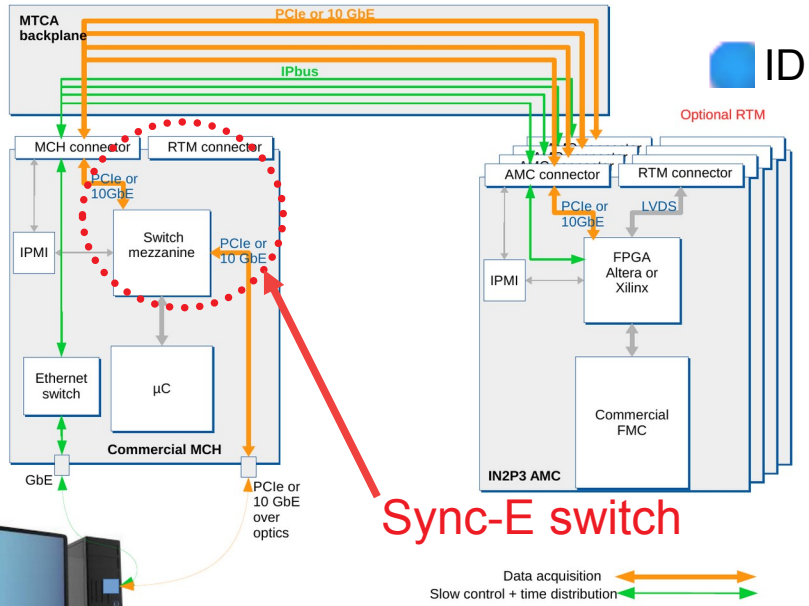



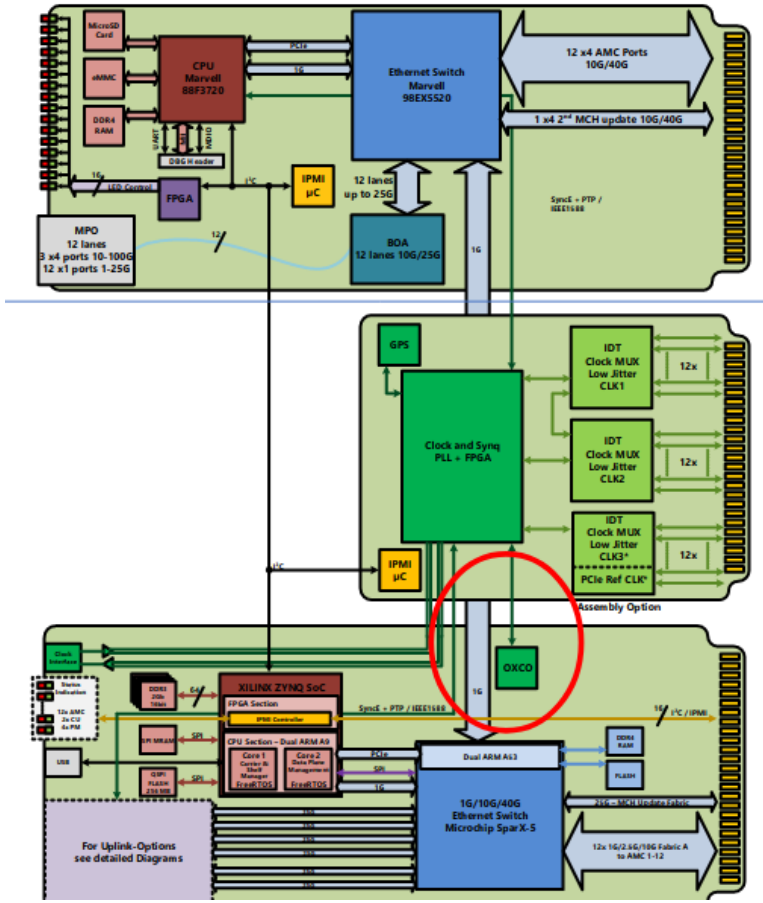
- FMC WR development
- 3 IN2P3 laboratories collaboration (LPSC Grenoble,LCA Clermont,IJCLab)
- 2 types of boards : SI536x, LMK4821
- All external functionalities
  - PLL, SFP, DAC, VCO, CLOCK, PPS, WR
- Test for new components
- FPGA : AGILEX, ….
- LMK4828/LMK4821
- SI5362
- VCXO
- Currently in layout design phase

# R & T TIMED : WR Crate integration

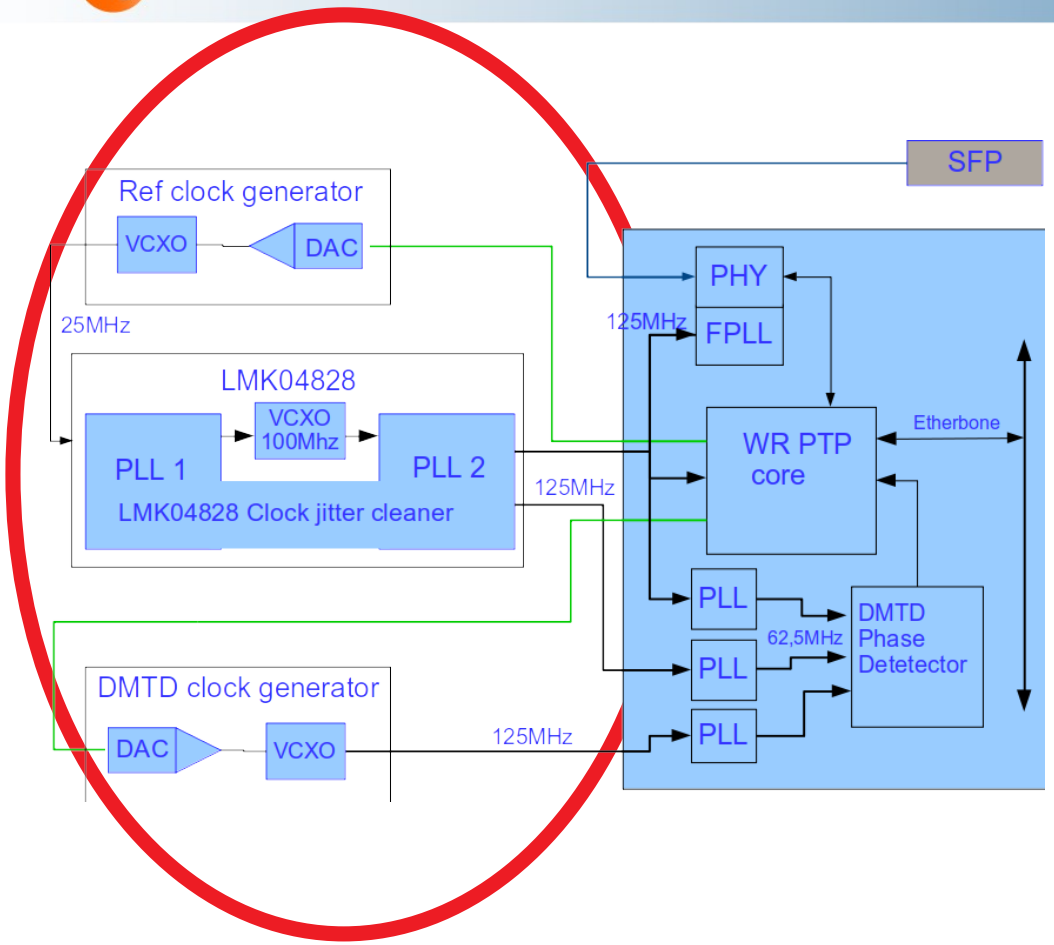


- WhiteRabbit on µTCA
  - Only switch functionality (no master)
  - WhiteRabbit on copper link
  - Sync-E function on MCH board
  - NAT-MCH-4
    - IEEE1588V2 compliant switch
  - IDROGEN board



# R & T TIMED : WR external function integration




- External PLL integration
  - Internal reconfiguration
- VCXO integration
  - Derived from video IP
- FPGA manufacturer dependent

- More challenging that I can imagine ...

Application Note: 7 Series FPGAs and Zynq-7000 AP SoCs

XILINX
ALL PROGRAMMABLE

XAPP589 (v2.3) April 29, 2015

**All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)**

Authors: David Taylor, Matt Klein, and Vincent Vendramini

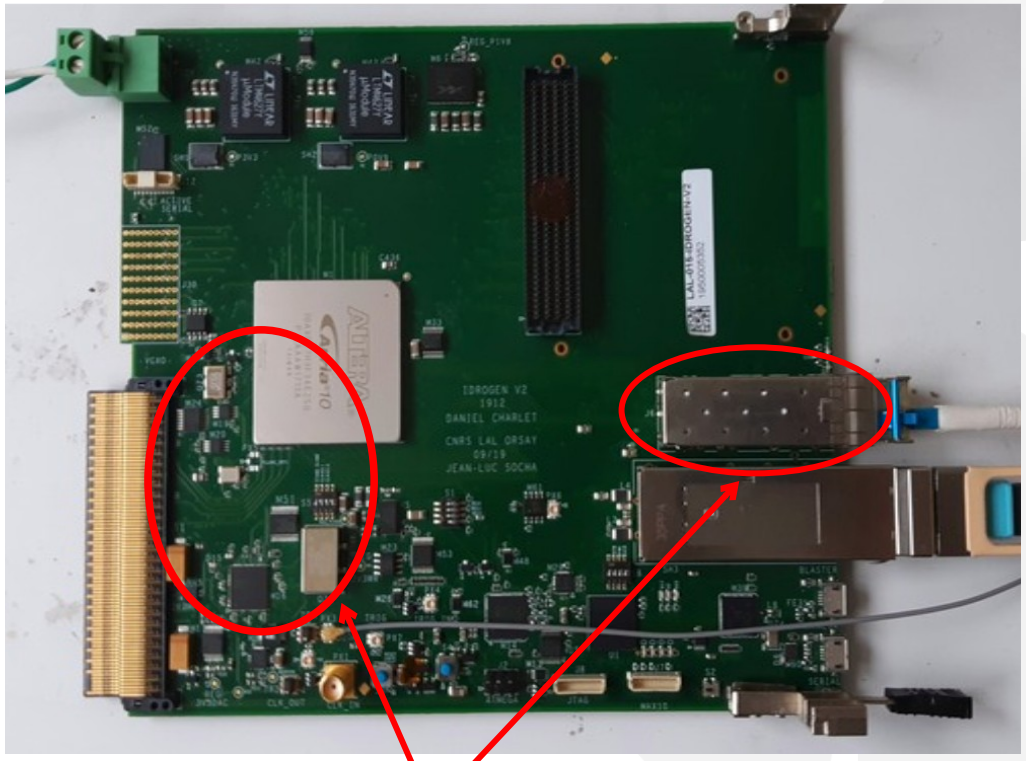
## Summary

This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver.

***Note:*** In this application note, *transceiver* refers to these types of transceivers:

# IDROGEN system

# IDROGEN board : Low phase noise WR node



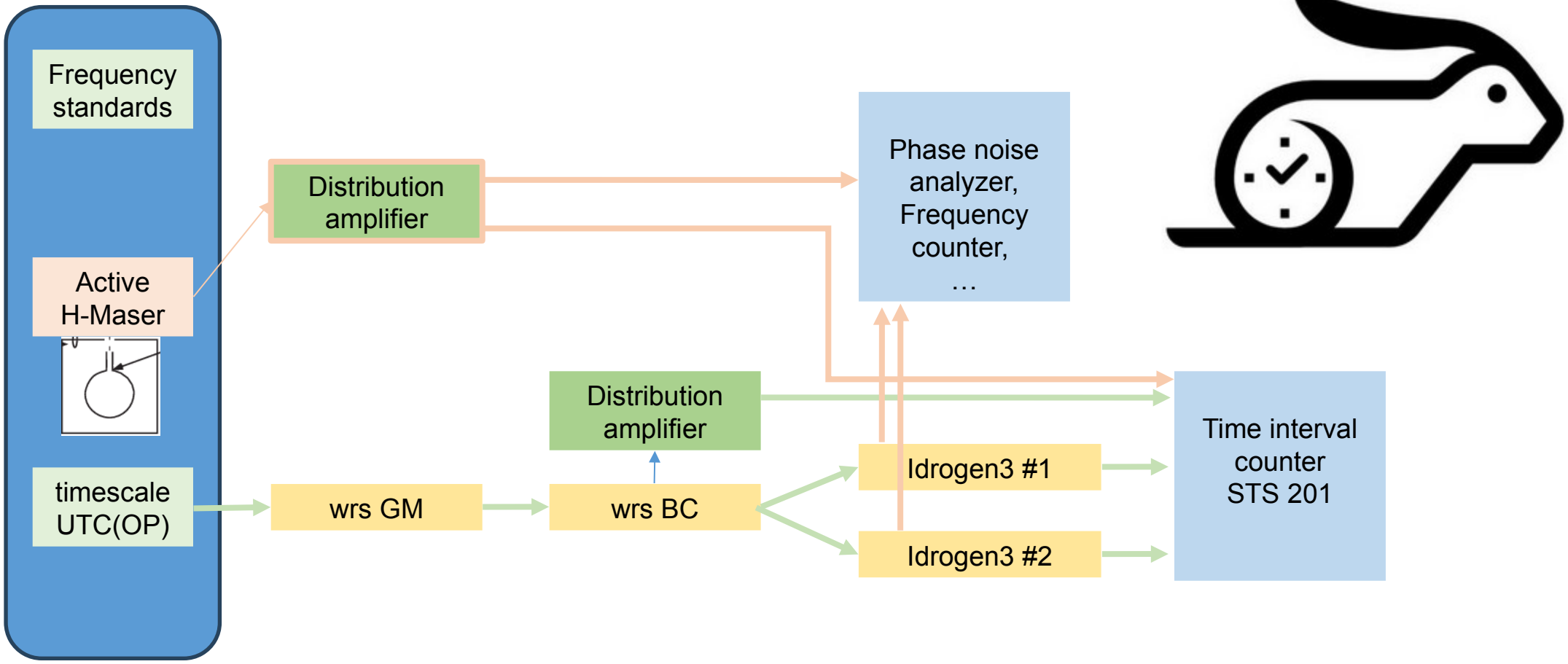

- Design & development done at IJCLab
- Crate (µTCA) or standalone use
- CERN schematic improved
  - Components upgrade : PLL, VCXO, FPGA
- PCB design compliant with EMC rules
- High performance data acquisition system:
  - PCI-Express gen3x4, Ethernet > 20Gb
- FMC+ carrier board for additional functions :
  - ADC, DAC, Clock synthesis, ...

# IDROGEN : Firmwares

- WhiteRabbit
  - Development of CERN & GSI
  - Adaptation for ARRIA 10
- IpBus 1G & 10G
  - Development by LPSC laboratory
  - Adaptation by IJCLAB for ARRIA 10
  - Streamer UDP 1G/10G
- PCIExpress v1
  - Based on INTEL-FPGA
- PCIexpress with enhance DMA (in development)
  - Based on CERN LHCb development
  - High and continuous data rate acquisition
- GBT to PCIe
  - Based on CPPM LHCb for PCIE40 development
- JESD 204B for high speed ADC
  - Base on INTEL-FPGA IP
- Parallel 64 data acquisition
  - For 2 ADC 125MBPS 16bits
- IpBus on WR link (in development)
  - One optical link : timing, synchronisation, configuration, data readout

# IDROGEN board WR performances

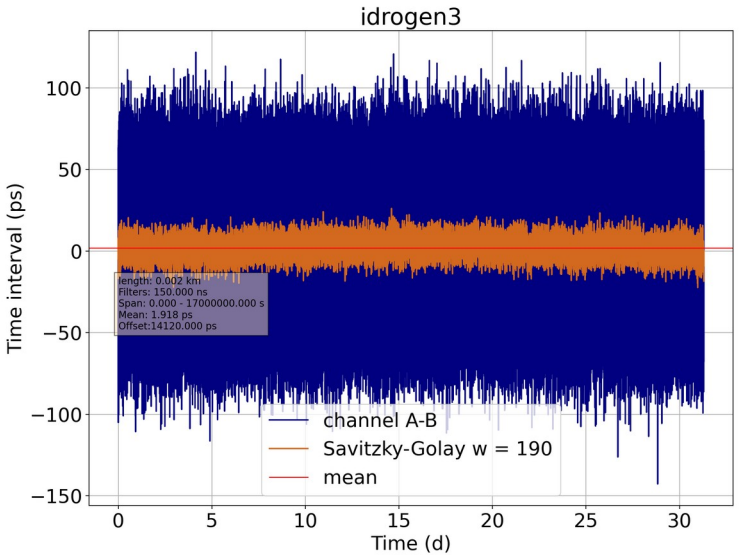
# Syrte test setup

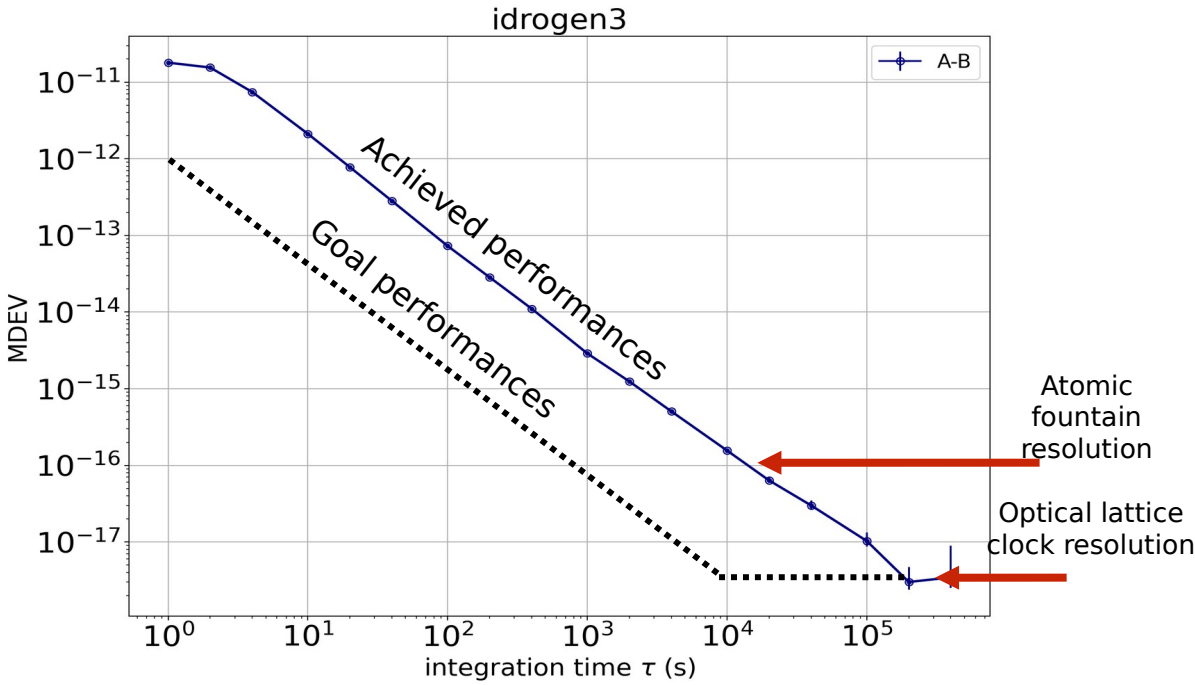



2 Idrogen boards, in the same chassis, connected by 2-m fiber to the same wrs. H-maser is in common view.

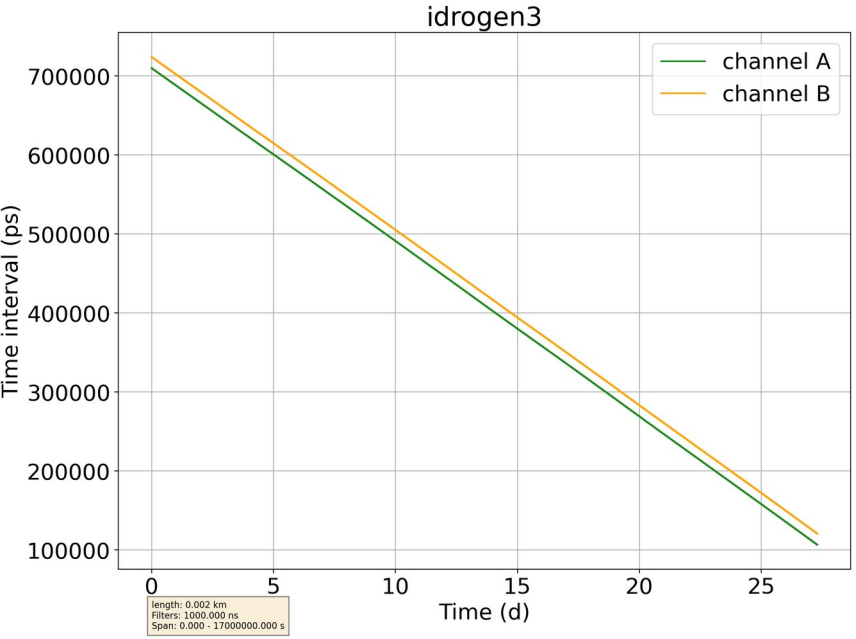
# IDROGEN board performances

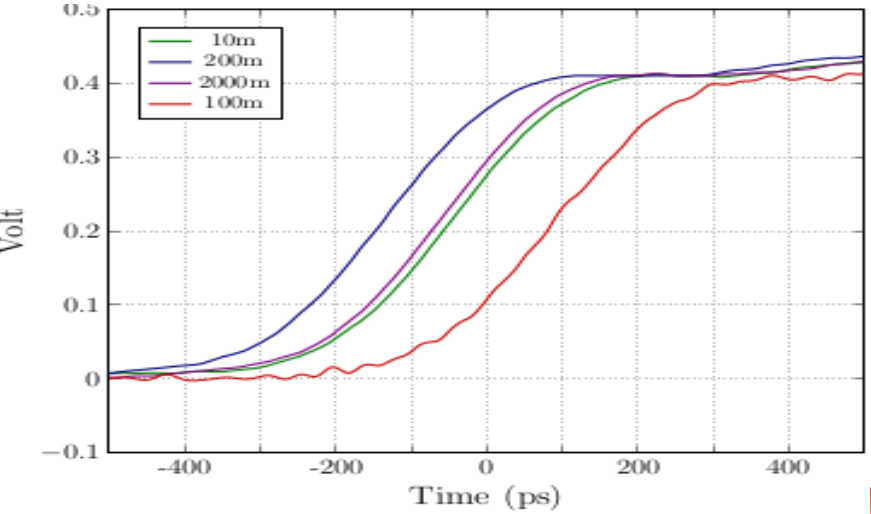
- PPS time difference between two independent IDROGEN3 boards
- Excellent long term stability : ~ 3E-18 s
- On-going work: improve short term performances



# IDROGEN board performances

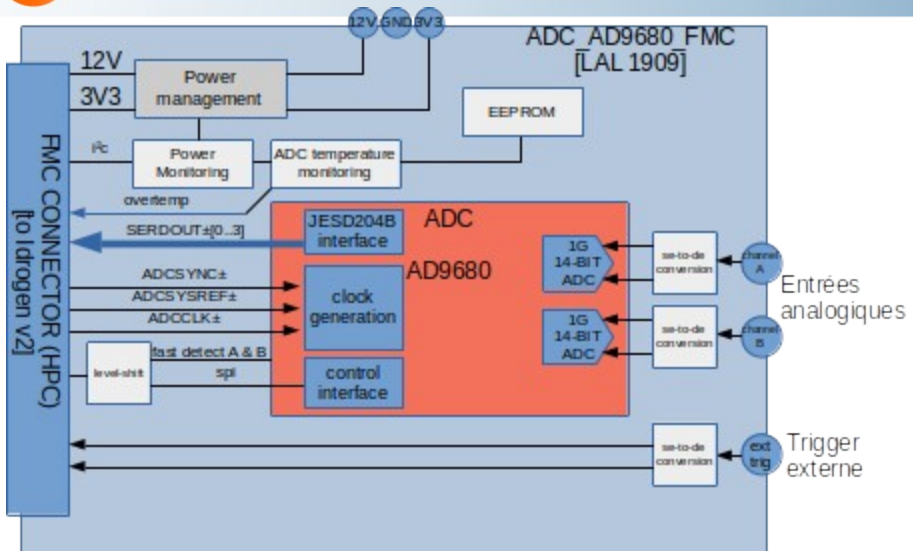


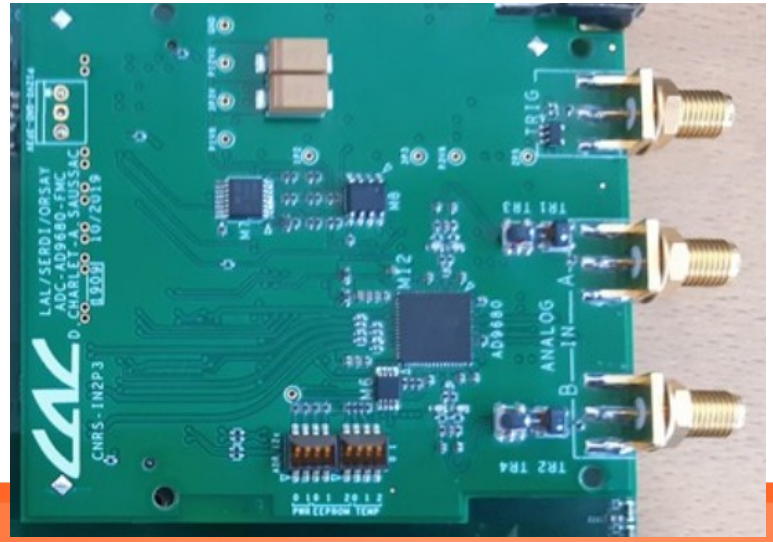




- the measurements were made by SYRTE (P.-E.Pottie)
- transfer from one WR switch to two IDROGEN boards
- Time difference between 2 IDROGEN board
- PPS measurements for different fiber lengths
  - From 10 m to 2 km
- Time accuracy below 100 ps

# IDROGEN board WR ADC development

# FMC_AD9680_500MSPS



- The motivation of the development of a new mezzanine instead of an off-the-shelf ADC mezzanine :
  - includes : its own PLL.
  - ADC clock source : External clock
- Mezzanine main features :
  - VITA57.1 (FMC),  ADC 9680, 2 channels, 14 bits
  - 500 MSPS, JESD204B, 2GHz analog bandwidth
  - External trigger in
- Bandwidth 500 MHz  to 1.5GHz
- Synchro & timing by WR
- Data transfer 2x  10G Ethernet
- Configuration by IPBus 10G

# FMC ADC_9680 : Synchronisation

LM04828

SYSREF Clock SYNC

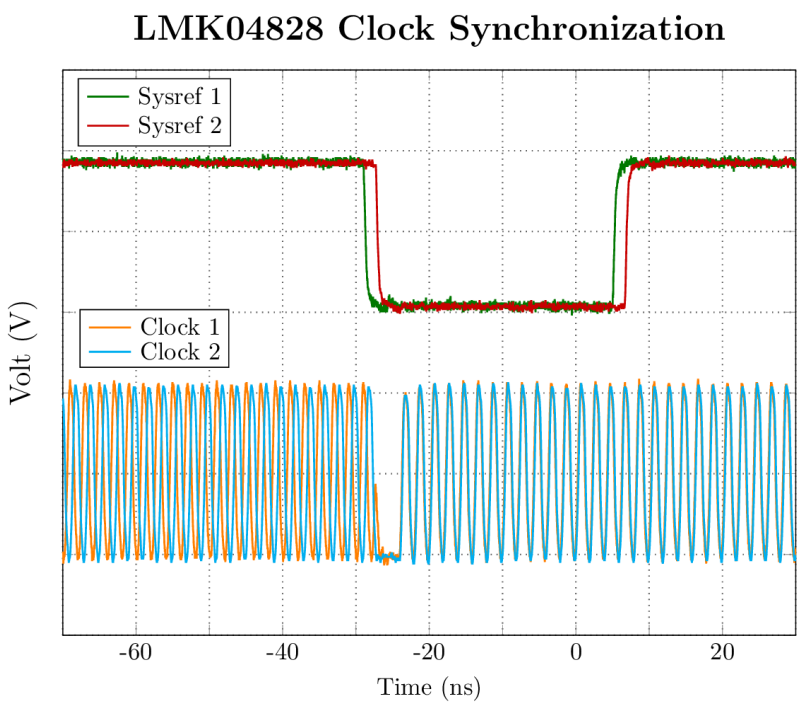
SYSREF

Clock

ADC9680

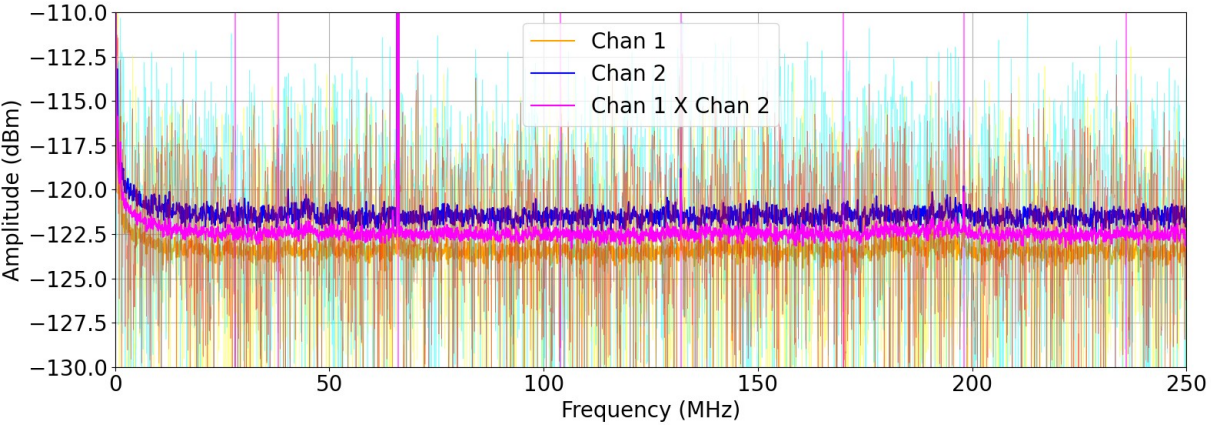
PPS

FPGA

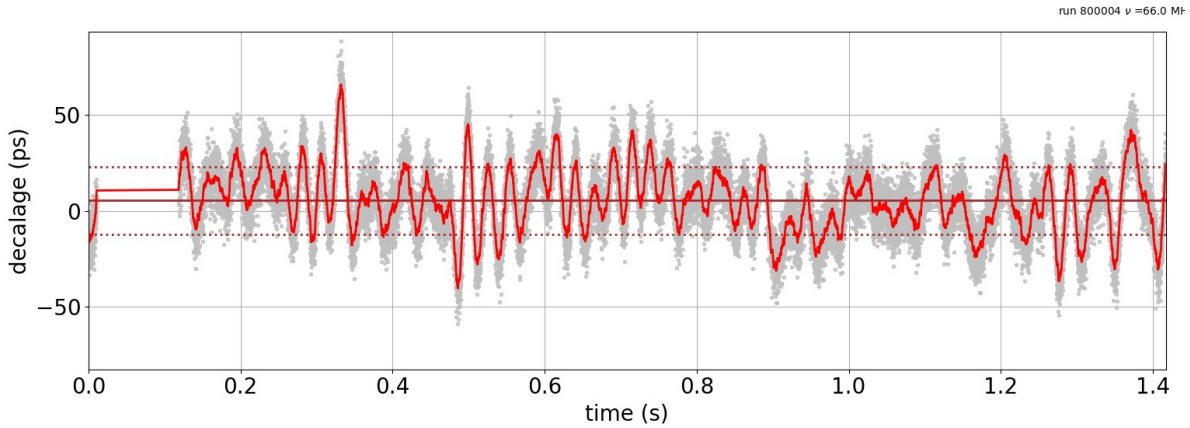


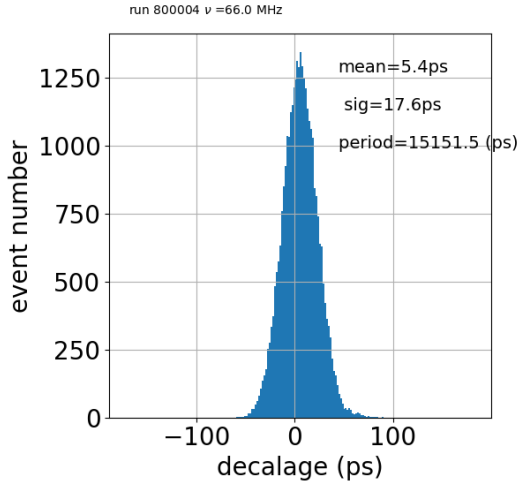

- 2 IDROGEN boards synchronize by WR
- PLL : LMK04828
- ADC data transfert : JESD204B class 1
- 500MHz Clock
- Phase alignment by PPS

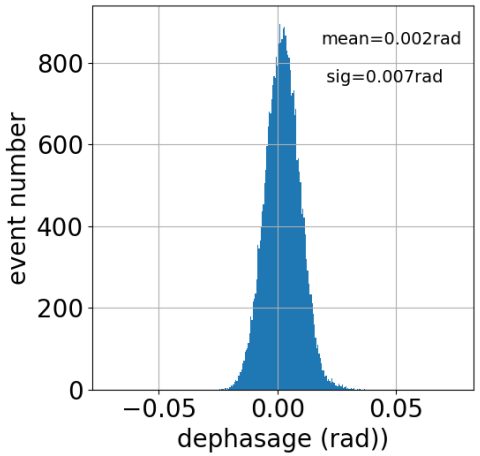
# FMC ADC_9680 : Synchronisation



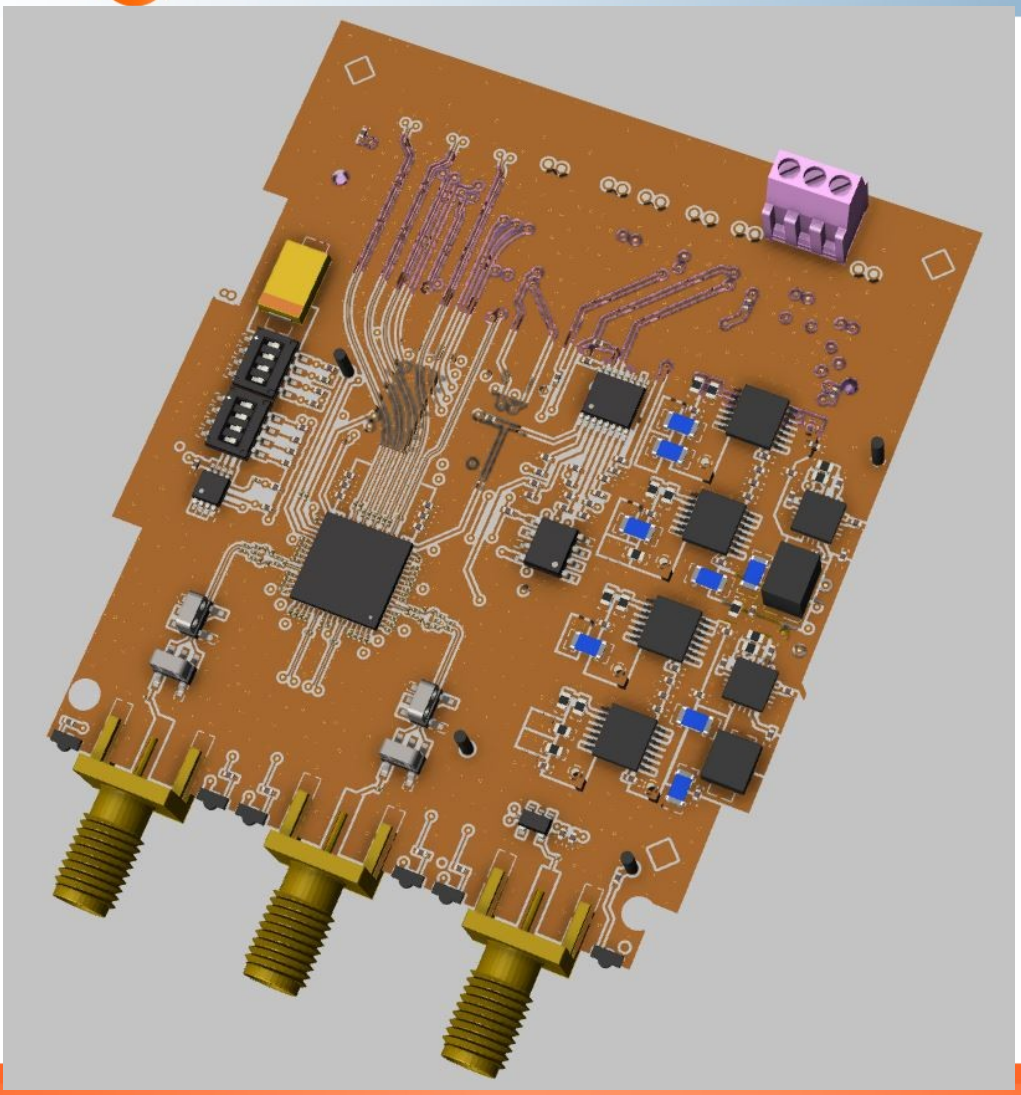

- 2 IDROGEN boards synchronize by WR
- Same RF signal (66MHz) split on boards
- FFT 16K point
- Cross correlation



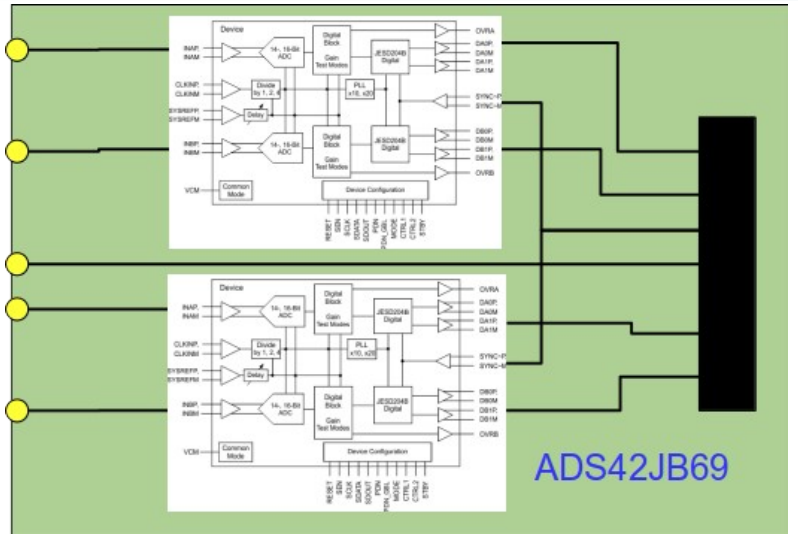



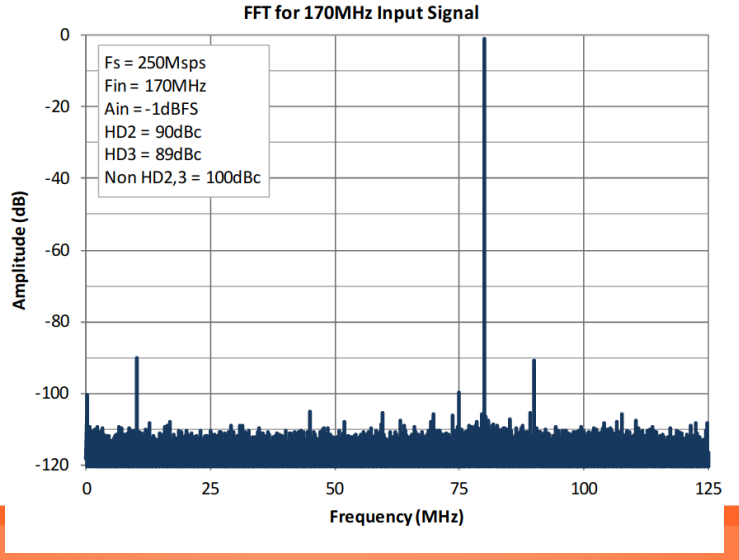
# FMC_AD9680_1GSPS



- Mezzanine main features :
  - VITA57.1 (FMC),  ADC 9680, 2 channels, 14 bits
  - 1 GSPS, JESD204B, 2GHz analog bandwidth
  - External trigger in
- Bandwidth 500 MHz  to 1.5GHz
- Synchro & timing by WR
- Data transfer 2x  10G Ethernet
- Configuration by IPBus 10G
- Layout finished, in production next week

# FMC_ADS42JB69 for IDROGEN

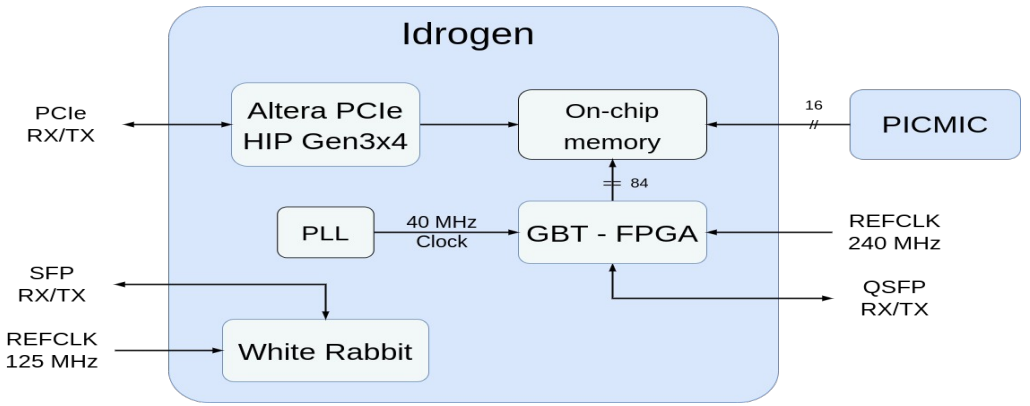


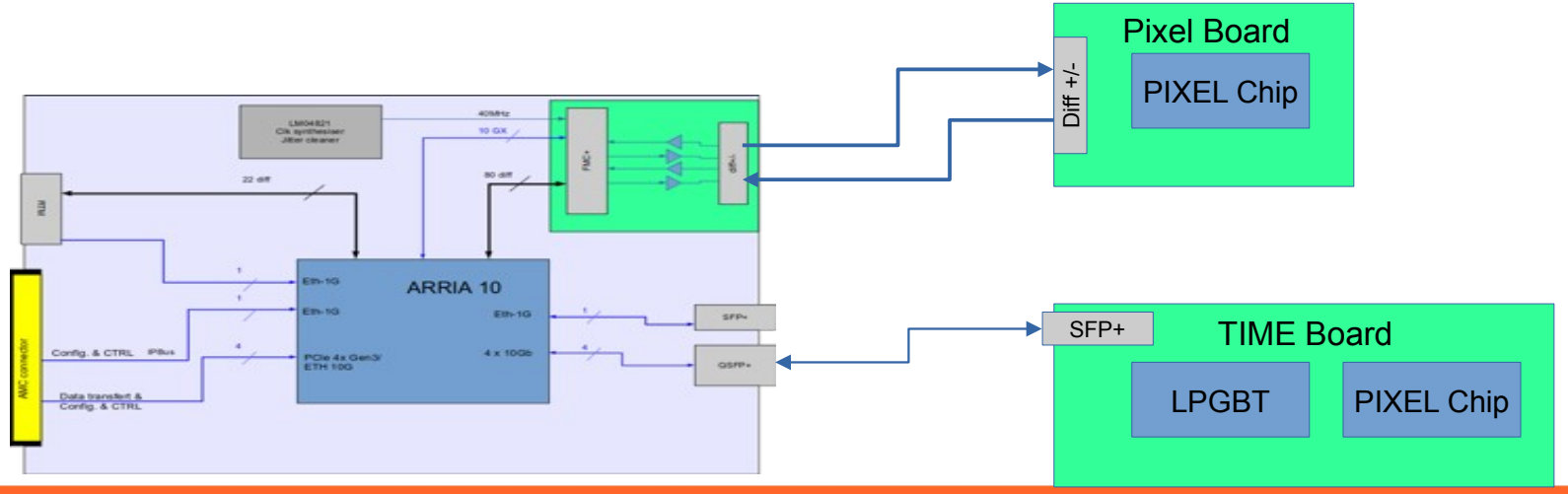

- The motivation to develop the FMC-ADS42JB69
  - **ADC Clock origine coming from IDROGEN**
- 4 channels 250MSPS 16bits
- One external trigger
  - Interface JESD204B
  - Analog input 900MHz
  - 2.5v input voltages

# PICMIC project

# PICMIC detector: readout architecture



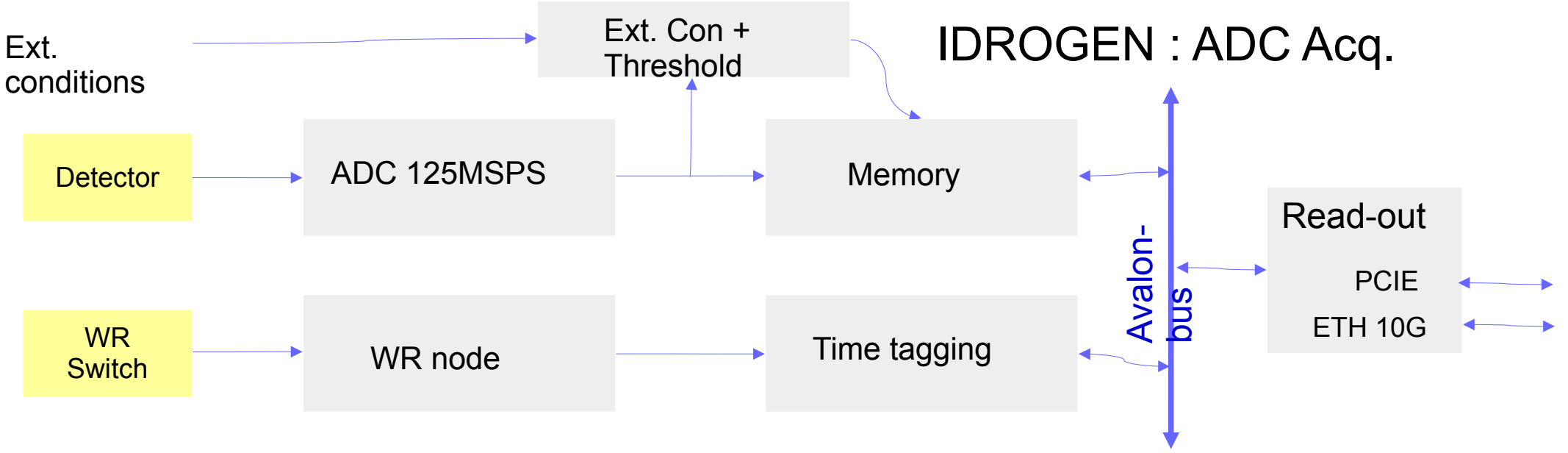

- Data readout
  - PCIE Gen 3 4x End-point mode, 128-bit layer interface payload 256 bytes (
  - DMA readout (INTEL IP)
  - DMA LHCb (in development)
- Data acquisition
  - Spatial data : LVDS parallel interface (IJCLAB firmware)
  - Timing : GBT (CPPM firmware)



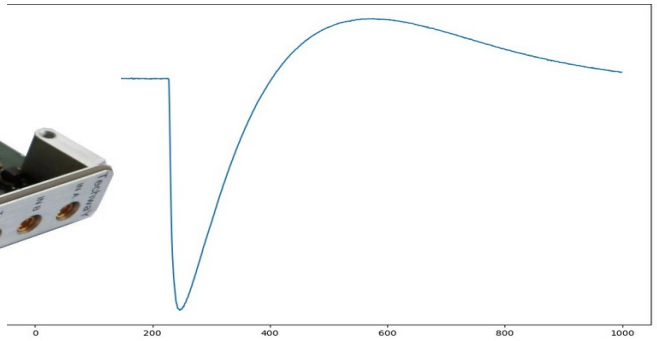
# New-Comet project

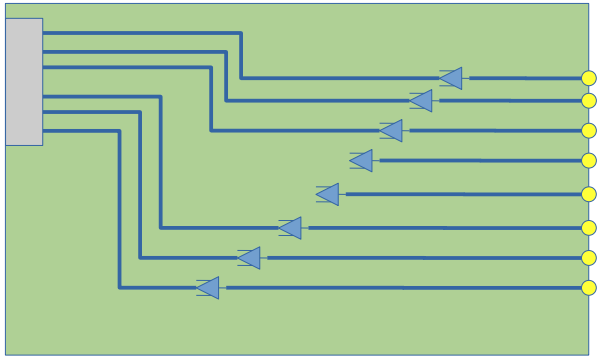
# Trigger less acquisition system : New-COMET

- Trigger-less detector acquisition system
- Continuous signal coding : 4 x 125MSPS 16bits
- WhiteRabbit time tagging
- High level treatment performed by the acquisition software
- Energy and timing correlation made by acquisition software
- Transfer Ethernet 10G
- Transfer PCIExpress for direct GPU access
  - Server or crate implemetation



# Trigger less acquisition system : New-COMET

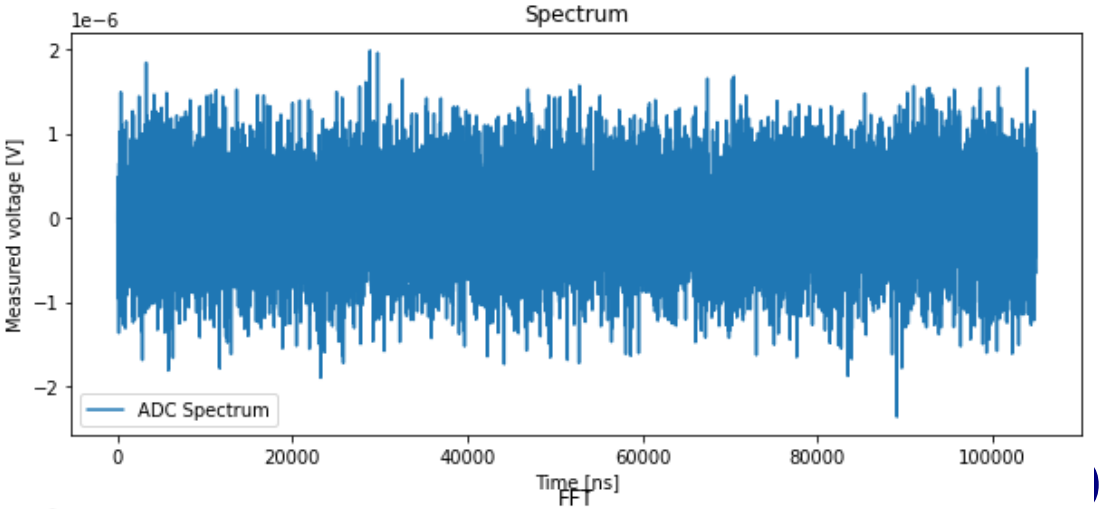


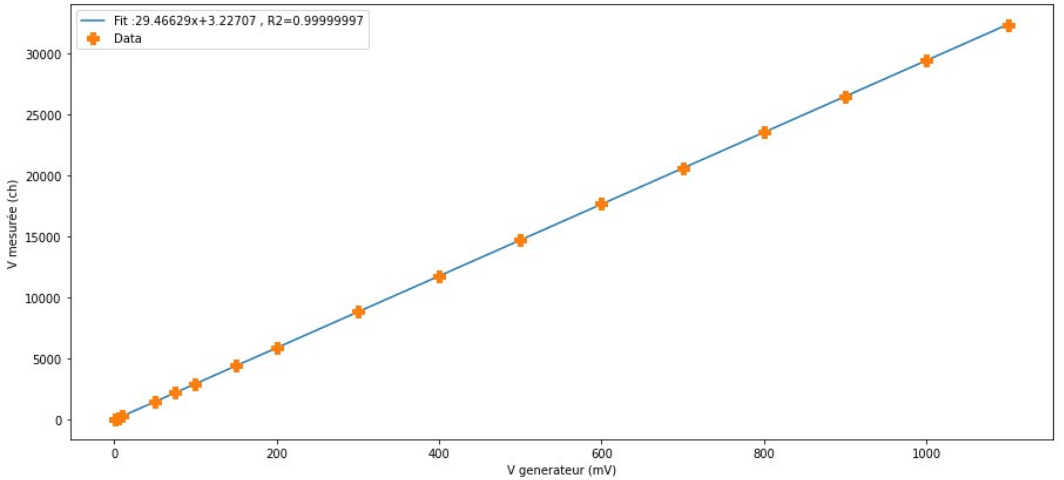



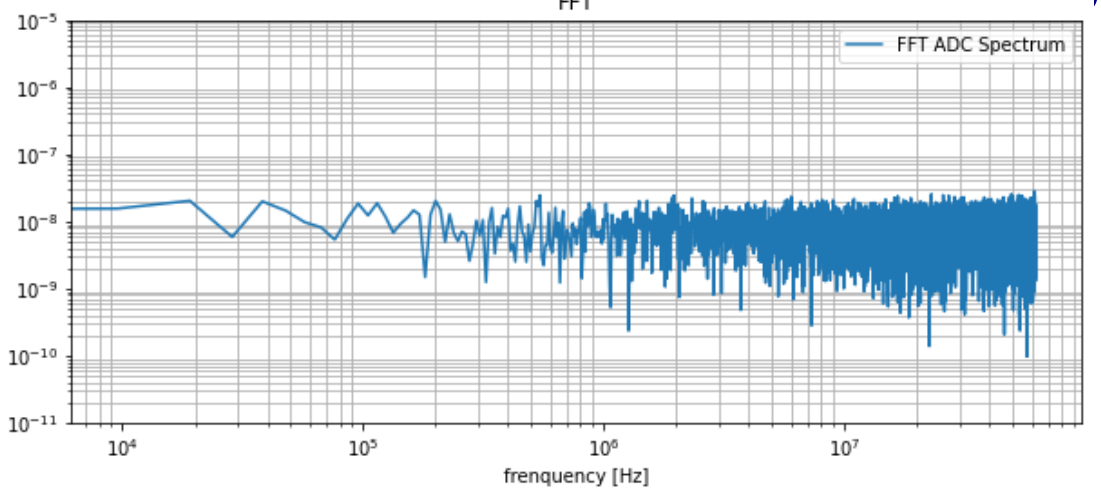
- Off the shelf mezzanine for proof of concept
- No dead-time data transfer
- 10G Eth or PCIe gen3 4x
- Data memory with sliding window
- Data taging by WR (4ns timing resolution)

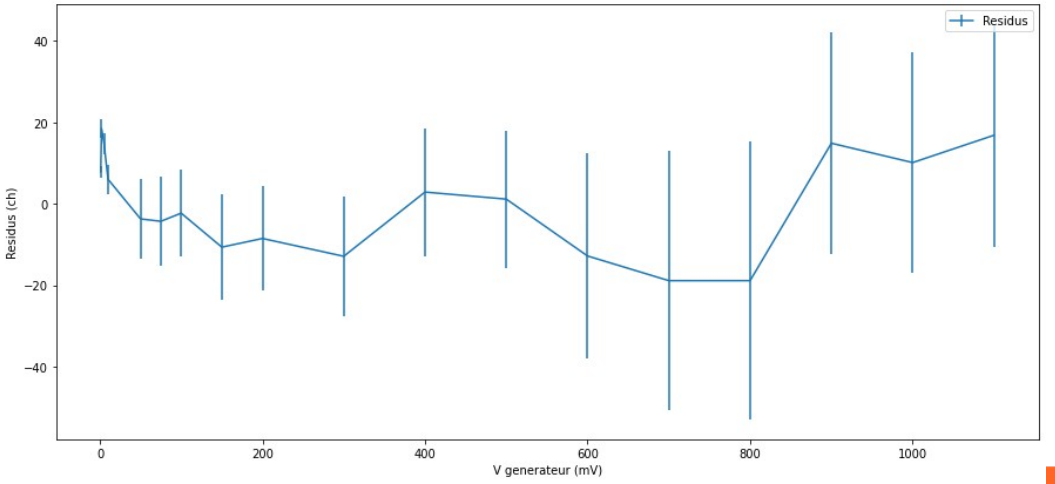
- New ADC board development
  - 4 channels 16b 250MSPS
  -
- RTM board development
  - External logic time tagging
  - 16 NIM to LVDS converter

# ADC & input filter validation

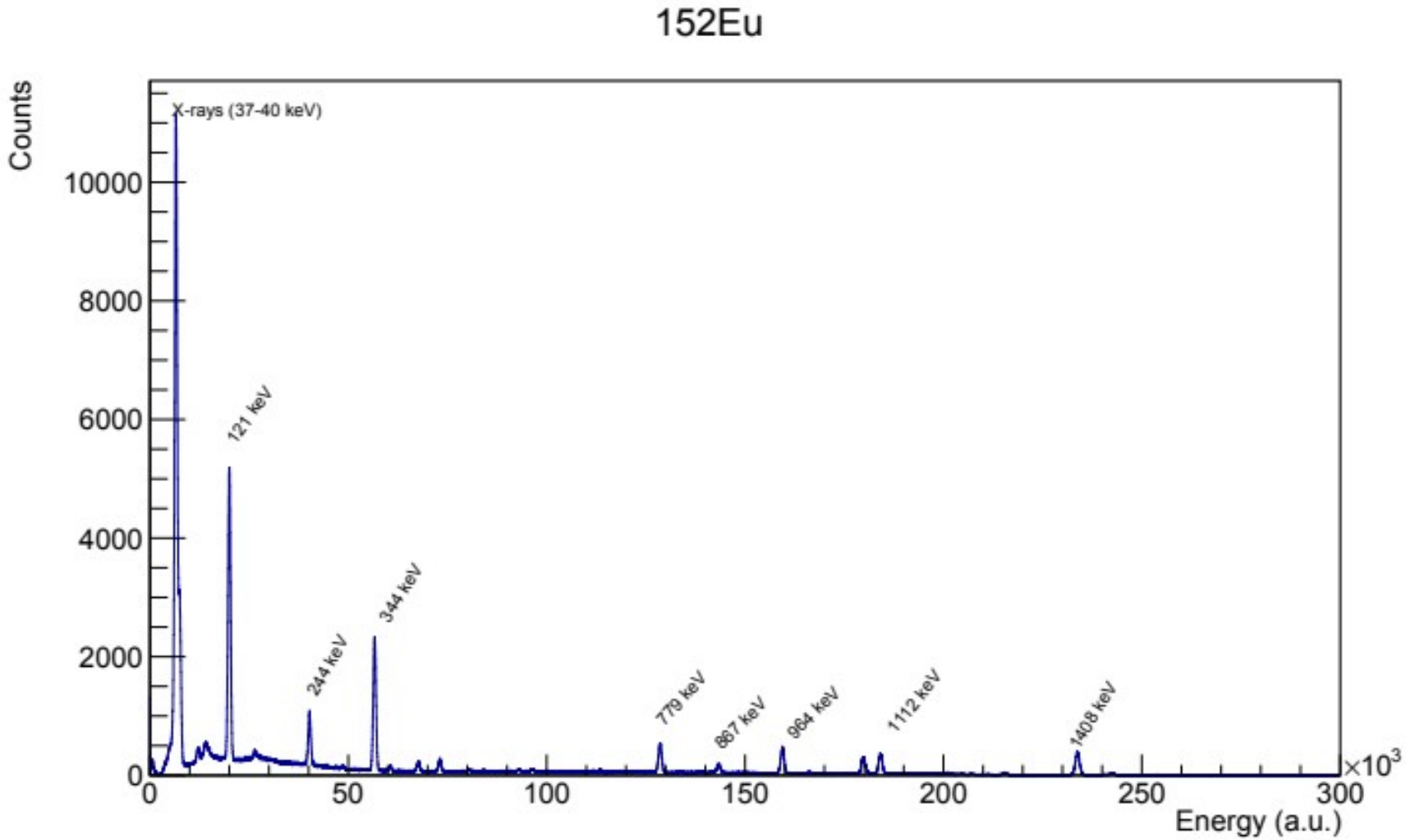


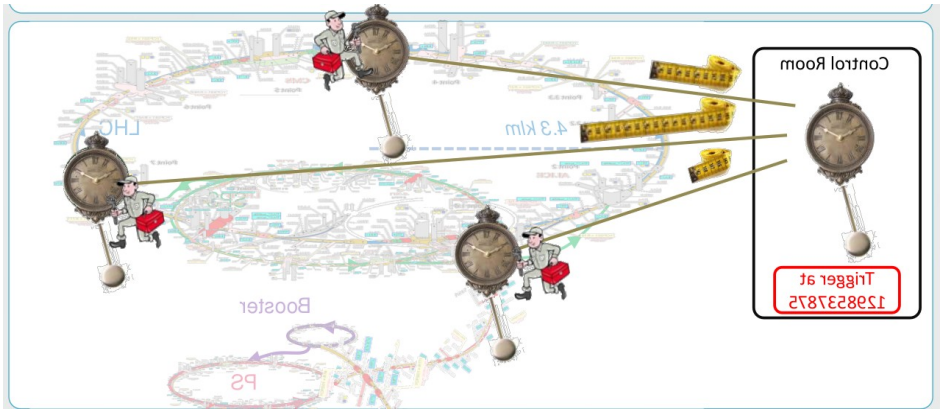



# Europium test

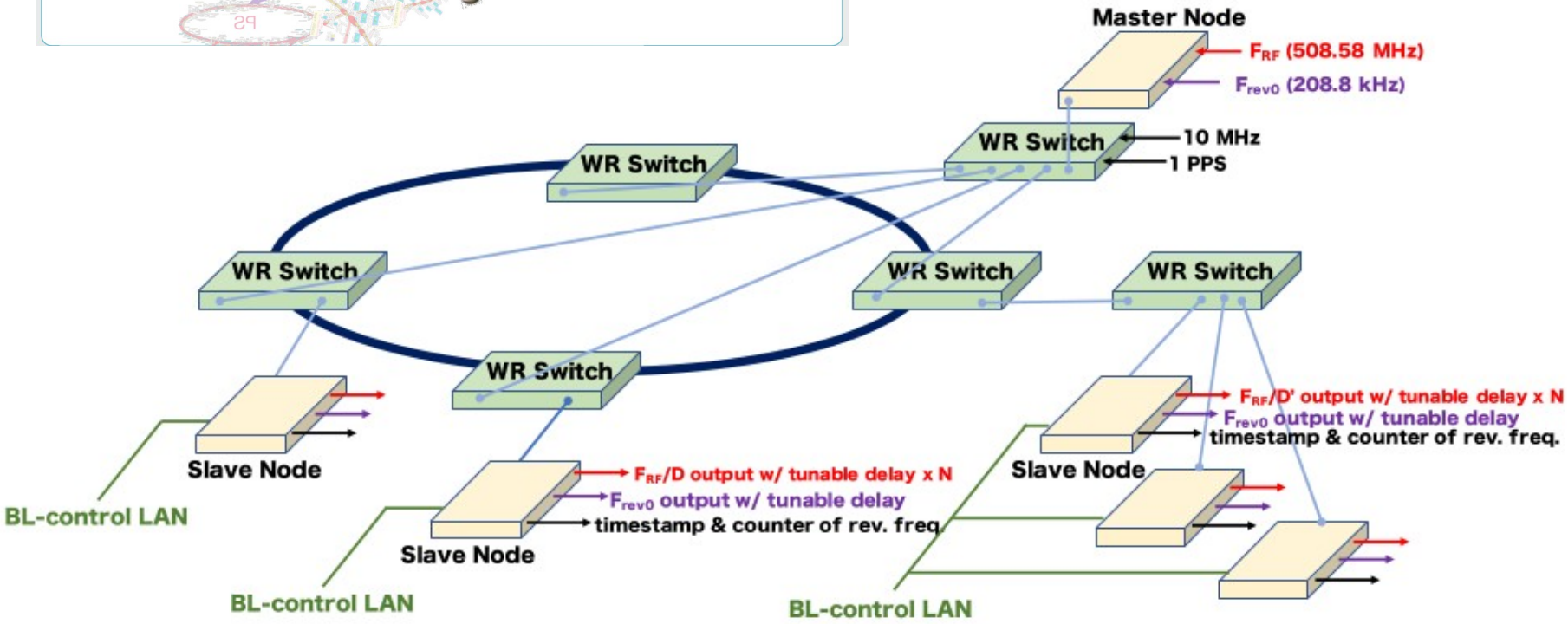


# Master oscillator distribution

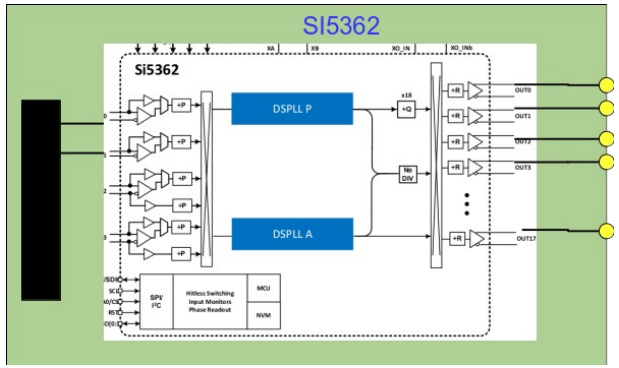
# ACCELERATOR : MASTER OSCILLATOR DISTRIBUTION IMPROVEMENT



- Japan collaboration : KEK RF group
- IJCLab : accelerator group
  - RF groupe PERLE project
  - ILE group synchro Laser



# FMC_SI536X for IDROGEN



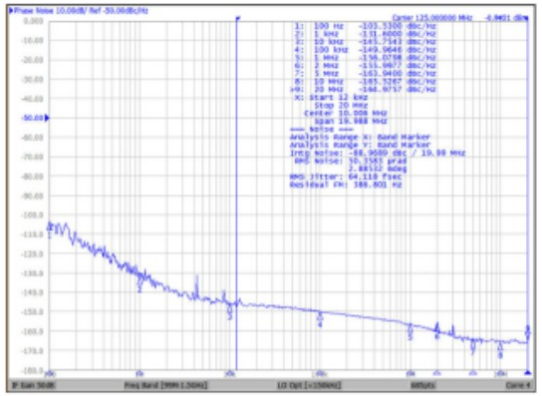
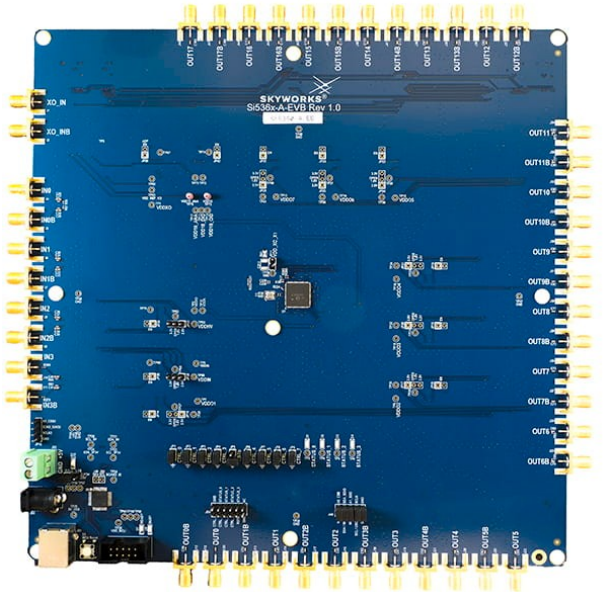
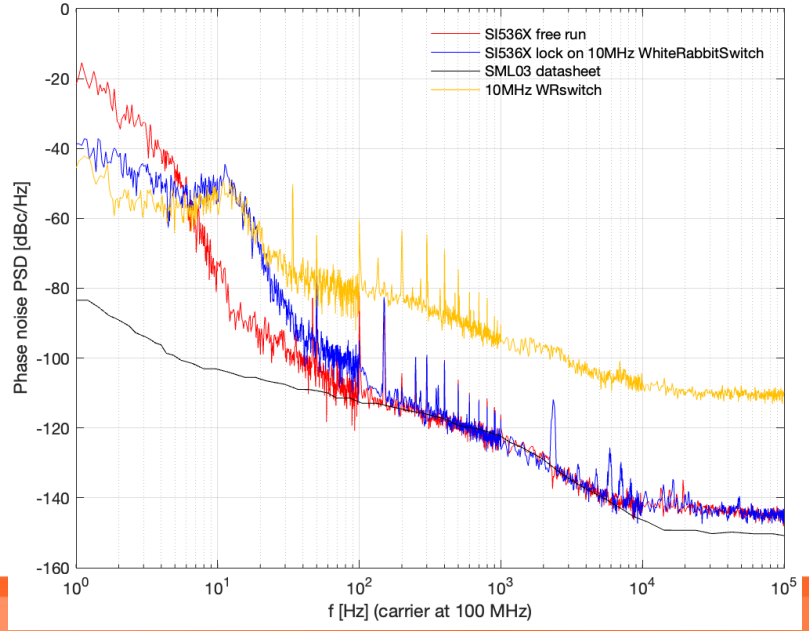
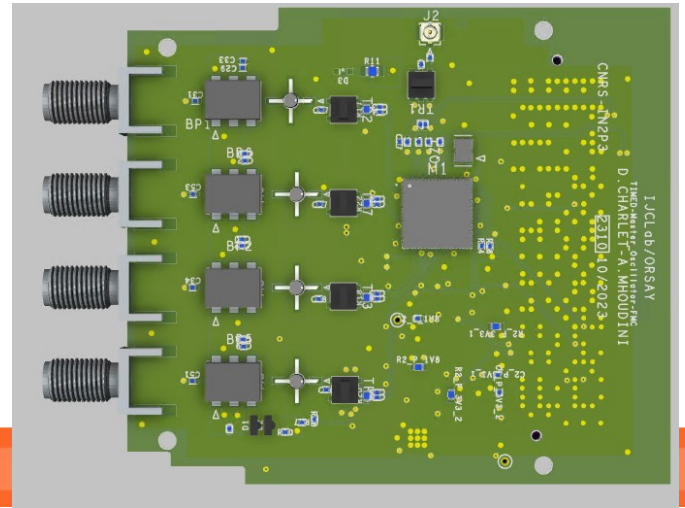



Figure 4.6. 64 fs Jitter for 125 MHz LVDS; Path=DSPLLP+Qdiv

- The motivation to develop the PLL FMC
  - **Generate any frequency disciplined by WR clock**
- Current test with SI536x evaluation board
  - ultra-high-performance jitter attenuator
  - Ultra-low phase jitter (<55 fs typ)
  - 18 outputs 10KHz to 2.75GHz
- FMC_SI536X
  - 4 single ended outputs clock
  - Currently in layout design phase



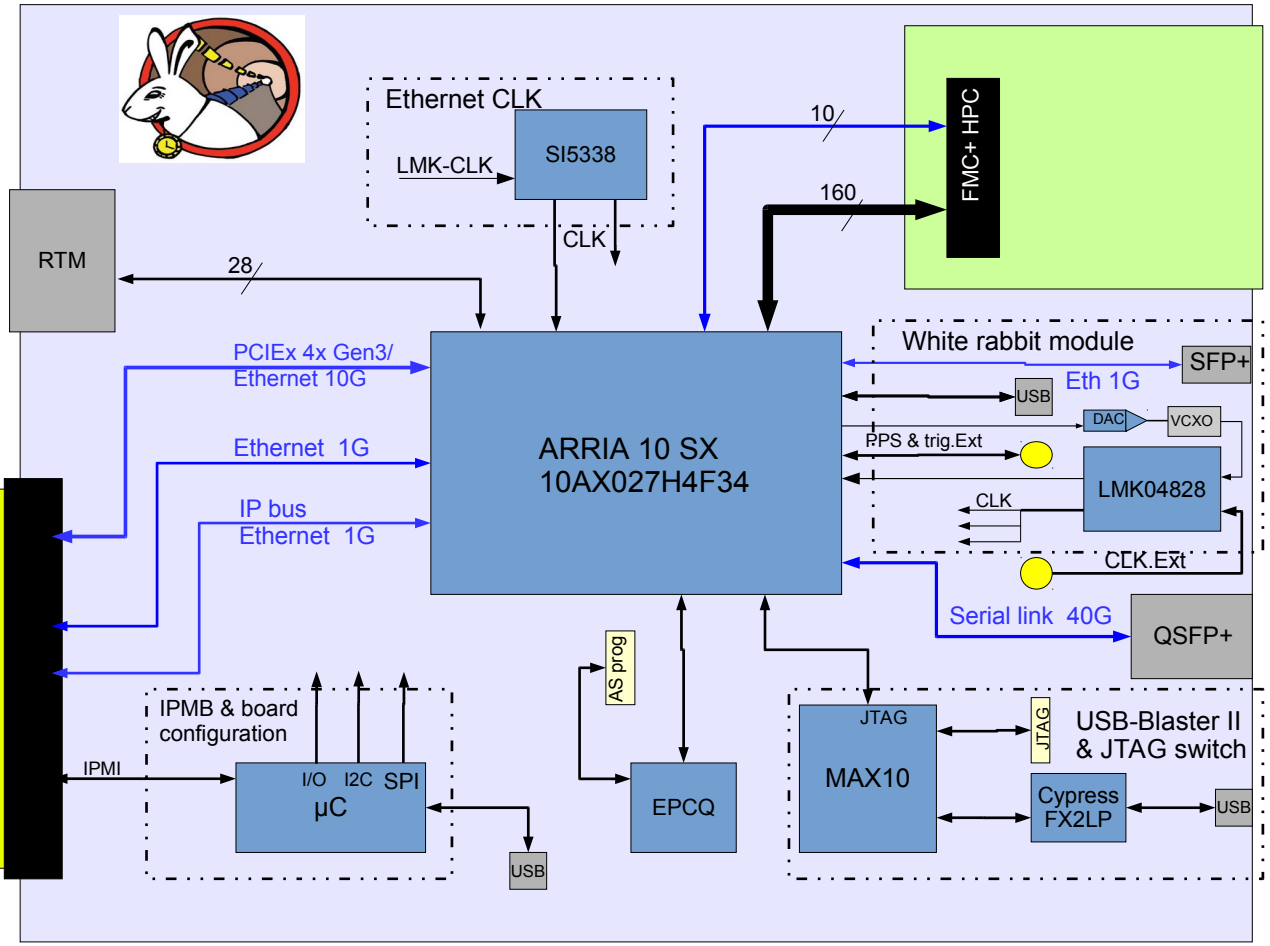



# Conclusion

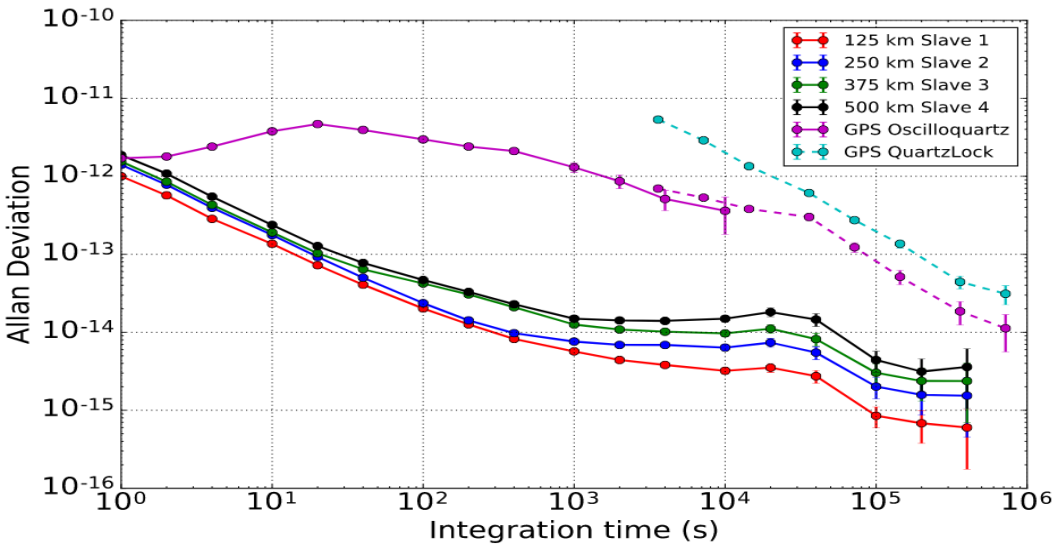
- Very promising results with IDROGEN board
- A new board version (V4) will be designed due to obsolescence of components
- New functionalities will be available in 2024 : Any frequencies generator, 2 channels ADC 1GSPS 14bits, 4 channels 250MSPS 16bits, LVDS parallel bus
- Development efforts are to be focused on low frequencies phase noise
- A lot of improvements are possible on the WR

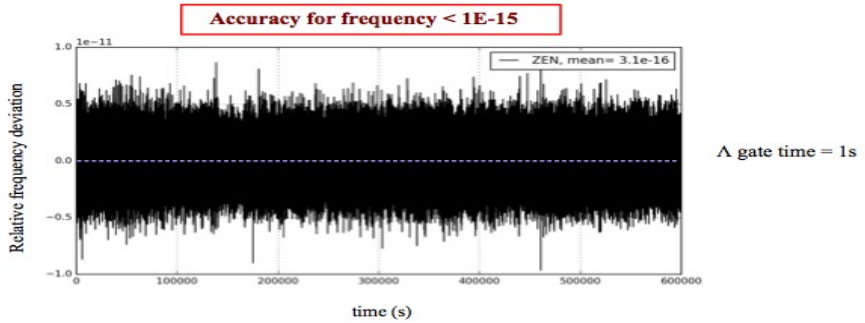
# IDROGEN board



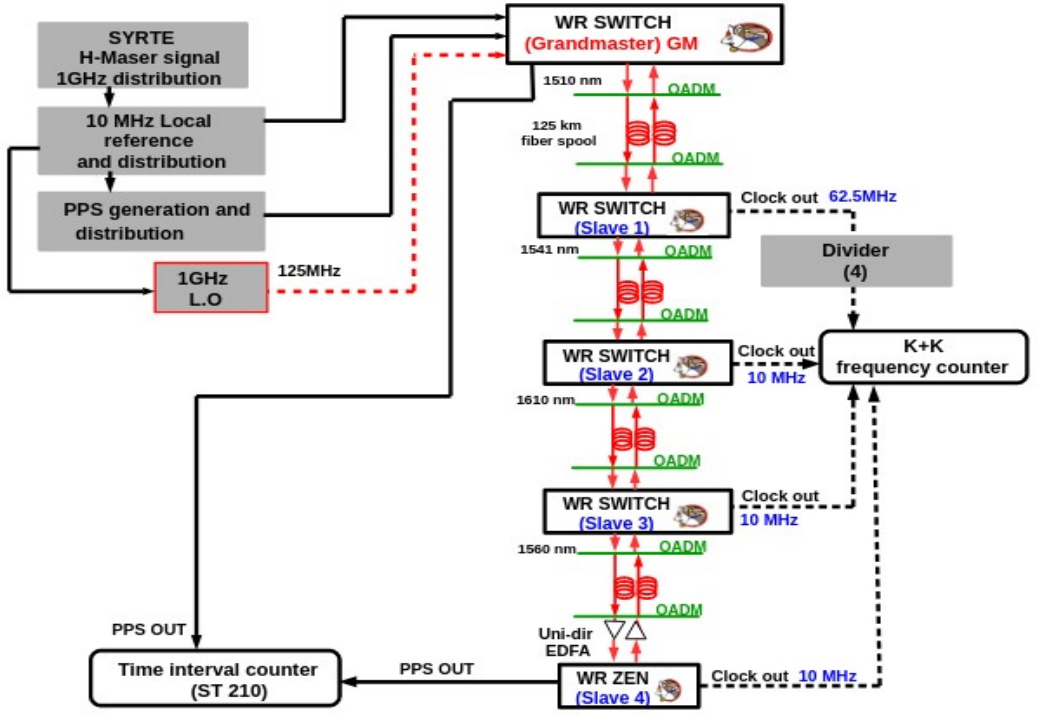

- MTCA 4.0 standard, double width full-size
- Stand-alone mode
- VITA57.1 (FMC+ slot)
- 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant
- Configurable output clock
- Front panel connectivity :
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane connectivity :
  - 1Gbe Ipbus, PCI 4x Gen3
  - IPMB, CLK & trigger lane
  - RTM connector : J30

# WR performance on long distance test

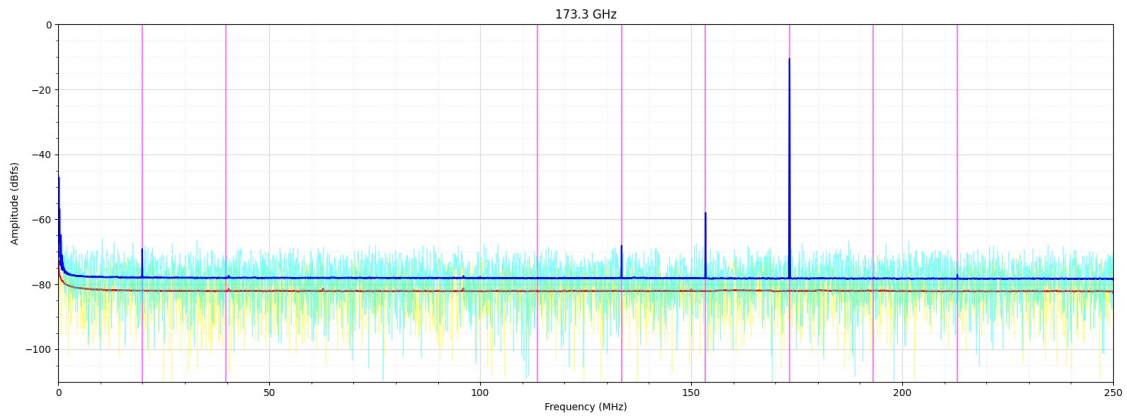


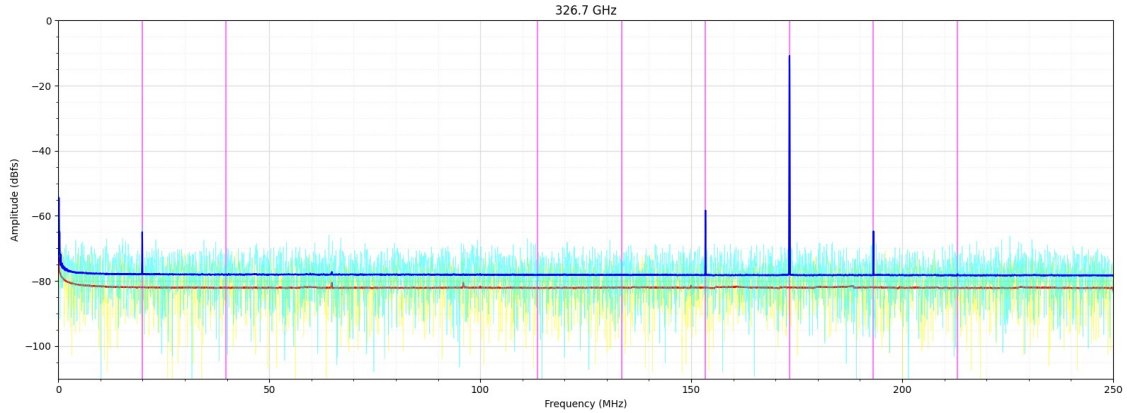



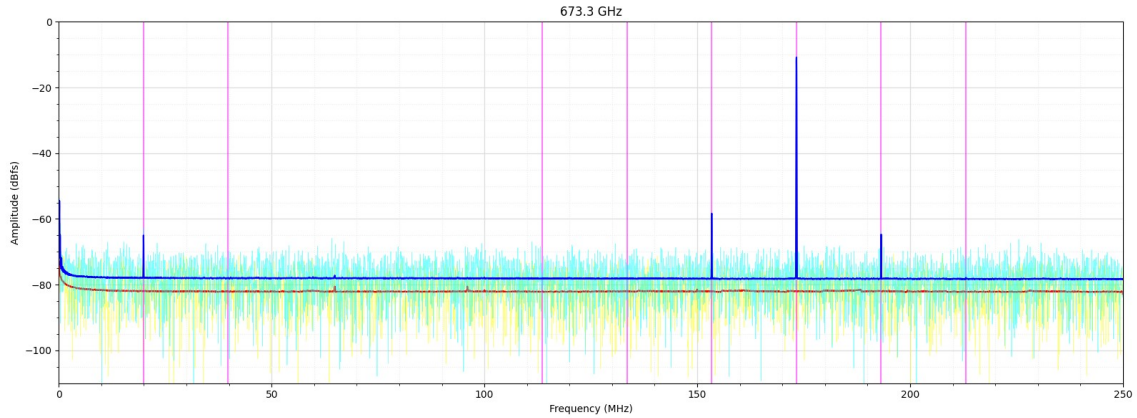

- Better than Oscilloquartz GPS receiver
  - 500Km (4 x 125Km) of fiber
  - Uni-dir fiber
  - 2 OADM (multi wavelength)
- Fiber noise become dominant with the length
  - System disparity, reciprocity of the link



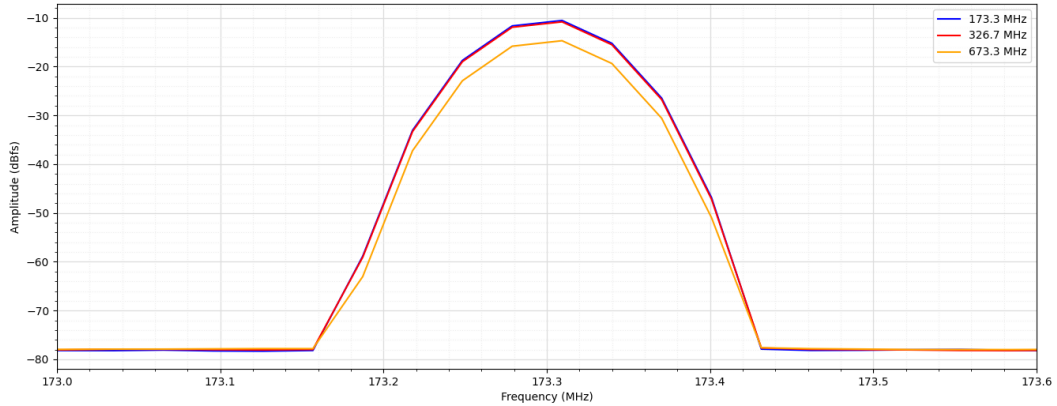
# FMC_AD9680 results




- Blue channel with signal
- FFT 16K, Average over  10000
- First : second , third Nyquist band




- Level of central frequency
- -0,4db on second Nyquist band
- -4db on Third Nyquist band
- Level calibration to be performed