High resolution time measurement on the LHC with the SPIDER ASIC

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AG GDR DI2I

Orsay – June 24th 2024

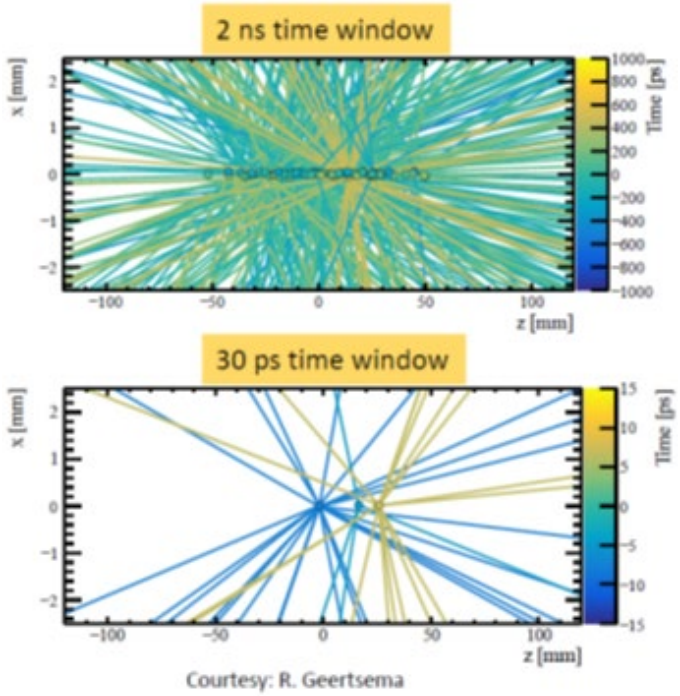
Introduction

- **In the detector R&D community, instrumentation based on fast waveform sampling is widely used**
  - This permits extracting all the possible information from the signal, thus learning as much as possible about the detector
- **Among all existing solutions, modules based on analog memories like DRS4, SAMLONG (WaveCatcher) and SAMPIC offer a few ps rms of time resolution.**
  - SAMLONG and SAMPIC are both originating from IJCLab/IRFU
  - Both act as circular buffers => asynchronous triggering
  - SAMLONG works like an oscilloscope with many channels (like the DRS4)
    - Long sampling depth (up to 1024 samples)
    - Limited counting rate (130 µs conversion dead-time at full depth)
  - SAMPIC works like a TDC which also gives the waveform
    - Short sampling depth (64 samples)
    - Much higher counting rate (1,5 µs maximum conversion dead-time)
  - Fine for many applications but still not sufficient for environments with channel rates >> 1 MHz

Why evoking ps at the LHC ?

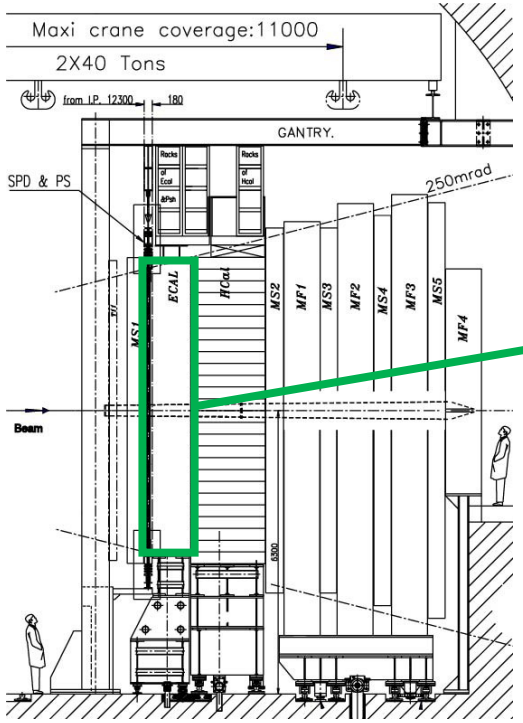
- **With the increase in luminosity, the average number of collisions per event is continuously rising**
  - Event reconstruction is becoming harder and harder due to pile-up in the detectors

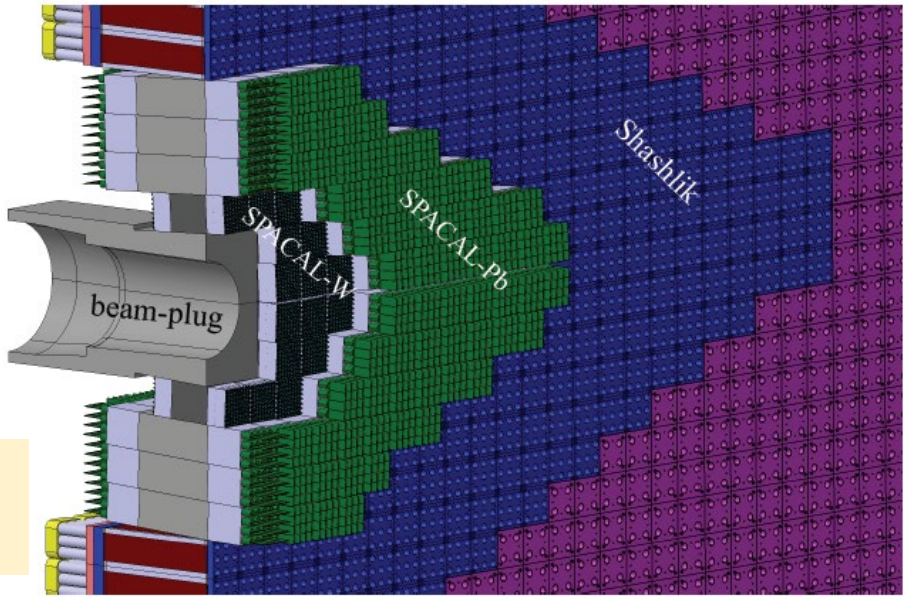
- **One smart way to get rid of pile-up is to precisely tag the signals in time in order to sort them**
  - Due to the length of the bunches, the collision time spreads over ~2ns
  - There can be more than 100 events superimposed over this period
  - Tagging the signals with a time resolution better than 30 ps rms would permit getting back to a few simultaneous events, thus making their reconstruction much easier



Courtesy: R. Geertsema

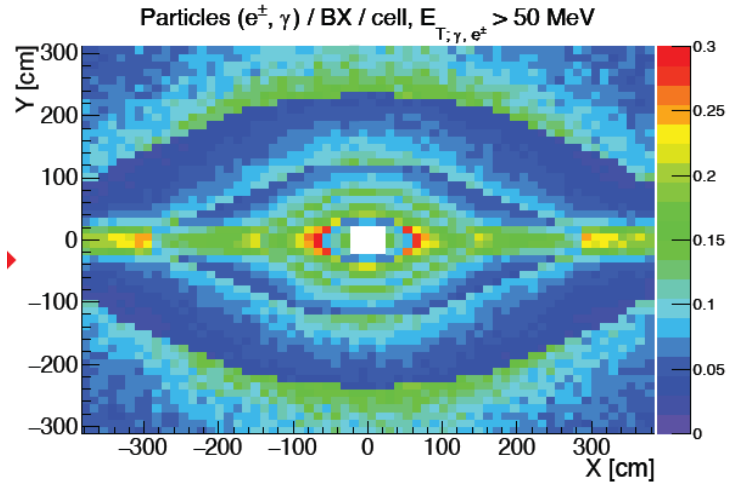
The Ecal of LHcb





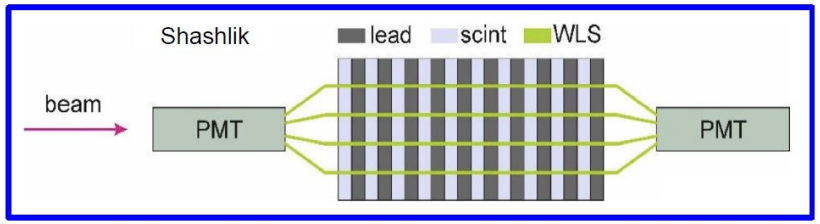
The future UII detector: « **PicoCal** »

- For the phase 2 upgrade, the central part of the detector will be equipped with SPACAL modules to deal with radiation (up to 1MGy).
- Shashlik will remain in the outer part (< 40kGy).
- In order to limit the occupancy, the size of the modules will be reduced thus their number increased
  ⇒ from 6,000 to ~ 15,000 channels
- Introduction of longitudinal segmentation and double sided readout => ~ 30,000 channels (baseline option)

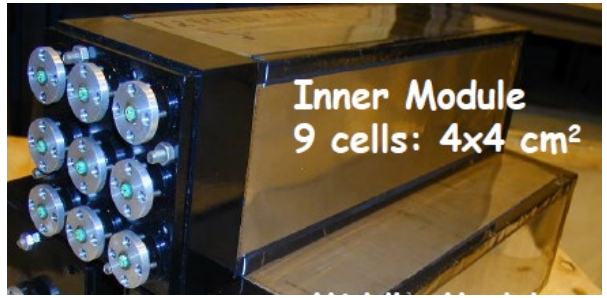


UII detector occupancy

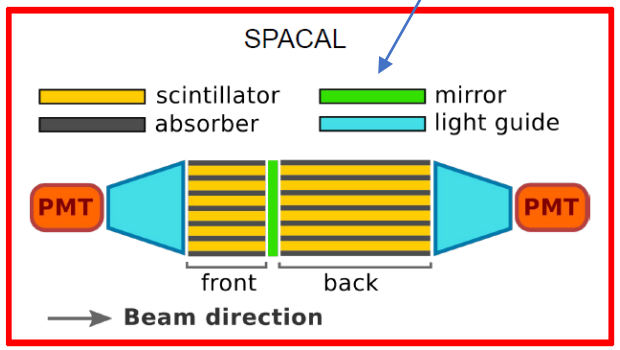
Technologies for PicoCal R&D

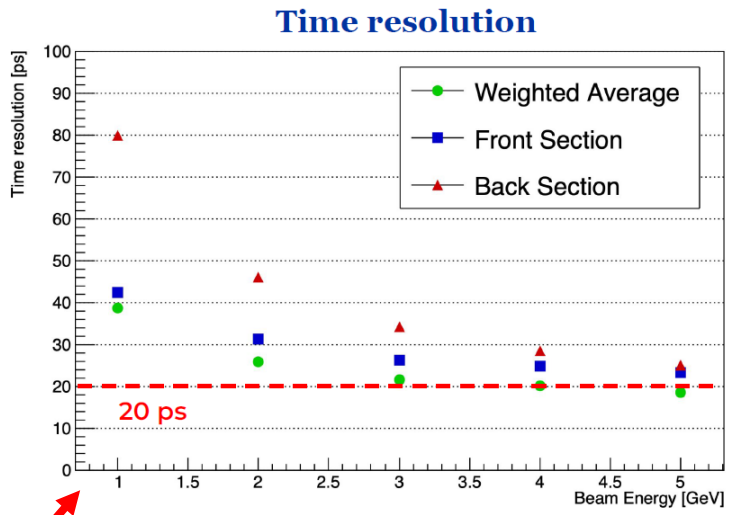


Shashlik
20ps@40GeV

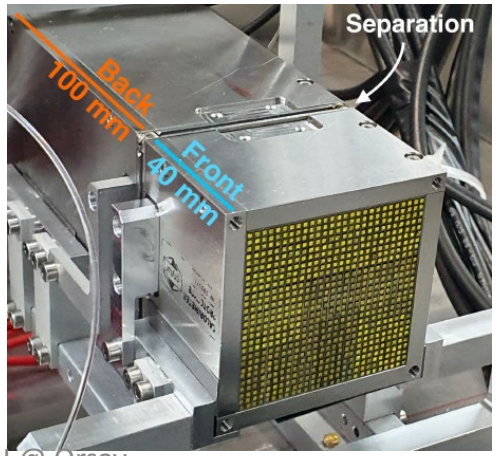


Dedicated timing layer option

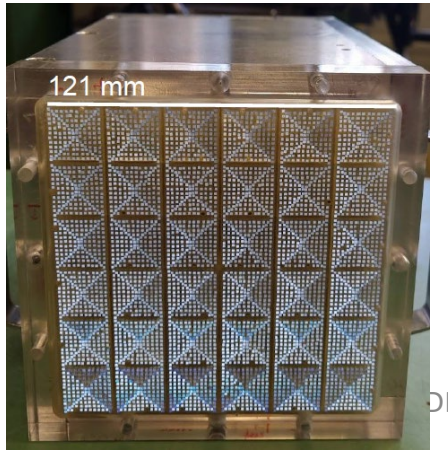




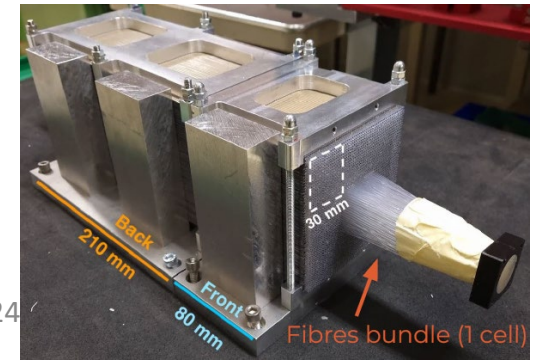
SPACAL W-GAGG
20ps@5GeV



SPACAL W-Polystyrene
20ps@20GeV, 10ps@100GeV



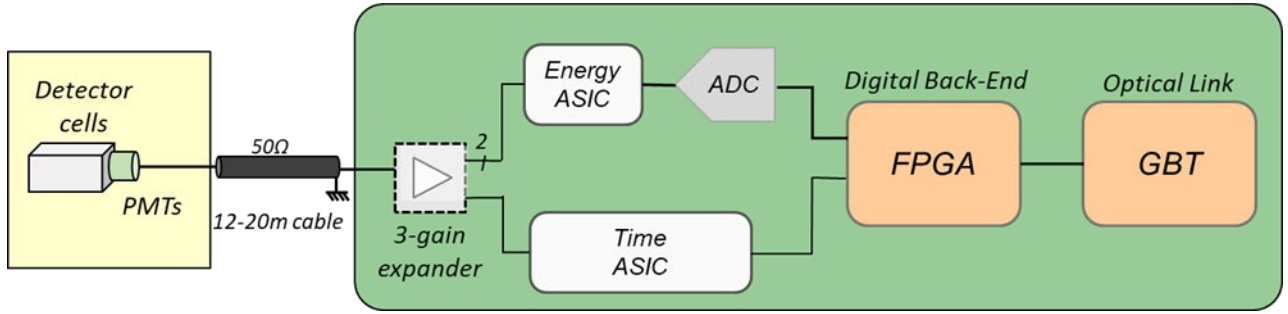
SPACAL Pb-Polystyrene
20ps@20GeV, 10ps@100GeV



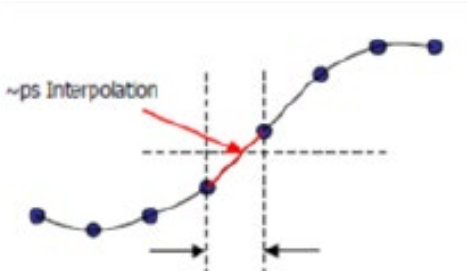
Readout chain for PicoCal

Time channel

- **Requirements**
  - Time resolution target **15 ps for E_T = [1-5 GeV]** to distinguish multiple interactions
  - Rise time between **1.5 ns and 4 ns**
  - Time measurement in range **E_T = [50 MeV - 5 GeV]**
  - Max occupancy up to **50% per channel** (20 MHz time average rate)
- **Time ASIC: Waveform TDC**
  - Associates a DLL-based TDC and a Waveform digitizer based on analog memories
    - TDC -> coarse time
    - Samples -> interpolation (digital CFD) => **few ps resolution**
  - Channels are self-triggered
  - The discriminator is used for triggering (not for timing)
- **Time resolution limit**
  - Detector conversion statistics ($\sim {E_T}^{-1/2}$)
  - Noise contribution ($\sim {E_T}^{-1}$) => constraint on SNR and rise time
  - Conversion on 10 bits and noise < 0.5mV rms

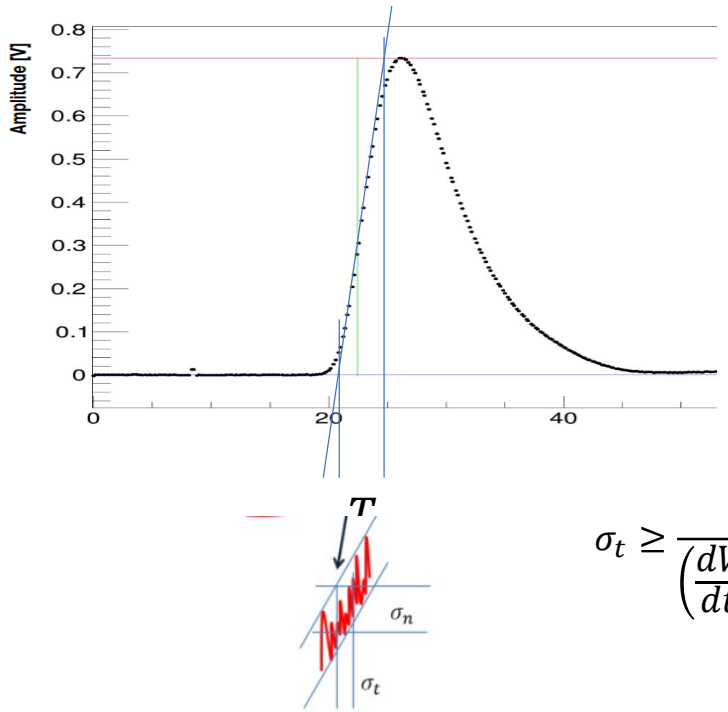


A separate time ASIC permits using it for other detectors or experiments …

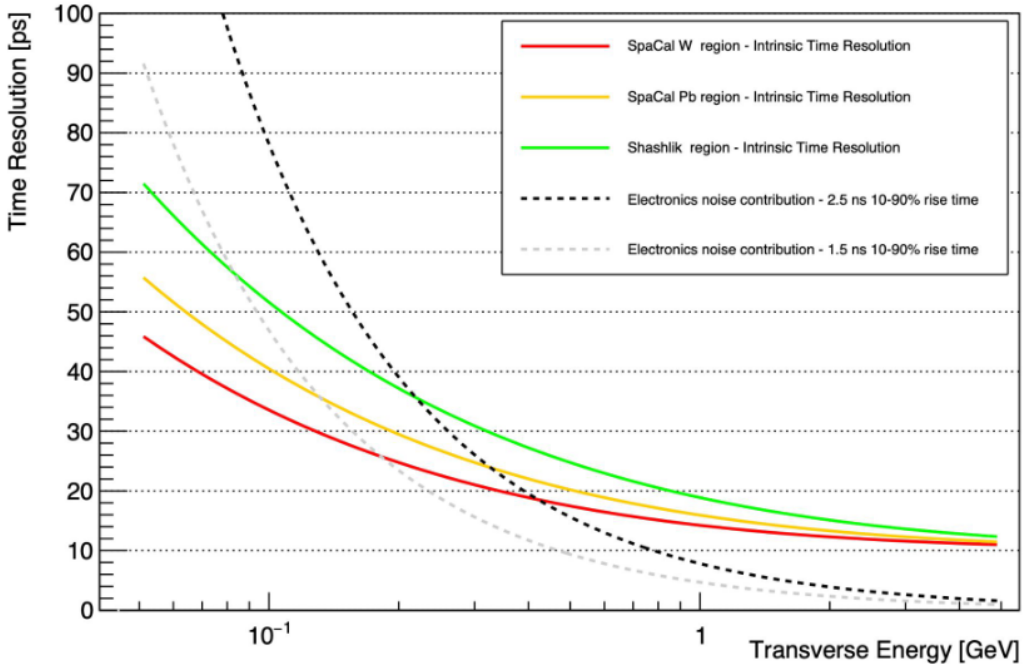


Time channel requirements

- Noise contribution to time resolution
  - Becomes dominant at low amplitude
  - Requires to be minimized (rise time / SNR)



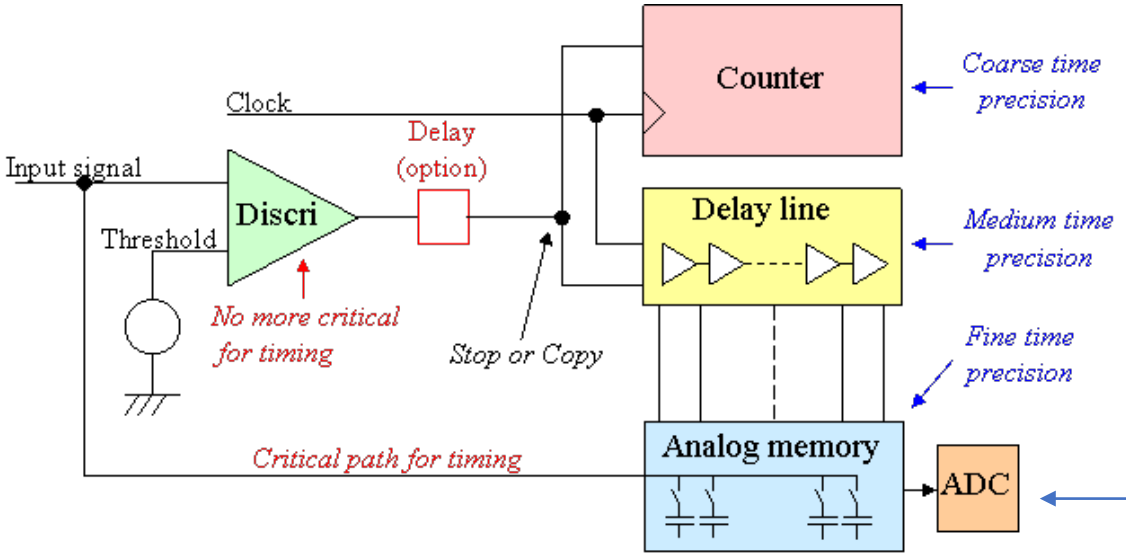
$$\sigma_t \geq \frac{\sigma_V}{\left(\frac{dV}{dt}\right)max} \qquad \sigma_t \geq \frac{T_{LR}}{SNR}$$

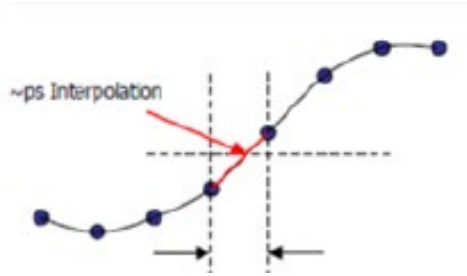


Projections from Loris Martinazzoli
https://indico.cern.ch/event/1392958/contributions/5864189/attachments/2819894/4924126/24-03-14_Martinazzoli_ElectronicsFollowup.pptx.pdf

Waveform TDC

Principle of Waveform TDC: adding an analog memory in parallel with the delay line of a TDC





Interpolation of Waveform samples gives the ps resolution

Wilkinson ADC: massively parallel conversion
But conversion time limits instantaneous rate

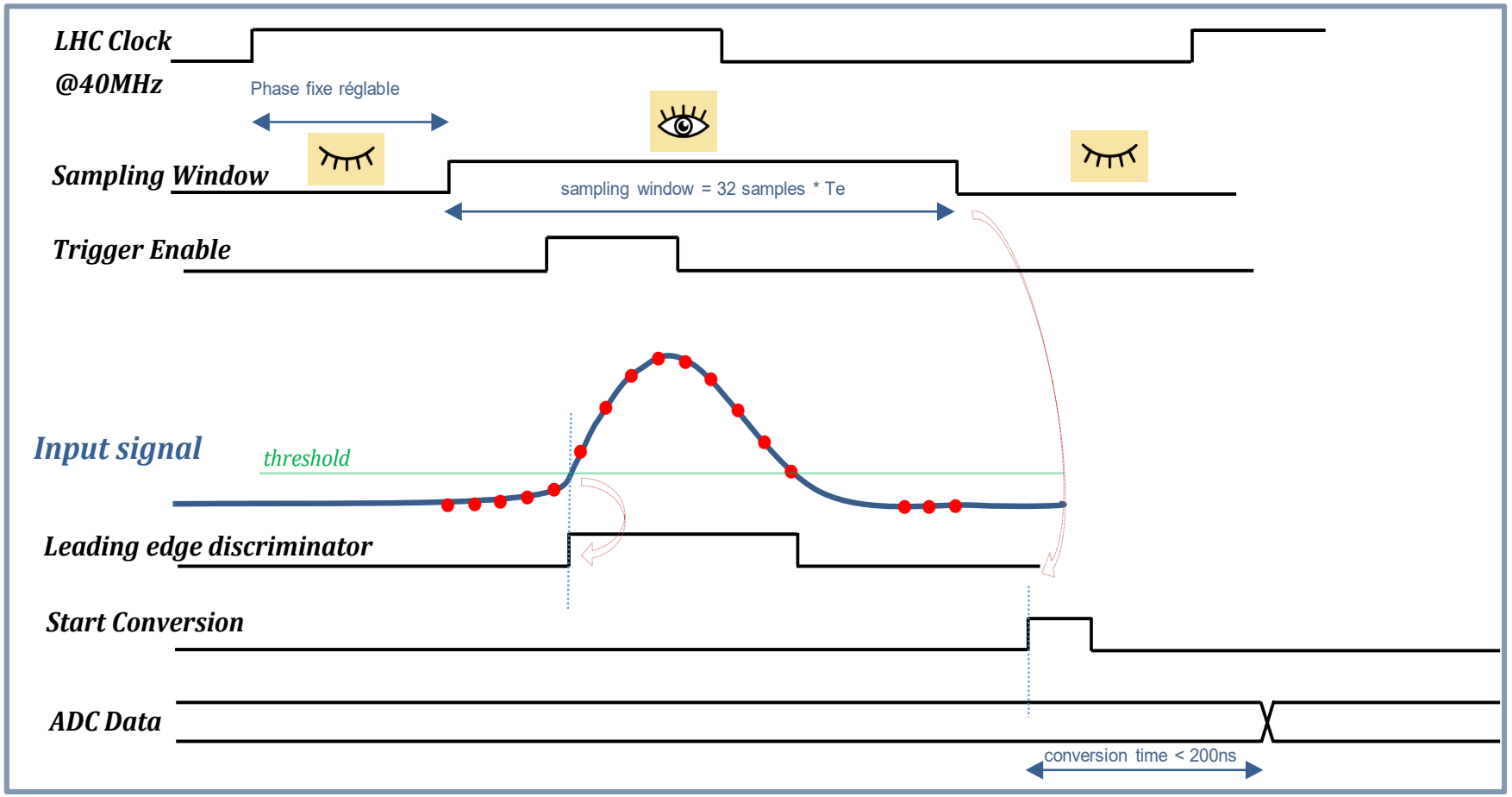
- Reference : SAMPIC digitizer based on **circular analog memory**
- After sampling is completed, A/D conversion time (~ 1 µs) induces dead time

=> Limits count rate to ~1 Mevts/s at best

- Need for a specific architecture to sustain higher count rates

How does SPIDER work …

Instead of being a circular memory, SPIDER finely records the signal during a programmable time slice after each beam crossing



- It takes benefit of the given Time Of Flight between the vertex and each detector cell
- Strong decrease of the number of samples wrt circular memory
- Idea of the “samples of interest”
- Adjustable phases wrt LHC clock:
  - sampling window
  - Trigger enable window

SPIDER specifications

Functional specifications – version “1” (reference with 8 channels)

- Analog sampling of 8 input signals in configurable time window w.r.t. LHC clock
  - Adjustable phase, by steps of 200ps
  - Analog bandwidth compatible with minimal rise time ~250ps => BW >> 1 GHz
  - Sampling period adjustable around : 50ps, 100ps, 200ps, 400ps, 600ps
  - Sampling region of 32 samples
    - Duration: 1.6ns to 19.2ns
  - Individual channel adjustment
- Self-triggered digitization on 10 bits, voltage range 0-800mV
  - Compatible with time resolution <15ps over 160mV-800mV range
- Noise < 0.5mV rms
- Readout can be restricted to a few samples (typ. 8)
  - Built-in “peak finder” locates the analog cell with max value
  - Cells to be read are relative to the peak (smart read)
- On-chip calibration generators

SPIDER main principles

SPIDER : “Swift Pipeline Digitizer”

- SPIDER is a sampler/digitizer working as Waveform TDC optimised for **synchronous** signals in **high rate** conditions
  - Signals have predictable phase *w.r.t* to clock
  - **Count rate capability** limited by **A/D conversion** and **readout** phases => both must be optimized

Main elements:

1. Reduce conversion dead time to increase instantaneous count rate: **8-bank memory**

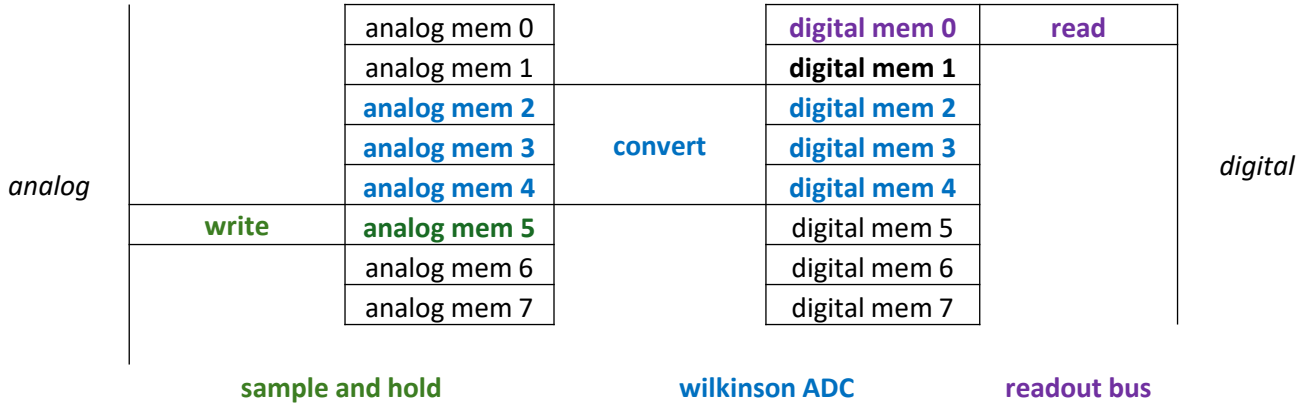
- Possible to write new events in next banks during conversion of previous banks
- Pipelined operation (write, convert, read)

2. Limit the **total number** of memory cells (physical constraint) : sampling restricted to the region of interest => **32 cells**

3. Average count rate still limited by sequential readout time => **only read 8 samples** (full rising edge) for dCFD algorithm in FPGA

Simultaneous operation

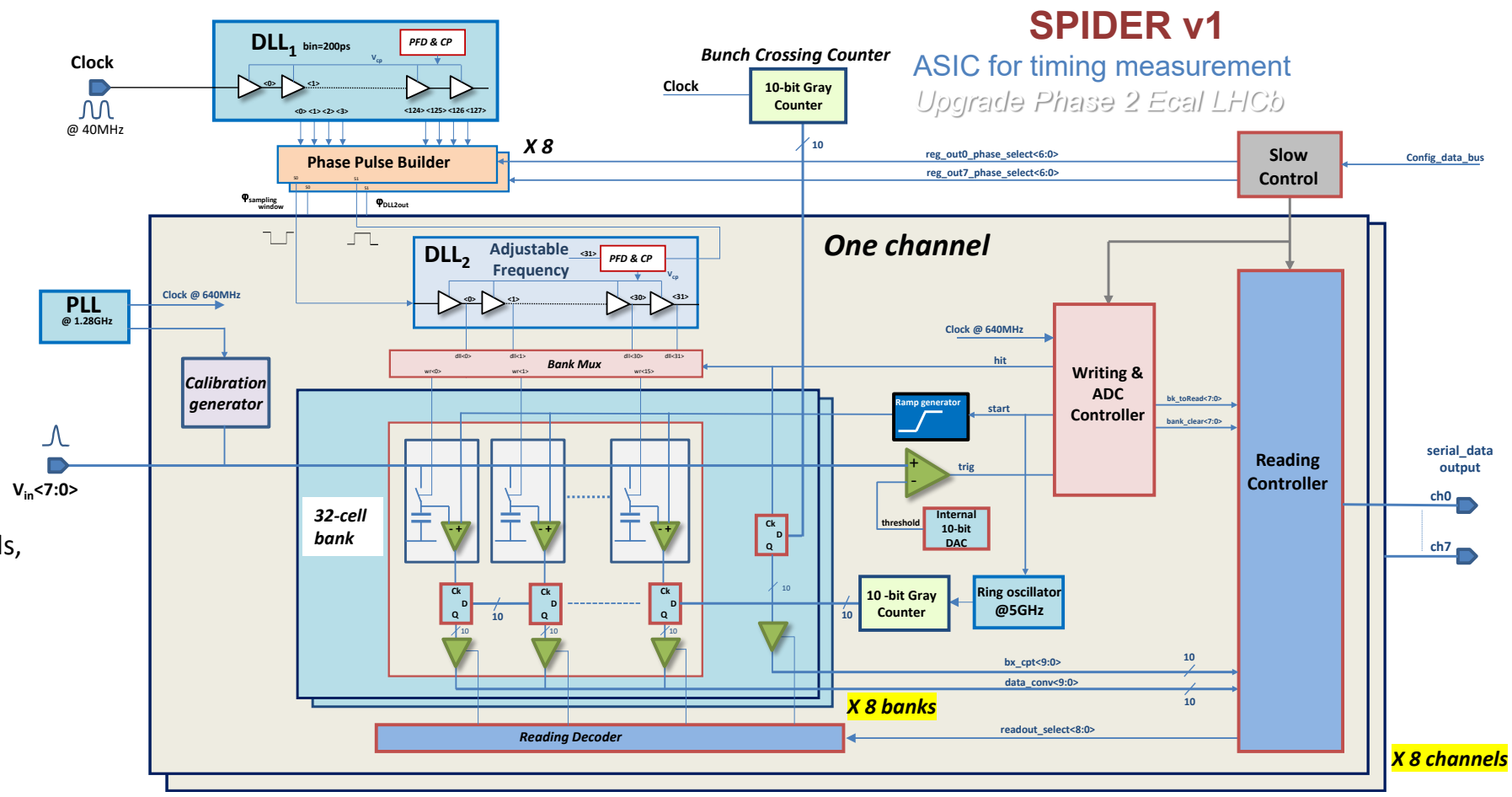
- Write 1 bank
- Convert n banks
- Read 1 bank



SPIDER architecture

Architecture specifications – version 1 (8 channels)

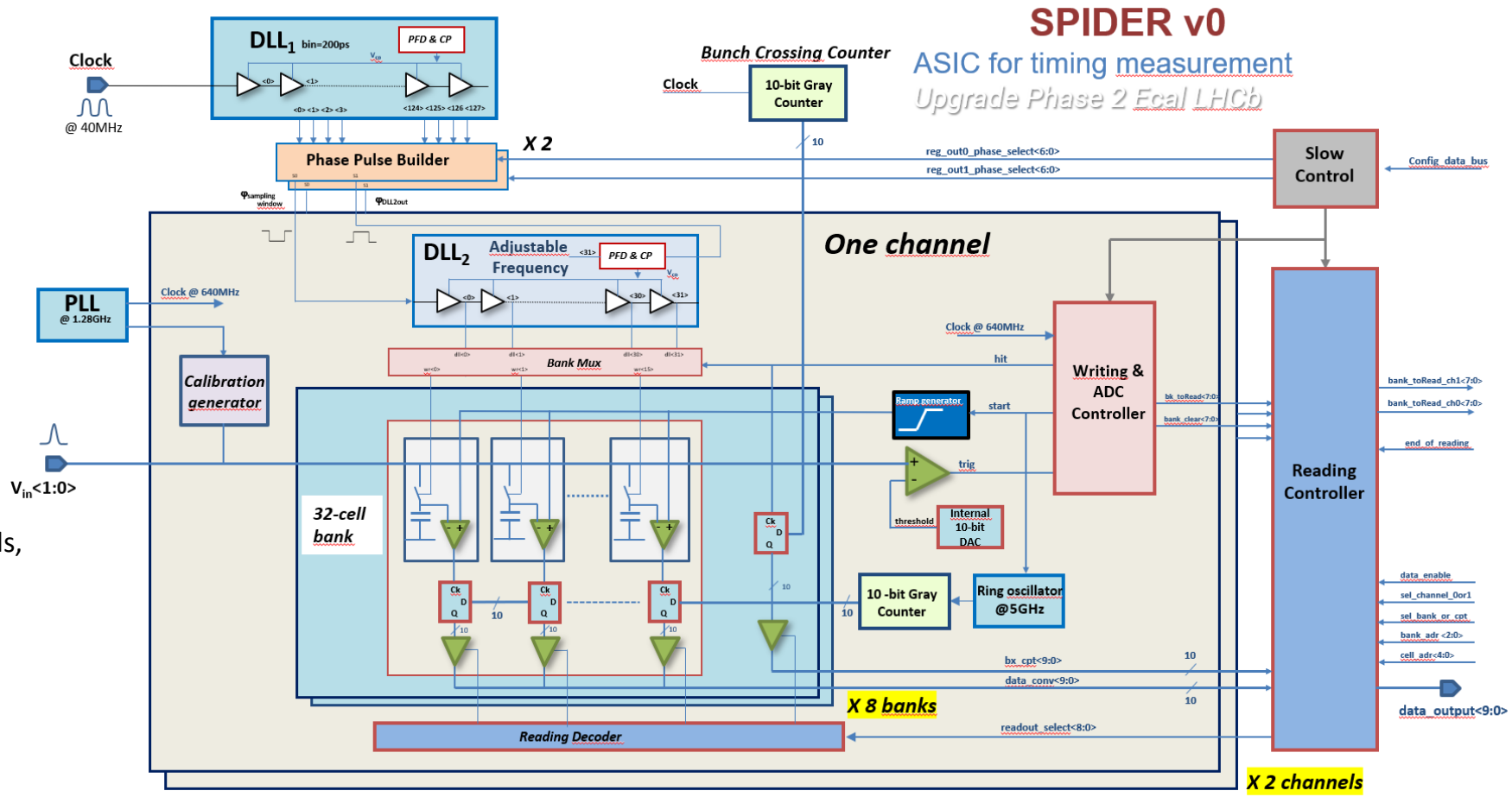
- TSMC 65nm, VDD 1.2V
- 8 self-triggering channels
- Clock distribution & DLLs
- Memory cell
  - Sample & hold, Wilkinson ADC
  - Noise < 0.5 mV
- Multi-bank system
  - Derandomization buffer
  - 8 banks of 32 cells, sequencing logic
- ADC 10-bit Wilkinson @5 GHz
  - Fast counter to limit conversion time (max 200 ns for 10 bits i-e 8 LHC periods, for 800 mV signals)
- PLL and DAC + buffer for calibrations
- Serial readout interface
  - Digital buffer
  - Up to 2Gb/s per channel, ASIC-driven ("push" mode)



SPIDER first prototype

Architecture specifications – version 0 (2 channels)

- TSMC 65nm, VDD 1.2V
- 2 self-triggering channels
- Clock distribution & DLLs
- Memory cell
  - Sample & hold, Wilkinson ADC
  - Noise < 0.5 mV
- Multi-bank system
  - Derandomization buffer
  - 8 banks of 32 cells, sequencing logic
- ADC 10-bit Wilkinson @5 GHz
  - Fast counter to limit conversion time (max 200 ns for 10 bits i-e 8 LHC periods, for 800 mV signals)
- PLL and DAC + buffer for calibrations
- parallel readout interface
  - Simplified logic
  - FPGA-driven (“pull” mode)



Specifications are complete for v0 and v1 at system level

Some features could be added to next versions (slide 14)

SPIDER collaboration

- "Projet R&T" @IN2P3 2021-2023 to be extended to 2029 (*RS: P. Robbe & RT: C. Beigbeder*)
- Co-coordinators for SPIDER ASIC design *: B. Joly & P. Vallerand*
- Organisation in 7 WPs
- Project submitted in 2021 for 3 years
- Regular meetings
- Prototype 0 to be submitted in November 2024 for ~50 k€, tests in 2025

IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis

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- R. De Neeff
- J. Maalmi
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lpc caen

- L. Alvado
- L. Leterrier

iP2I LES 2 INFINIS LYON

- E. Béchetoille
- H. Mathez

Development status

- Prototype v0 in layout and verification phases
- Manpower:
  - Design ~6 FTE
  - Test (hardware + firmware + software + analysis) ~4 FTE from 2025
- Design status
  - Design
    - Analog part : 90%
    - Digital part : 90%
  - System simulations (mixed and transistor-level) : 60%
  - Layout
    - Manual : 50%
    - Digital flow : 90%
- Test benches
  - 2 test benches foreseen for 2025, design started @ IJCLab and LPCA

Design & verification methodology

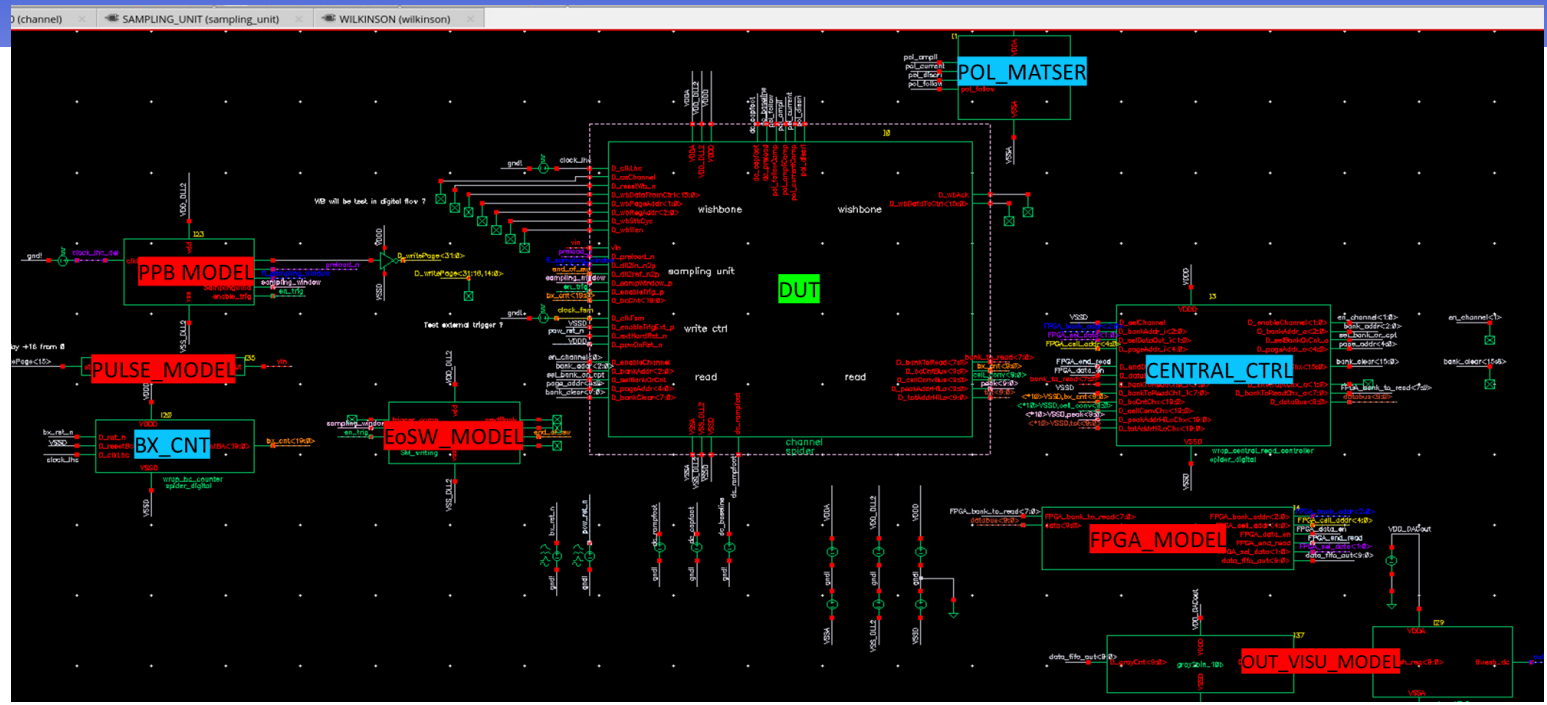
- Complex design => high risk of critical fault
- Analog on top methodology chosen for v0 (top cell is schematic as well as a large part of the design)
- Thorough verification strategy required at *cell level* and *system level* with simplifications
- Test bench (TB) per design cell
  - schematic or digital
  - Post-layout

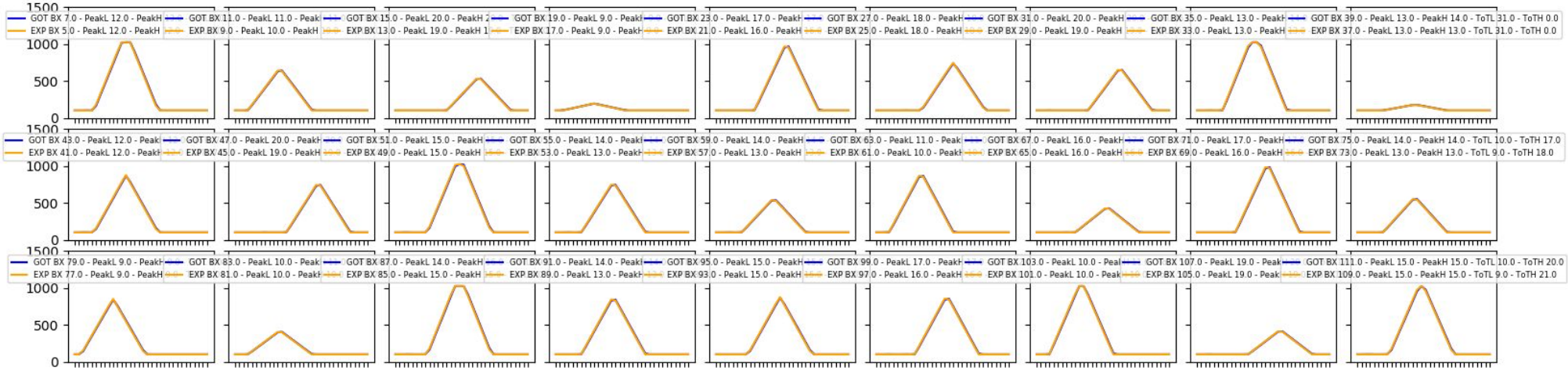
simulation	Device under test		
	hierarchy	top view	sub-cells
analog	cell	schematic, post-layout	
digital	cell	verilog, SystemVerilog	
analog / mixed	subsystem	schematic, post-layout	
digital	subsystem	verilog, SystemVerilog	
analog/mixed	channel / top cell	schematic	schematic, Verilog-A(MS), Verilog, SystemVerilog
digital	top cell	SystemVerilog	Verilog, SystemVerilog

- Digital TBs per subsystem (slow control, readout…)
- Mixed TBs for sampling subsystem
  - Sampling cell, bank, full array of 8 banks => schematic or post-layout
  - Behavioral models for environment (DLL, Wilkinson counter…)
- Full system verification
  - **UVM (Universal Verification Methodology)**, **digital-oriented**, in SystemVerilog, with "Real Number Models" (discrete time, continuous values) for analog parts
  - **schematic**, **mixed** TB for "**channel**" (achieved) and for **top view** (next step) with behavioral models for some cells (Verilog-A, Verilog-AMS) or functional models (Verilog, SystemVerilog)

Channel test bench

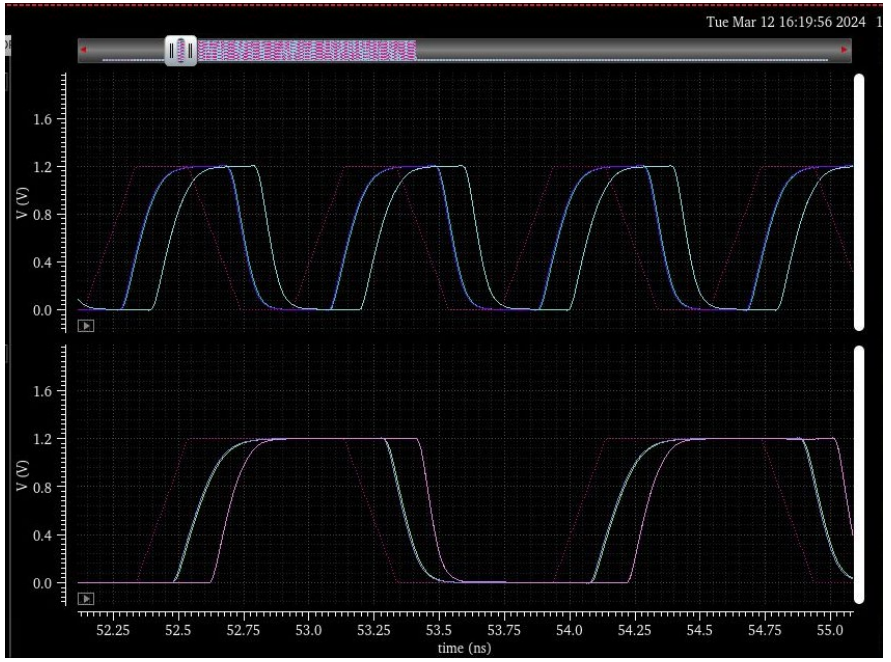
- **Behavioral** models designed for some blocks (internal and environment)
- Check multi-bank operation (write, convert, read)
- Schematic-level verification of sampling array
- Signal amplitude and time with random distributions.
- Checker cell for automatic comparison of expected data *vs.* digital output => match
- Validates the functionality of sampling, conversion, readout in full mode and “smart read” mode (8 samples) with peak finder

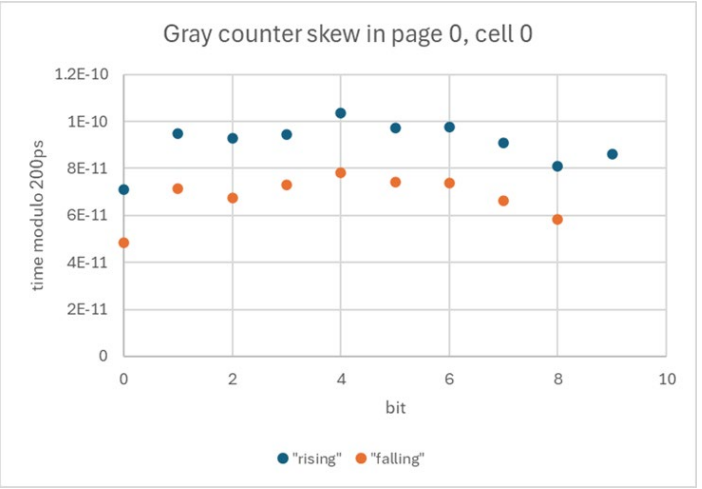




Layout design & post-layout simulation

- 1 channel => 32*8 = 256 sampling cells
- Length 2.8 mm
- Channel layout designed in bottom-up order, many hierarchical levels
- Post-layout simulations required (signal integrity, timing, couplings)
  - Ex : Gray counter bus (10 bits) => skew between bits must be << 200 ps
- Ongoing : optimizations to reduce power consumption, current transients on VDD



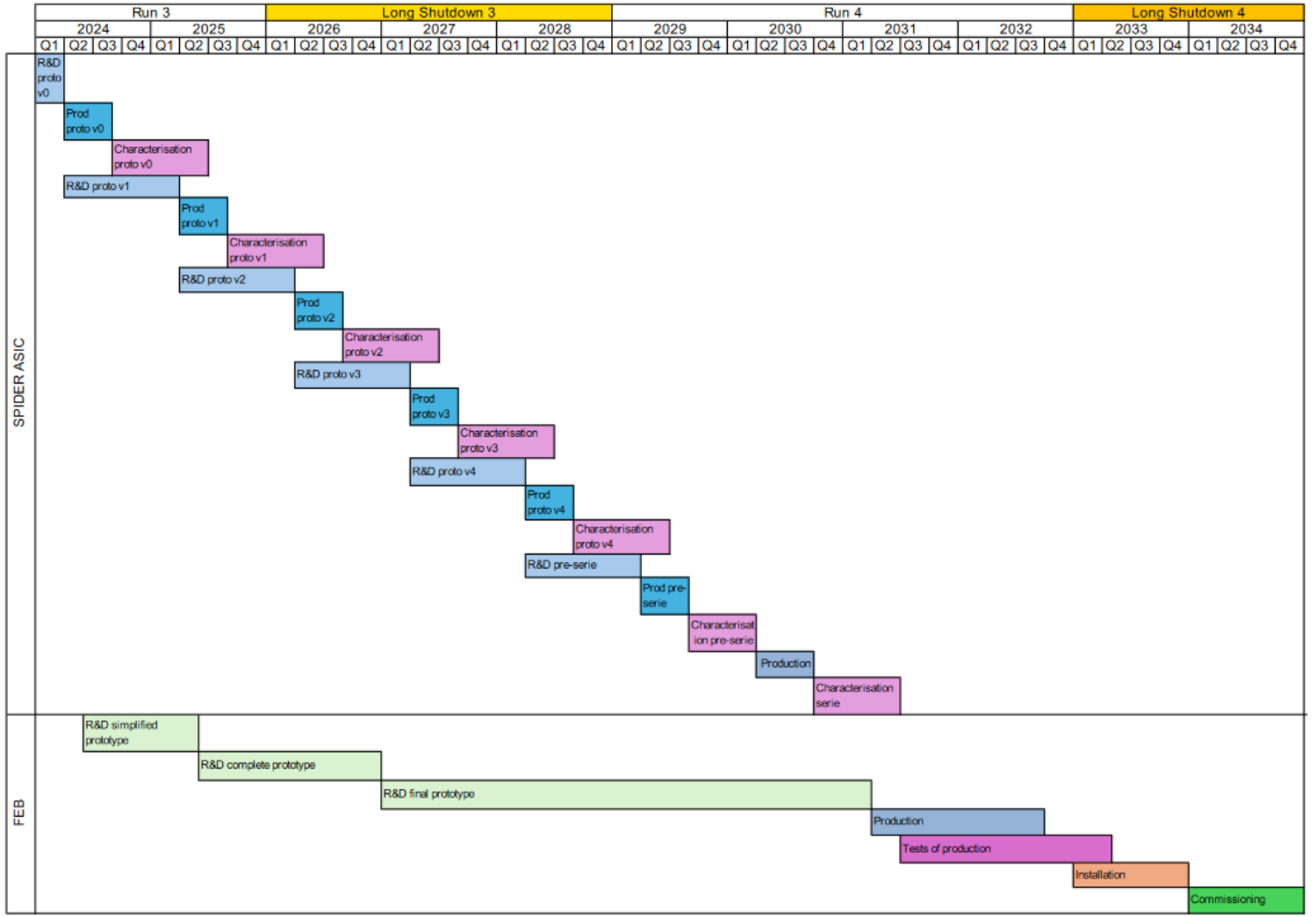


Development schedule

Basis: ~1 engineering run per year 2024-2029

2 x 2-channel and 3 x 8-channel prototypes

- SPIDER V0 (2 channels prototype), design 2023-24, test 2025
- V1 if required (2 channels prototype with corrections) design 2025, test 2026
- V2 (8 channels + radiation tolerance),
- V3 (8 channels + radiation tolerance + optimisations),
- V4 (+ target « yield »),
- 2028: V4 validation ; preproduction design,
- 2029: preproduction characterisation,
- 2030: SPIDER production (30k channels), Front-end card production
- 2031-2032: Card production and test
- 2033: installation
- 2034: commissioning



Path for future developments

- Increasing the counting rate
  - Reducing conversion time (or go to 16 banks)
  - Reducing frame size (64 bits per event @ 40 MHz => 2,56 Gb/s per channel)
    - On-chip dCFD => on-chip INL calibration
    - Data compression
    - …
- Evaluating differential input: potential gain (x2) on input voltage range but less on SNR => design of a differential memory cell
- Using the 32 samples for simultaneous time and energy estimation => ultimate resolution to be evaluated
- SPIDER will be usable with any kind of fast detector on a 40 MHz collider.
  - We target the best possible time resolution
  - The latter will directly depend on the signal rise time

Thank you for your attention

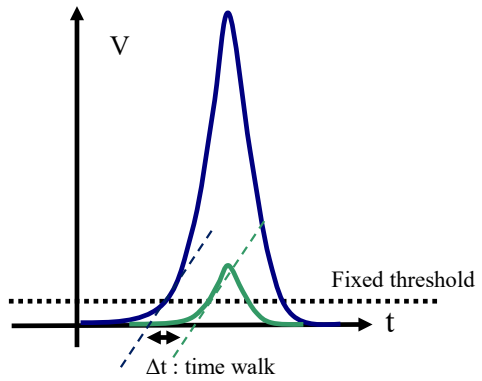
Questions ?

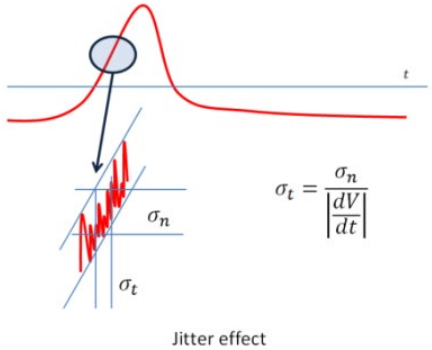
Backup slides

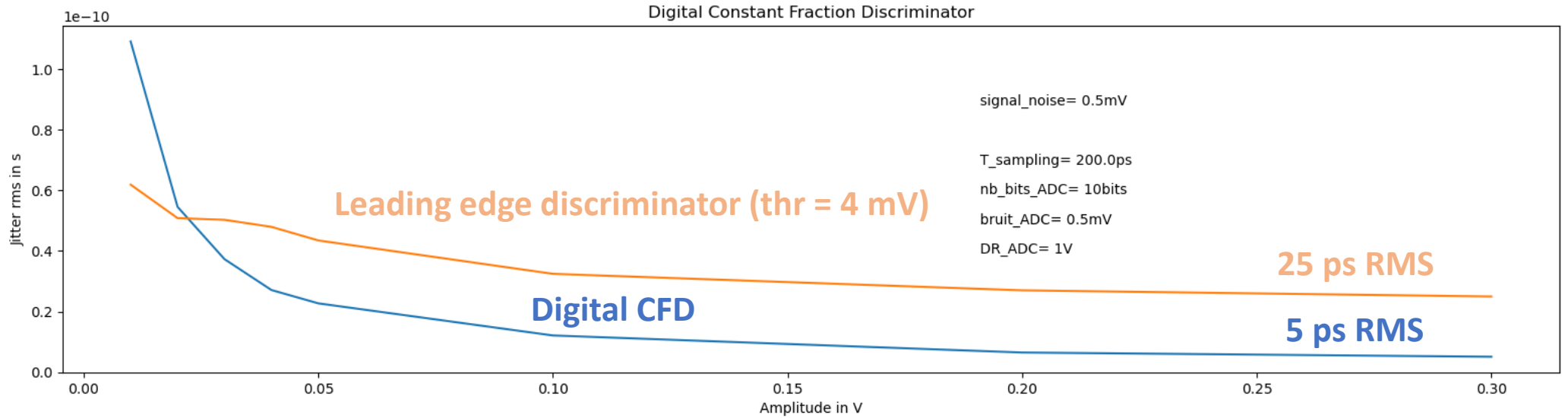
Digital CFD vs fixed threshold + TDC

Time jitter vs signal amplitude for large dynamics (100)

- **Example** : rise time (10-90%) = 1 ns ; σ_{noise}= 0.5 mV RMS
- Voltage range : 10 mV to 1 V
- **dCFD**: σ_{time} < 15 ps over large dynamic range
  - Quantization error on low signals
- Even with ideal time walk correction, leading edge discriminator is affected on large signals by non-optimal threshold (constrained by smallest signals)







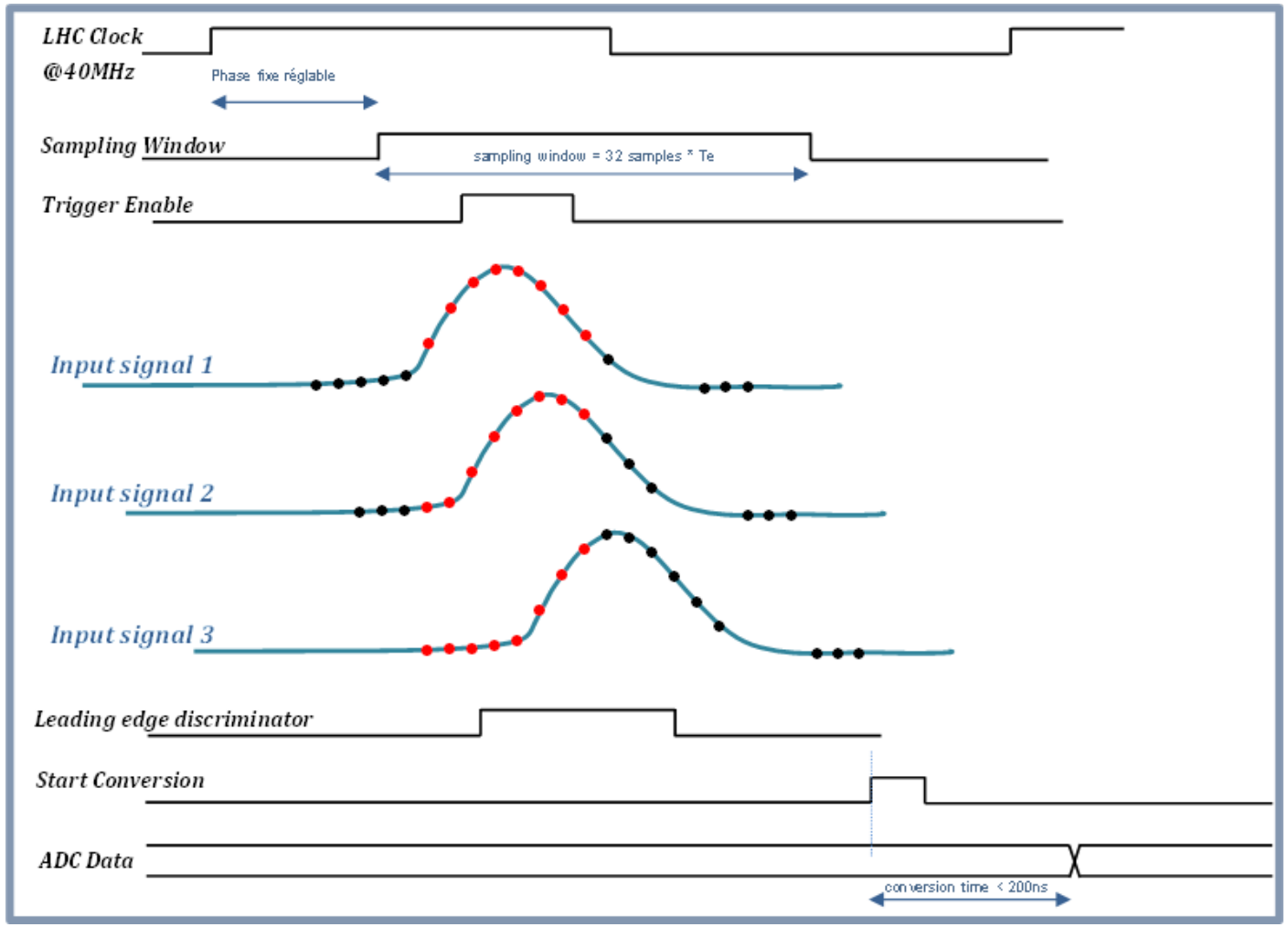
Peak finder

Recent improvements: peak finder

- Input signals from collisions have a fluctuating phase wrt LHC clock due to TOF
- Problem: need for limiting to 8 samples to reduce data throughput

=> need to optimally cover the rising edge for dCFD

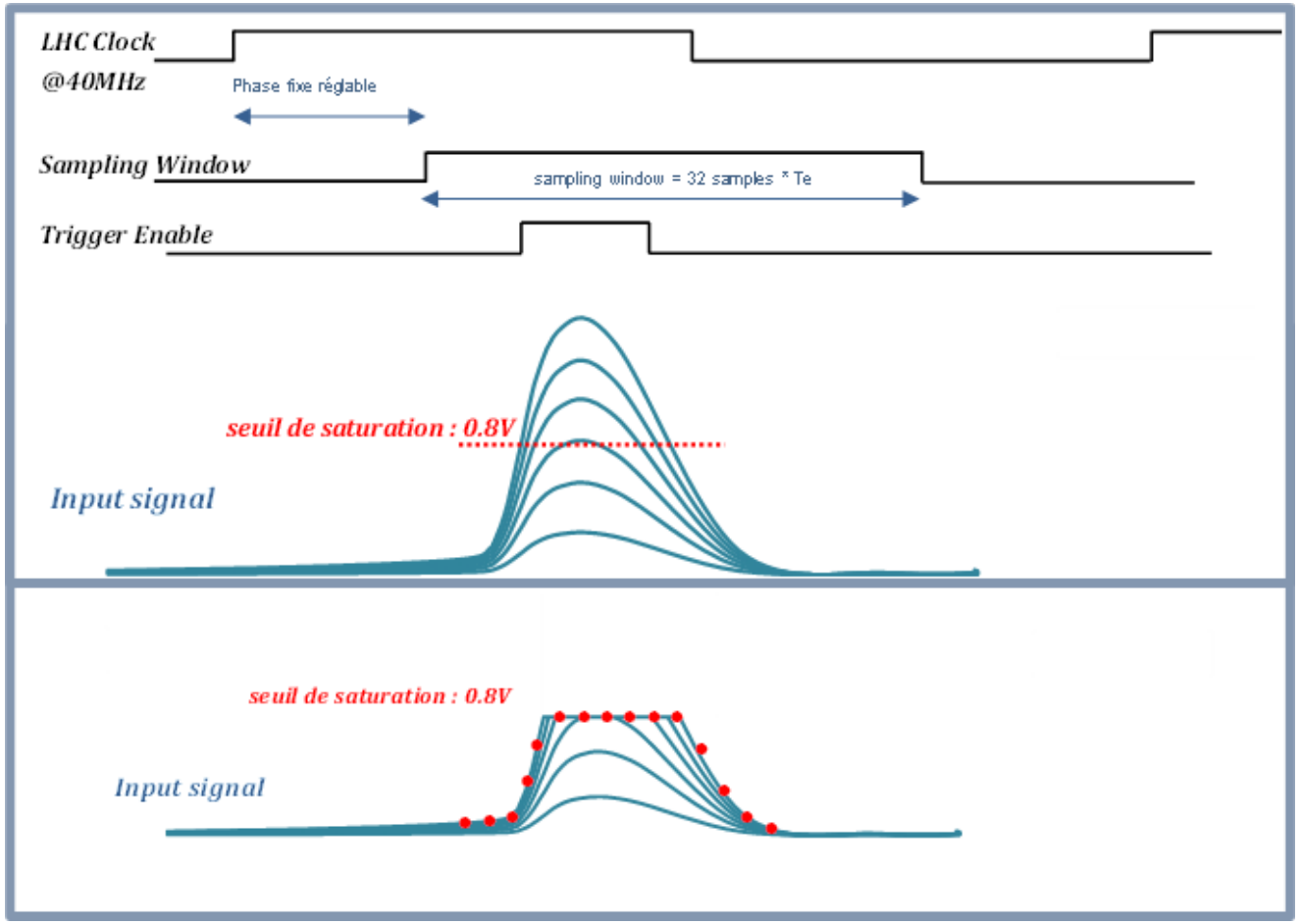
- The “peak finder” determines the address of peak sample
  - Reference for the 8 useful samples address



Dealing with saturation (1)

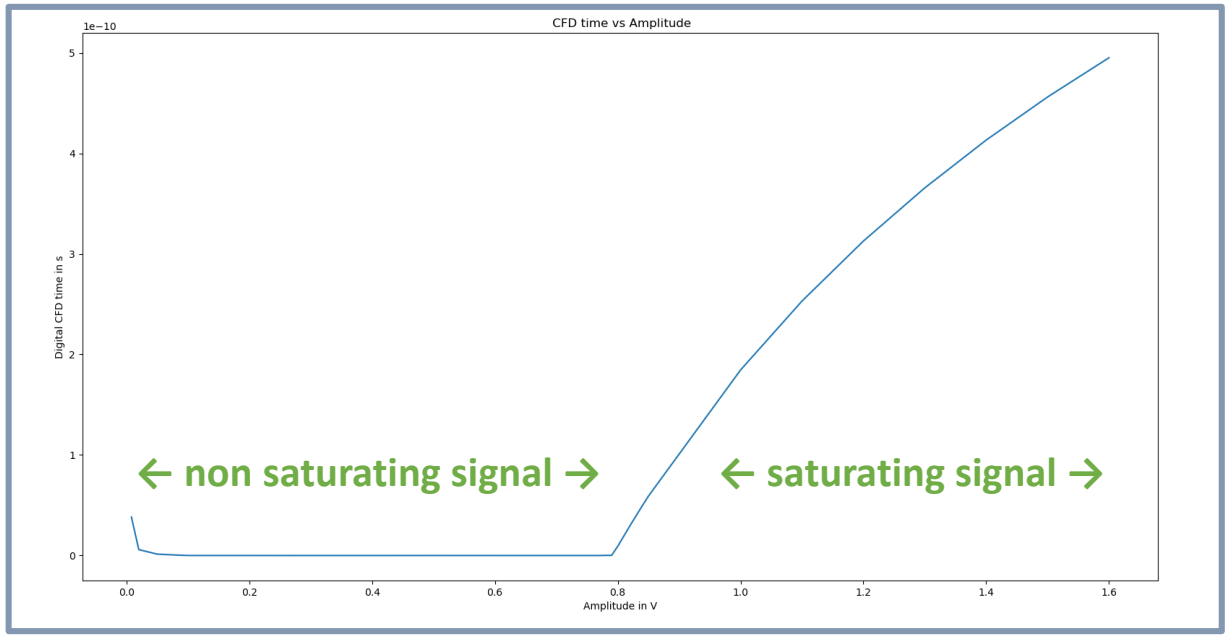
Recent improvements: saturated cells

- Digital CFD not directly valid for saturated signals
  - Timing threshold becomes constant
- Energy can be used to correct for time walk of saturating signals
- Nb of saturated cells can be used to correct for time error
- Logics implemented to extract saturated cell addresses (min-max)



Dealing with saturation (2)

Recent improvements: saturated cells



Walk error ~500 ps for true amplitude 0.8V to 1.6 V

Walk error reduced to ~20 ps after compensation (2nd order polynom based on nb of saturating cells)