News from CMOS Sensors: MIMOSIS and CE-65nm

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eurizon European network for developing new horizons for RIs

AIDA innova

Slides are courtesy of M. Deveaux

News from MIMOSIS

A. Besson, M. Deveaux, Ziad EL BITAR for the CBM-MVD collaboration

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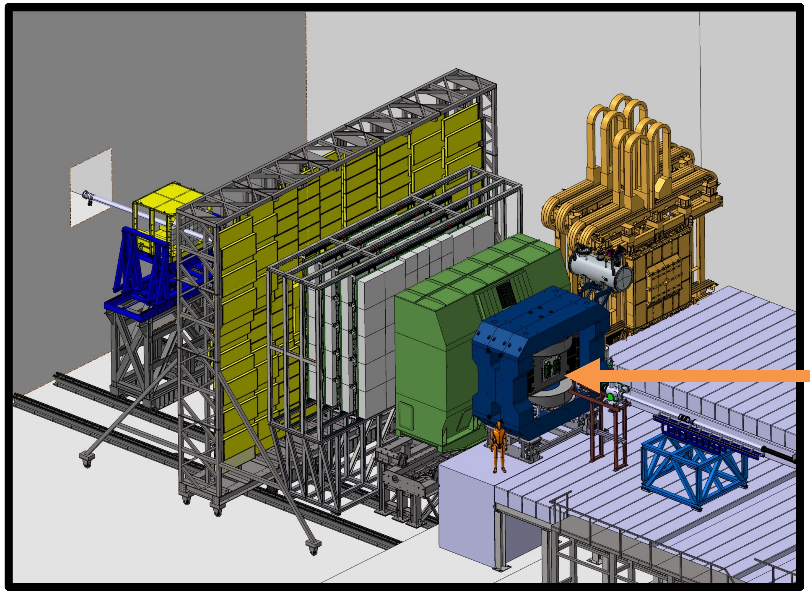
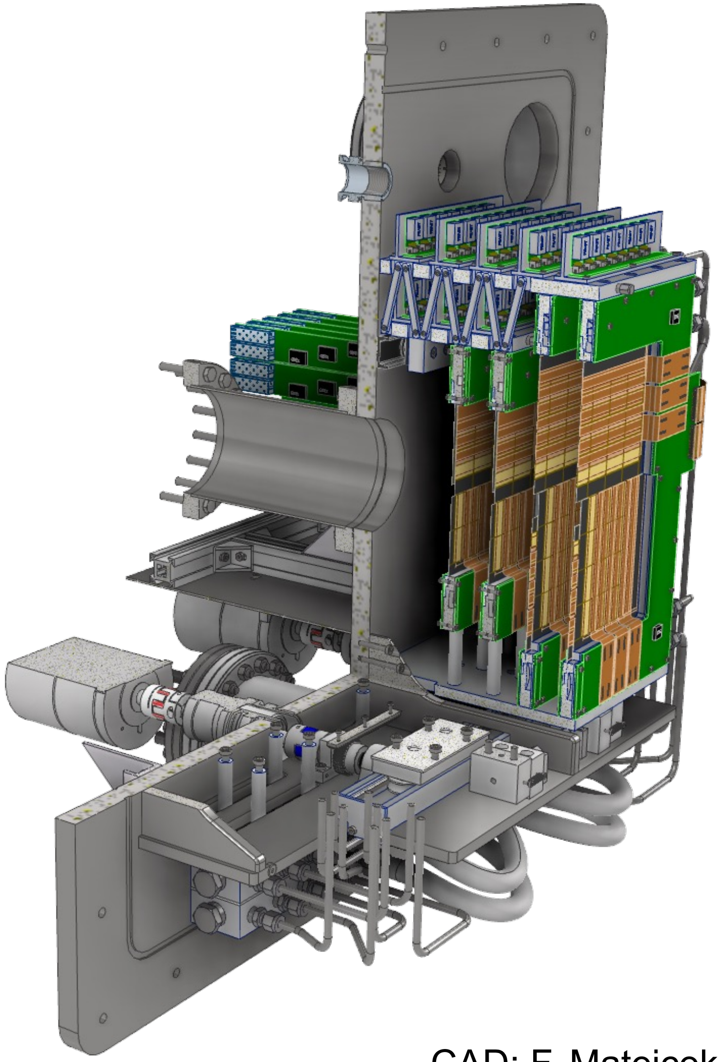
Measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)





CAD: F. Matejcek

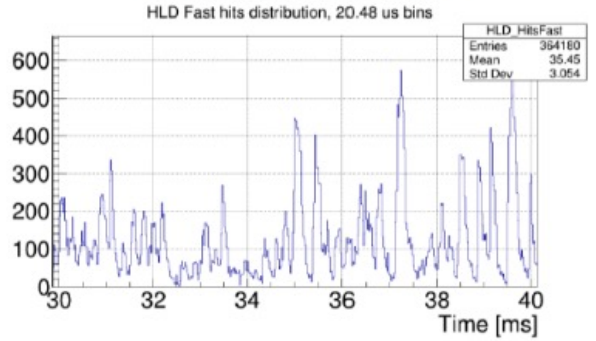
Missions for the CBM MVD:

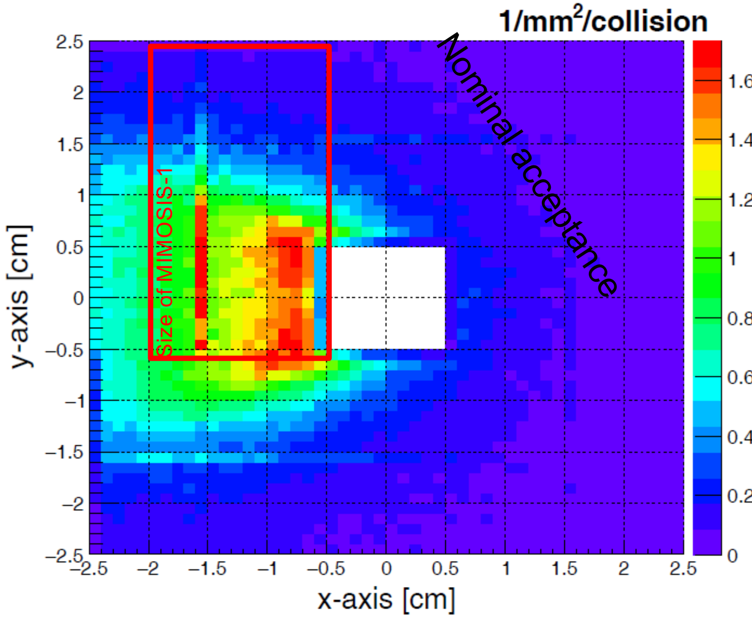
- Low-momentum tracking.
- Conversion electron suppression.
  → Vector meson reconstruction.
- Hyperon reconstruction.
- Open-charm reconstruction.
- High particle rates => Max. 10 MHz p+ p
  100 kHz Au+Au

Requirements on the sensor

	Requirements
Spatial, time resolution	~5 µm, 5 µs
Sensor thickness	~ 50 µm
Power dissipation	<100 mW/cm²
Radiation doses	7×10^{13} n_{eq}/cm² ~ 5 MRad
Radiation gradient over sensor	~ 100%
Heavy ion tolerance	1 kHz/cm²
Rate (average/ 50 µs peak)	20 / 80 MHz/cm²

kHz modulation ON





MIMOSIS-0 (2018)
- Demonstrate pixel concept. ✓
- Demonstrate zero suppression. ✓
- Demonstrate readout concept. ✓

MIMOSIS-1 (2020)
- Full dimension sensor ✓
- Add buffer structure. ✓
- SEE hardening 1/2 ✓

MIMOSIS-2 (Q2/2023)
- On-chip pixel grouping.
- Final pixels.
- SEE hardening 2/2

MIMOSIS-2.1 (Q2/2024)

MIMOSIS-3
- Final sensor for mass production

In synergy with:
eurizon
European network for developing new horizons for RIs

Add features
Fix issues
Design optimization

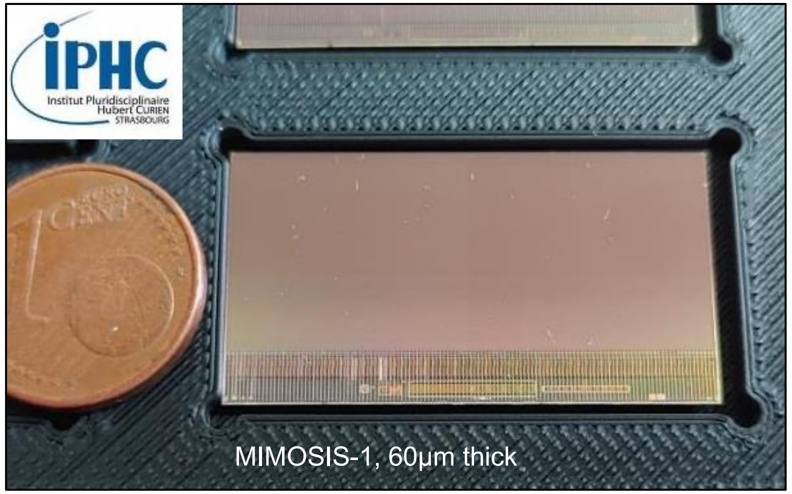
Add features
Fix issues
Design optimization

Fix issues

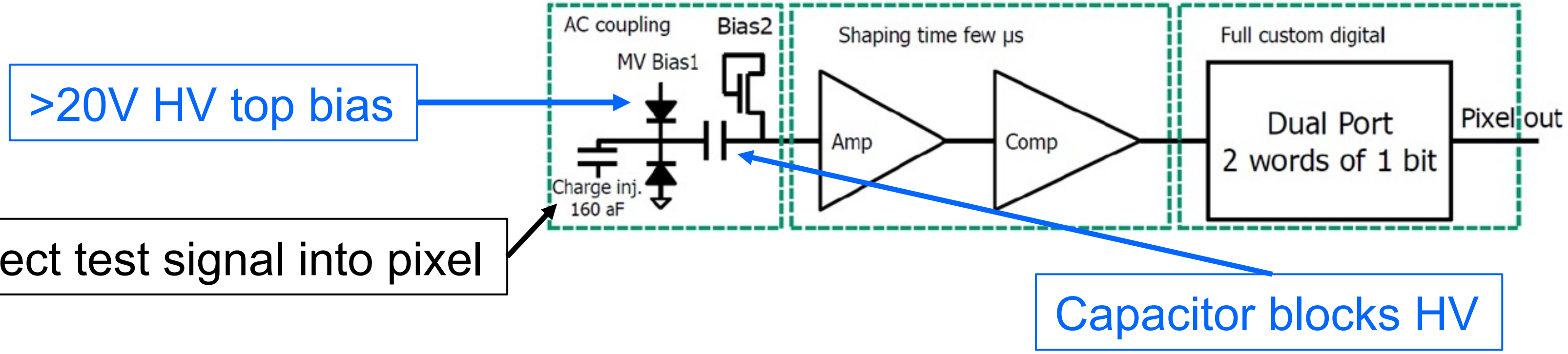
We are here

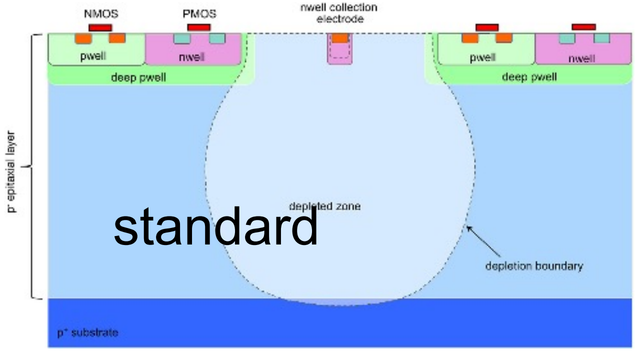
Final design choice
Fix issues

MIMOSIS, the sensor for the MVD (inspired by ALPIDE)



Size: 504 x 1024 pixels (27x30µm²), 5µs time binning
Full integrated: 20 MHz/cm² (80 MHz/cm² for 35µs), ~70mW/cm²
Fully depleted: >20V top bias

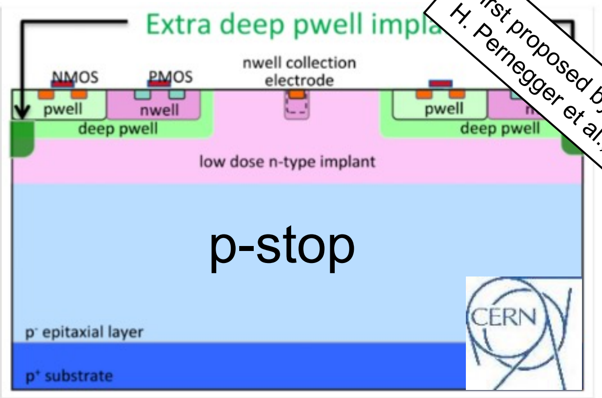




Standard

Known from ALICE/ALPIDE

+ Radiation hardness
- Spat. Resolution



First proposed by W. Snoeys et al.
H. Pernegger et al., 2017 JINST 12 P06008

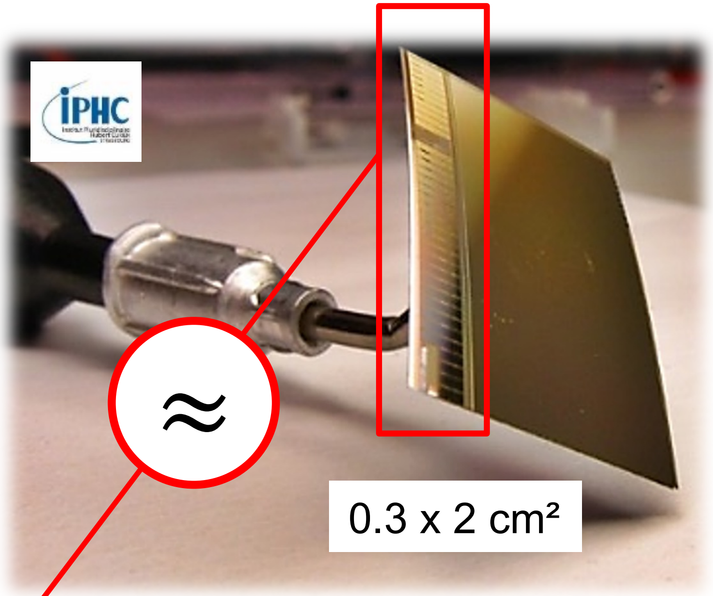
Rad. hard, candidate 1

Epitaxial layer thickness: 25µm, 50µm (new => reported today).

How to control 500’000 channels?

MIMOSIS integrates:
- Analog & Digital FEE
- Voltage regulators, trim DACs.
- Slow control interface.
- Data pre-processing.

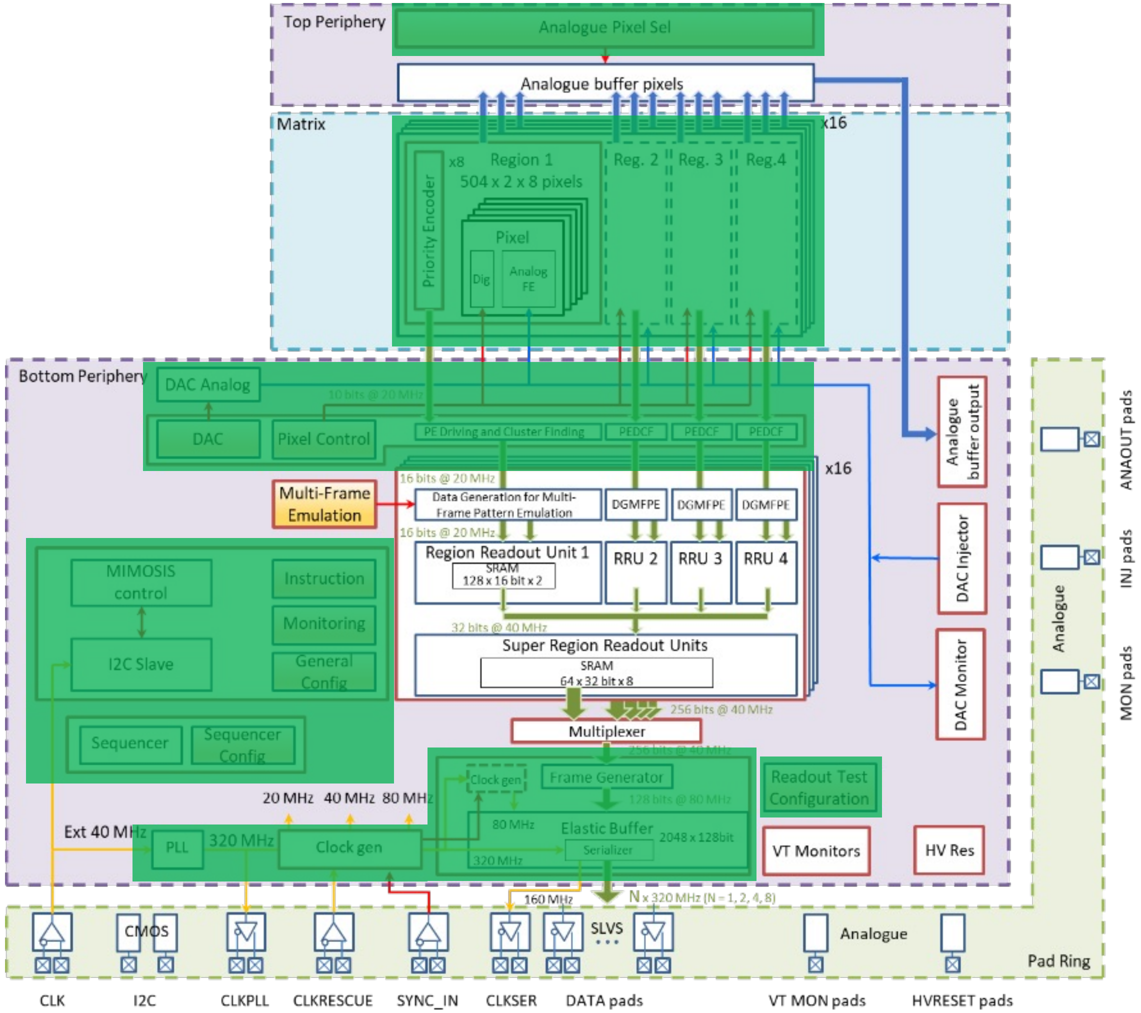
…



MIMOSIS is an unusually complex piece of technology, also during R&D.

Reworked blocks in MIMOSIS-2

(F. Morel @ Mimosis sensor perspectives and next steps towards the CBM-MVD
https://indico.gsi.de/event/15130/)

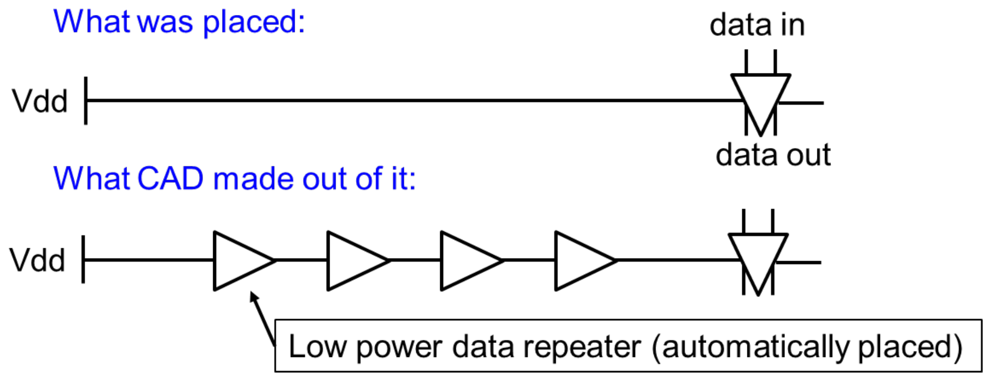


MIMOSIS-1 and MIMOSIS 2 follow the same outside specs but:

- Major features added.
- Majority of all blocks reworked.

⇒ High risk submission

Bug example: Output driver powering issue:



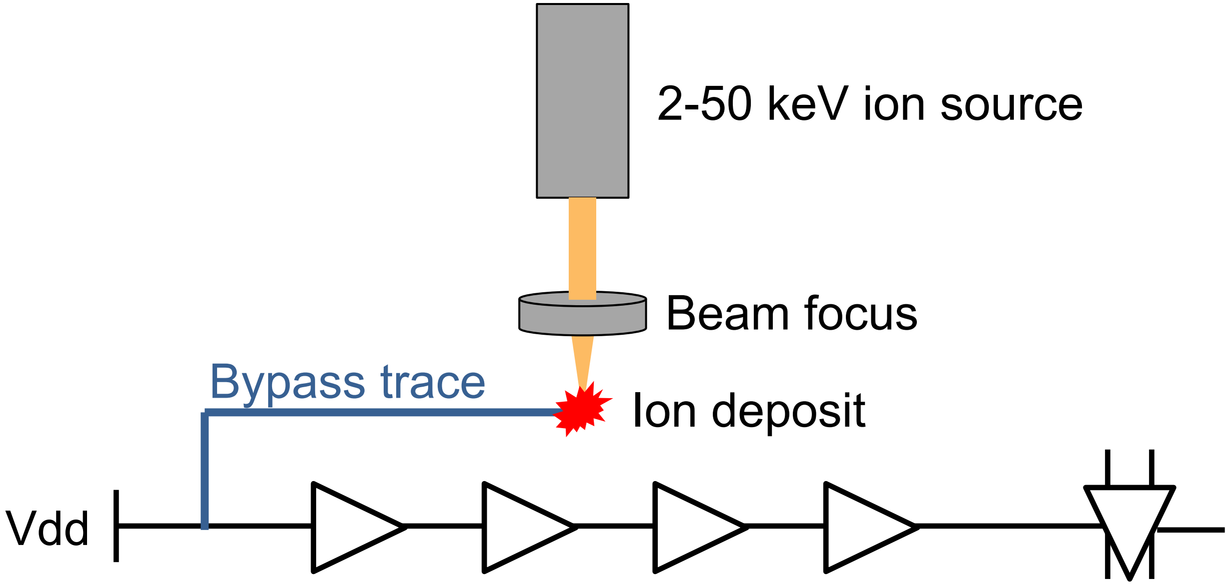
Status Sept. 2023:

- 3 bugs spotted, fixes under evaluation.
- Resubmission required for full bug fix.
- Updated test plans accounting for MSIS-2 limits.

Fight the issues…

Focused ion beam (FIB):

- Ion deposit in existing ASICS allows to add/cut traces.
- May be used to correct for bugs (equivalent to soldering cables on buggy PCB).



Limitation:

- Space constraints.
- Individual ASICS only.

FIB used on 5 sensors to confirm bug repair strategy.

Sept 2023: “FIB corrected MIMOSIS-2 will plausibly allow to test a significant part of the open questions…”

MIMOSIS-2 test results (by Dec. 2023)

Scheduled test	Test possible despite bugs?	Test result
Sensor performance	No	MIMOSIS-1 matches specs.
I2C issues (multiple)	Yes	OK
Analog output failure	Yes	OK (next talk)
Vulnerability to HV pickup	Yes	OK (next talk)
Vulnerability to HI-impacts	Yes	Q1-2 2024 (UNILAC beamtime)
Clk triplication	Restricted	So far ok.
PLL stability	After FIB	Improved, still too much jitter
Cluster finding	After FIB	OK
Pixel to output data transfer	After FIB	OK
Power grid (ohmic loss)	Restricted, after FIB	OK (but only few pixels)
…		

New

Validated bug fixing strategy.
MIMOSIS 2.1 submitted Dec. 2023.

Effect of heavy ion hits on electronics

Heavy ions show high d*E*/dx or LET:

- Scales with z^2 of the projectile => Au = 6200 M.I.P
- Bethe Bloch: "Slow" ions create higher LET than relativistic ions.

Minority charge carriers excited by ions may:

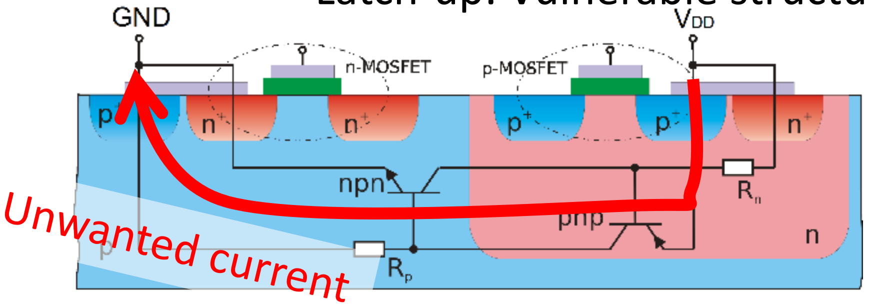
- Break transistor gates => Gate rupture — **Irreversible destruction**
- Switch digital electronics => Bit flip — **Malfunction if ignored**
- Open unwanted conduction paths => Latch-up (like short cut, extinguish by power cycle) — **Thermal destruction if ignored**

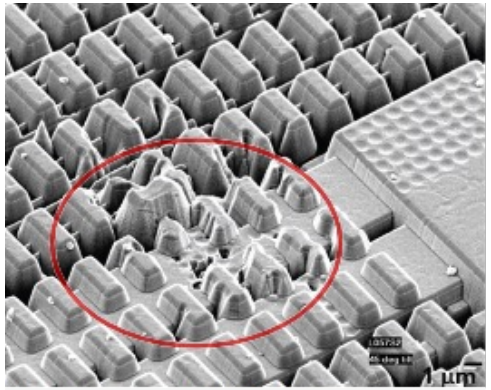
Macroscopic damage by individual ion: **Single Event Effect.**

Ways to spot SEE:

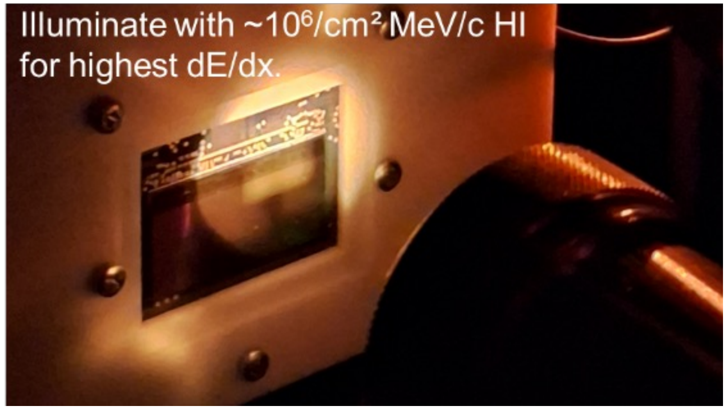
- Gate rupture: Search for permanent failure (not observed).
- Bit flip: Write register with known date, read back, compare.
- Latch-up: Detect increase of current consumption.

Latch-up: Vulnerable structure



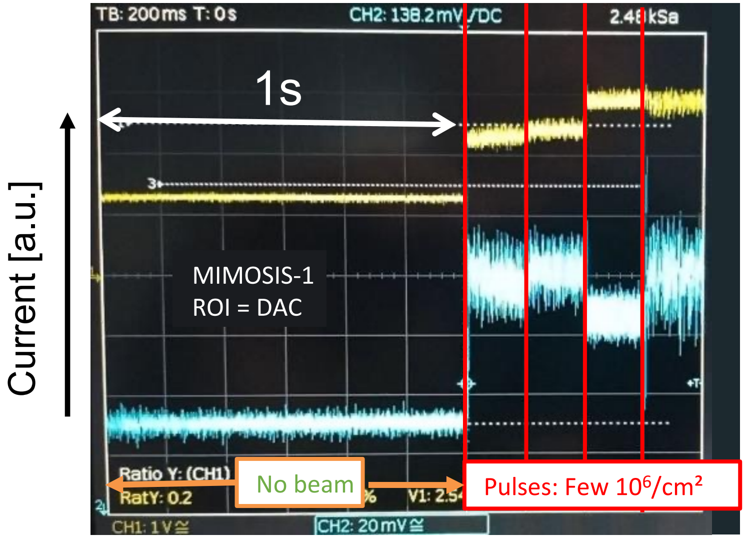


Latch-up in ULTIMATE sensor
G. Contin, JINST 11 C12068 (2016)



Beam test UNILAC – heavy ions and SEE

MIMOSIS-1:



Hits in DAC steering registers confuse sensor.

- 1-bit flip automatic recovery does not work.
- Need power cycle to restart.

No latch-up observed (for LET = 20 MeV cm^2/mg). ✓

Sensor withstands 400 MHz/cm^2 HI (beam impact scenario) w/o damage. ✓

MIMOSIS-2:

Hits in DAC steering registers tolerated.

- 1-bit flip automatic recovery does work. ✓
- May be overwhelmed (2 sync bitflips).
  - Observed at fluences ~10^2 above specs.
  - Recovered by reprogramming (most of the time). ✓

Single bit flip recovery circuits now working.
=> Major improvement in robustness (as hoped).

Requirement for MVD:

- Must withstand LET< 35 MeV cm²/mg.
  (H. Darwish, PhD under preparation)

Test with MIMOSIS-1:

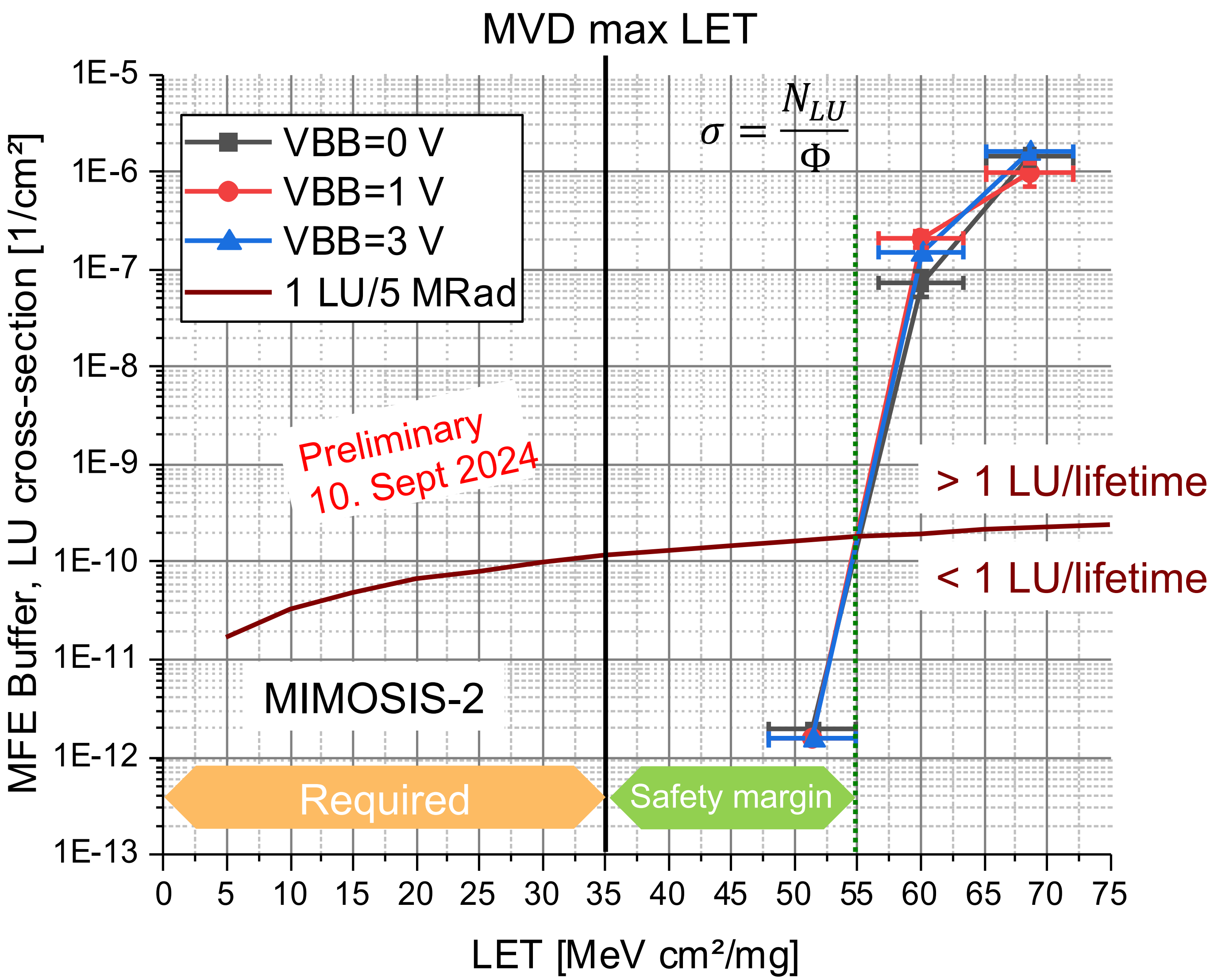
- Withstands LET=20 MeV cm²/mg.
- Limitation: dE/dx of Ca-ions used

Test with MIMOSIS-2 (Au ions):

- No LU for LET≲50 MeV cm²/mg.
- Some LU seen above.

=> MIMOSIS-2 meets requirements

Protection system for Latch-up (1 fast electronic fuse/sensor) likely not required.



MIMOSIS 2.1 – The error corrected MIMOSIS-2

Date	Event
Dec. 2023	MIMOSIS 2.1 submitted. Expect return March 2024

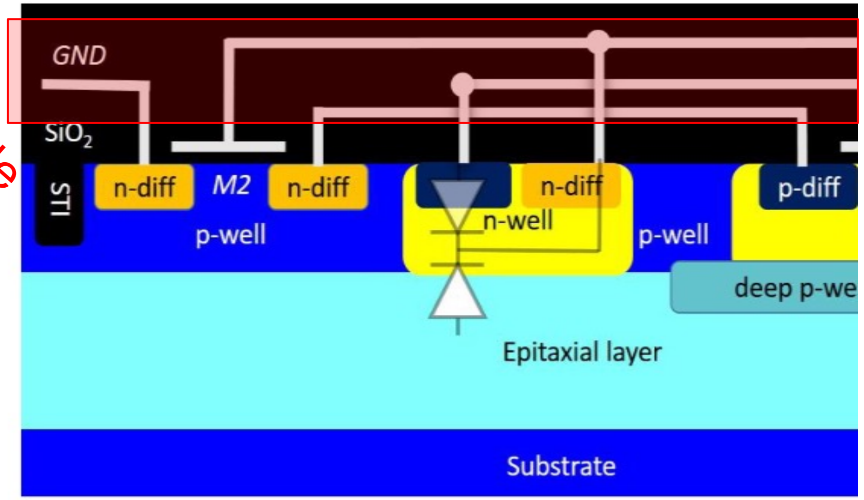
Prepare MIMOSIS-2 re-submission => MIMOSIS 2.1

Strategy: Modify only few masks out of ~30 to save costs.
- few 100 kEUR saving (needed to finance MIMOSIS-3).
- may re-wire transistors but not move/replace them.
  ⇒ Some issues (PLL) cannot be addressed.

Expect working sensor requiring external 320 MHz clk.

Paid extra fee for fast processing.

reworkable



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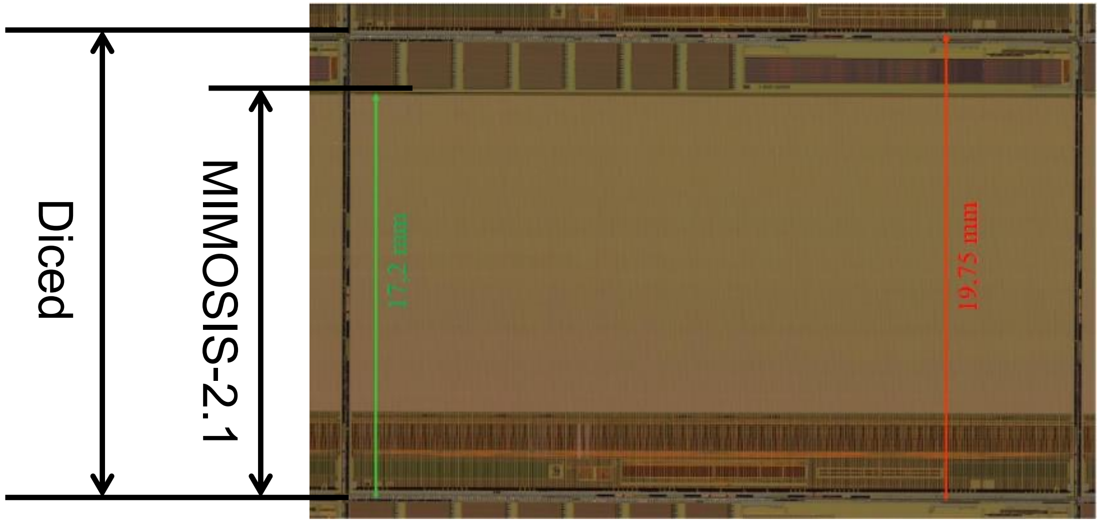
4 diced wafers (one of each split) & 8 full wafers



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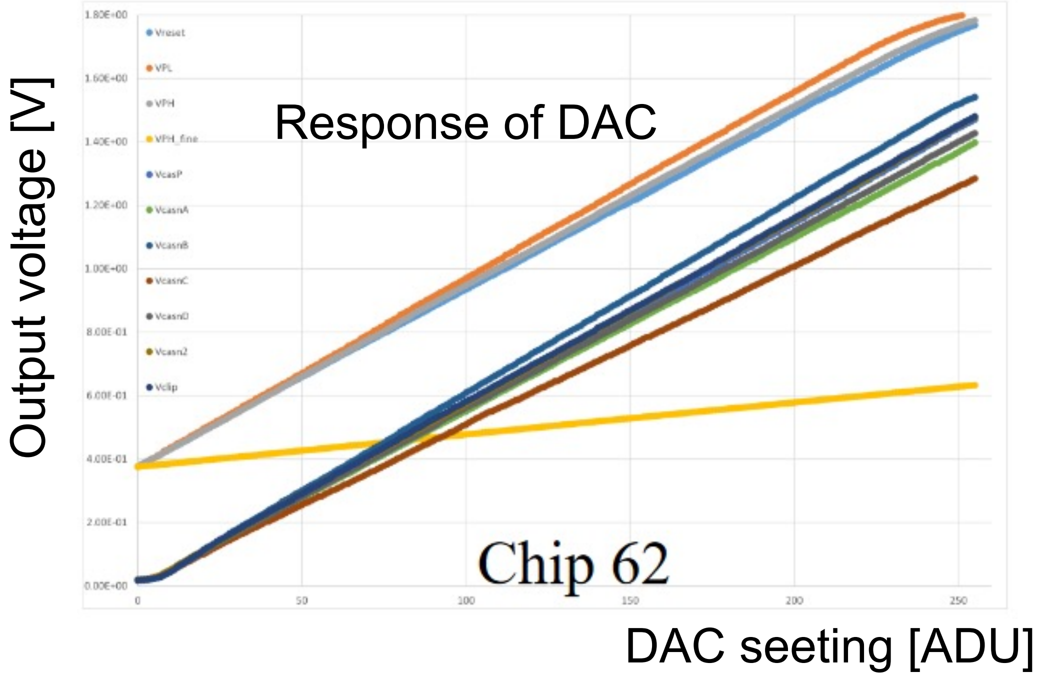

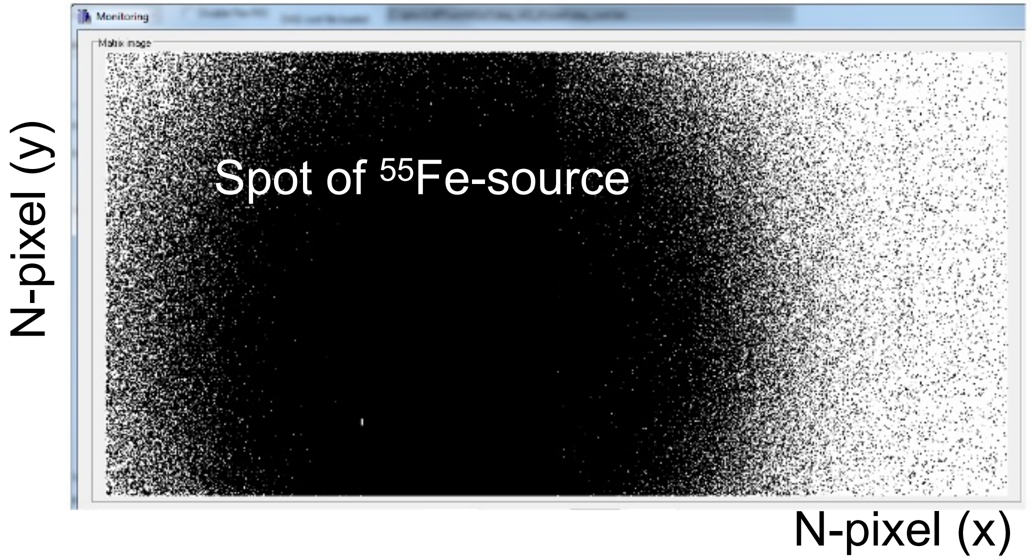

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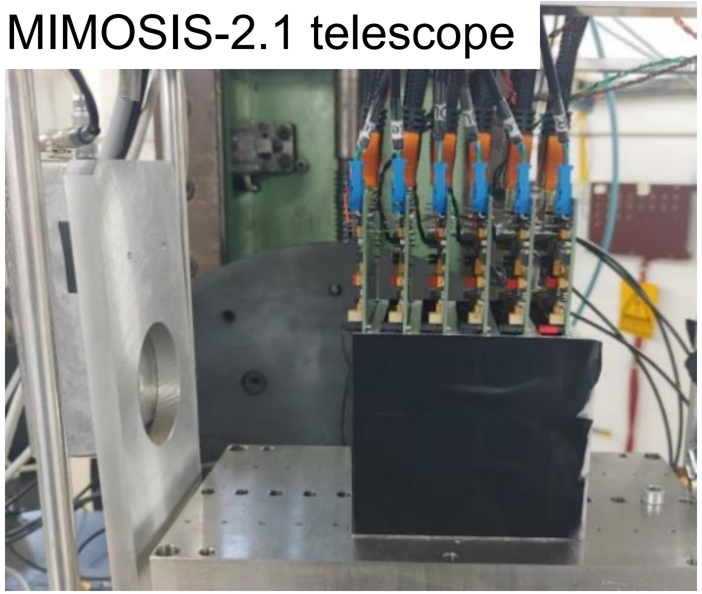
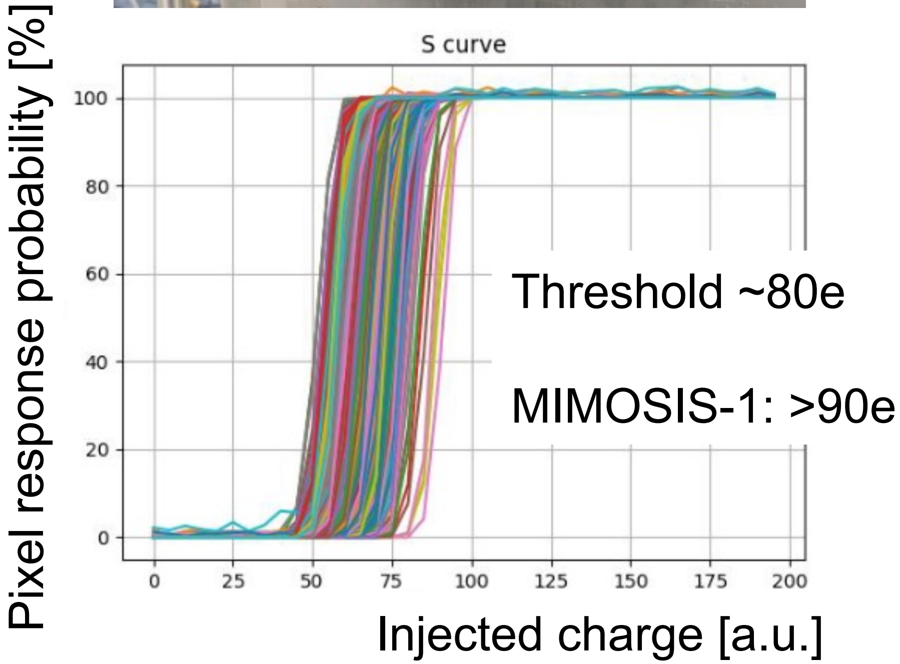
MIMOSIS-2.1 telescope





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Shopping of last items


Arrival at DESY

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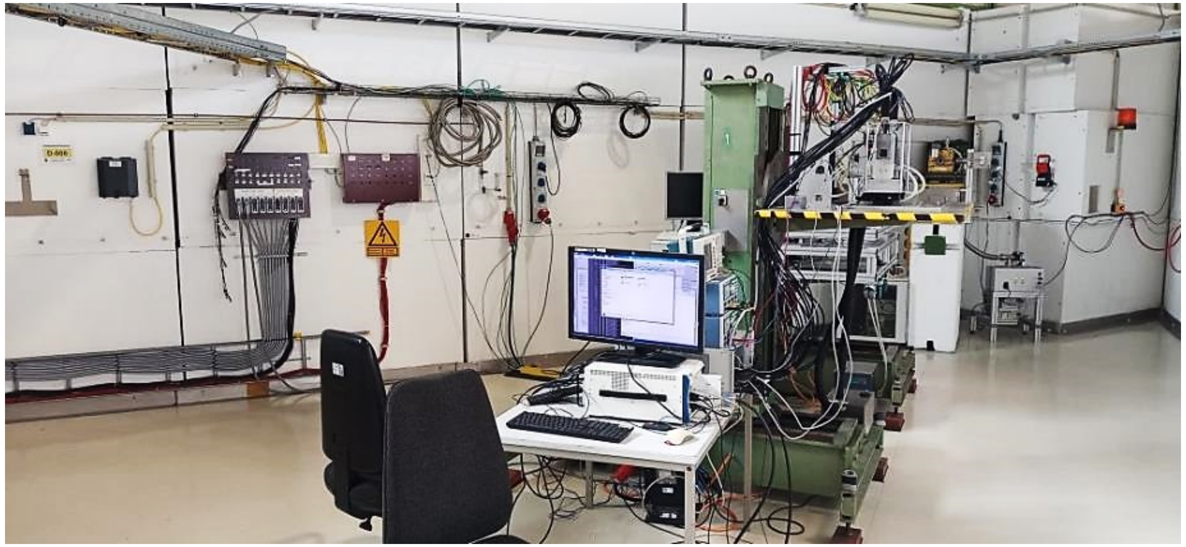

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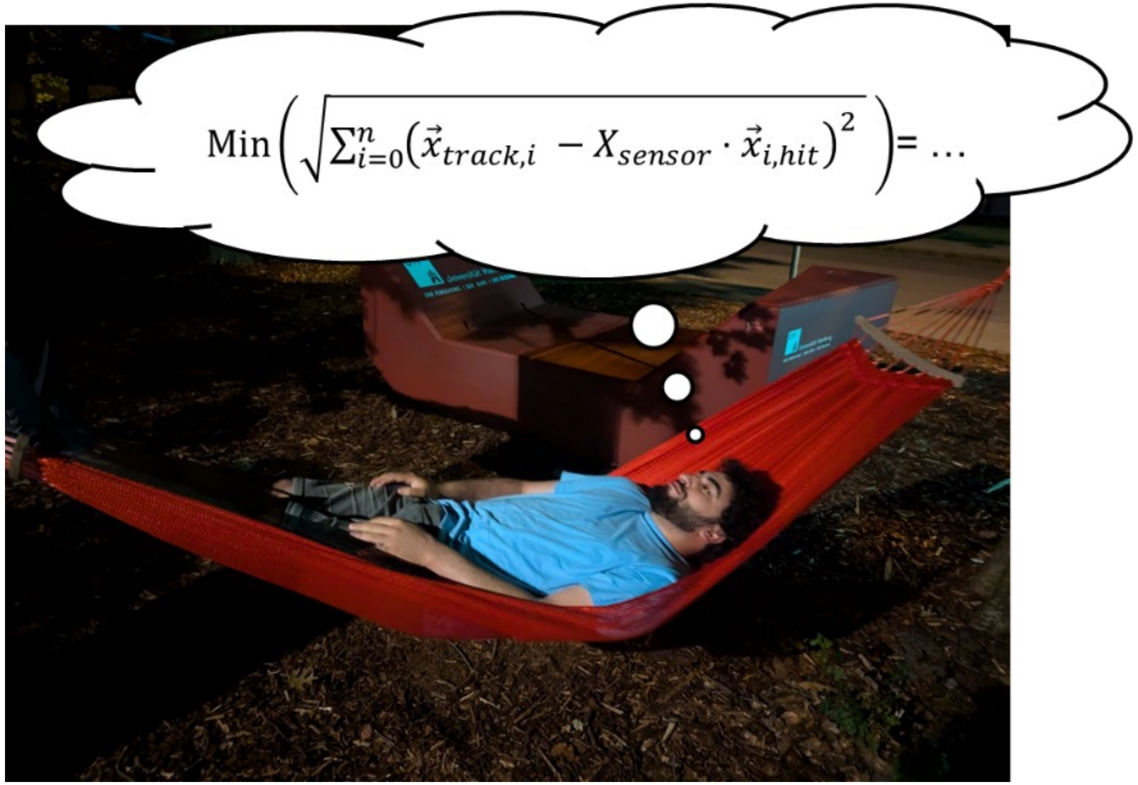

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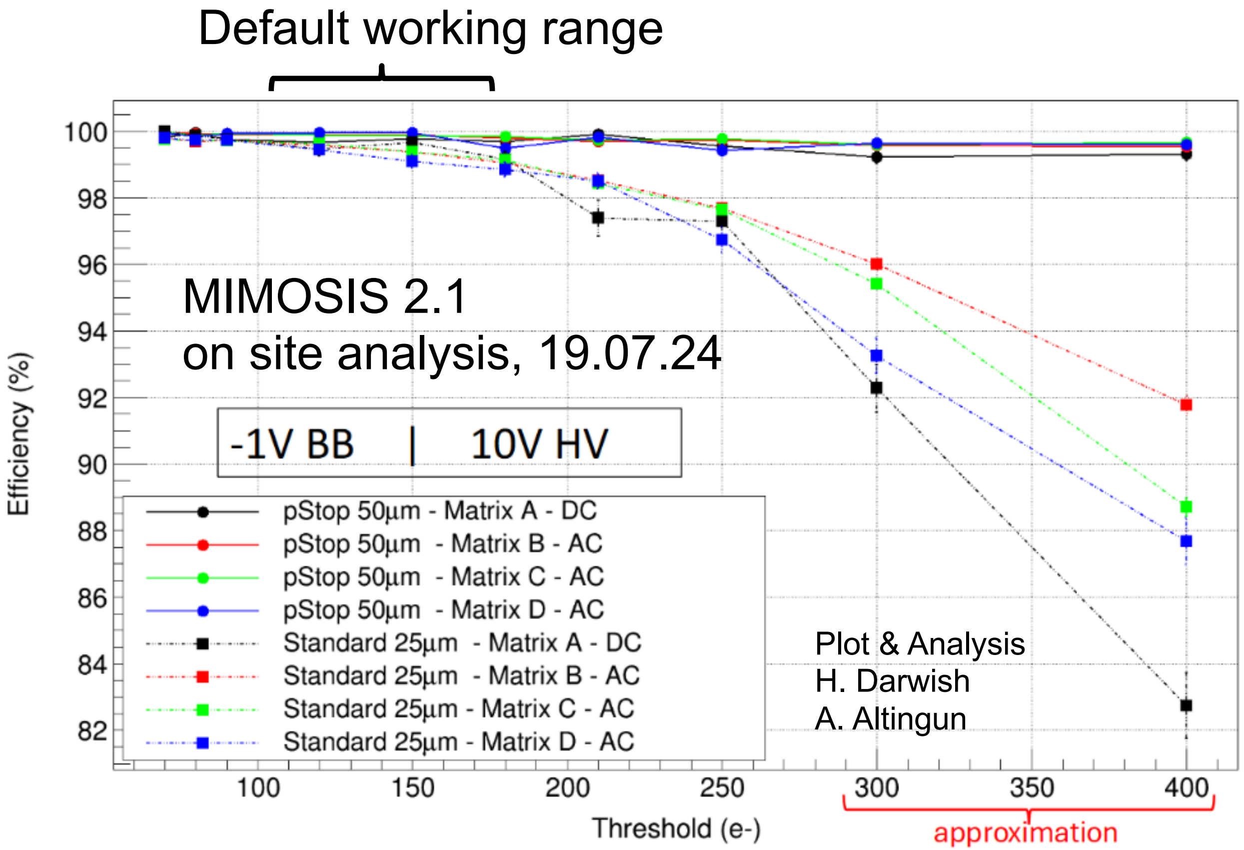
19.07.2024	Beam test results shown in regular Friday meeting.



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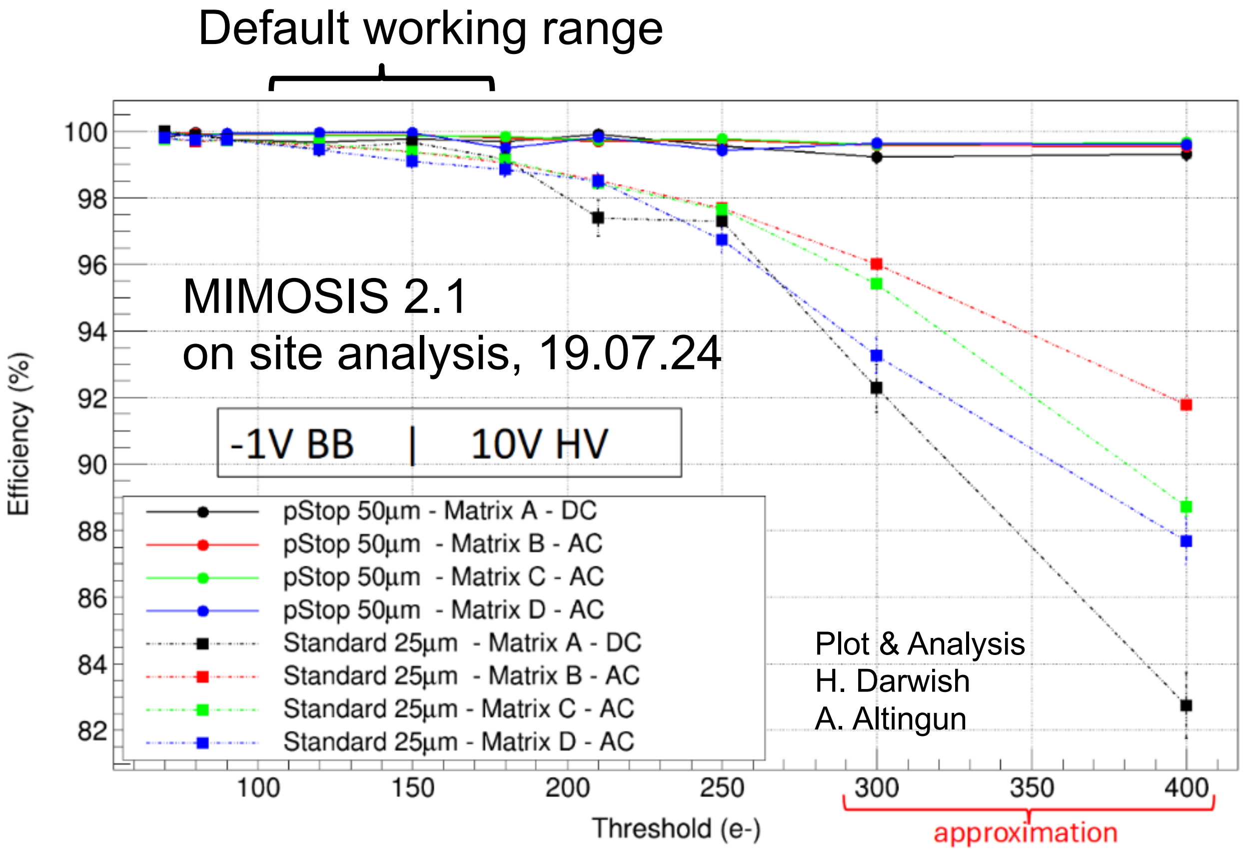
26.08.2024	First preliminary analysis: 50 slides of plots.

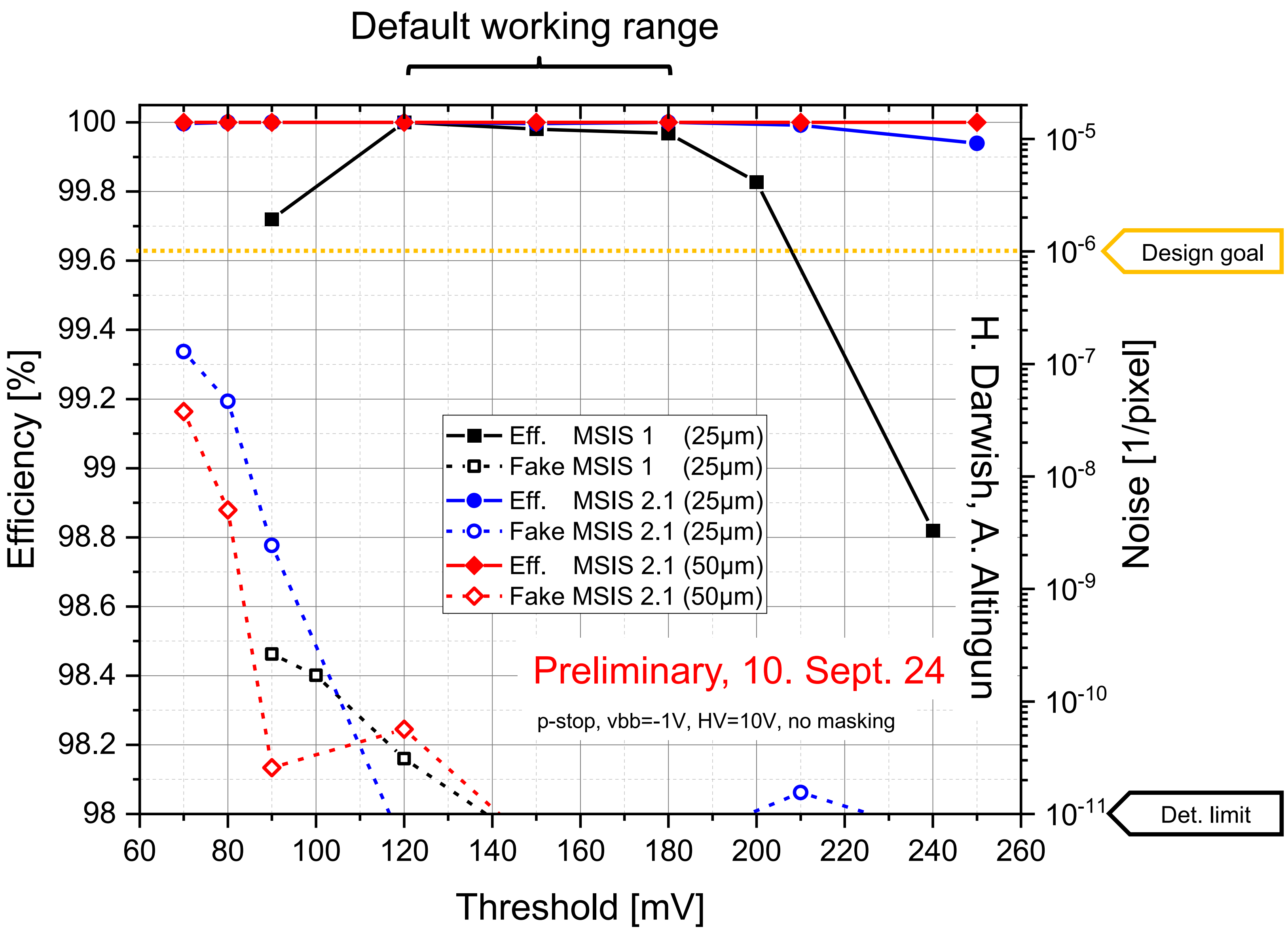


Pixel performance: p-stop AC (most likely pixel for MVD)

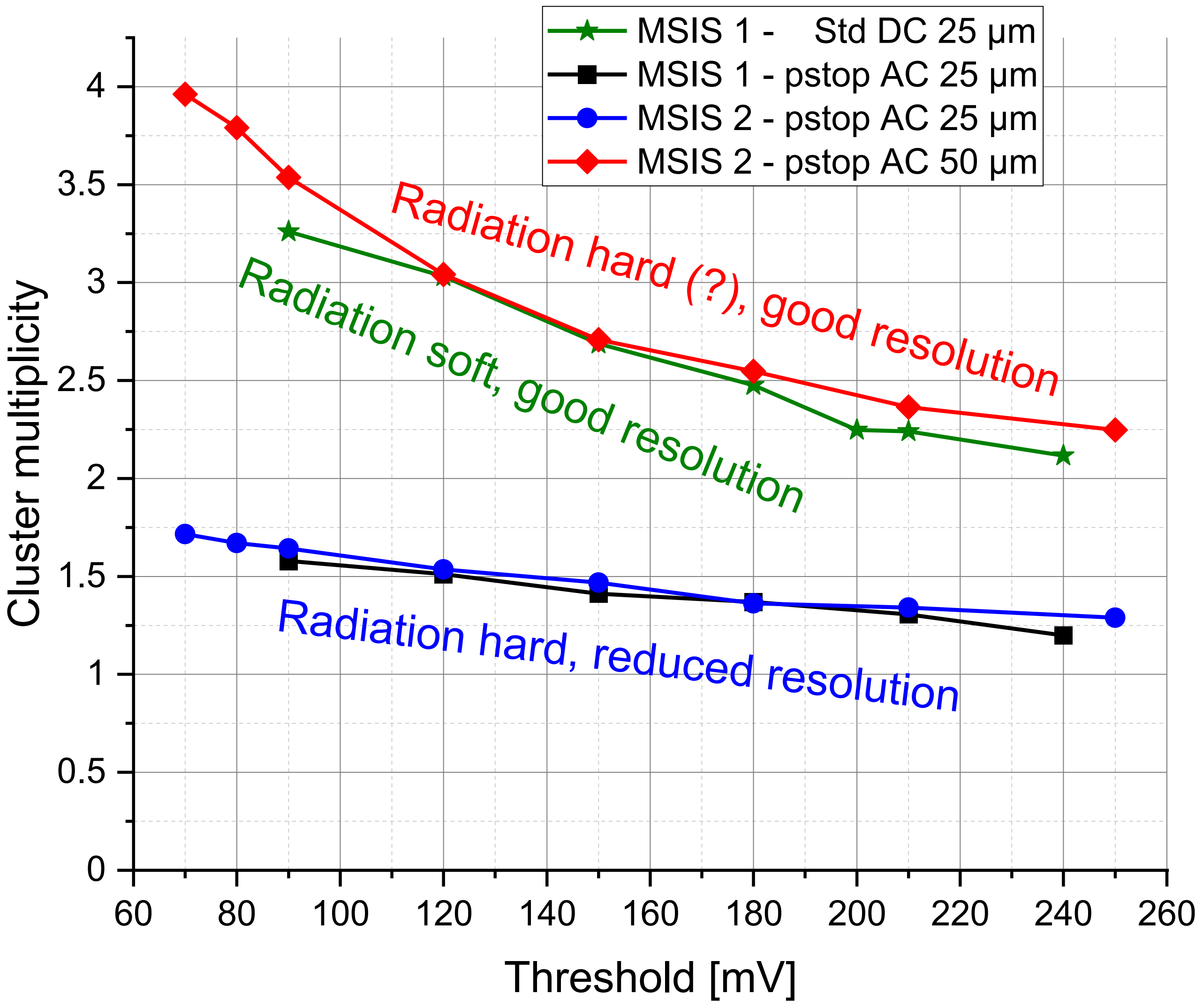
Observations:

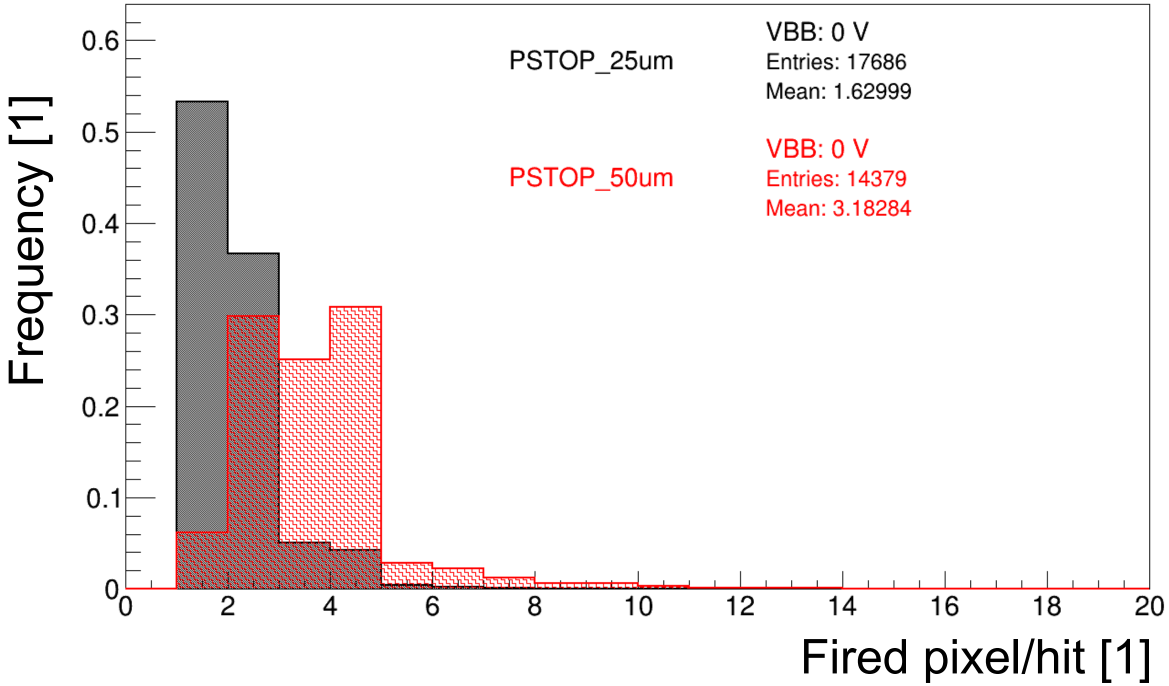
- MIMOSIS-2.1 reaches lower threshold than MIMOSIS-1.
- MIMOSIS-2.1 reaches even(!) higher efficiency than MiSIS-1.
- Best performance: Novel 50µm epitaxial layer with p-stop.

- Dark occupancy marginal for all sensors (noisy pixels NOT masked).



Cluster multiplicity





Observation:

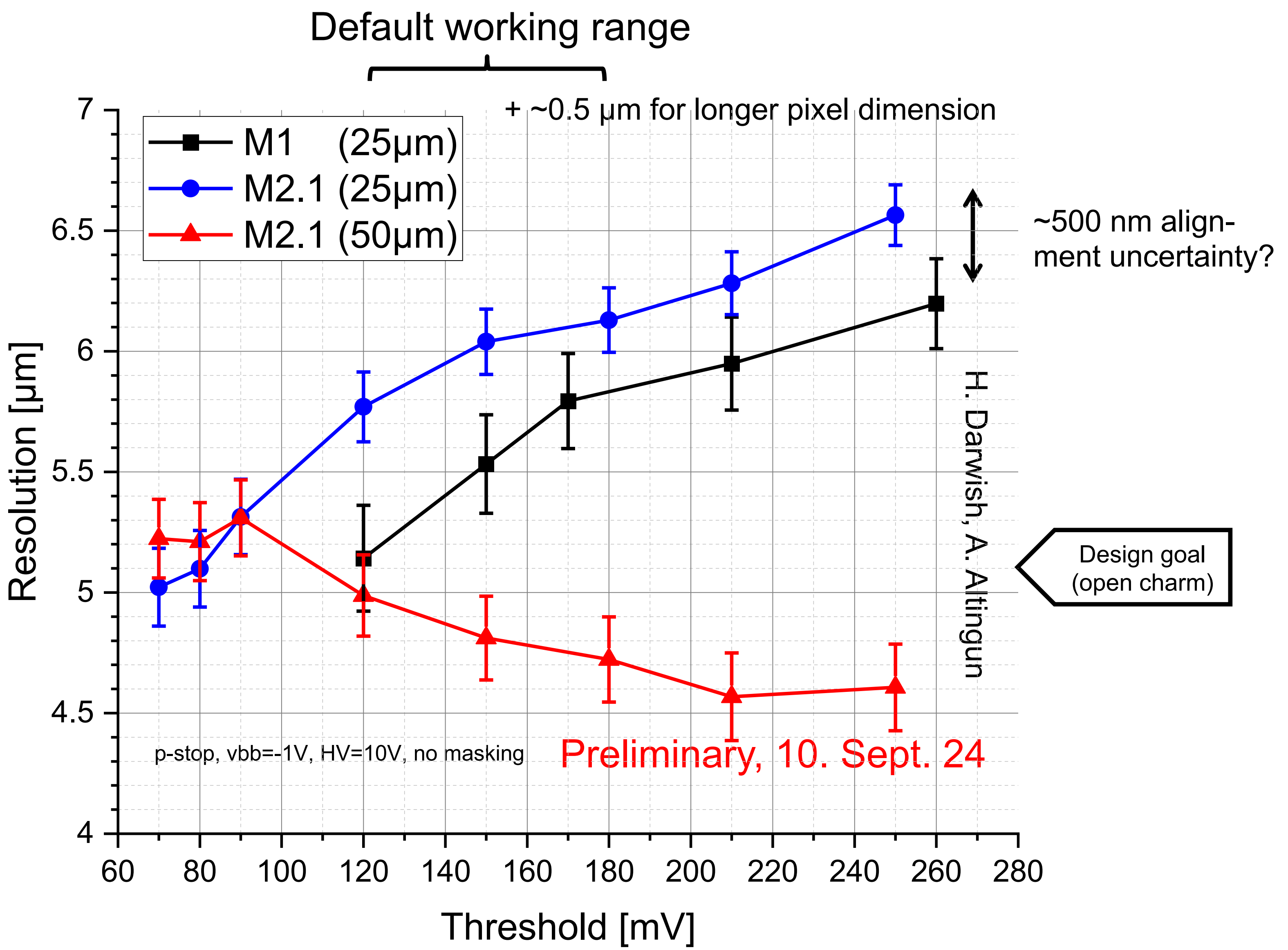
⇒ MIMOSIS-2.1 p-stop 50µm combines high cluster multiplicity with rad. tolerant structure.

Might yield best combination of spatial resolution and radiation tolerance (rad tolerance t.b.c).

Observations:

- MIMOSIS-2.1 and MIMOSIS-1 show mostly same resolution for 25 µm (expected, discrepancy to be studied).

- MIMOSIS-2.1 50 µm reaches better resolution (as hoped).



Preliminary conclusion:

- Novel 50 µm p-stop appears most promising.
- Need to study radiation tolerance before concluding.

MIMOSIS 2.1 works as expected (so far):

- Novel 50µm p-stop sensor shows further improved performance.
- Full readout chain validated.
- Tolerance to SEE now established (gate rupture, Latch-up, slow control).

⇒ Sensor fulfills requirements

Open ends:

- Internal PLL still not fixed.
  - Expert review planned for Q4/2024.
  - Worst case: May have to distribute 320 MHz clk.
- Yield not satisfactory – under study with tools available since 2024.
  - Worst case: Additional money and effort to buy/test more wafers.
- Impact of SEE on data taking not yet rigorously excluded – Need beam test.

Next steps:

- Beam tests (starting this week, Q1/2025) to understand sensors better.
- Participation to mCBM (test in real environment).
- Test with realistic LV-distribution.

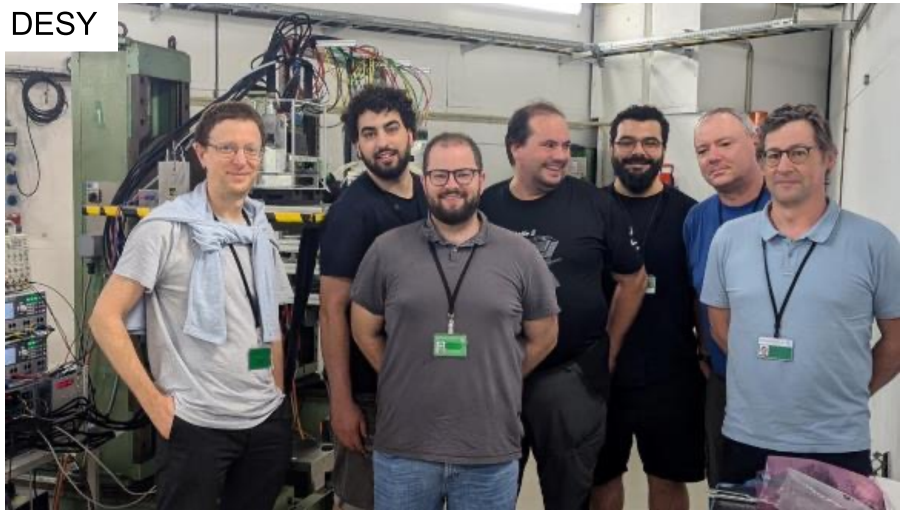
MIMOSIS R&D back on track.
Program in schedule (presented at ECE in Apr. 2024).
Expect MIMOSIS-3 (final sensor) by end 2025.

Test team:

UNILAC

M. Dx, Ben Arnoldi, Kay O. Voss, Benedikt Gutsche, Oliver Keller

DESY



Auguste Besson, Hasan Darwish, Mathieu Goffe, Ali Al-tingun, Mathieu Specht

…Julio Andary, Gilles Claus, Kimmo Jaaskelainen…

News from CE65

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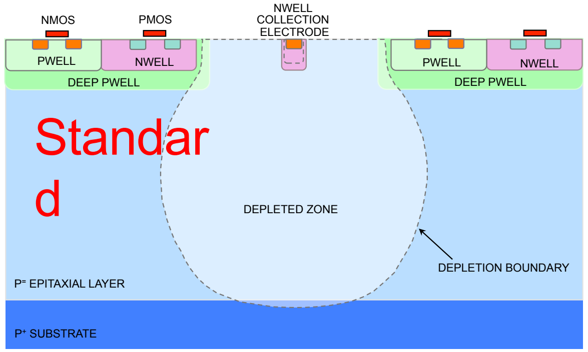
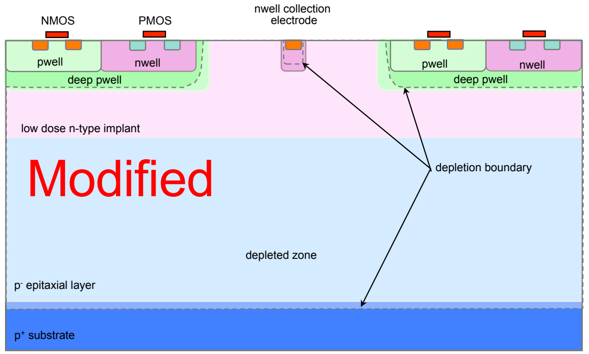
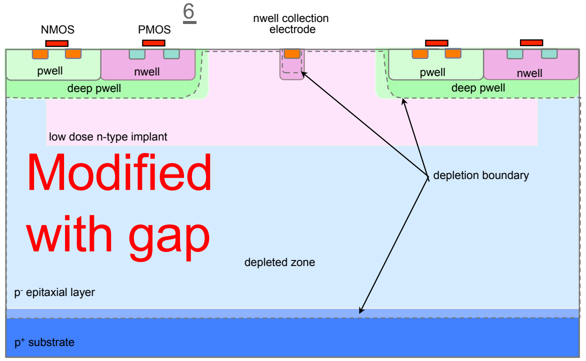
- Benefits: 65 nm vs 180 nm
  - Better spatial resolution due to smaller feature size
  - Larger wafers: 300 mm vs 200 mm => final sensor: 27x9 cm^2
  - Lower power supply: 1.2 V vs 1.8 V => Low power consumption
  - Lower material budget: thinner sensitive layer (~ 10 um)
- Provides 2D stitching
- 7 metal layers
- Process modifications for full depletion:
  - Standard (no modifications)
  - Modified (low dose n-type implant)
  - Modified with gap (low dose n-type implant with gaps)





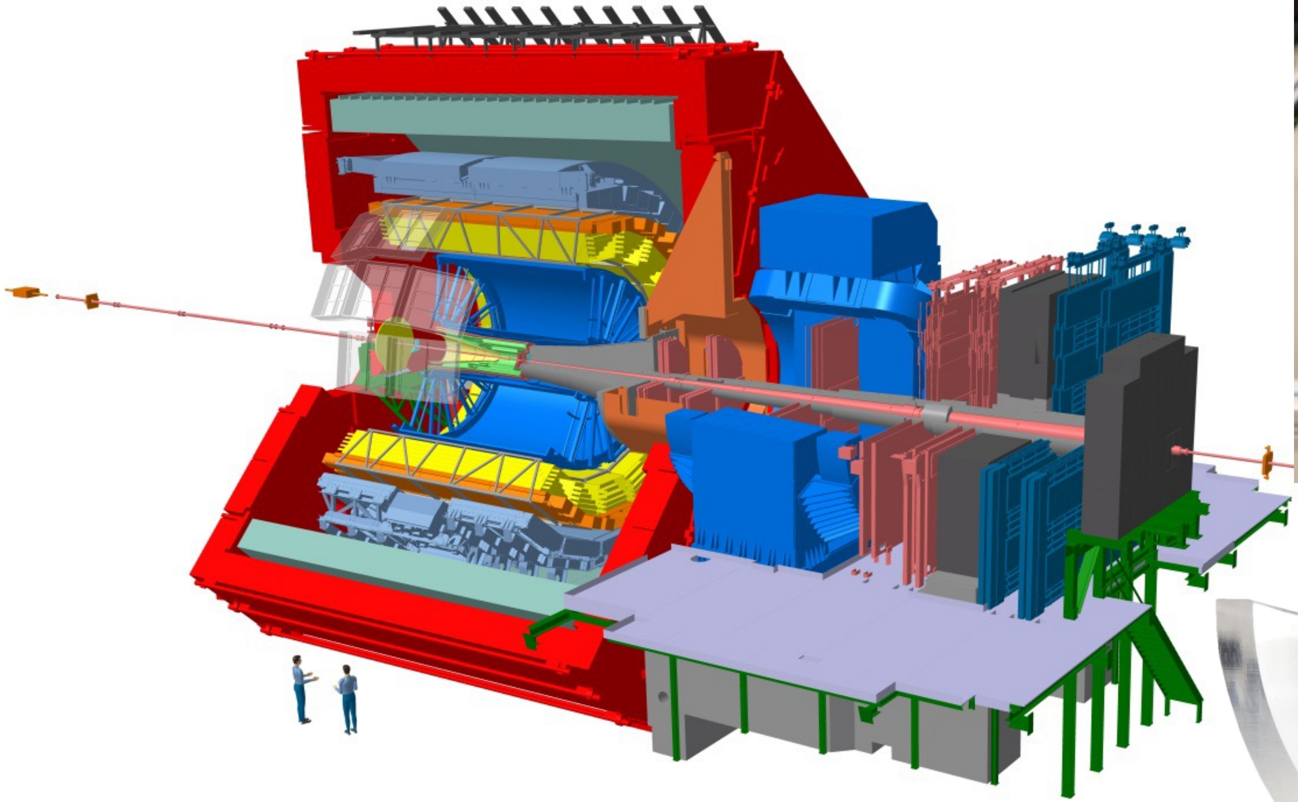
https://doi.org/10.1016/j.nima.2017.07.046



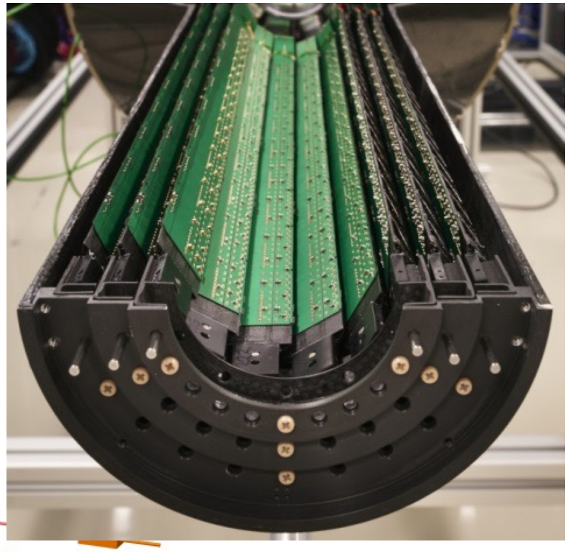
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

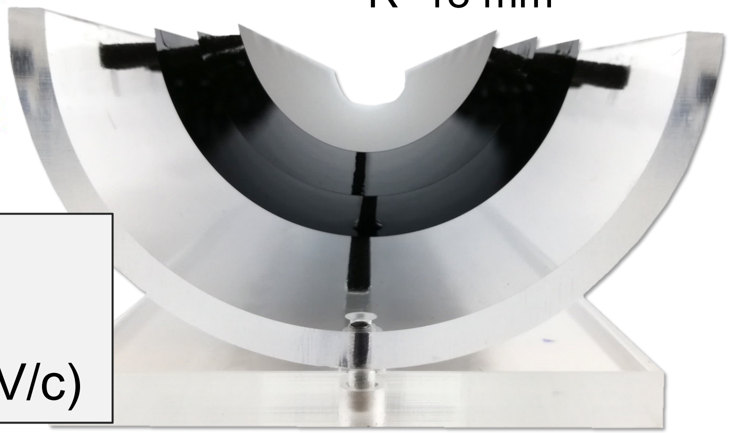
ALICE DETECTOR LS3 UPGRADE: ITS2 (180 nm) → ITS3 (65 nm)

R. Ricci, PSD 2023



ALICE – general purpose detector at LHC:
- Tracking (100 MeV/c – 100 GeV/c)
- Particle identification: π, K, p, e (0.1 – 50 GeV/c)



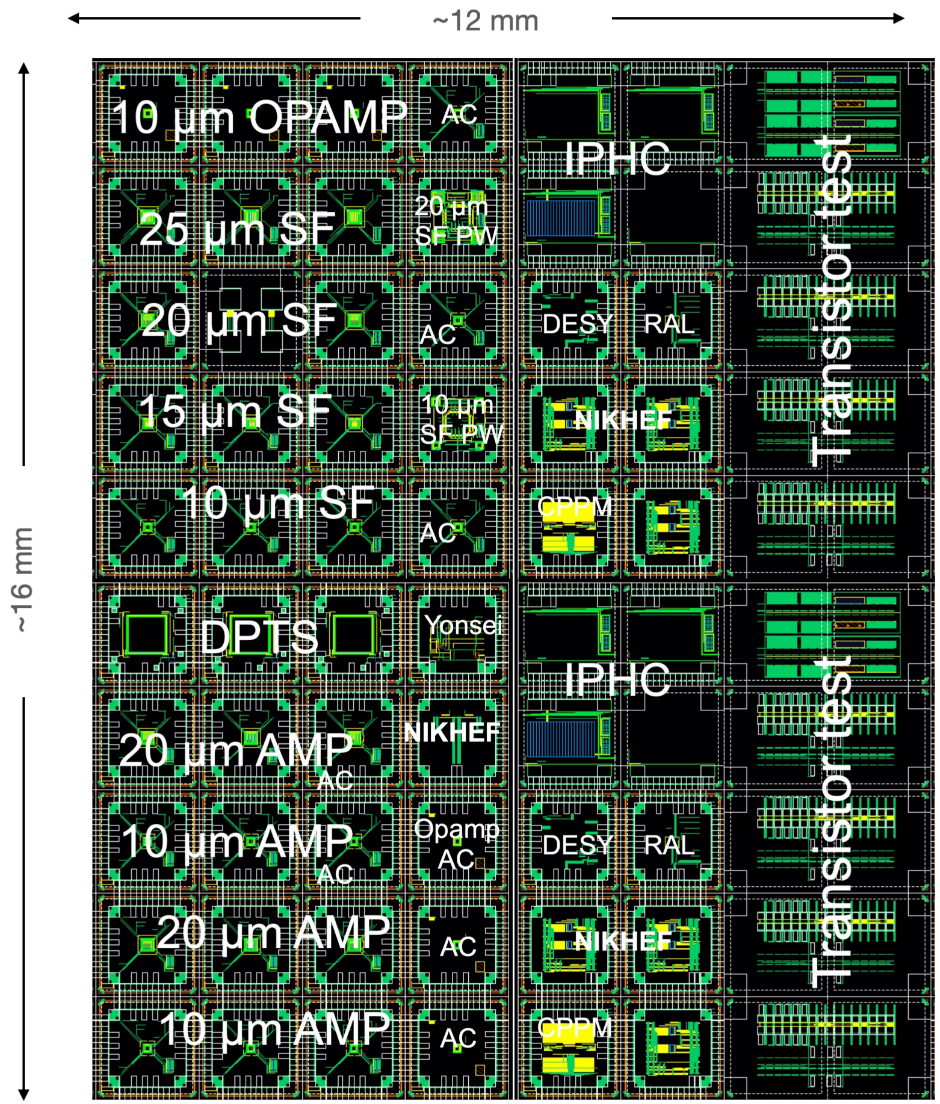


ITS2:
(S.Beolé, iWoRiD 2022)
- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size: 27×29 μm^2
- Water cooling
- **0.3 % X_0 / inner layer**

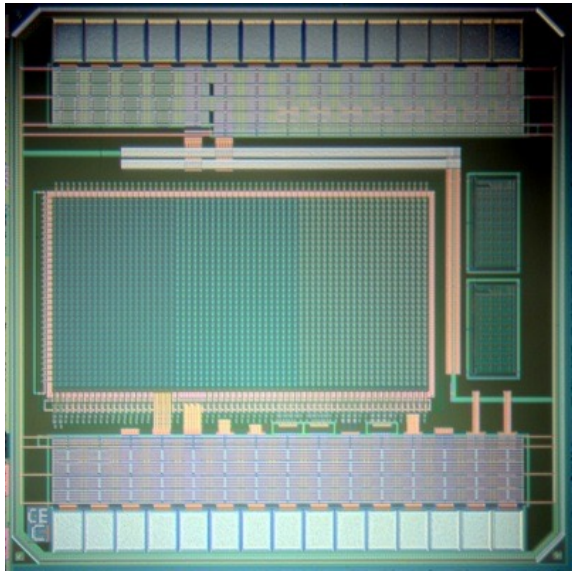
ITS3
(M. Šuljić, iWoRiD 2023)
- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to 27×9 cm
  - Thickness <= 50 μm
  - No FPCs
  - Air cooling in active area
- **0.05 % X_0 / inner layer**

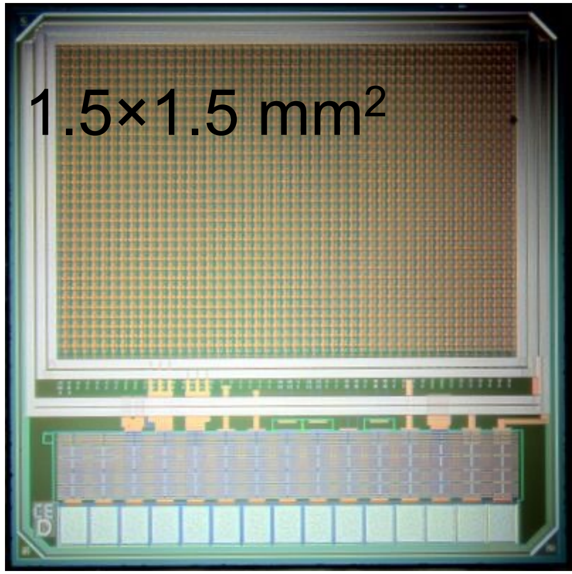
First test submission : MLR1

- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm^2):
  - 10 transistor test structures (3×1.5 mm^2)
  - 60 chips (1.5×1.5 mm^2)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**



- 2 matrix sizes
  - 64×32 with 15 µm pitch
  - 48×32 matrix with 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - **Standard process 15 µm pitch**
  - Modified process 15 µm pitch
  - **Modified process with gaps 15 µm pitch**
  - Standard process 25 µm pitch
- Fabrication in September 2021
- Presented results from CERN PS beam test : May 2022

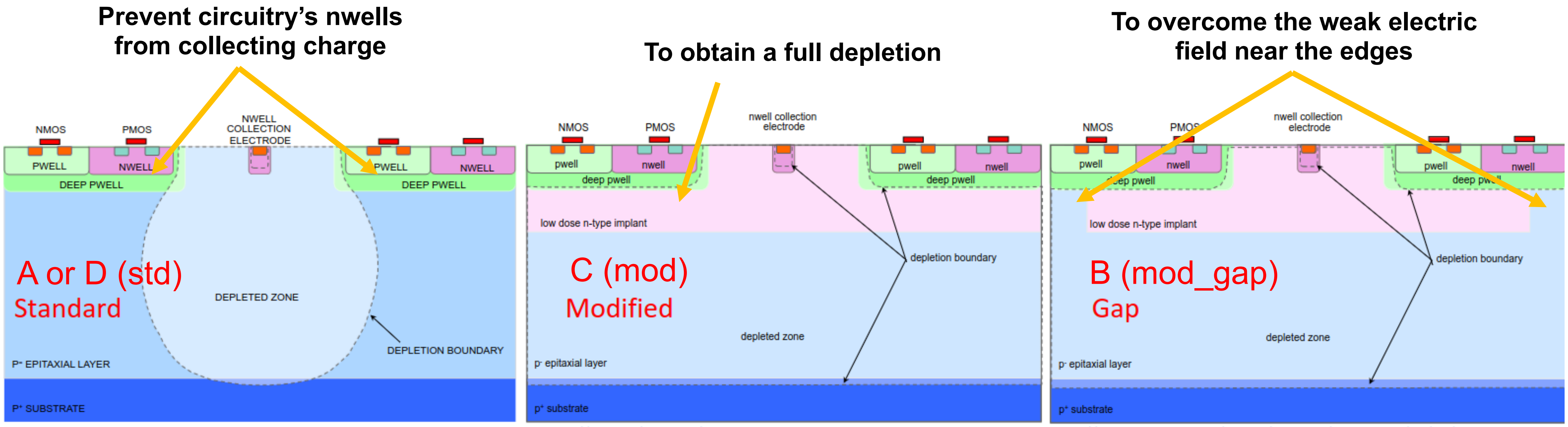




$1.5 \times 1.5\ mm^2$

CE-65 nm variants: pixel pitch and process

Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	15μm	64×32	AC/21, DC/21, SF/22
CE65-B	mod_gap	15μm	64×32	AC/21, DC/21, SF/22
CE65-C	mod	15μm	64×32	AC/21, DC/21, SF/22
CE65-D	std	25μm	48×32	AC/16, DC/16, SF/16



Beam Test Setup

Telescope:
Reference Arms : 4 ALPIDE planes for track reconstruction
DUT : CE65
TRG : DPTS

Test beam:
May 2022 at CERN-PS

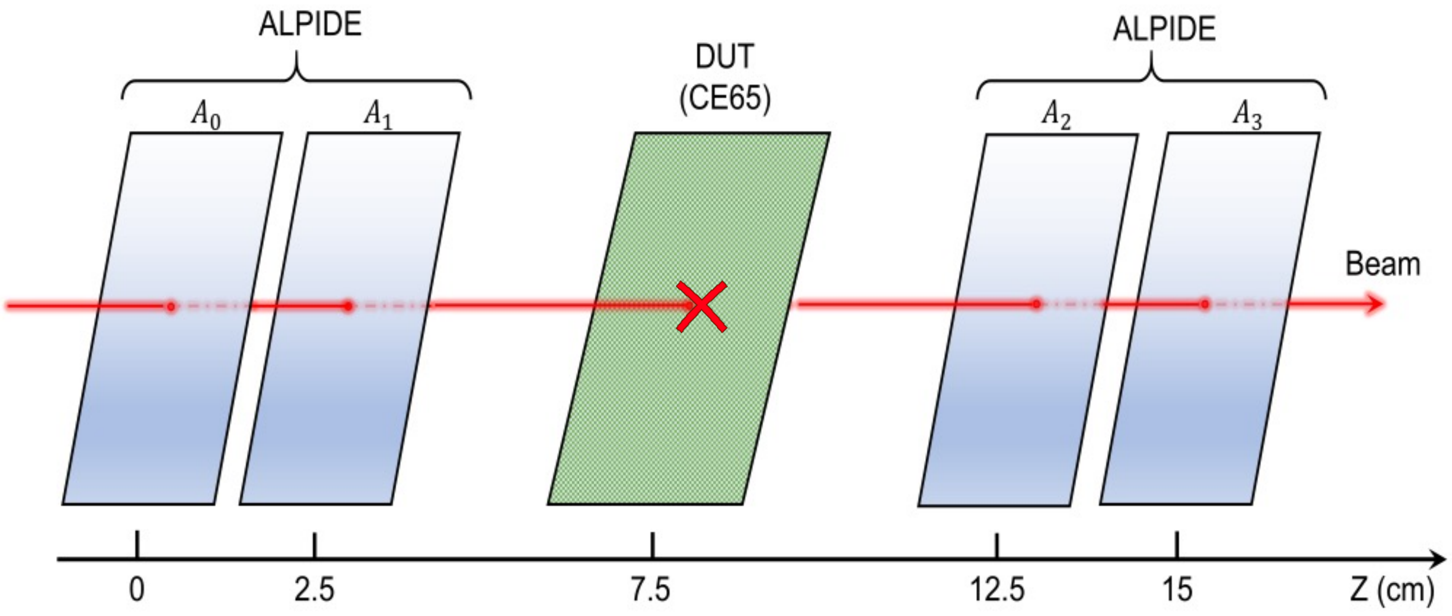
Data acquisition:
EUDAQ2
Event reconstruction algorithm and data analysis framework:
Corryvreckan

Noise run-**Beam** run:
correlated double sampling method (**CDS**)

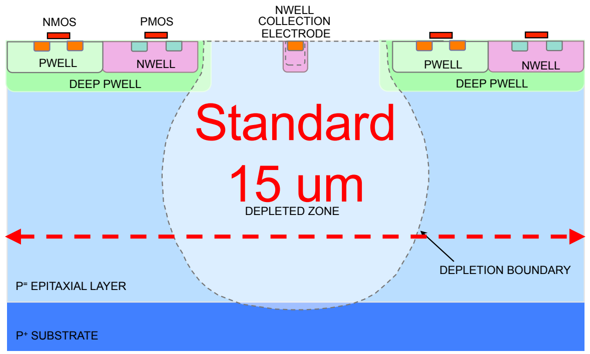
Support provided by Alice Collaboration

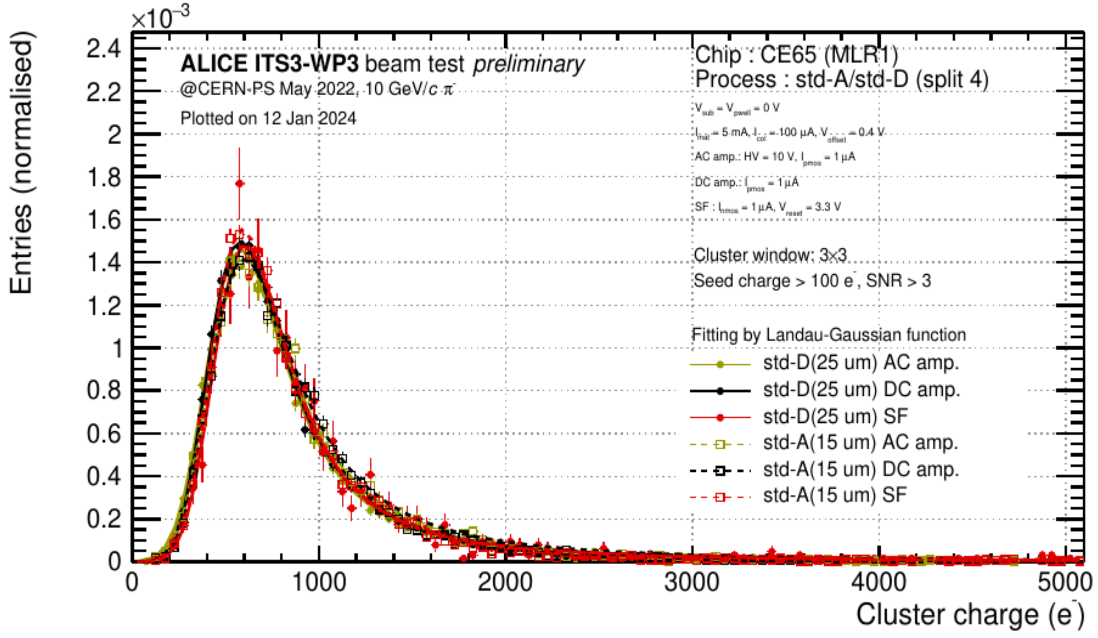
4 frames for each event → **Pedestal map** **Noise map**

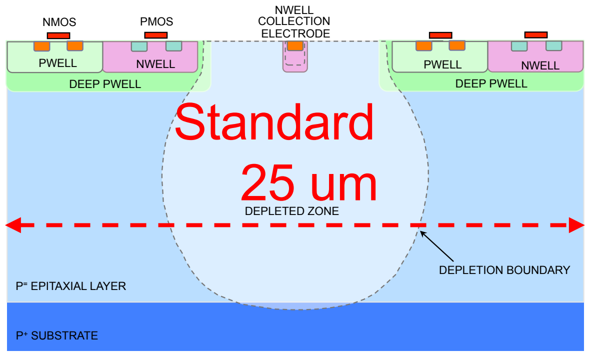
Calibration file

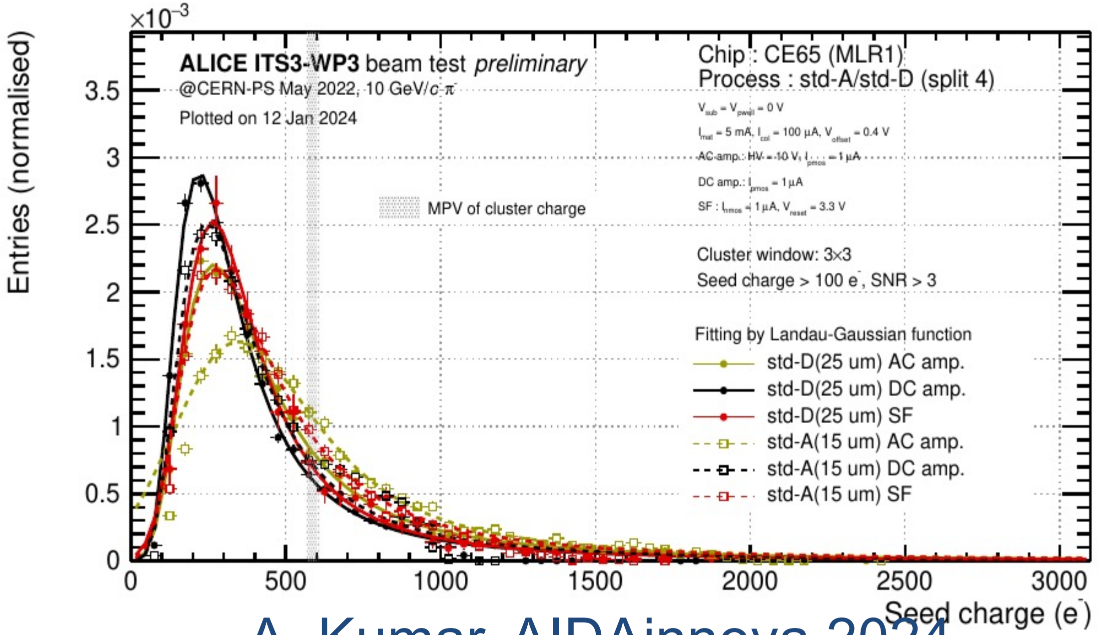


Pixel size impact



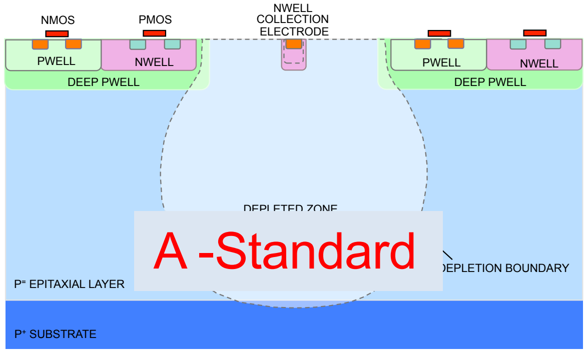


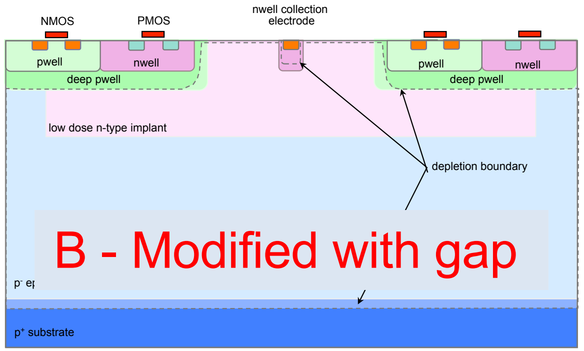


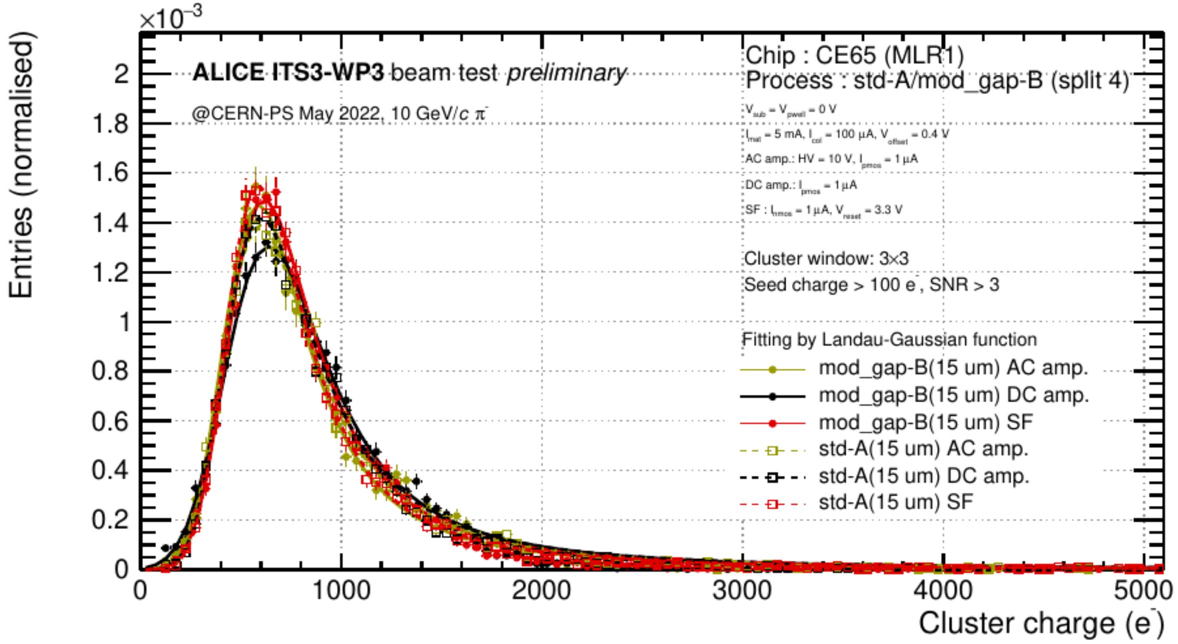


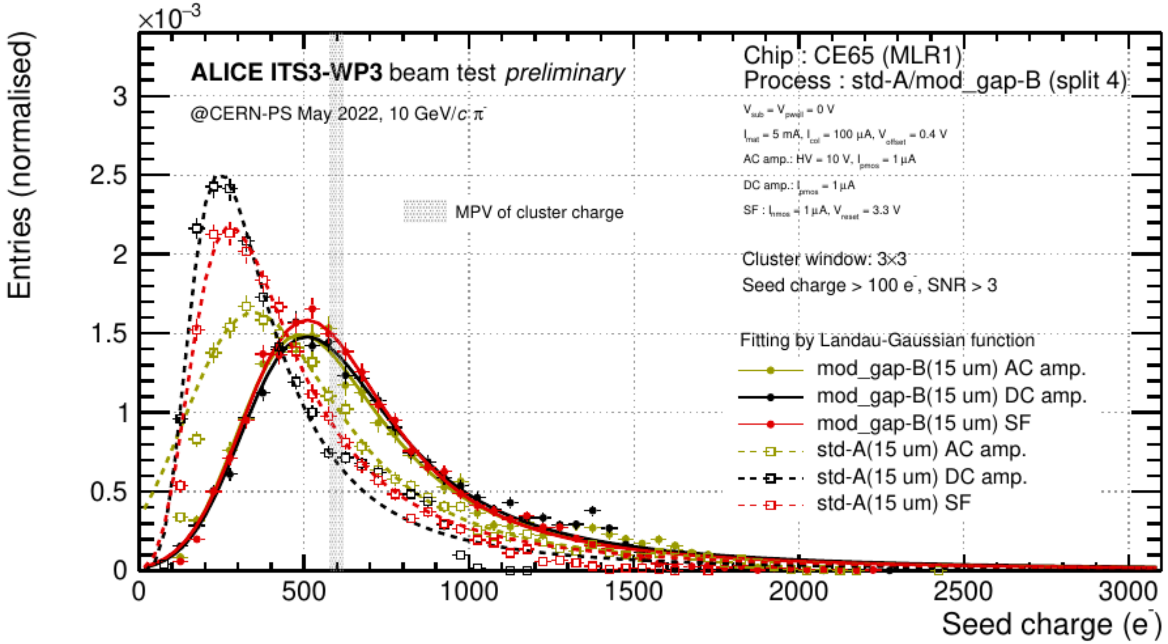
A. Kumar, AIDAinnova 2024

Process Modification Impact

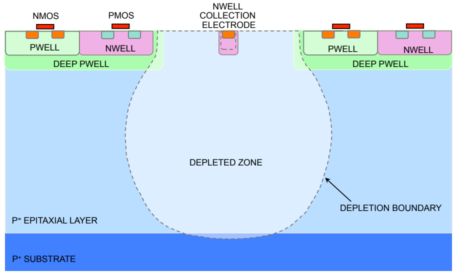


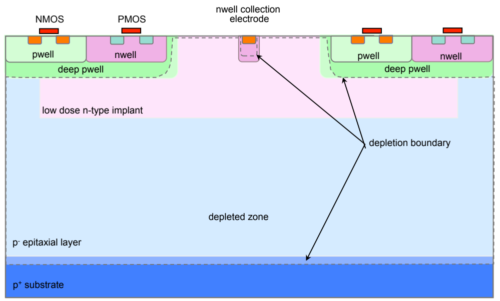


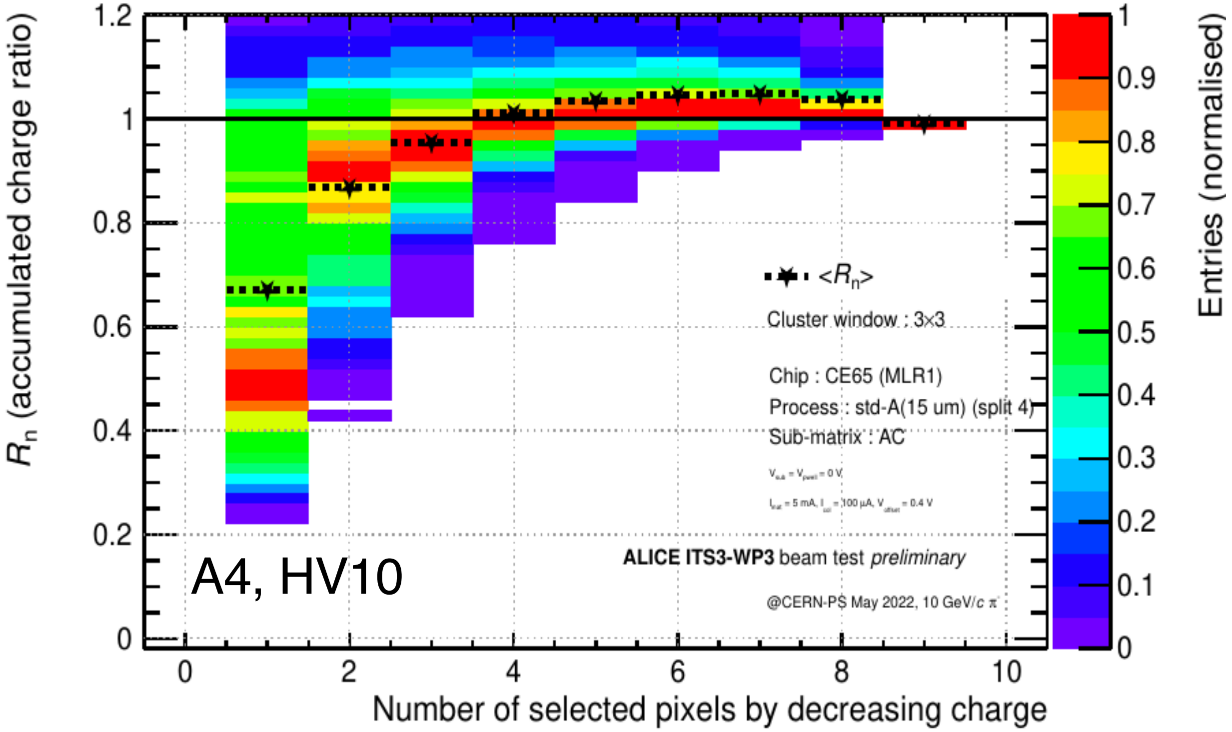


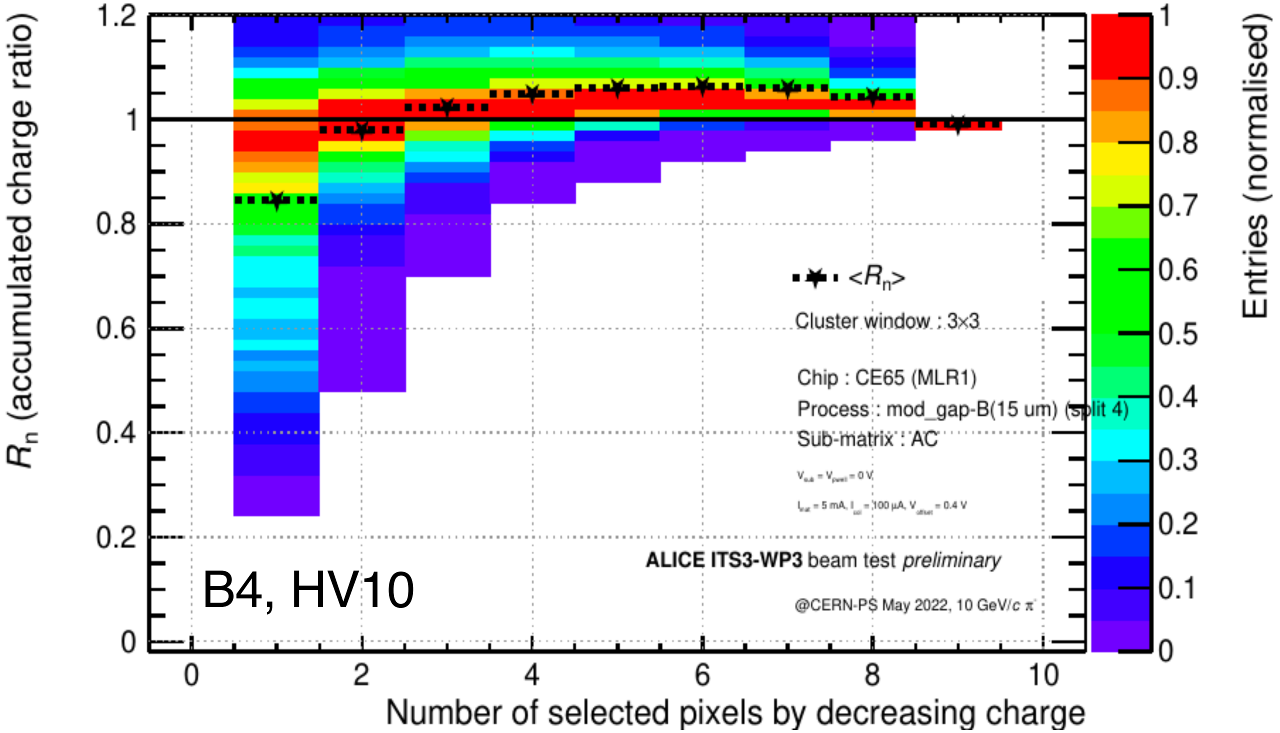


Process Modification: Charge Sharing



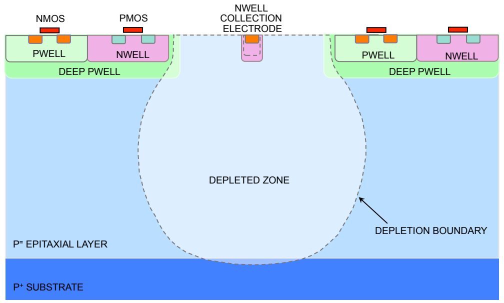


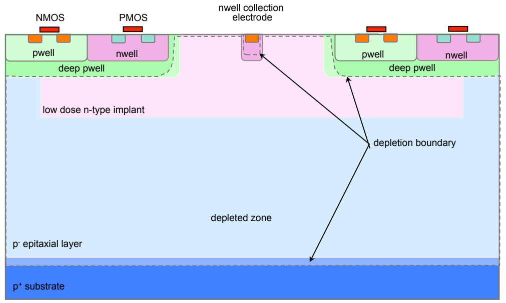


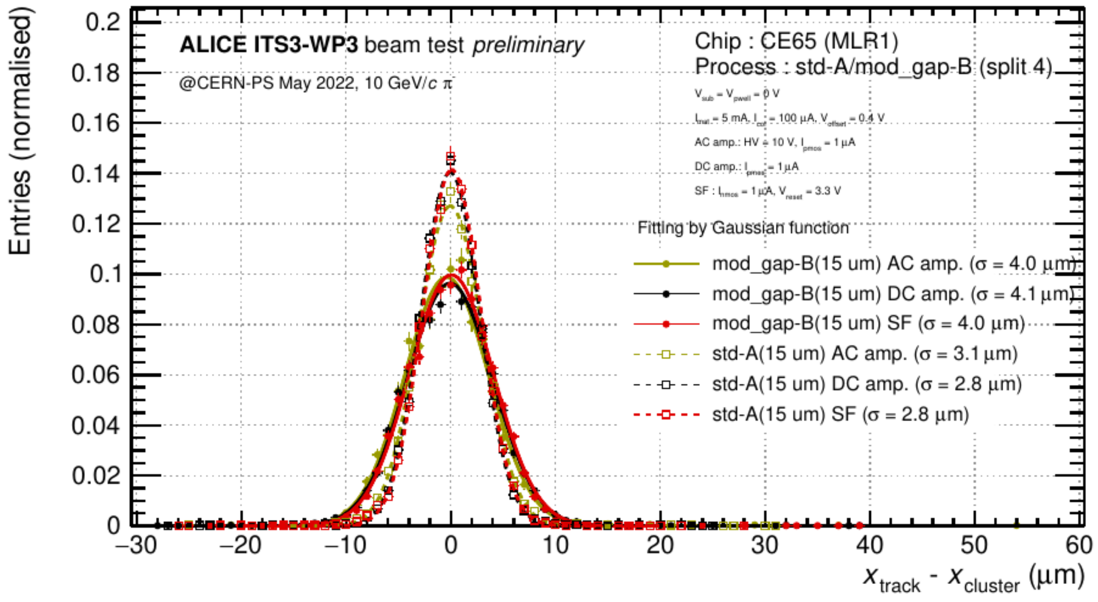


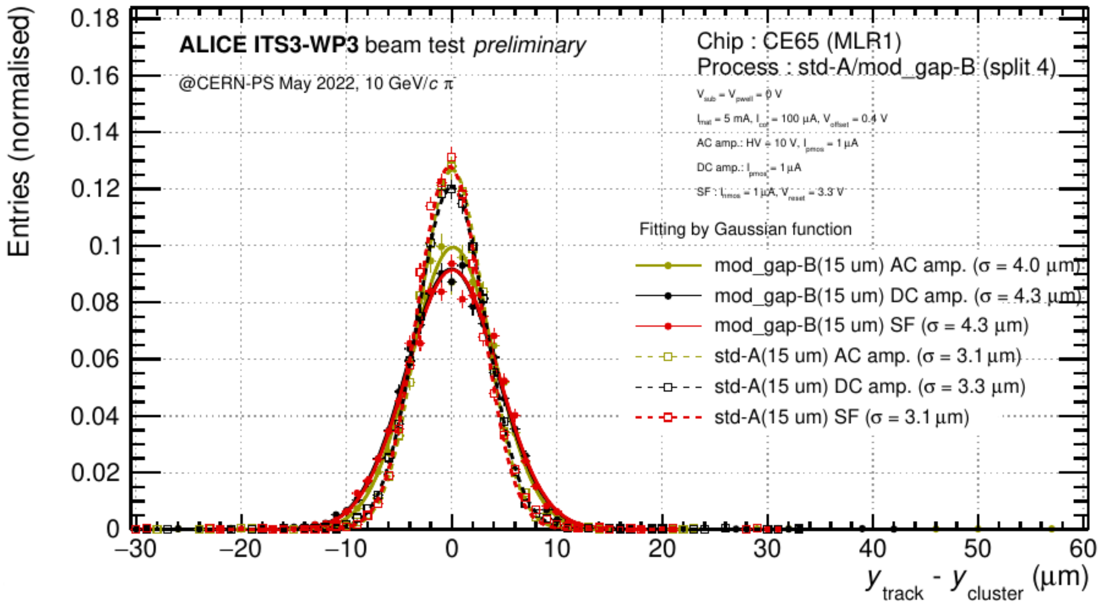
Charge sharing (std) > Charge sharing (mod)

Process Modification : Spatial Resolution





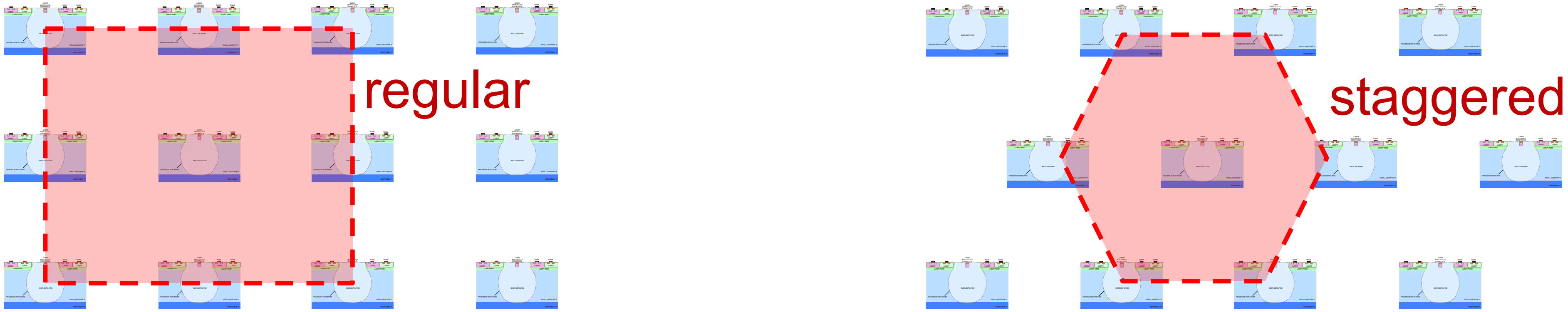




Residual (std) < Residual (mod)

CE65-v2

- AC-coupled
- Three processes (STD, GAP, BLANKET)
- Three pixel pitch values (15 um, 18 um, 22.5 um)
- Pixel arrangement



Spatial resolution summary

PCB	Geo	Process	Pitch(um)	HV(V)	Sp. Res.(um) (telescope resolution subtracted)
10	SQ	GAP	22.5	10	~5.1
02	SQ	GAP	18	10	~4.1
19	SQ	GAP	15	10	~3.2
18	SQ	STD	22.5	10	~2.4
23	SQ	STD	18	10	~1.8
06	SQ	STD	15	10	~1.3

Telescope resolution: **~2.1um** (Calculated from https://mmager.web.cern.ch/telescope/tracking.html)

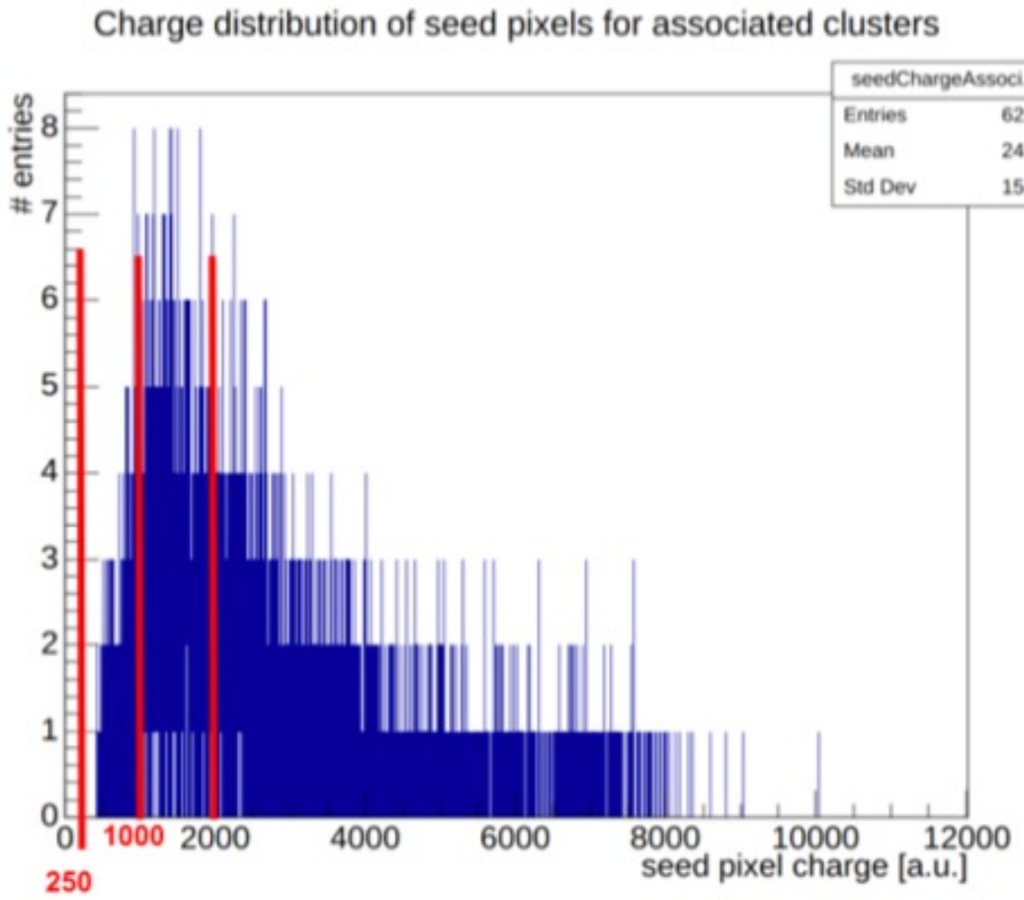
Digitization

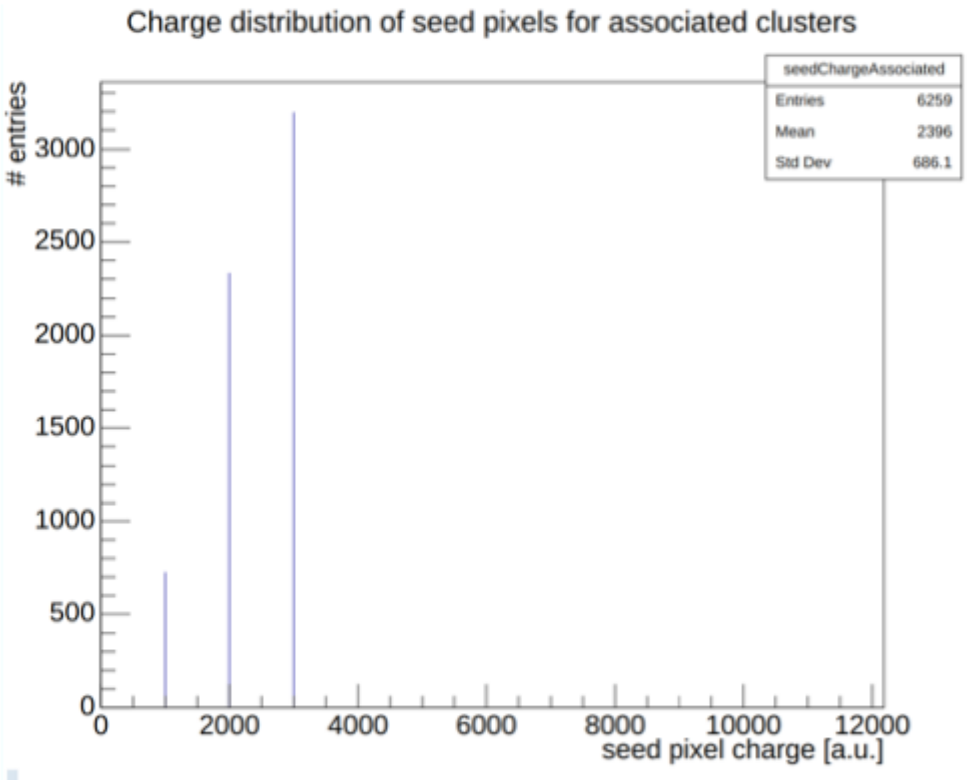
What is required from a sensor?

- Fast Readout → Digital Readout
- Low spatial resolution → Analog Output
- Radiation tolerance…
- etc ….

Is there any trade-off that preserves the spatial resolution without sacrificing the readout speed?
What if we use two bits for digitization, three or maybe four instead of 1 bit?

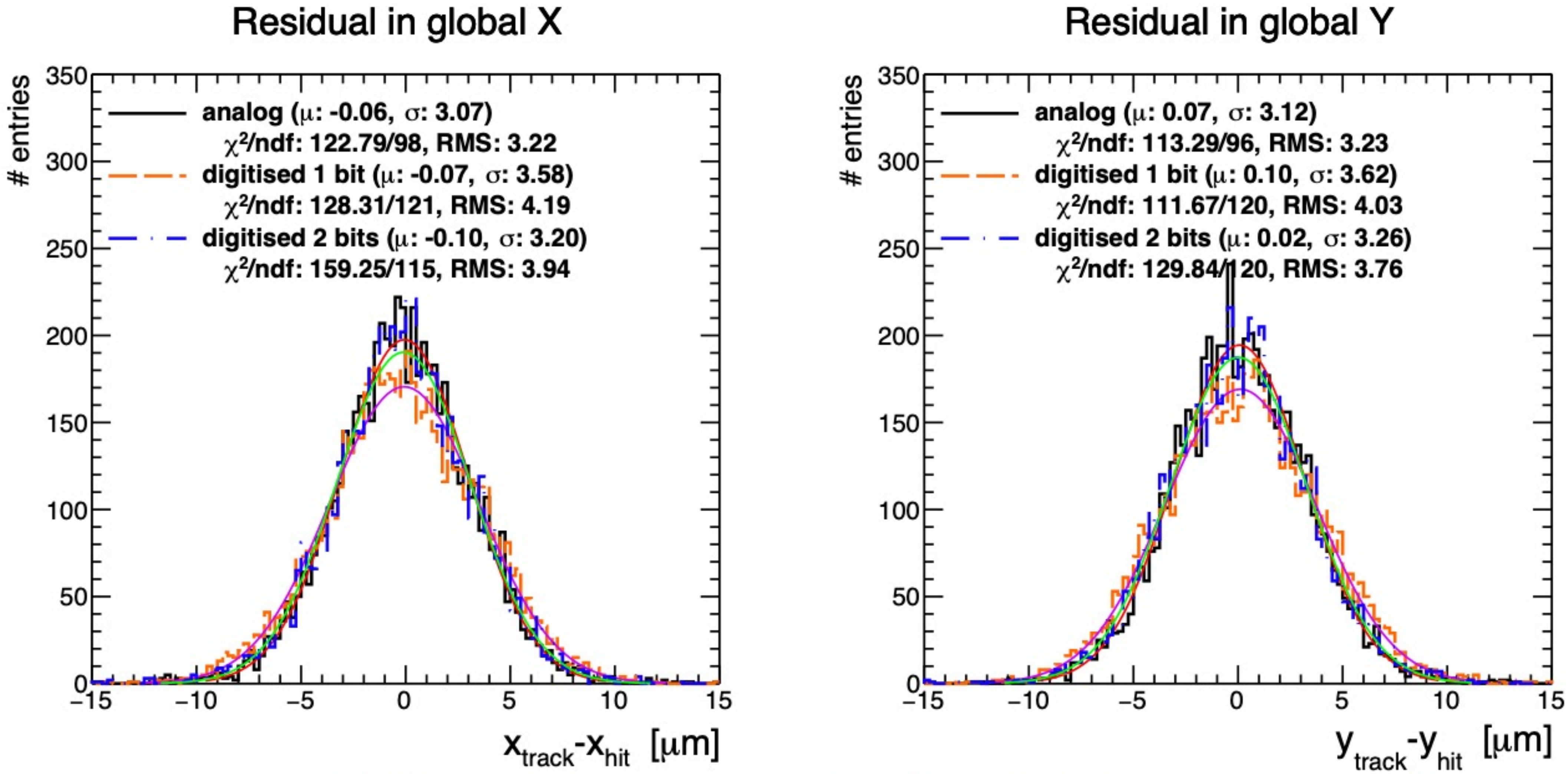
Digitization* : seed pixel signal – 2 bits examples





*PhD Gaëlle SADOWSKI

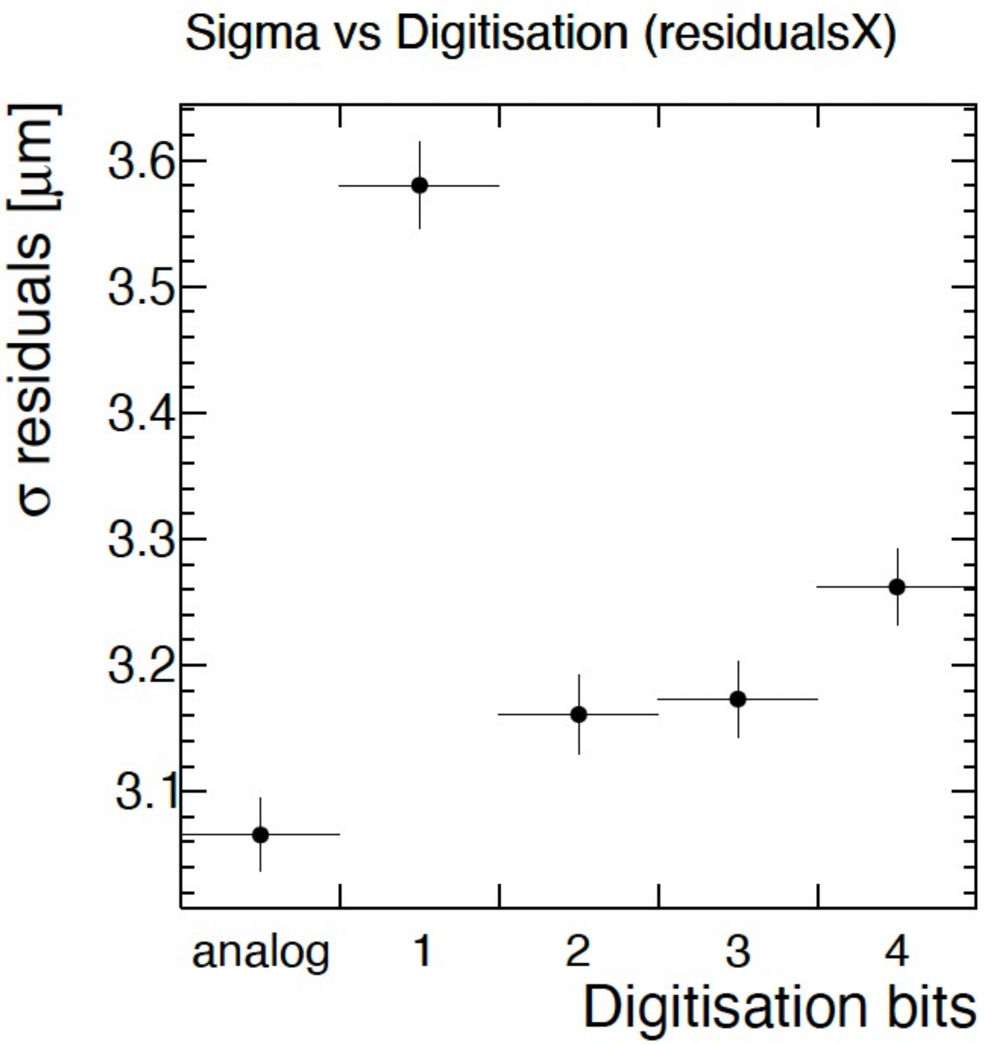
Digitization*: the impact of the number of bits on the position residuals

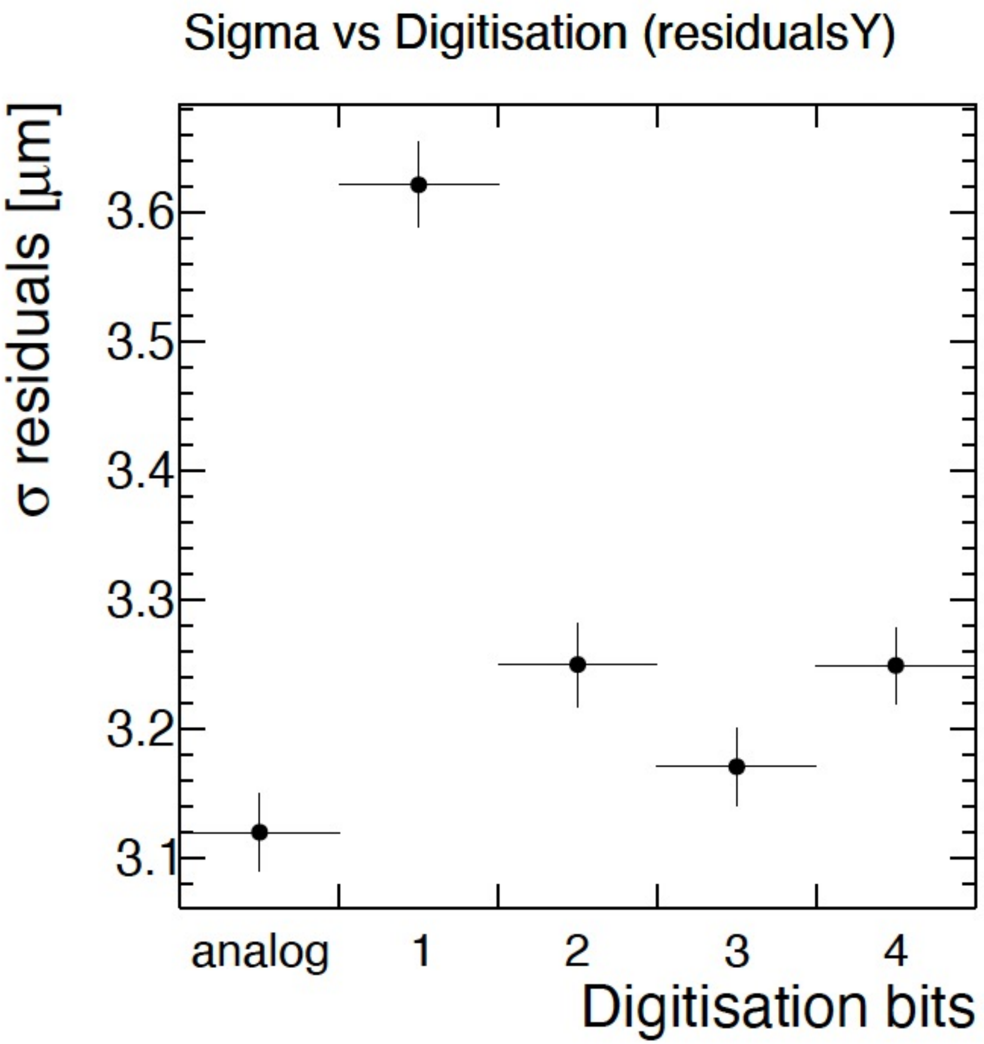


analog → red fit, 1 bit → purple fit, 2 bit → green fit

*PhD Gaëlle SADOWSKI

Digitization*: effect of Nbits





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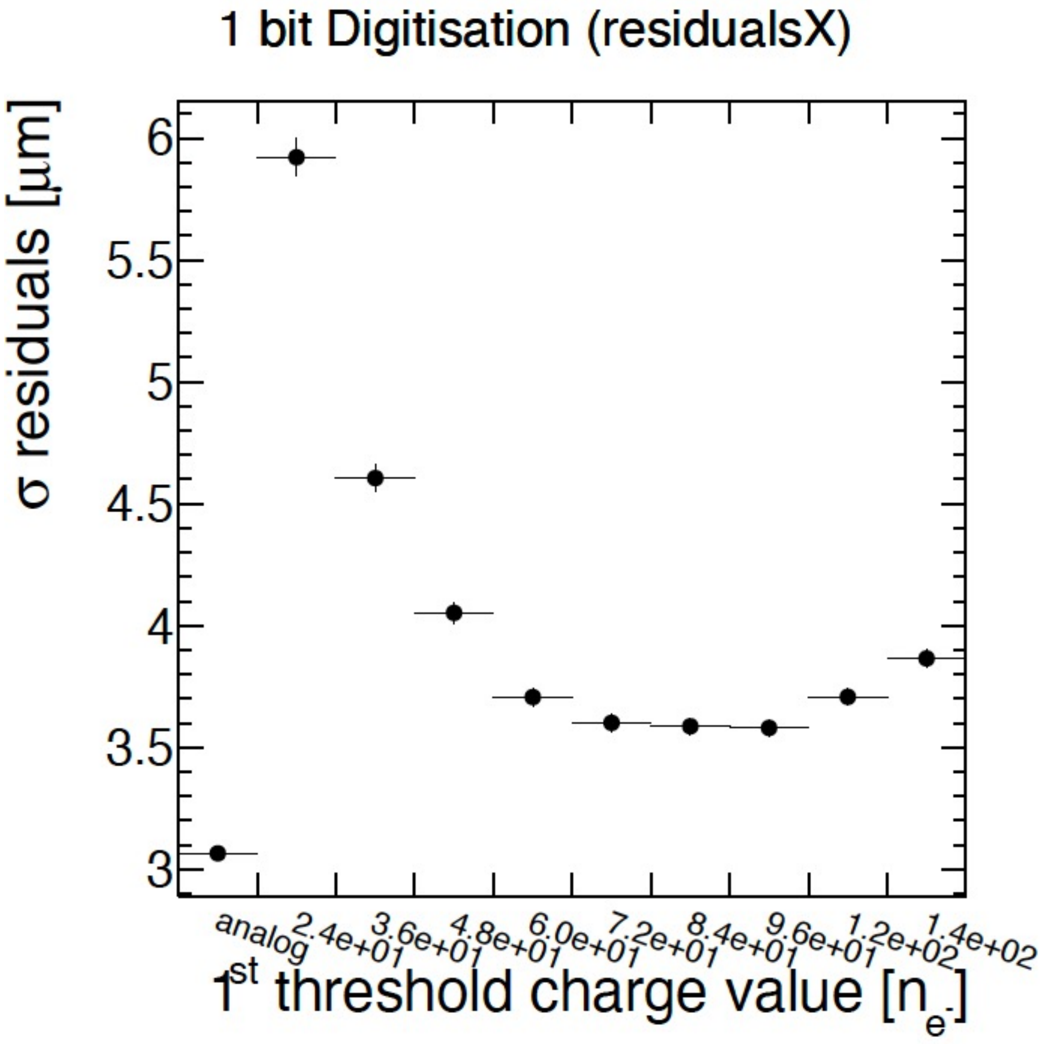
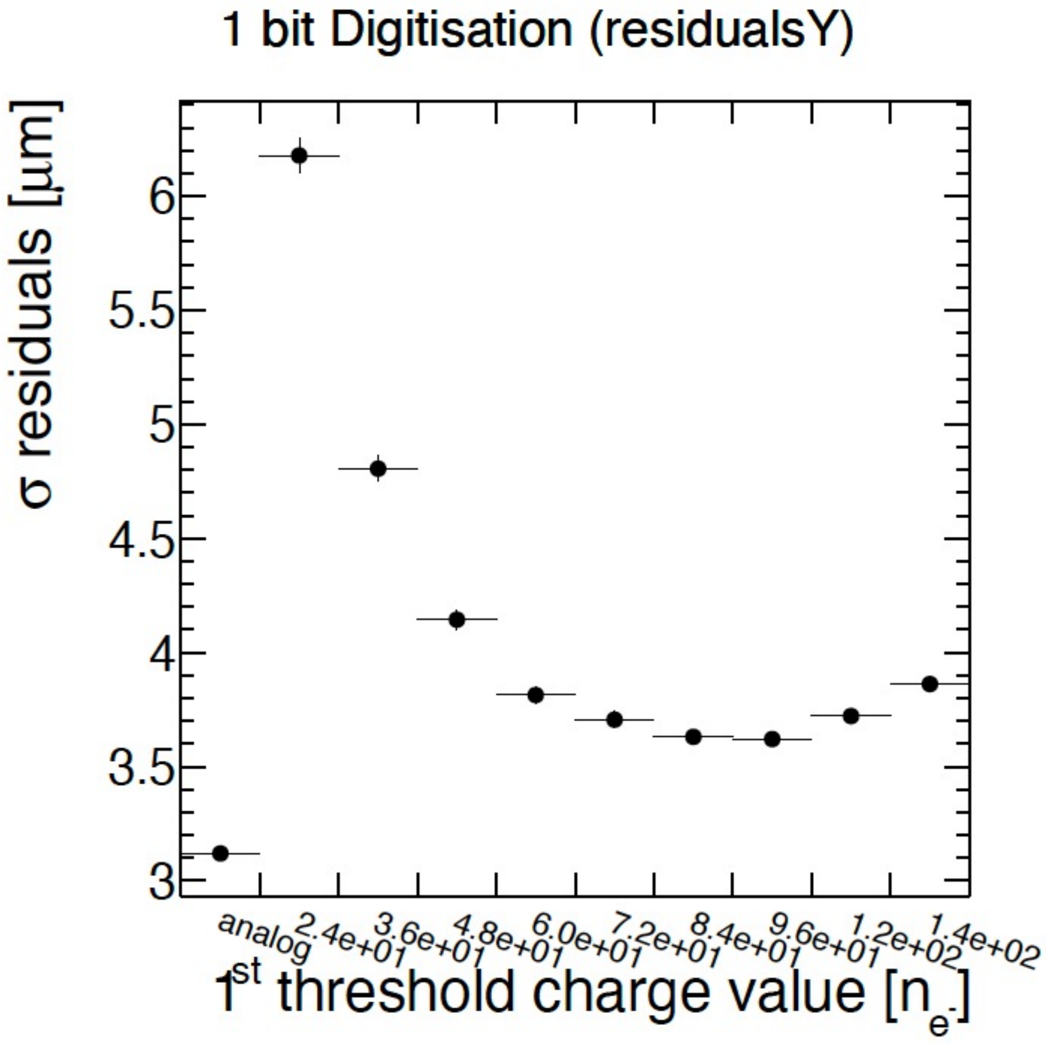
Digitization: Effect of threshold value on the position residuals





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Summary

- MIMOSIS sensor is being continuously improved

- 65 nm Technology is being scrutinized
  - ✓ Impact of pixel pitch
  - ✓ Impact of the process (std, gap, …)
  - ✓ Impact of pixel geometry

- Digitization is on progress

Thanks for your attention